RC31312A-EVK

VersaClock® 8 Evaluation Kit

Description

The RC31312A evaluation boards are designed to support users evaluating the clock generation in synthesizer mode for PCIe® Gen Compliance or jitter attenuation mode.

Specifications

Best in class performance for various frequencies:

- 156.25MHz Phase Jitter (12kHz–20MHz) 102fs RMS (typical)
- PCIe Gen7 CC jitter: 4.2fs RMS (maximum)
- PCIe Common Clock (CC) and Independent Reference clock (IR) support

Features

- USB powered
- Specialized device socket
- Access to CLKIN differential input clocks
- Test points for output clocks
- On board crystal or crystal overdrive (REFIN) via SMA
- Onboard I^2C and SPI communications

Board Contents

Items shipped with the evaluation kit (EVK):

- Evaluation board
- USB-C cable

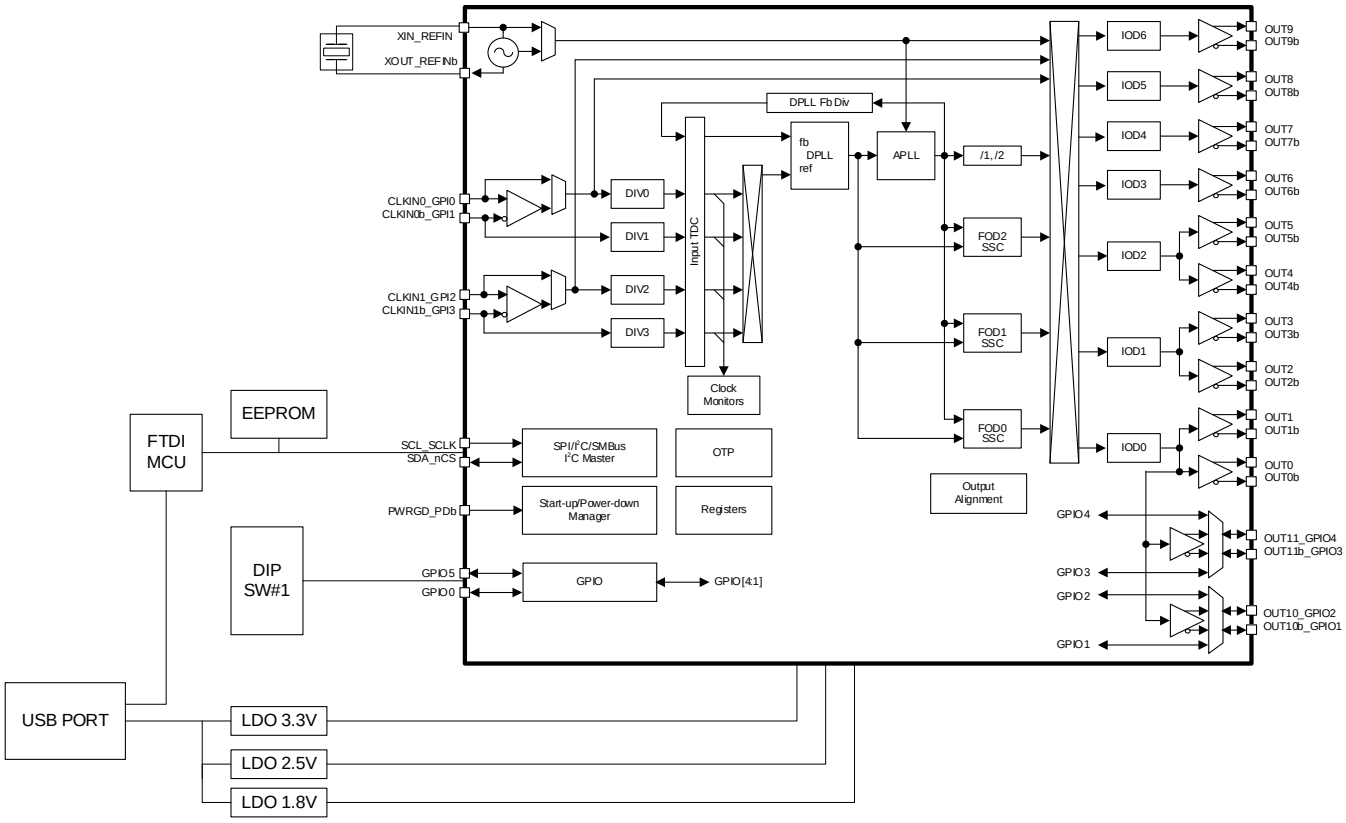

Figure 1. RC31312A Block Diagram

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1. Functional Description

The VersaClock 8 (VC8) evaluation boards (EVB) are designed to support users evaluating VC8 devices using clock generation in synthesizer mode for PCIe Gen compliance or jitter attenuation mode. When the EVB is connected via USB to the user's computer running Renesas Integrated Circuit Toolbox (RICBox™) software, the devices can be configured in various frequencies with best-in-class performance. The devices offer various feature with a total of 5, 9, and 12 pairs of differential outputs. Each pair of outputs can be programmed to LVCMOS or LP-HCSL style outputs. There are up to 6 general purpose input/output (GPIO) and 4 general purpose inputs (GPI) to support output enables, configuration selection, and status outputs. There is also a dedicated PWRGD_PDb pin as well. Voltage levels for VDDX, VDDR0/1, VDDA, VDDCA, VDDD, and VDDBK0-6 can be set via a jumper. The EVB kit also has a socket for installing an EEPROM. This manual also applies to RCx1309A and RCx1305A as they share the same reference designators.

1.1 Operational Characteristics

The EVB is capable of function in temperature range of -40°C to 85°C. The EVB is capable of operating in the VDD values of 3.3V, 2.5V, and 1.8V. The VDD banana connection can be used to set any desired voltage within the range of 1.71V to 3.63V.

1.2 Setup and Configuration

The following sections explain the Crystal, Input Clock, Serial, GPI/GPIO, Output and Power functions used for setting up and configuring the devices using RICBox software.

1.2.1 RC31305A vs RC31309A vs RC31312A

The RC31305A is a 5 output device. The RC31309A is a 9 output device. The RC31312A is a 12 output device. The RC313xxA supports synthesizer and jitter attenuator (JA) operations. The RC31312A and RC31309A also have a Q-variant meaning internal crystal, for example RC31312AQ. The crystal pins will not be bonded out to the package.

The following table summarizes to differences between the devices.

Table 1. Product Variants

Device	Crystal Interface	Input Clocks	JA Support	Output Clocks
RC31305A	Yes	CLKIN0/nCLKIN0	Yes	OUT0, OUT3, OUT5, OUT8, OUT10
RC31309A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	Yes	OUT1, OUT2, OUT3, OUT4, OUT5, OUT7, OUT8, OUT9, OUT10
RC31312A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	Yes	OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, OUT11

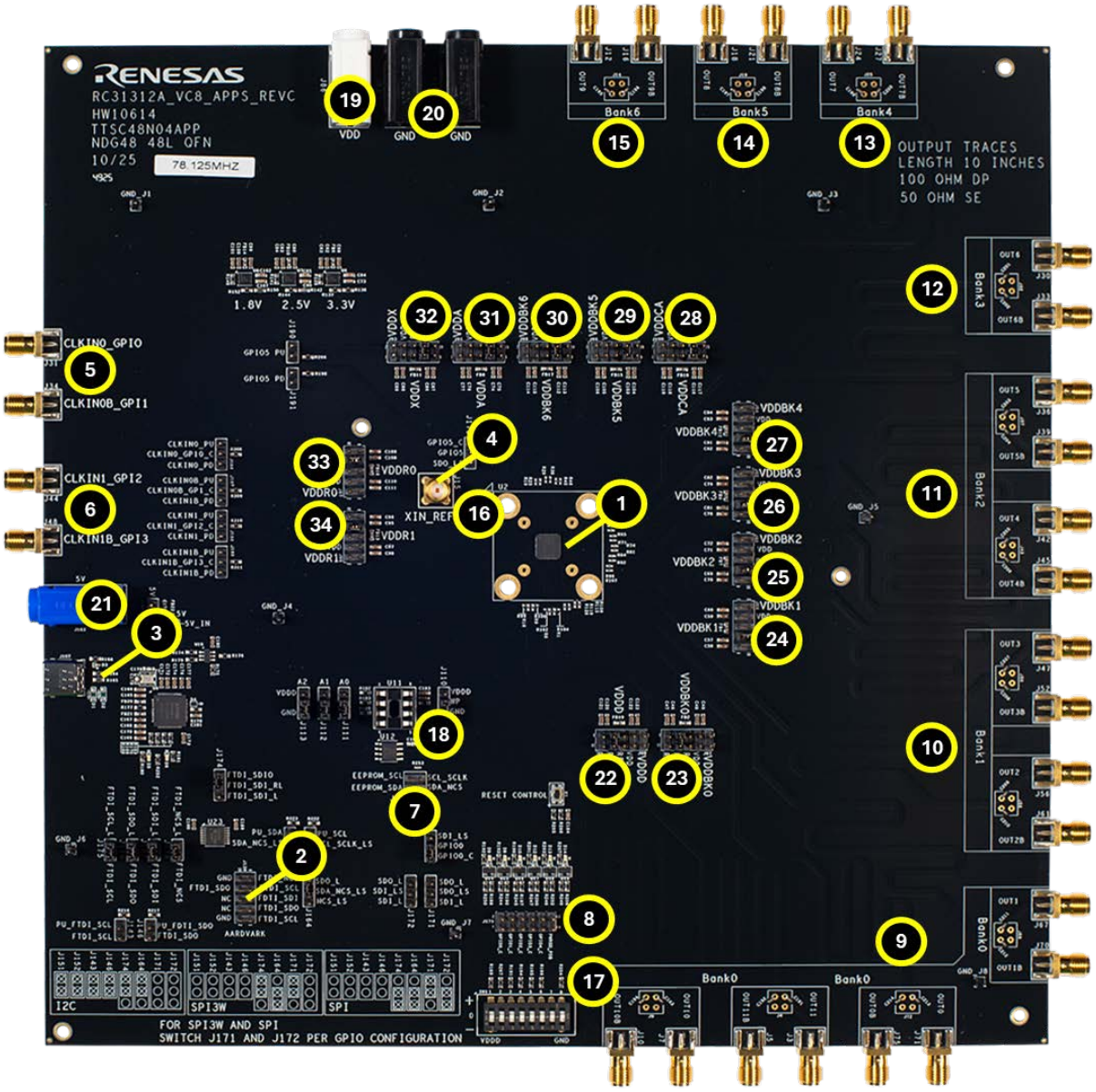


Figure 2. VersaClock 8 Evaluation Board

Table 2. EVB Functions

Ref.	Name	On-Board Connector Label	Function
1	RC31312A RC31309A RC31305A	U2	Evaluation device, 6 x 6 x 0.9 mm 48-pin QFN Evaluation device, 5 x 5 x 0.9 mm 40-pin QFN Evaluation device, 4 x 4 x 0.9 mm 32-pin QFN
2	I2C/SPI for Aardvark connector	J139	6 pins header of I2C/SPI pins. FTDI can pigtail off these headers.
3	USB Interface	J107	USB Type C Jack for connection with the user's computer and interaction with RICBox Software.
4	XIN/REFIN	J15	Crystal overdrive - 0V to VDDX DC coupled (singled ended) or 1.4 Vpp AC coupled.
5	CLKIN0, CLKIN0B	J31, J34	Differential Clock 0 input positive on J31 and negative on J34 CMOS single-ended reference clock input.

Ref.	Name	On-Board Connector Label	Function
6	CLKIN1, CLKIN1B (RC31312A and RC31309A only)	J44, J48	Differential Clock 1 input positive on J44 and negative on J48 CMOS single-ended reference clock input
8	GPIO jumper	J179	The header can be utilized to provide LED feedback by adding a jumper
9	Test points for OUT0, OUT1, OUT10, OUT11	J3, J5, J7, J10, J67, J70, J71, J75	SMA connectors for differential outputs using VDDBK0 power rail: populate with a pair of SMA connector J7, J10 for OUT10 populate with a pair of SMA connector J3, J5 for OUT11 populate with a pair of SMA connector J71, J75 for OUT0 populate with a pair of SMA connector J67, J70 for OUT1
10	Test points for OUT2, OUT3	J47, J52, J56, J61	SMA connectors for differential outputs using VDDBK1 power rail: populate with a pair of SMA connector J56, J61 for OUT2 populate with a pair of SMA connector J47, J52 for OUT3
11	Test points for OUT4, OUT5	J36, J39, J42, J45	SMA connectors for differential outputs using VDDBK2 power rail: populate with a pair of SMA connector J42, J45 for OUT4 populate with a pair of SMA connector J36, J39 for OUT5
12	Test points for OUT6	J30, J33,	SMA connectors for differential outputs using VDDBK3 power rail: populate with a pair of SMA connector J30, J33 for OUT6
13	Test points for OUT7	J24, J27	SMA connectors for differential outputs using VDDBK4 power rail: populate with a pair of SMA connector J24, J27 for OUT7
14	Test points for OUT8	J18, J21	SMA connectors for differential outputs using VDDBK5 power rail: populate with a pair of SMA connector J18, J21 for OUT8
15	Test points for OUT9	J12, J16	SMA connectors for differential outputs using VDDBK6 power rail: populate with a pair of SMA connector J12, J16 for OUT9
16	Crystal pads	U1 (bottom)	To mount different Crystals. Footprint 3.2 x 2.5
17	DIP Switches	SW1	DIP switch devices are used to setup GPIO pins based on RC31312A device condition. See **Figure 9** below for detail.
18	EEPROM IC	U11 or U12	An external EEPROM IC and an 8-lead DIP8 socket. Populated with AT24C64 or **R1EX24064ASAS0I#U0** 64-Kbit EEPROM as default
19	Power VDD Jack	J86	External power supply, Positive terminal, Apply 3.3V 2.5V, or 1.8V as default only.
20	Power GND Jack	J83, J85	External power supply ground.
21	Power 5V Jack	J183	External 5V to power onboard LDO that generate 3.3V, 2.5V, 1.8V.

Ref.	Name	On-Board Connector Label	Function
22	VDDD	J99	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for digital circuit power
23	VDDBK0	J87	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK0
24	VDDBK1	J89	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK1
25	VDDBK2	J90	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK2
26	VDDBK3	J92	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK3
27	VDDBK4	J94	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK4
28	VDDCA	J100	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for analog calibration circuit power
29	VDDBK5	J96	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK5
30	VDDBK6	J98	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for BANK6
31	VDDA	J91	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for analog circuit power
32	VDDX	J93	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for crystal circuit power
33	VDDR0	J97	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for reference input circuit power
34	VDDR1 or VDDR01	J95	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for reference input circuit power

1.2.2 On Board Crystal PAD and Reference Input

The EVB has a pad U1 that can be used for installing a crystal. Different crystal frequencies between 8MHz and 80MHz can be used to match the specific application where the RC31312A will be used. For example, we recommend using a 62.5MHz or 78.125MHz crystal for Ethernet applications with output frequencies like 156.25MHz or 312.5 MHz. Please refer to the datasheet for more information on crystal recommendations. The RC31312A supports a range of C_L from 6pF to 12pF. C3 and C14 can be used to trim the crystal C_L.

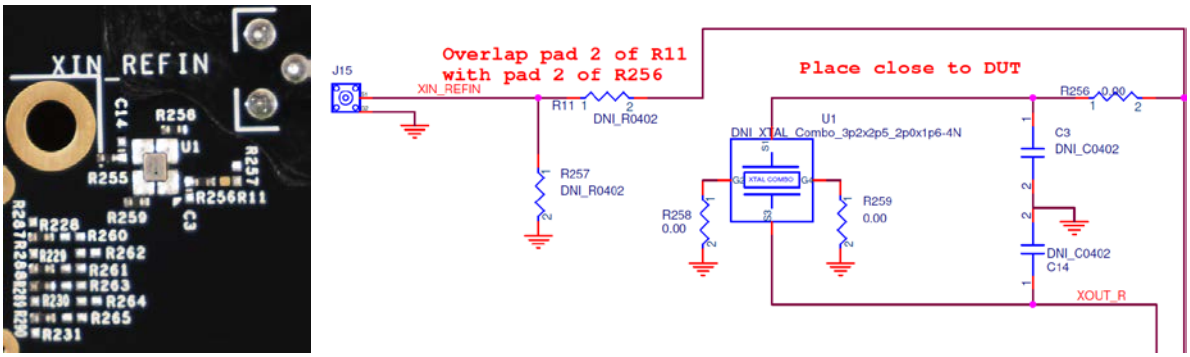


Figure 3. Crystal Footprint and Schematic

The XIN_REFIN input (J15) can be used to overdrive the XIN pin with an external clock with SMA connectors in single-ended mode. Supported frequency range of the reference input are 8MHz to 80MHz in single ended mode. Please be sure to install R11. In this configuration, R257 can be used for 50ohm termination if needed.

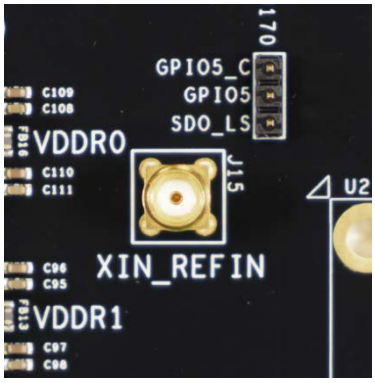


Figure 4. XTAL Single-ended Ref Input

1.2.3 CLKIN0/CLKIN1 Clock Inputs

The RC313xxA can accept two differential clock inputs or four single-ended clock inputs (J31/J34) (J44/J48) to be used as an alternate reference for synth mode or a jitter attenuator source. To enable proper connection, make sure R228, R229, R230, and R231 are populated and R287, R288, R289, and R290 are unpopulated. The RC313xxA contains internal termination to support LVDS, HCSL, CML, LVPECL or CMOS levels. AC coupling is also available. The supported reference clock frequency range in differential mode is 8kHz to 650MHz, and 8kHz to 250MHz in single-ended mode. When CLKIN are not used, they can be configured as GPI.

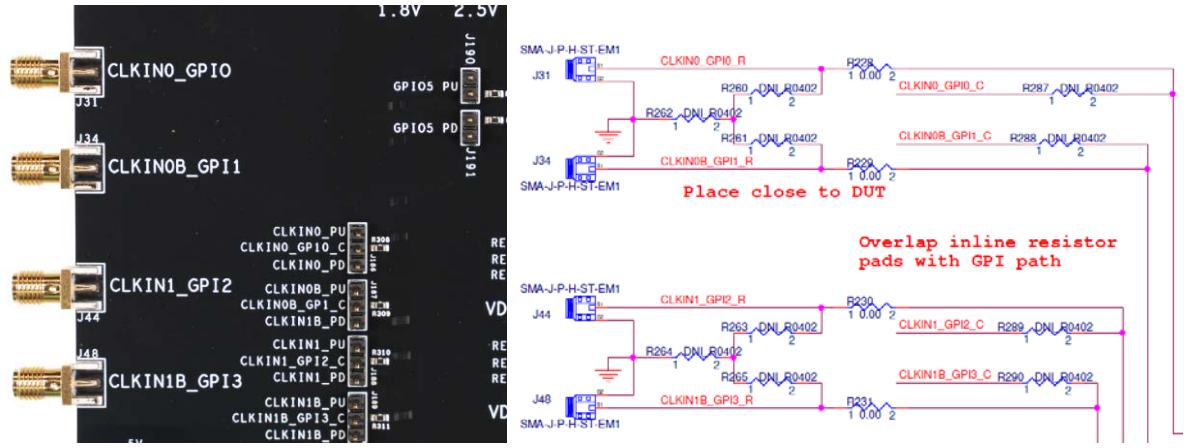


Figure 5. CLKIN0/1 Single-ended / Differential Ref Input

1.2.4 Serial Connection

The EVB can be connected to a computer via a USB. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) can handle the data communication. The +5V from the USB powers the on-board regulators or external 5V via banana connector J183. Jumper J184 is used for selecting 5V rail is powered.

RC313xxA supports I2C and SPI. By default, blank VC8 units are configured as SPI 3 wire. However, dash-codes 001 and Q01 units are EEPROM load enabled and are default I2C. The jumpers in the lower left part of the board (J175, J176, J177, J178) can be removed to disconnect the FTDI chip from the serial bus. By removing these jumpers, an Aardvark can be used instead. J139 can be used to probe the serial bus. Refer to the schematic for configuration options. The I2C or SPI signals are level shifted to match RC313xxA (see Figures 6 and 7).

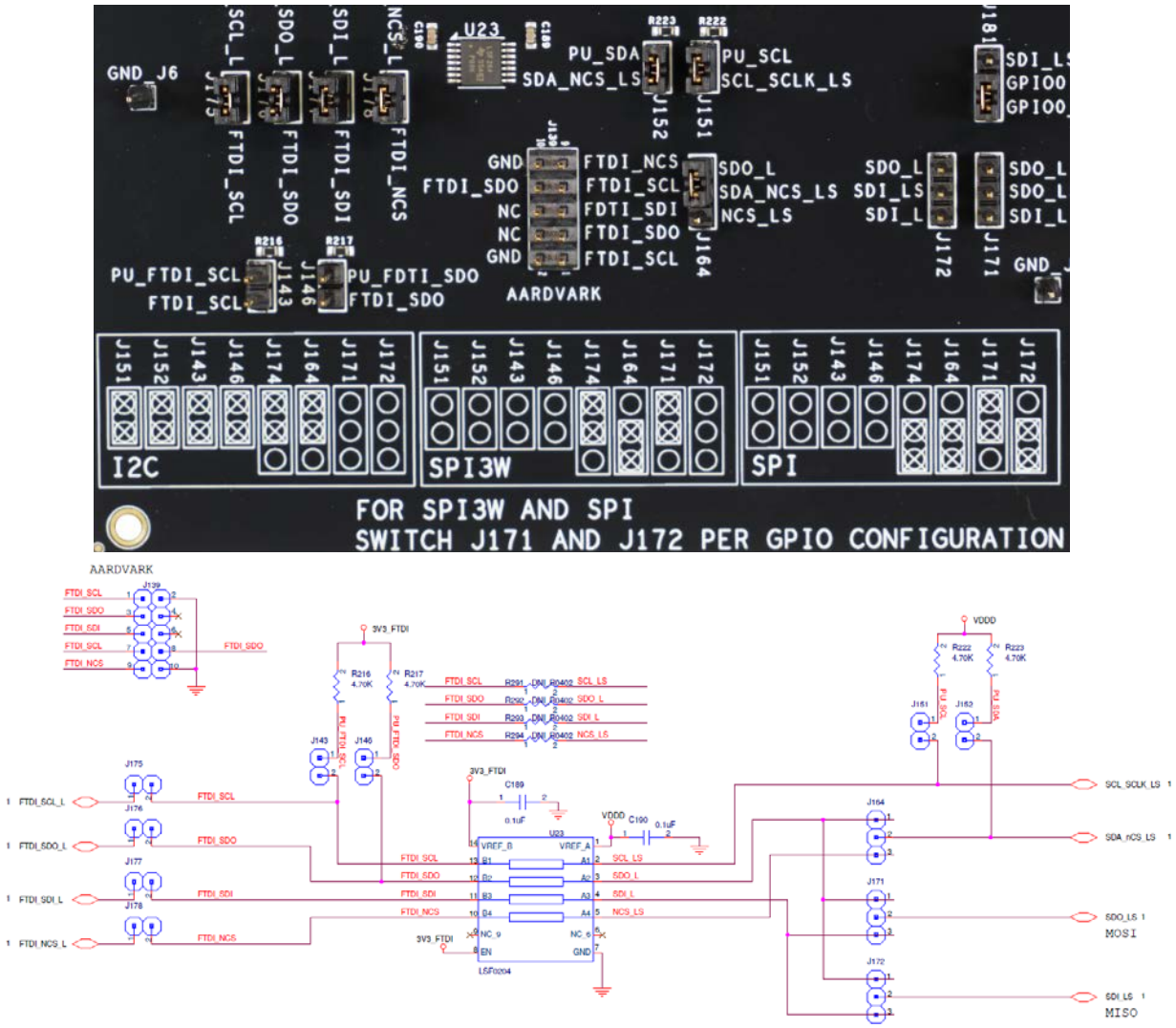


Figure 6. Serial Communication Jumpers

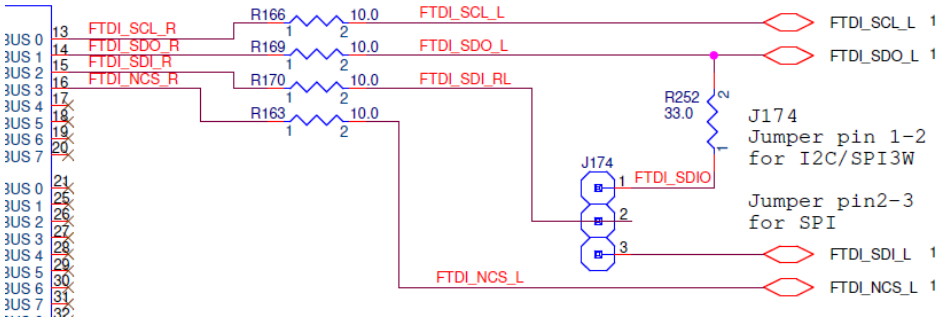


Figure 7. Jumper for I2C/SPI 3W or SPI 4W

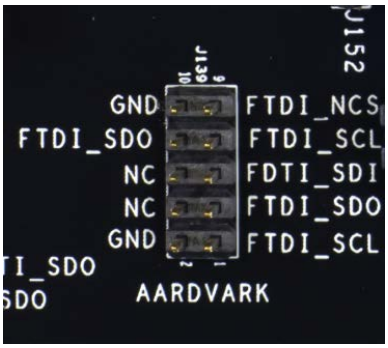
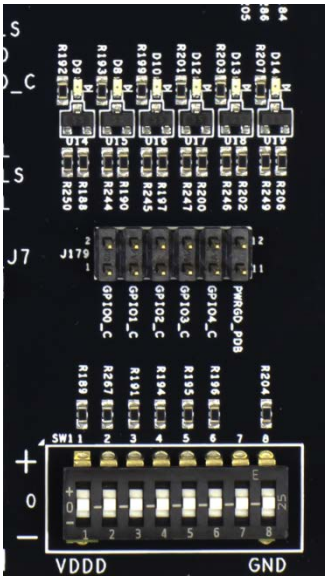


Figure 8. Aardvark Adapter Connection J139

1.2.5 GPI Header and GPIO DIP Switch Selectors

The EVB has 3 pin headers for GPI pins and a DIP switch (SW1) to support GPIO on RC313xxA device. In order to use GPI0, GPI1, GPI2, and GPI3, jumpers J186, J187, J188, and J189 can be used to pull up or down the input respectively. For GPIO, DIP switch SW1 can be used. The middle position of DIP switch leaves the pin open. GPIO0 has the first 2 DIP switches connected to the signal. To allow for DIP switch control move jumper J181. The DIP switch can now pull high or low as needed. Setting a switch high and the other low results in a mid voltage. To allow the DIP switch to control GPIO1,2,3,4 resistors R99, R100, R102, R104 need to be populated. Move the DIP switch to the “+” side to pull the pin high and move to the “-” side to pull the pin low. By installing jumpers on J179, the LED can be used to indicate the state of the GPIO pin. GPIO5 is referenced by VDDX so the pull up and down jumpers (J190 and J191) are near that VDD pin. RC313xxA has a dedicated PWRGD_PDb. Push button K1 can be used to momentarily reset the device. This pin will need to be configured for soft or hard reset.

Table 3. SW1 Description



Switch 1 = GPIO0	Connects via J181 as General Purpose Input/Output 0. Set to middle as default on EVB
Switch 2 = GPIO0	Connects via R181 as General Purpose Input/Output 0. Set to middle as default on EVB
Switch 3 = GPIO1	Connects via R99 as General Purpose Input/Output 1. Set to middle as default on EVB
Switch 4 = GPIO2	Connects via R100 as General Purpose Input/Output 2. Set to middle as default on EVB
Switch 5 = GPIO3	Connects via R102 as General Purpose Input/Output 3. Set to middle as default on EVB
Switch 6 = GPIO4	Connects via R104 as General Purpose Input/Output 4. Set to middle as default on EVB
Switch 7 = NA	No connection
Switch 8 = PWRGD_PDb	Connects as PWRGD_PDb

Figure 9. DIP Switch SW1

1.2.6 Outputs

Each of the 5, 9, or 12 differential output pairs can be programmed (output mode) to LP-HCSL or LVCMOS logic type. LVCMOS is a single ended logic type and the output pair will essentially be 2 CMOS outputs of the same frequency.

LP-HCSL is the most versatile output because it can be customized. The LP-HCSL driver is simply a voltage push-pull driver. The RC313xA LP-HCSL can be programmed to different amplitudes ranging from 800mV to 940mV. The slew rate can be programmed (lpsr) to slow, 2-4 V/ns or fast, > 4V/ns. The output driver has source termination. The output impedance can be programmed (lpimp) to 100 ohm, 85 ohm, or 33 ohm differential. When AC coupled, the LP-HCSL driver can be compatible with LVDS and LVPECL signal swing requirements.

For LVCMOS output type, output phase can be programmed (prog0 or prog1) to be out of phase or in phase. Each output can also be tri-stated (prog2/prog3). The slew rate can also be programmed (cmsr) to 2 or 3 V/ns. The single-ended outputs support CMOS swings of 1.8V, 2.5V, or 3.3V as determined by their VDDO voltage, or 1.0V or 1.2V CMOS swings as determined by programming.

RC313xxA is default with LP-HCSL output type on all outputs of EVB.

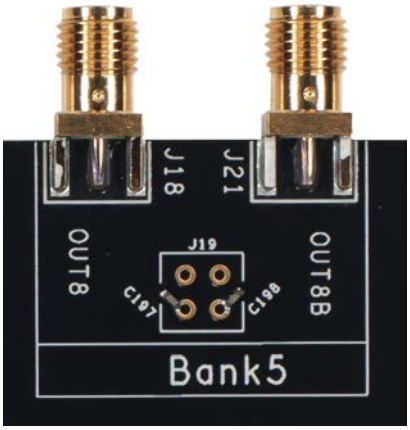


Figure 10. Output Termination with SMA Connector, Top Side

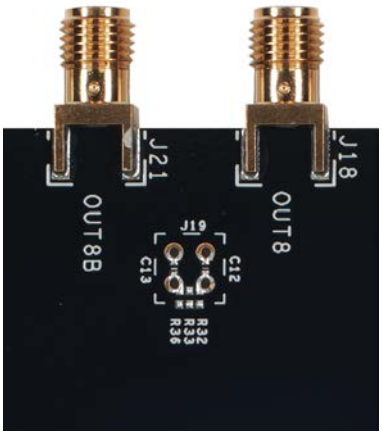


Figure 11. Output Termination with SMA Connector, Bottom Side

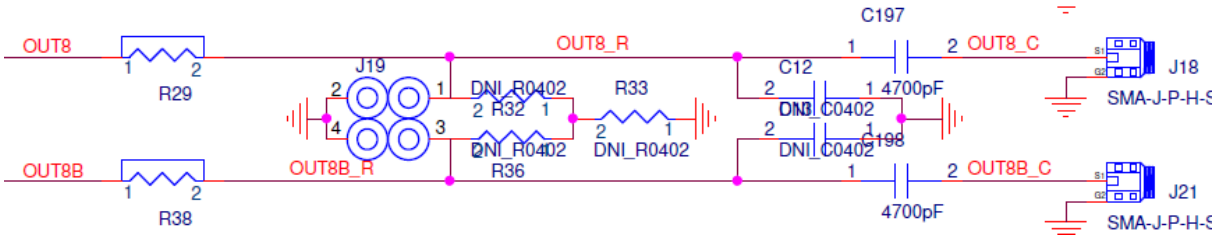


Figure 12. Output Schematic

Figure 10 shows the default output termination for LP-HCSL (100 ohms) with SMA connectors (J18, J21). There are place holders for termination resistors on the bottom side of the EVB. C197 and C198 are installed by default for measurement via SMA connector. To make Hi-Z measurements, simply leave C197 and C198 unpopulated. For LPHCSL (33/85 ohms), simply cut R29 and R38 and install the correct resistors to impedance match the output trace. For LVCMOS, install a 33 ohm resistor for R29 and R38.

1.2.7 Power and USB Connection to Computer Host

As mentioned before the EVB is connected to a computer via the USB cable. It is recommended that the cable is connected to at least a USB2.0 port. The USB provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V, 2.5V, and 1.8V voltages to the entire EVB

The voltage source can be either from on-board voltage regulators for 3.3V, 2.5V, 1.8V or from VDD_J banana connector. The banana connector can connect to a bench supply and the connection can be used to measure total supply current into pins as reference. When all powers are selected from VDD_J power jack, the USB connection will still be needed in order to connect to computer for programming RC31312A using RICBox.

In Figure 13, the source for pin VDDO1 (J52) is chosen to be 3.3V. If VDD_J is provided, the jumper can be moved to pin 3-4 of header J52.

Figure 13. Power Source from USB Connector, 5Vin, or VDD Banana

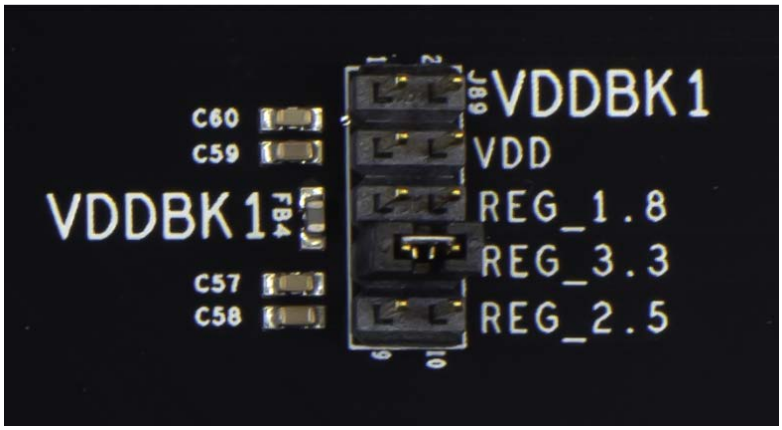


Figure 14. Power Source Selection for BANK Voltage

1.2.8 Renesas Integrated Circuit Toolbox (RICBox)

The Renesas Integrated Circuit Toolbox (RICBox) software can program the RC313xxA on the EVB using either the on board FTDI chip or Aardvark tool. RICBox provides a user-friendly interface to support programming configurations into the RC313xxA on the board. For more information about RICBox, see the Renesas IC Toolbox User Guide.

1.2.8.1 Programming the RC313xxA using RICBox Software

1. Connect J107 on the EVB to the user's computer using a USB cable.
2. Launch RICBox as described in the user's guide.
   a. The software and guide are downloadable from the product page.
3. For a new configuration, click on "Create new project"

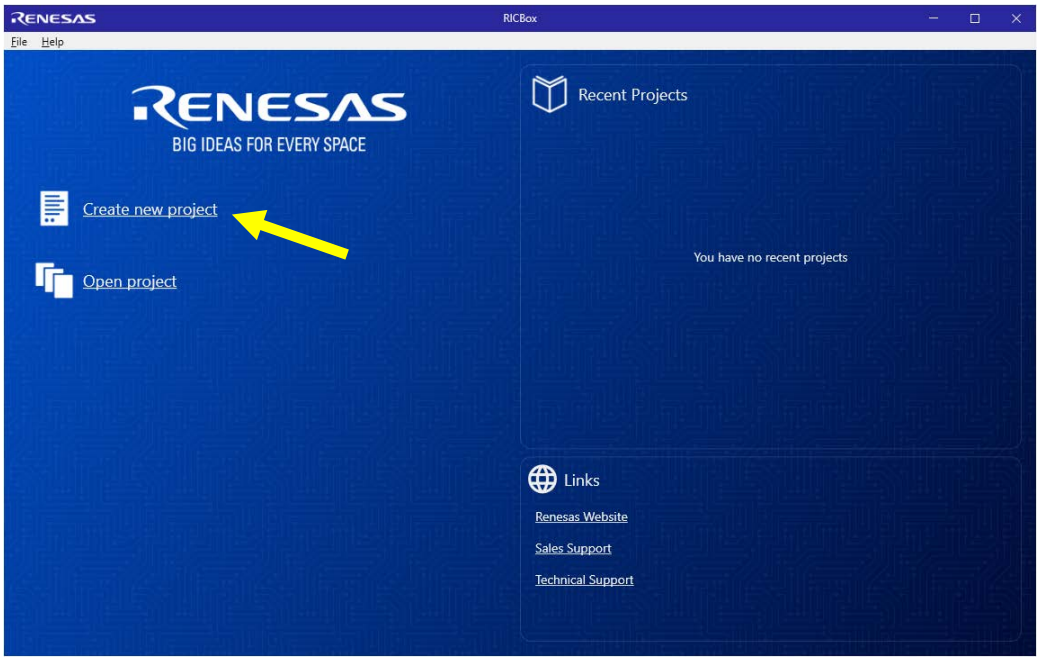


Figure 15. RICBox Start Page

4. Select the product family (VersaClock8), then select a product variant (part number) and push OK.

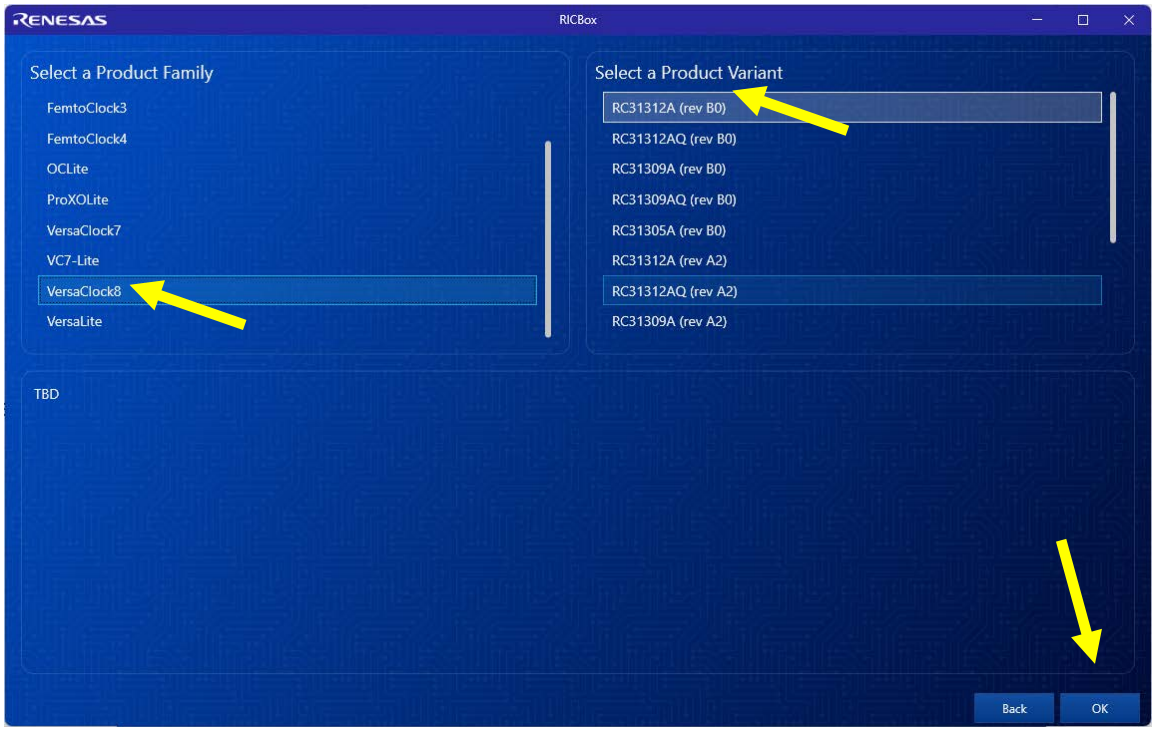


Figure 16. Select Product Family and Variant

5. On the Inputs wizard page, mode for XTAL REFIN can be set (Xtal, XIN overdrive). Expected input frequency needs to be entered. The CL can also be set internally between 6pF to 12pF.

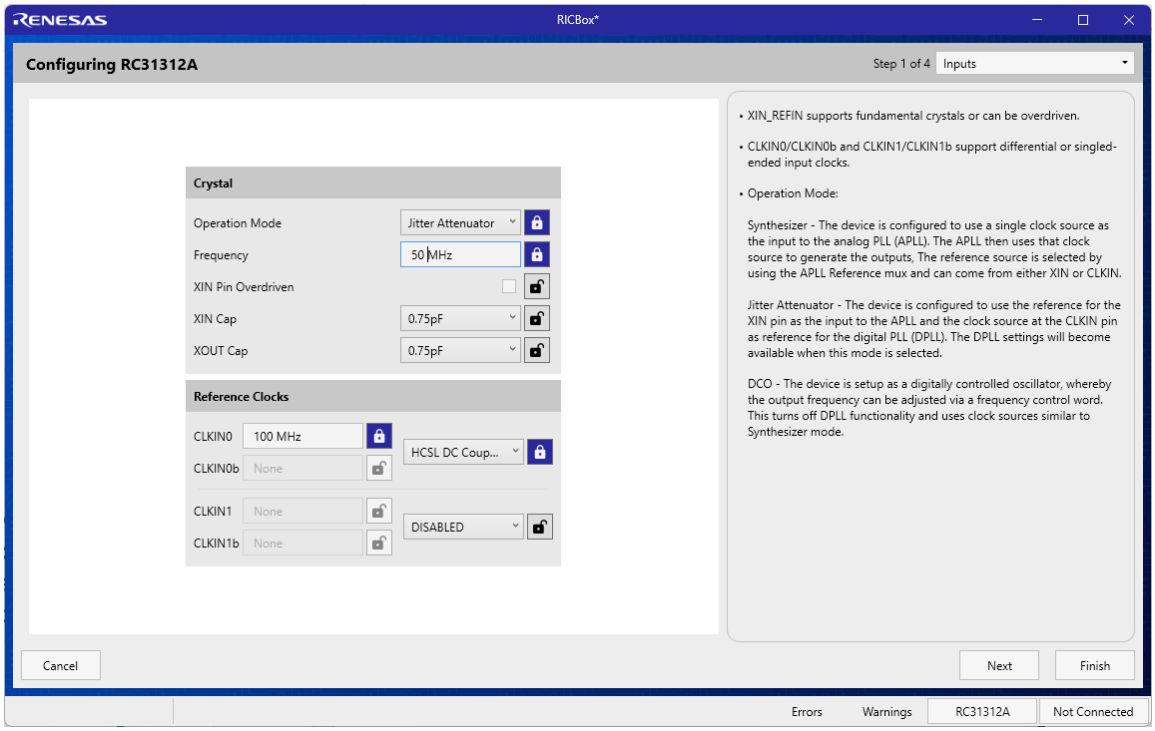


Figure 17. Inputs Wizard Page

If Operation Mode is set to Jitter Attenuator, the next wizard page is DPLL. Pick a premade profile or create your own.

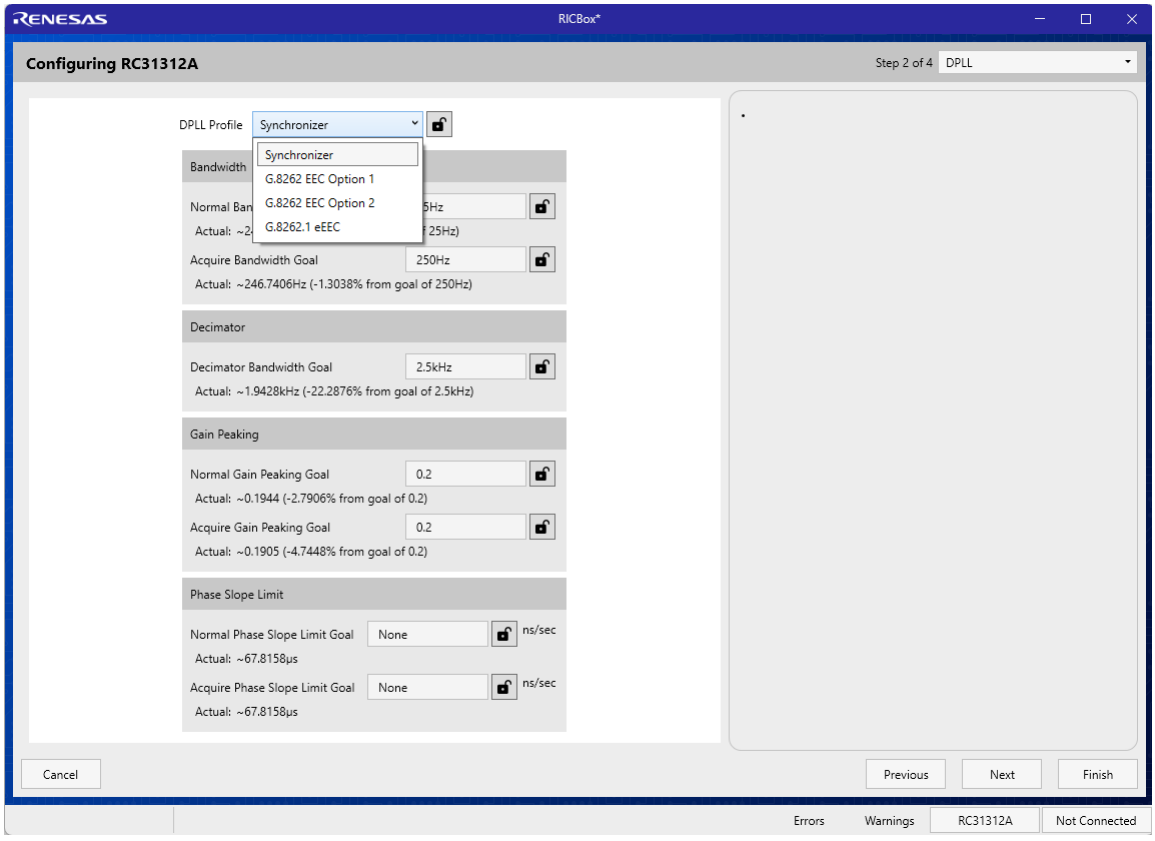


Figure 18. DPLL Wizard page

The next page is to configure spread spectrum clocking, if needed for your application. On this page, any FOD can be enabled for SSC for down or center spread. Percentage and modulation frequency can be set as well.

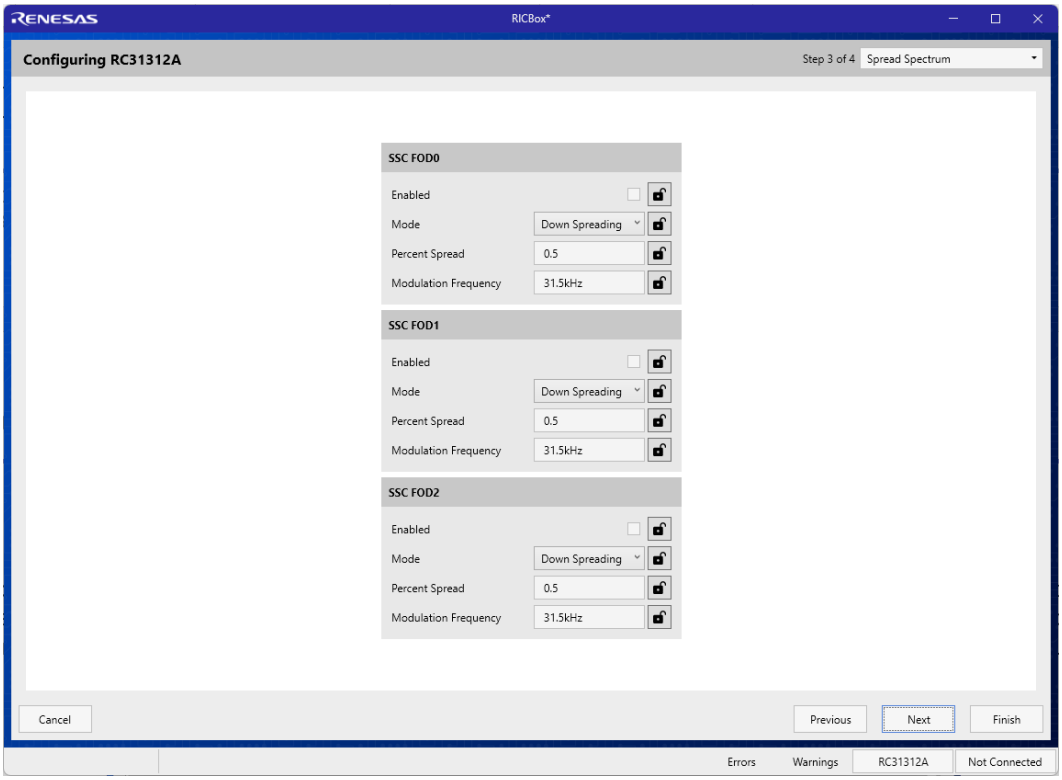


Figure 19. Spread Spectrum Clocking Wizard Page

6. Configure the output settings which includes the divider source (VCO post div, FOD0-2, IOD source mux), output frequency and output mode (LPHCSL, LVCMOS). If a bank is to be unused, use the power down check box to turn off the bank. Click on the settings icon to adjust amplitude, impedance, and slew rate for each output.

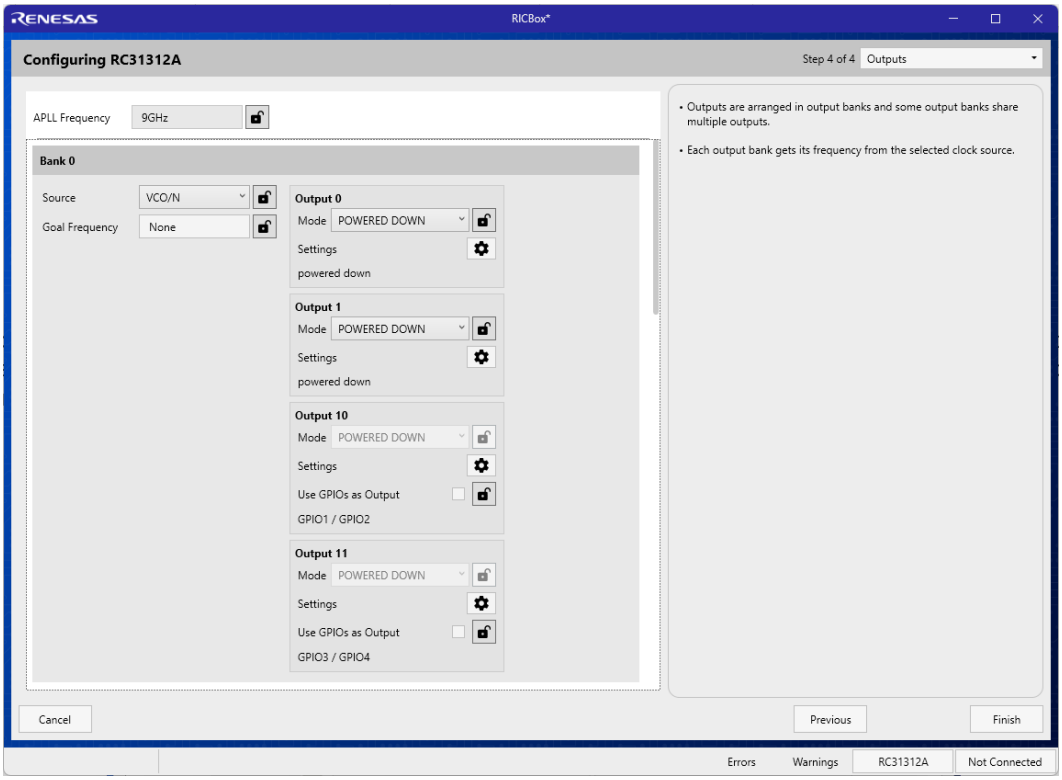


Figure 20. Outputs Wizard Page

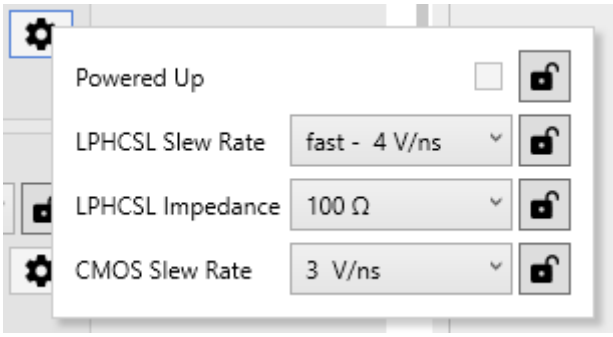
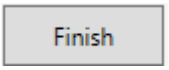


Figure 21. Advanced Output Settings

7. Click the Finish button  to view the summary of the configuration.

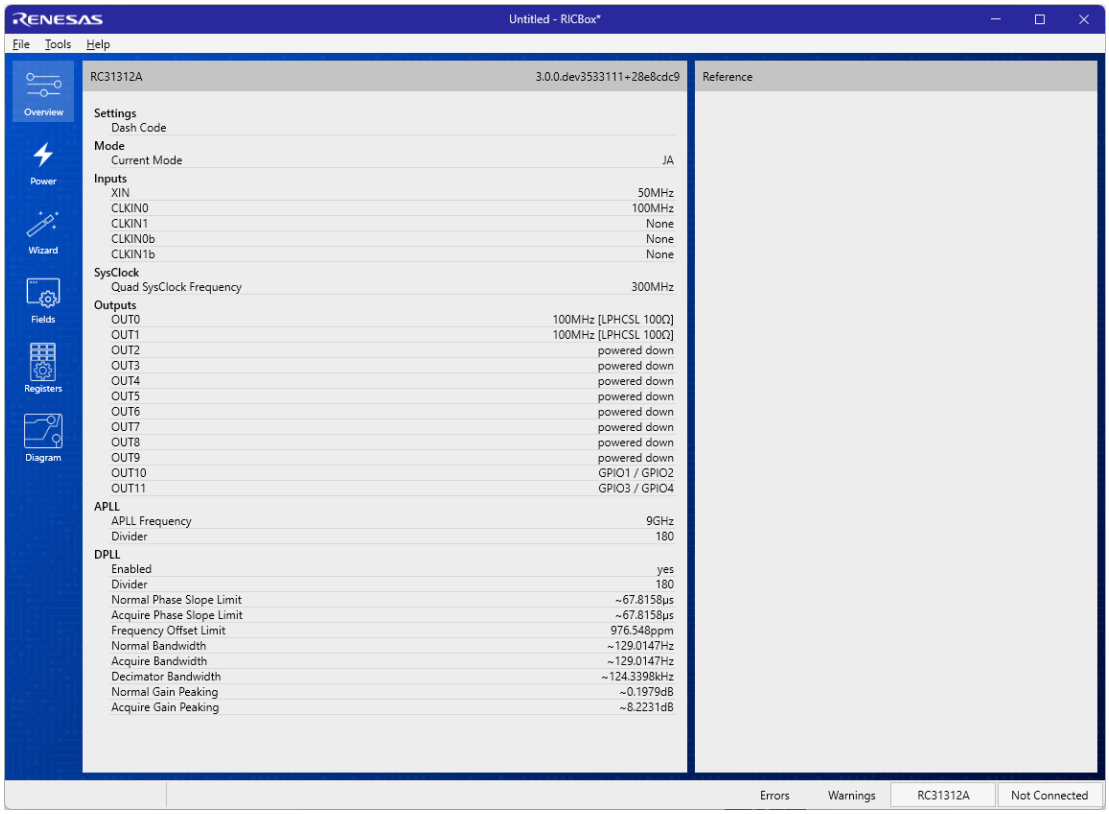


Figure 22. Configuration Summary

8. To go back to any of the previous wizard pages, click the wizard  icon.
9. RICBox is now ready to connect to RC313xxA. Push the “Not Connected” button in the lower right part of RICBox tool. Then push “Connect”. Note, RICBox will still connect to VC8 if no XIN in present.

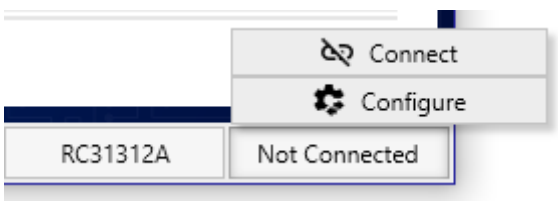


Figure 23. Connect to VersaClock 8

10. The “Not Connected” button will turn green and changed to “Connected”. Click the button again to “Program” the part.

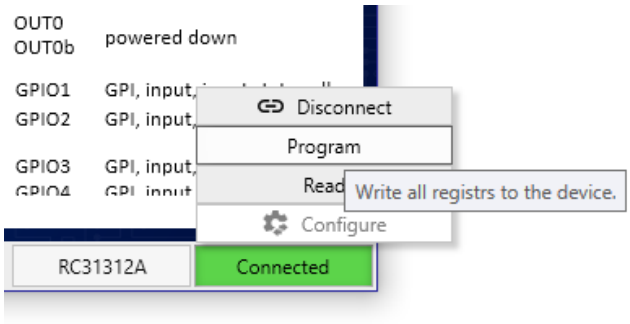


Figure 24. Program VersaClock 8

11. View the block diagram by pushing the Block Diagram icon.

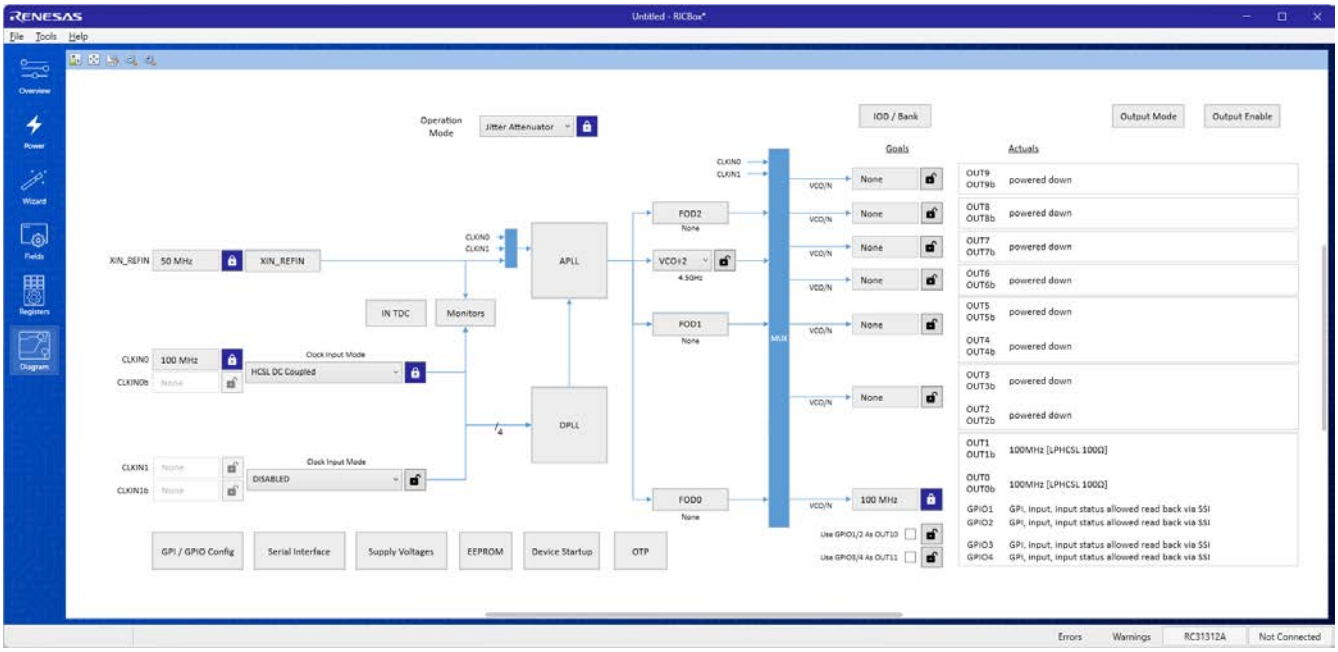


Figure 25. Block Diagram

RICBox can also load RBS files others have created for repeatable and fast configuration setup later.

2. Evaluation Board Components

2.1 Layout Guidelines

For designing the layout around the RC313xxA, below is a list of items to keep in mind.

2.1.1 EPAD

Make sure there are enough vias to allow for proper thermal dissipation. The EPAD may be connected to VEE (negative power supply) to allow for split power planes for different input/outputs styles. The EVB has VEE connected to ground.

2.1.2 Crystal/Reference Input

Place the crystal as close to VC8 as possible. Make XIN/XOUT trace lengths the same. For external tuning caps, connect them from XIN/XOUT to EPAD reference voltage. For single-ended reference input, route only the REFIN trace as single ended 50 ohm.

2.1.3 Serial Connection

The serial interface can function from 1.8V to 3.3V for VDDD. If serial communication is needed, the SCL and SDA pull up resistor need to connect to VDDD. Use a level translator if needed. Refer to section 1.2.3 to understand more about the level translator. Acceptable values for pull up resistors are 1K ohm to 10K ohm. It is recommended to route the serial signals close to each other. Be mindful of EEPROM operating voltage.

2.1.4 GPI/GPIO

In order to utilize GPI, CLKIN must be disabled as they share the same pins. The logic levels are determined by VDDD relative GND. The GPI can be configured to have internal pull up/down while GPIO can only have internal pull down. Signals should be routed to minimize return loops. GPI0-1 reference VDDR0, GPI2-3 reference VDDR1. GPIO5 reference VDDX.

2.1.5 Outputs

For LVCMOS outputs type, route single ended 50 ohm and place an inline 33-ohm resistor near VC8. For differential outputs type, route differential 100 ohm. For LPHCSL, an inline 7.5-ohm resistor near VC8 is needed if output impedance is set to 85 ohms. An inline 33-ohm resistor near VC8 will be needed if the output impedance is set to 33 ohms. Inline capacitors may be used to AC couple the outputs as needed.

2.1.6 Power

Please follow the recommended schematic for power filtering. Each 0.1µF needs to be placed as close as possible to the respective RC31312A power pin. When using the 5Vin banana, the expected current for 50MHz crystal and all outputs set to LPHCSL (100 ohm) running at 156.25MHz is about 370mA (1.85 W). The 5Vin powers the FTDI, isolators, level shifters, 3 x LDO. Powering VC8 using VDD banana (3.3V), the expected current for the same config is about 360mA (1.19 W).

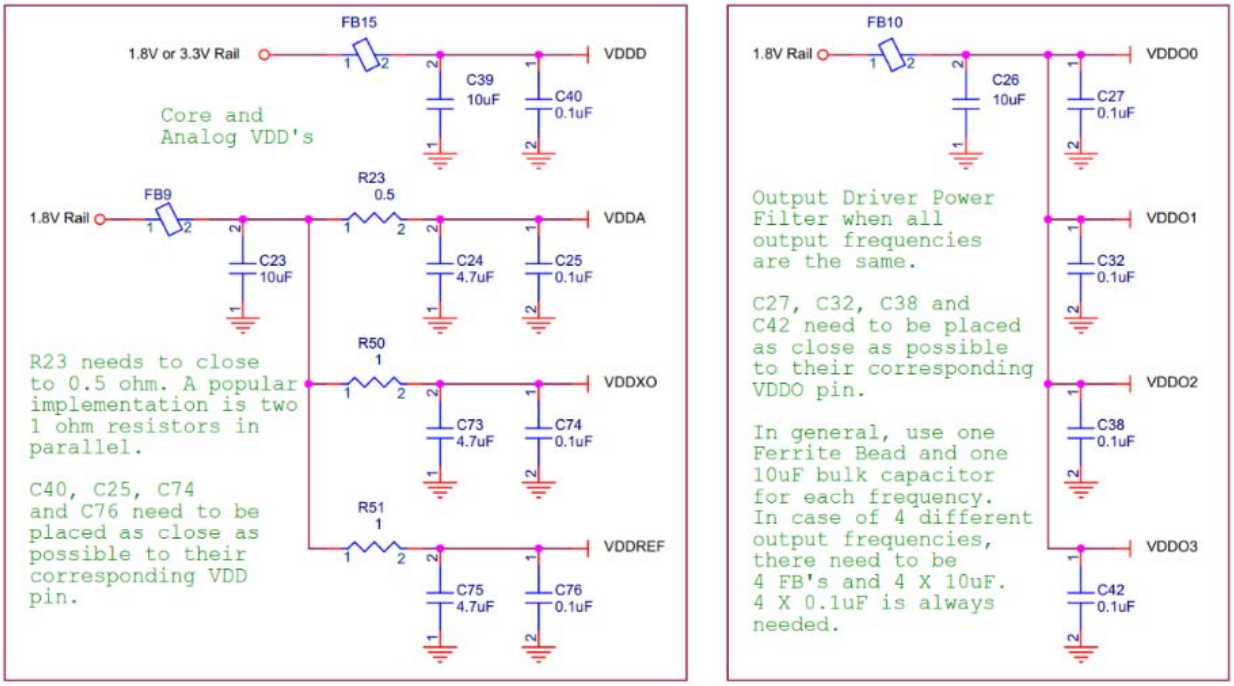


Figure 26. Power Supply Filtering

2.2 Schematic Diagrams and Board files

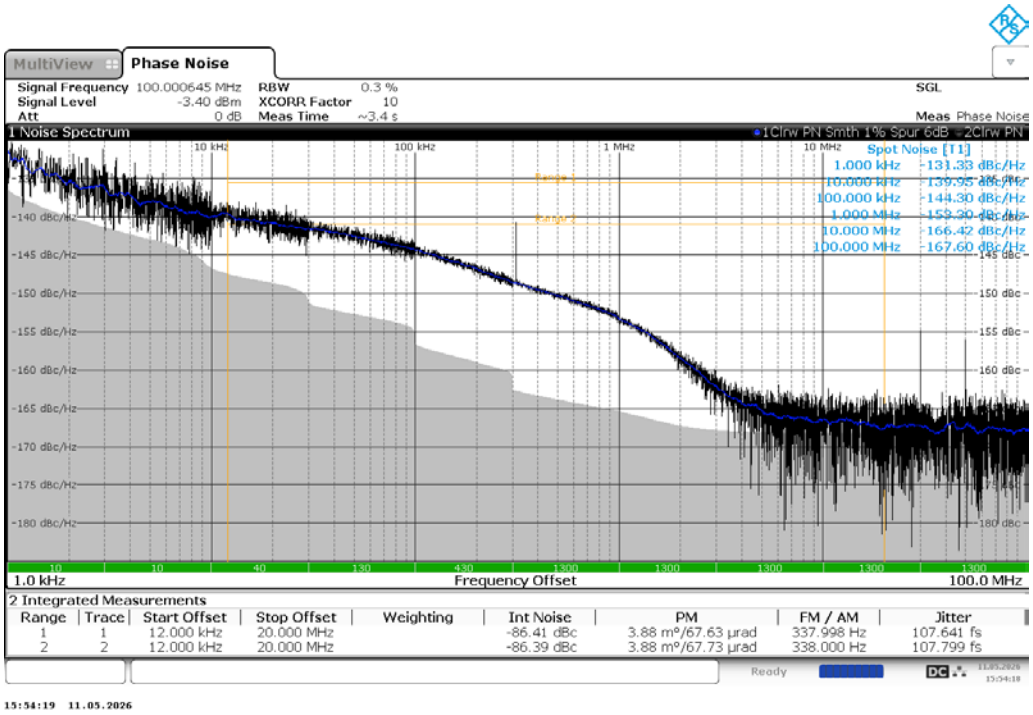
The evaluation board schematics can be found on the landing page of the VersaClock 8 EVK.

2.3 Bill of Materials

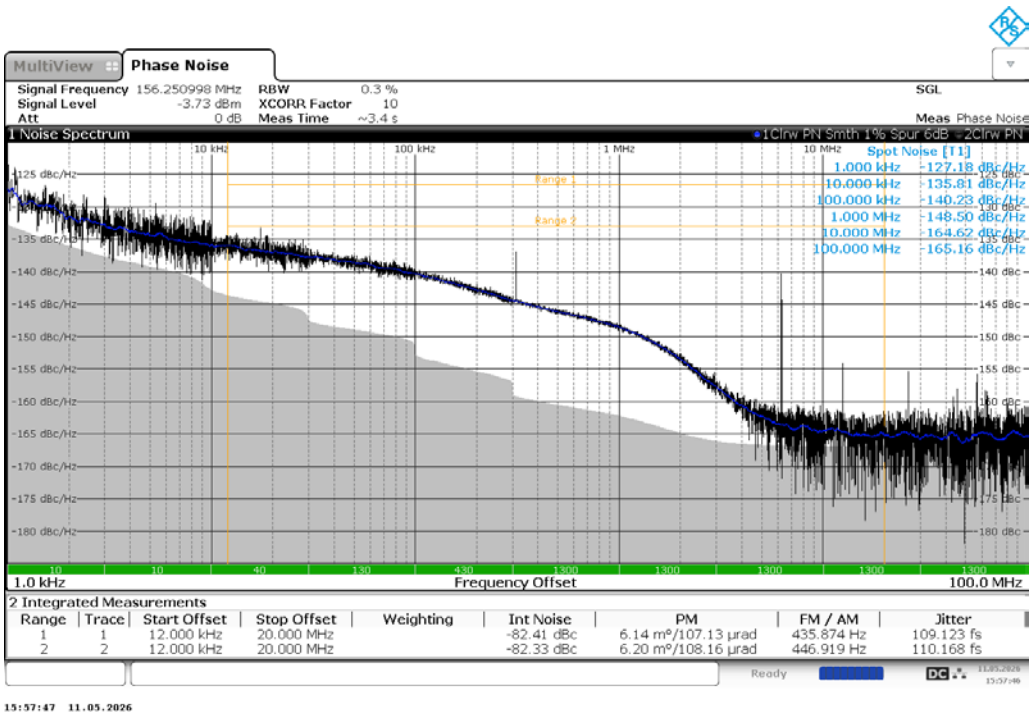
The bill of materials can be found on the landing page of the VersaClock 8 EVK.

3. PN Typical Performance Graphs

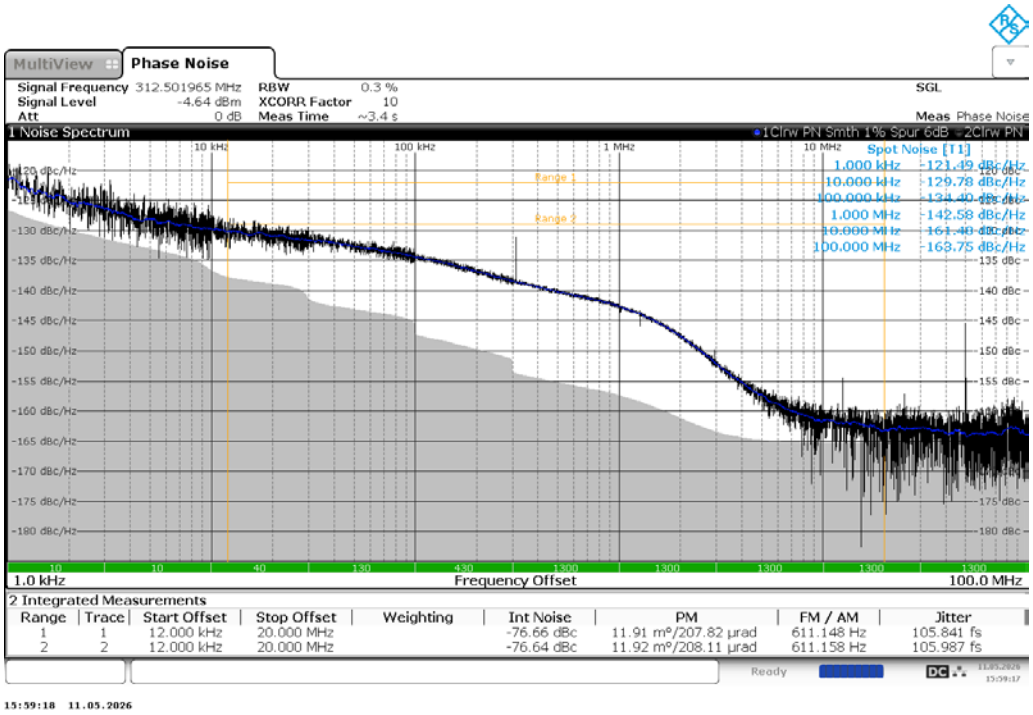
3.1 50MHz Crystal 100MHz OUT3



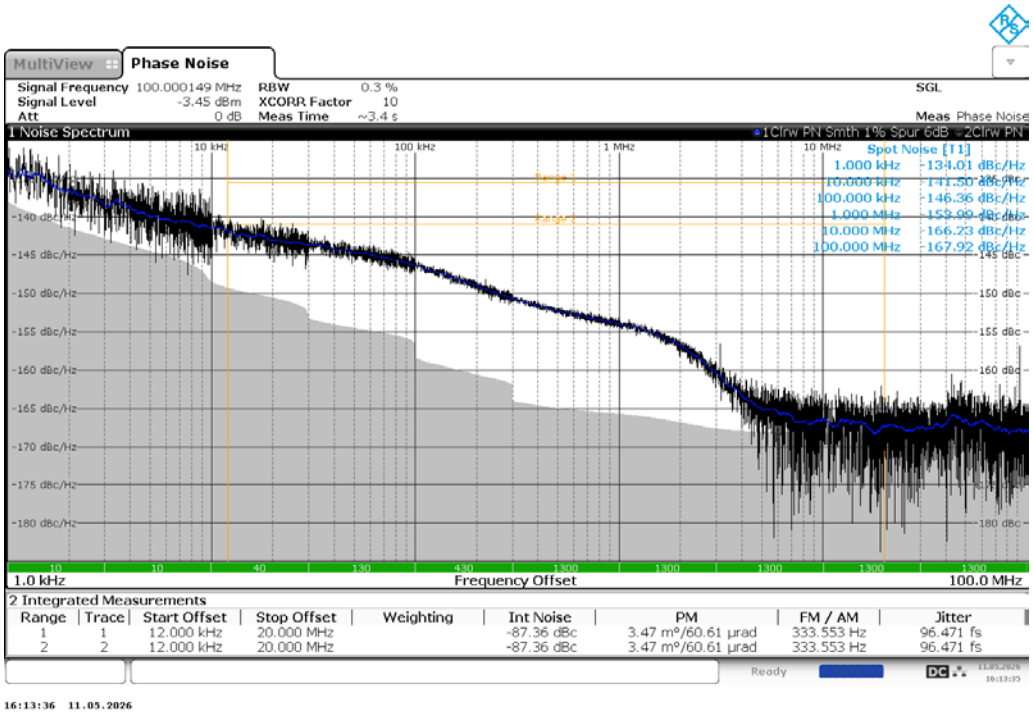
3.2 50MHz Crystal 156.25MHz OUT3



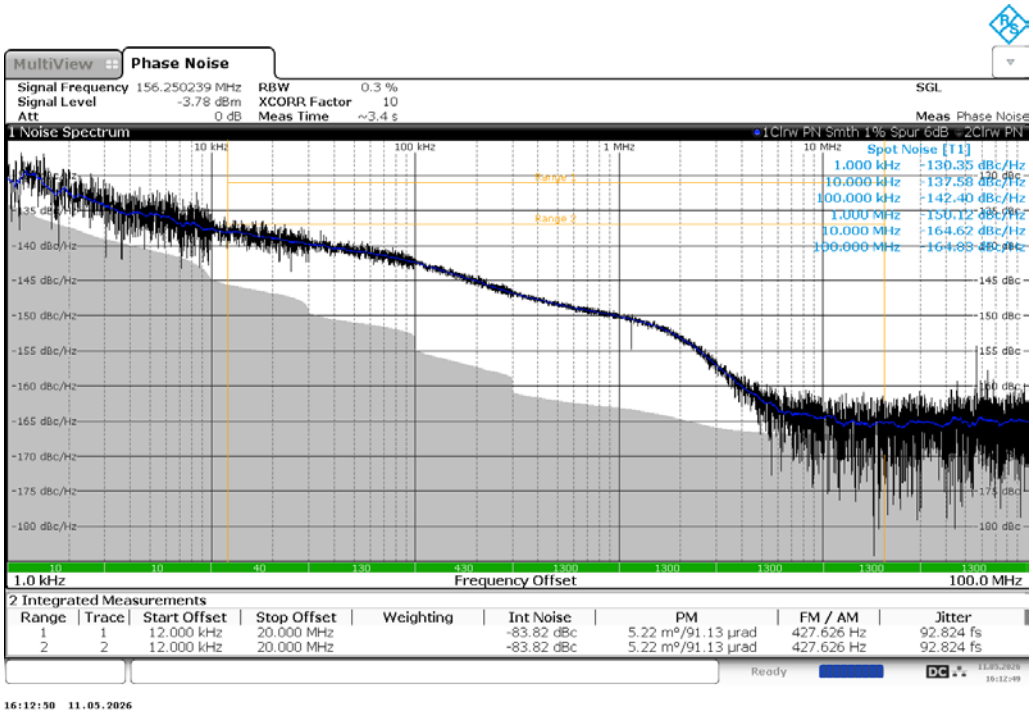
3.3 50MHz Crystal 312.5MHz



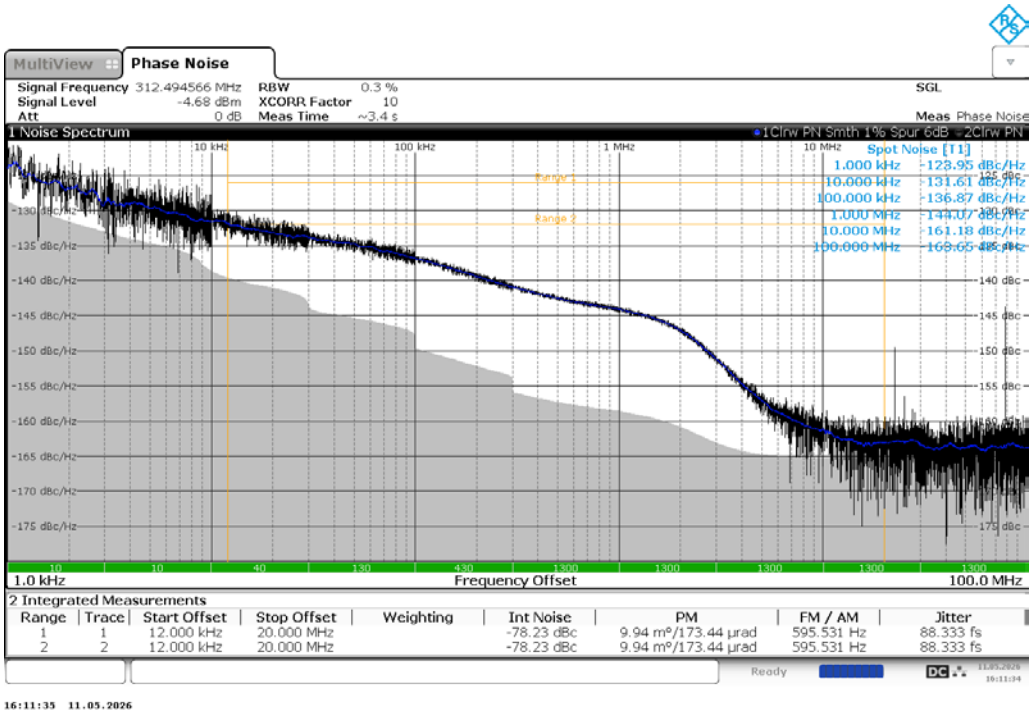
3.4 78.125MHz Crystal 100MHz



3.5 78.125MHz Crystal 156.25MHz



3.6 78.125MHz Crystal 312.5MHz



4. Ordering Information

Part Number	Description
RC31312A-EVK	RC31312A Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Jul 30, 2026	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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