

## RC32508A

**Evaluation Board** 

The RC32508A evaluation board (EVB) is designed to help users evaluate the RC32508A Clock Generator, also known as FemtoClock 2x2. The RC32508A supports jitter attenuator and synthesizer functionality.

When the evaluation board (EVB) is connected via USB to a computer running the Renesas RICBox<sup>™</sup> Software, FemtoClock 2x2 can be configured and programmed to generate frequencies with best-inclass performance. FemtoClock 2x2 has eight output pairs that can be programmed to CMOS, LVDS, or HCSL style outputs.

### Features

- Develop configurations with Renesas RICBox software and upload to the EVB through USB
- Can be powered from the USB connection
- EVB is a combination evaluation with Renesas Low Noise power supply regulators
- Clock input and output pairs are DC coupled

## **Board Contents**

- Renesas RC32508A ultra-low noise synthesizer and jitter attenuator
- Renesas RAA214020 low-noise power supply regulators
- FTDI FT232HQ USB-to-I2C bridge



Figure 1. RC32508A Board

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# 1. Functional Description

## 1.1 Connecting the Board to a Computer

The evaluation board can be connected to a computer via the USB connector (see Figure 2). This board has a USB-C type connector. The on-board USB-to-I2C bridge (FTDI chip) handles the data communication, and the +5V in the USB bus powers the on-board regulators. Using a bench power supply with the V<sub>DD</sub> jacks is optional. The board can fully function with just the USB cable to a computer.

Renesas' *RICBox Software* is used to control the RC32508A on the board. RICBox is compatible with both the on-board USB-to-I2C bridge and the Aardvark adapter. RICBox uses a software wizard for entering the overall configuration and has several tools to fine tune the configuration (for example, block diagram GUI).



Figure 2. Connecting to USB and Aardvark

When the board is shipped, jumpers are assembled for using the on-board FTDI chip.

Both the FTDI chip and the Aardvark adapter require 3.3V levels for the I<sup>2</sup>C bus. For I<sup>2</sup>C control, it is recommended to set VDDD-0 and VDDD-1 to 3.3V.

A FemtoClock 2x2 plugin for the RICBox software is available. Complete the following steps to set up the RC32508A EVB using  $I^2C$ .

- 1. Connect the user computer to the board through USB cable.
- 2. Download and set up the Renesas RICBox Software according to the instructions in the <u>Renesas IC Toolbox</u> (<u>RICBox</u>) Software Manual.
- 3. An I<sup>2</sup>C connection is established between the GUI software and the RC32508A.
- 4. Start a new configuration. Click Create New Project (see Figure 3)



Figure 3. Create New Project Window

5. From the **Select Product Family** section, select the device family that is being used. From the **Select a Product Variant** section, select the working device. Click the *OK* button to open the new configuration.

RENESAS	RICBox* - 🗆 🗙
Select a Product Family	Select a Product Variant
FemtoClock2  Product family	RC32504A
VersaClock7	RC32514A
	8P49N344
	RC22504A
	RC22514A
	RC32508A Select Product
The FemtoClock2 series of Clock Generators and Jitter Attenuators is an excellent cl clocked – the 'point-of-use'. The combination of small size (4x4mm), low power and	hoice for generating and/or cleaning up noisy clock signals right near the device being dexcellent noise performance sets this family in a class by itself
RC22504: Clock Generation	والاستعمال والمتعالية والمتعالية والمتعالية والمتعادية المتعادية المتعادية والمتعادية والمتعادية والمتعادية وا
RC22514: Clock Generation with internal crystal	
RC32504: Jitter Attenuation RC32514: Jitter Attenuation with internal crystal	
	Select OK When Done
	والكالج الكالج الكالج الكالج الكار
التنجدا للالمحداد للالمحداد الالمحداد	Back OK

Figure 4. Select Product Plugin

## 1.2 Board Power Supply

The power source for each  $V_{DD}$  pin can be selected with jumpers. The voltage for each pin, except two pins, is 1.8V. The exception is VDDD-0 and VDDD-1, which can be powered with 1.8V or 3.3V.

The power source can be either an on-board voltage regulator or the white  $V_{DD}$  jack. Most power source selectors have only two choices, 1.8V from an on-board 1.8V regulator or connect to the white  $V_{DD}$  jack. The VDDD selectors have an extra 3.3V choice. The jack can connect to a bench supply. This connection can be useful, for example, to measure supply current into pins. The jack can also be useful to prevent overloading the USB power supply. Total supply current of the board can be up to 800mA. The recommended typical configuration is to use the  $V_{DD}$  jack for each  $V_{DD}$  pin, except the VDDD pins. Connect the VDDD pins to the onboard 3.3V regulator that is powered by the USB bus.

In Figure 5, the source for the pin VDDO0-1 is chosen to be the on-board 1.8V regulator #1. Because of the total expected supply current, there are two 1.8V regulators on the board. It is good practice to use regulator "\_0" for  $V_{DD}$  pins "\_0" and regulator "\_1" for  $V_{DD}$  pins "\_1". This practice ensures the load on the two regulators is similar.



Figure 5. Power Source Selector Example

In Figure 6, the source for the pin VDDD\_1 is chosen to be the on-board 3.3V regulator. J183 allows three choices for VDDD\_1: 1.8V, 3.3V, or the  $V_{DD}$  jack. The jumper position at pins 1–2 is a special test setting that has no use for normal device evaluation.



Figure 6. Power Source Selector for VDDD\_1

## **1.3 Differential Outputs**

The right side of the board has eight SMA pairs for the eight differential outputs. See Figure 7 for an SMA pair example.



Figure 7. Differential Output Pair Example

The board is shipped with the SMA connectors DC coupled to the RC32508 output pins. Output pairs can be programmed to LVDS, HCSL or CMOS logic. In the case of an LVDS output, it is recommended to AC couple before test equipment with a DC coupled  $50\Omega$  termination, like an oscilloscope. A "DC Block" can be inserted at the SMA connector to facilitate the AC coupling.

In the case of an HCSL output, the DC coupling can be beneficial. When the on-chip termination at the driver is disabled, the DC coupling allows for the oscilloscope input to provide the DC coupled termination. When the on-chip termination is enabled, external AC coupling with a "DC Block" can be used, but DC coupling will work as well. Please note that this situation will be double-terminated with a termination both at the source and the destination, resulting in half the specified signal amplitude.

In the case of a CMOS output, the probe point J187 can be used to connect a high impedance probe. The short traces to the SMA connectors will be open stubs and can create a small reflection. When this interferes with measurements, R291 and R292 can be opened to disconnect the stub. Nothing will be assembled on the R291 and R292 footprints but the footprints are shorted with a thin trace. To be able to use the footprint or to open the footprint, cut the thin trace that shorts the footprint.

After opening the R291 and R292 footprints,  $0.1\mu$ F capacitors can be placed to create AC coupling on the board. This avoids having to insert "DC Block" devices.

*Note*: This will not work with HCSL where the on-chip termination is disabled. The HCSL driver needs to see a DC path to ground. When adding AC coupling capacitors on the board, HCSL can only be used with the on-chip termination enabled.

## **1.4 Differential Inputs**

The SMA connectors for the differential input CLKIN are DC coupled to the CLKIN and nCLKIN pins on the RC32508A device (see Figure 8). There is no termination assembled on the board. When needed, on-chip termination can be enabled. On-chip termination can be used with HCSL and LVDS style clocks. In the case of LVDS, it is recommended to AC couple the differential clock and use the DC Bias option of the RC32508A device to set the desired common mode voltage for the CLKIN input. This way, the CLKIN input can handle almost any differential swing from 300mVppdiff to 2400mVppdiff (0.15 ~ 1.2Vpp single ended).



Figure 8. CLKIN/nCLKIN Differential Input

In the case of LVCMOS, use a 1.8V amplitude single-ended clock at CLKIN. For LVCMOS, the on-chip termination at the CLKIN input can be disabled. It is actually possible to have an LVCMOS clock at CLKIN and another LVCMOS clock at nCLKIN where CLKIN is the primary clock and nCLKIN is the secondary (backup) clock, in case of a Jitter Attenuator configuration.

## 1.5 On-Board Crystal

The evaluation board does not come with crystals pre-assembled. However, there are footprints for crystals on the bottom side of the board.



Figure 9. XIN Inputs

The SMA connector XIN\_REF0 AC couples to the pin XIN/REF-0 and the SMA connector XIN\_REF1 AC couples to the pin XIN/REF-1 of the RC32508A device. A clock can be used to overdrive XIN. When deciding to use an actual crystal for XIN/REF-0 / XOUT-0, ensure to remove the AC coupling capacitor assembled at R10 to disconnect the PCB trace to J25.

XIN\_REF1 can be used for loop back of a clock from APLL0 to APLL1. This is mostly used with jitter attenuator configurations where APLL0 is doing the jitter attenuation and APLL1 acts as a fanout synthesizer to create more clock outputs.

## 1.6 Setup and Configuration

Complete the following steps to start the configuration of the board.

1. When creating a new configuration, the wizard page is the first screen to appear (see Figure 10). The wizard contains a pull-down list of configuration pages (located in the upper right-hand corner of the window) pertaining to different sections of the device that require overall configuring.

RENESAS	RICBO	x*.	- 🗆 X
Configuring RC32508A			1 of 3 Inputs •
Operation Mode APLL-0 Reference APLL-1 Reference XIN/REF-0 Frequency Load Capacitance (p ClxIN/REF-1 Frequency Load Capacitance (p CLKIN/nCLKIN Input Mode CLKIN Frequency nCLKIN Frequency	50MHz C	the input to the analog I source to generate the o using the APLL Reference Jitter Attenuator - The of XIN pin as the input to t as reference for the digi available when this mod XIN/REF-0 - Configure tt REF-0 pin. The frequency • XIN/REF-1 - Configure tt REF-1 pin. The frequency • CLKIN/nCLKIN - Configure CLKIN pin (and optional	is configured to use a single clock source as PLL (APLL). The APLL then uses that clock butputs. The reference source is selected by e mux and can come from either XIN or CLKIN. evice is configured to use the reference for the he APLL and the clock source at the CLKIN pin tal PLL (DPLL). The DPLL settings will become e is selected. he settings for the clock reference at the XIN/ y may range from 25MHz to 80MHz. he settings for the clock reference at the XIN/ y may range from 25MHz to 80MHz. re the settings for the clock reference at the y nCLKIN for LVCMOS mode). Set the signal node menu and adjust the frequency between
Cancel			Next Finish

Figure 10. Wizard Page Navigation Window

2. If **Jitter Attenuator** mode is selected, the jitter attenuator configuration window (screen 2 of 3) appears with a list of settings (see Figure 11). If *Synthesizer* mode is selected, the jitter attenuator window is skipped and the user is then directed to the **Output Clocks** window (screen 3 of 3) See Figure 12.

RENESAS	RICBox*	×
Configuring RC32508A		2 of 3 DPLL -
DPLL Profile Bandwidth Normal Bandwidth Goal Actual: ~23.8203Hz (-4.71899 Acquire Bandwidth Goal Actual: ~22.3226Hz (-11.070 Decimator Decimator Decimator Bandwidth Goal Actual: ~0.1804 (-9.7888% fro Acquire Gain Peaking Goal Actual: ~0.192 (-3.9756% fro	250Hz 9% from goal of 250Hz) 2.5kHz 0.2 0.2 0.2 0.2 1 1 1 1 1 1 1 1 1 1	• The DPLL profile drop-down allows for quick configuration of the Renesas timing device for specific ITU-T equipment clock recommendations. Selecting a specific profile will configure the device the same way Renesas tests for ITU-T equipment clock compliance in our labs. Modifications to the configuration can be made, but care must be taken to make sure compliance is not broken. For more complex clock trees, please contact Renesas for additional support.     • Jitter Attenuator =================================
Phase Slope Limit	Name ns/sec	to synchronous equipment designed to interwork with networks optimized for the 2048 kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 8-5 of IITU-T G.8031.
Cancel	Nono II 🖌 I nS/Sec	Previous Next Finish

#### Figure 11. Jitter Attenuator Mode Settings Window

- 3. The Output Clocks window (screen 3 of 3) sets up the outputs (see Figure 12).
  - a. Fill in the desired output frequencies. Leave blank unused outputs.
  - b. Click on Advanced Settings at the red arrow to select Logic Type and Signal Amplitude.
  - c. Click *Finish* to end the Wizard and enter the main configuration utility.

RICBO	x* — 🗆
onfiguring RC32508A	3 of 3 Outputs
Output Clocks (MHz)	VCO Frequency – This indicates the frequency that the internal VCO runs at inside the APLL. The target frequency is automatically adjustee
APLL-0 APLL-0 Frequency 10GHz OUT0-0 156.25   OUT0-0 156.25   OUT0-1 None   powered down (Hi-Z)	<ul> <li>Adjust the output and input frequency settings. The frequency range available is 9.7GHz to 10.7GHz.</li> <li>Adjust the output frequency by entering the desired frequency in the available space. This can range from 10MHz to 1GHz for a differential signal and up to 180MHz for LVCMOS. Leaving this blank will disable and power down the output.</li> <li>Press the settings button next to the output frequency entry field to configure the outputs even further. Use the mode menu to change th output signal type.</li> </ul>
OUT0-2 None ef to powered down (Hi-Z) powered down (Hi-Z)	
APLL-1	
APLL-1 Frequency 10.625GHz OUT1-0 None powered down (Hi-Z) OUT1-1 None powered down (Hi-Z)	
	Previous Finish





Figure 13. Block Diagram

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 The side panel consists of five separate buttons. The buttons on the top left are Control Panel (the above screen), Wizard, Configuration, Registers, and Block Diagram. For more information, see the <u>Renesas IC</u> <u>Toolbox (RICBox) Software Manual</u>.



Figure 14. Side Panel Buttons

5. Transfer the Configuration from RICBox into the FemtoClock 2x2 device:

The bottom right of the screen has buttons to control the I<sup>2</sup>C connection with the device.

a. Click the Not Connected button to connect. Click the Connect button to the right of Program to connect.



Figure 15. Device Connection

b. Once fully connected to a device, the connection button will be illuminated green.



Figure 16. Connected Button Illuminated

c. The **Connection Settings** screen allows you to select a specific device and connect. After attempting to connect, the small *Connected* button turns green to indicate that the connection was successful. Now click *Program* to transfer all settings to the device.



Figure 17. Program Button

## 2. Board Design



Figure 18. RC32508A EVB – Block Diagram

Each differential output clock is available on a pair of SMA connectors. Each pair of SMA connectors is DC coupled to the output pair pins.

Power is provided through the USB connection and regulated with RAA214020 low noise LDOs. Each power pin can also be switched to a banana plug jack for supply current measurements or relieve the USB port from most of the supply current.

The board has an FTDI USB-to-I2C bridge for programming FemtoClock 2x2 from a computer. Renesas RICBox software is available for easy development of configurations.

The LOCK pins drive LEDs and the LEDs light up when the pin is high. Default function assigned to a LOCK pin is "APLL Lock" so the LED shows if the APLL is locked or not. Several other status items can be assigned to the LOCK pin.



Figure 19. RC32508A Board – Top View

#### Table 1. RC32508A – EVB Pins and Functions

Note: See Figure 19 for reference numbers in the following table.

Ref.	Name	On-Board Connector Label	Function
1	Output0_0	J65, J66	Differential Clock Output 0-0
2	Output0_1	J63, J64	Differential Clock Output 0-1
3	Output1_0	J61, J62	Differential Clock Output 1-0
4	Output1_1	J59, J60	Differential Clock Output 1-1
5	Output2_0	J57, J58	Differential Clock Output 2-0
6	Output2_1	J55, J56	Differential Clock Output 2-1
7	Output3_1	J53, J54	Differential Clock Output 3-1
8	Output3_0	J51, J52	Differential Clock Output 3-0
9	RC32508A	U7	FemtoClock 2x2 DUT
10	XIN_REF0	J25	Clock Input to overdrive XIN/REF-0
11	XIN_REF1	J29	Clock Input to overdrive XIN/REF-1
12	CLKIN	J33, J35	Differential Reference Clock Input
13	USB Interface	U10	USB-C Type Jack for connection with the computer and interaction with Renesas RICBox Software.
14	RAA214020	U6, U22, U23	Low Noise Voltage Regulators
15	VDDREF	J240	Power Source Selector for pin VDDREF
16	VDDD_0	J239	Power Source Selector for pin VDDD-0 (Digital VDD)
17	VDDD_1	J183	Power Source Selector for pin VDDD-1 (Digital VDD)
18	VDDO3_1	J237	Power Source Selector for pin VDDO3-1
19	VDDO3_0	J181	Power Source Selector for pin VDDO3-0
20	VDDO2_1	J180	Power Source Selector for pin VDDO2-1
21	VDDO2_0	J200	Power Source Selector for pin VDDO2-0
22	VDDO1_1	J179	Power Source Selector for pin VDDO1-1
23	VDDO1_0	J199	Power Source Selector for pin VDDO1-0
24	VDDO0_1	J178	Power Source Selector for pin VDDO0-1
25	VDDO0_0	J198	Power Source Selector for pin VDDO0-0
26	VDDA_1	J182	Power Source Selector for pin VDDA-1
27	VDDA_0	J238	Power Source Selector for pin VDDA-0
28	VDDXO_0	J197	Power Source Selector for pin VDDXO-0
29	VDDXO_1	J176	Power Source Selector for pin VDDXO-1
30	GND Jack	J222	Jack for external Power Supply Ground



Ref.	Name	On-Board Connector Label	Function
31	VDD Jack	J201	Jack for external Power Supply VDD
32	VEE Jack	J6	Jack for external VEE connection For factory testing only. Is connected to GND by default.
33	GND Jack	J5	Jack for external Power Supply Ground

## 2.1 Schematic Diagrams



Figure 20. RC32508A Evaluation Board Schematics – Page 1



Figure 21. RC32508A Evaluation Board Schematics – Page 2



Figure 22. RC32508A Evaluation Board Schematics – Page 3



# 3. Ordering Information

Part Number	Description
RC32508A-EVK	RC32508A Evaluation Board; A-male to USB-C cable.

# 4. Revision History

Revision	Date	Description
1.00	Aug 11, 2023	Initial release.

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