

RZ SMARC Series Carrier Board II

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (<http://www.renesas.com>).

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Renesas RZ SMARC CARRIER II Disclaimer

By using this RZ SMARC CARRIER II, the User accepts the following terms, which are in addition to, and control in the event of disagreement, with Renesas' General Terms and Conditions available at <https://www.renesas.com/en-us/legal/disclaimer.html>.

The RZ SMARC CARRIER II is not guaranteed to be error free, and the entire risk as to the results and performance of the RZ SMARC CARRIER II is assumed by the User. The RZ SMARC CARRIER II is provided by Renesas on an "as is" basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of good workmanship, fitness for a particular purpose, title, merchantability, and non-infringement of intellectual property rights. Renesas expressly disclaims any implied warranty.

Renesas does not consider the RZ SMARC CARRIER II to be a finished product and therefore the RZ SMARC CARRIER II may not comply with some requirements applicable to finished products, including, but not limited to recycling, restricted substances and electromagnetic compatibility regulations. Refer to Certifications section, for information about certifications and compliance information for the RZ SMARC CARRIER II. It is the kit User's responsibility to make sure the kit meets any local requirements applicable to their region.

Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RZ SMARC CARRIER II, even if Renesas or its affiliates have been advised of the possibility of such damages.

Renesas has used reasonable care in preparing the information included in this document, but Renesas does not warrant that such information is error free nor does Renesas guarantee an exact match for every application or parameter to part numbers designated by other vendors listed herein. The information provided in this document is intended solely to enable the use of Renesas products. No express or implied license to any intellectual property right is granted by this document or in connection with the sale of Renesas products. Renesas reserves the right to make changes to specifications and product descriptions at any time without notice. Renesas assumes no liability for any damages incurred by you resulting from errors in or omissions from the information included herein. Renesas cannot verify, and assumes no liability for, the accuracy of information available on another company's website.

Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Introduction	8
1.1 Kit Contents	10
1.2 Assembly	12
2. System Description	13
2.1 Functional Block	15
2.1.1 G3S SMARC EVK.....	15
2.1.2 G3E SMARC EVK.....	16
2.2 Interface Mapping	17
2.2.1 G3S SMARC EVK.....	17
2.2.2 G3E SMARC EVK.....	19
2.3 Board Configuration and Status	21
2.3.1 VBUS_SEL – Main Power	21
2.3.2 VBAT_SEL – VDD_RTC Power	22
2.3.3 SW_PWR_12V – PCIe Slot Power.....	23
2.3.4 RSVD_PWR – Module Power	24
2.3.5 PMOD_PWR_SEL – PMOD Power.....	25
2.3.6 SW_PMOD0_PWR_SLP – PMOD Power/Sleep Control	26
2.3.7 SW_GPIO_OPT_SEL – GPIO Options	27
2.3.8 SW_GPIO_CAN_PMOD – CAN Standby.....	28
2.3.9 SW_MODE – Boot Mode (and Power)	29
2.3.10 SW_M2_DIS – M.2 Card Control Signals.....	30
2.3.11 SW_OPT_MUX.....	32
2.3.12 SW_PCIE_MUX.....	34
2.4 User IO	37
2.4.1 Push Buttons.....	37
2.4.2 LED Indicators	38
2.5 Recommended Operating Condition	39
3. Functional Specifications	40
3.1 Power.....	40
3.1.1 USB-C – Main Power.....	42
3.1.2 BAT_RTC – VDD_RTC Power	42
3.1.3 PWR 12V EXT – PCIe Slot Power.....	42
3.2 Clock.....	43
3.3 Serial UART.....	44
3.3.1 SER1_UART	44
3.3.2 SER3_UART	44

3.4	USB.....	45
3.5	Ethernet	45
3.6	Camera	46
3.6.1	Pi Camera Adaptor	47
3.7	PMOD	49
3.8	Audio.....	50
3.9	CAN	51
3.10	microSD1 Card Interface	51
3.11	M.2.....	52
3.11.1	M.2 Key E	52
3.11.2	M.2 Key B	53
3.12	Display	55
3.12.1	HDMI	55
3.12.2	DISP0 and DISP1	55
3.13	I2C	58
3.13.1	I2C_PM	58
3.13.2	I2C_GP	59
3.13.3	I2C_CAM0, I2C_CAM1	60
3.13.4	I2C_LCD	60
3.13.5	HDMI_CTRL	60
3.14	Miscellaneous.....	61
3.14.1	FAN	61
3.14.2	GEN_PURPOSE I/O	61
3.14.3	M2B_GPIO.....	62
3.14.4	M2B SIM	62
3.15	SMARC Module Connector	63
3.15.1	Display Interfaces	63
3.15.2	Camera Interfaces	65
3.15.3	SDIO Card (4-bit) Interface	65
3.15.4	SPI Interfaces	66
3.15.5	Audio	67
3.15.6	I2C Interfaces.....	67
3.15.7	Asynchronous Serial Ports.....	68
3.15.8	CAN Bus	68
3.15.9	USB Interfaces	69
3.15.10	PCI Express	69
3.15.11	SATA.....	69
3.15.12	Ethernet.....	70
3.15.13	GPIO	71

4. Certifications72

4.1 EMC/EMI Standards72

4.2 Material Selection, Waste, Recycling and Disposal Standards.....73

4.3 Safety Standards73

REVISION HISTORY74

1. Introduction

The RZ SMARC Series Carrier Board II (hereinafter referred to as "RZ SMARC Carrier II") is an 8-layer 190 × 130 mm PCB, a platform designed according to the SMARC 2.1.1 Specification providing a carrier for Renesas RZ SMARC Module Boards.

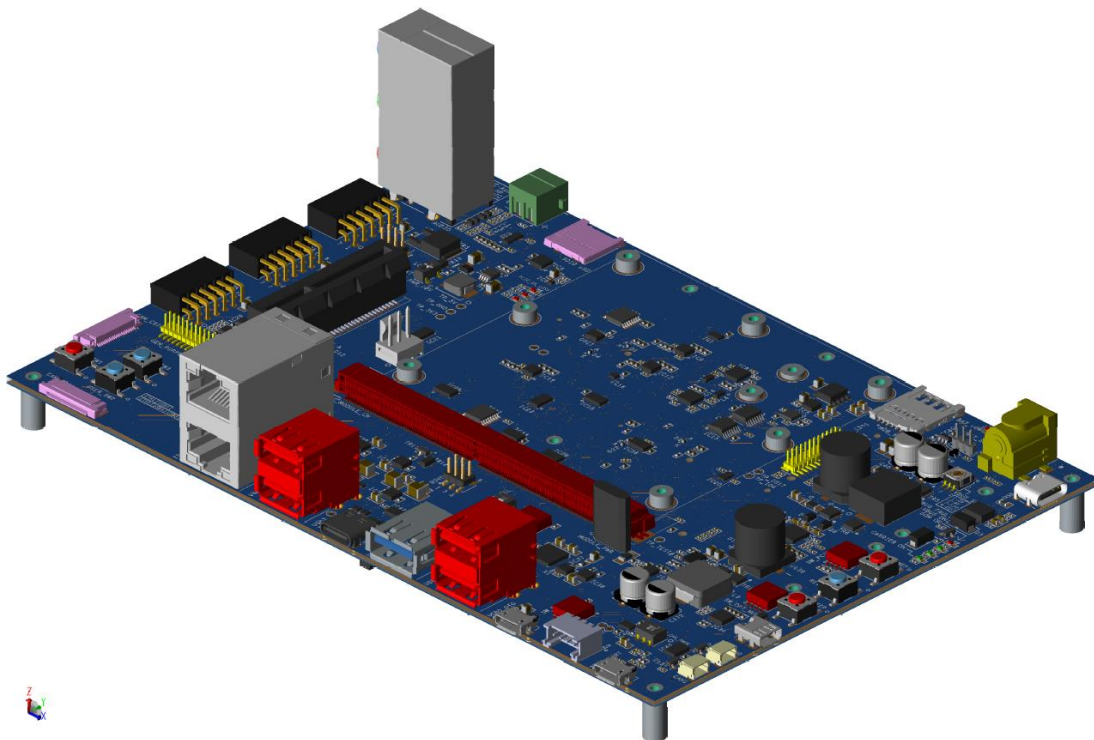
Basically, the RZ SMARC Carrier II is connected to the Renesas RZ/G3S SMARC Module board (hereinafter referred to as "G3S SMARC Module") (*1) and used as the RZ/G3S SMARC Evaluation Board (hereinafter referred to as "G3S SMARC EVK").

This guide is based on a combination of the RZ SMARC Carrier II and the G3S SMARC Module.

This guide includes system setup and configuration. This guide also provides detailed information on the overall design and use of the RZ SMARC Carrier II from a hardware system perspective.

Details of the Renesas RZ SMARC Module boards are to be found in the **RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals**.

Note 1. Other target module boards that can be connected to the RZ SMARC Carrier II are below:
 Renesas RZ/G3S Secure SMARC Module board
 Renesas RZ/G3E SMARC Module board (hereinafter referred to as "G3E SMARC Module")



Note: The colors in this image differ from the actual product.

Figure 1.1 RZ SMARC Series Carrier Board II

The key features of the RZ SMARC Carrier II are as follows.

Board Features	Details
Power supply	USB Type-C with USB-PD support (input range: 5V2A to 20V4A)
Memory	Micro SD card slot with default, high-speed, UHS-I/SDRR50, SDR104 transfer modes support
Supported interface and peripherals	4x USB2.0 Type A
	1x USB2.0 Type microAB
	1x USB3.0 Type A
	1x USB3.0 Type C
	Speaker, Headphone, Microphone, Auxiliary
	2x Gigabit Ethernet interface supporting 10/100/1000 Mbps data rate on the RJ45 connector
	PCIe 4-lane slot
	M.2 Key E interface
	M.2 Key B interface and SIM card interface
	2x CAN interface
	2x UART interface for debugging (1 is micro-USB)
	2x LVDS/MIPI-DSI display connector
	HDMI interface
	2x MIPI CSI-2 camera connector
	3x PMOD connectors (Type-2A SPI, Type-3A UART and Type-6A I2C)
Expansion connectors/headers	Coin cell battery holder
	GPIO pin header
	GPIO pin header for M.2 Key B
	ISL28022FRZ current monitor for the module power supply
Board dimensions	190 mm (W) * 130 mm (L), 8-layer

1.1 Kit Contents

If you have purchased the RZ/G3S SMARC Evaluation Board Kit (P/N: RTK9845S33S01000BE or RTK9845S37S01000BE), your contents will include:

- RZ/G3S SMARC Carrier Board II
- USB Type-A to USB Micro B cable for serial debugging
- Accessories bag:
 - 2 off M2.5 × 6 mm pan-head machine screws (for securing M.2 cards)
 - 1 off 2.5 mm spacer (for securing M.2 key B cards)
- RZ/G3S SMARC Module Board (hereinafter referred to as “G3S SMARC Module”)
- RZ SMARC Series JTAG Adaptor Cable (hereinafter referred to as “SMARC JTAG Adaptor”)

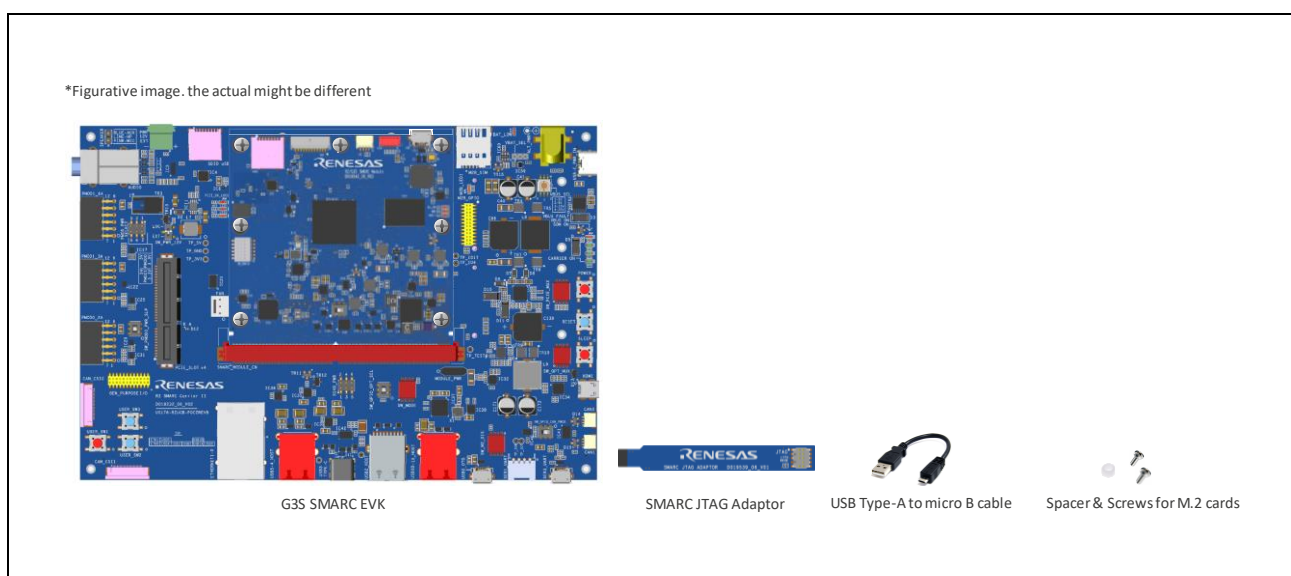


Figure 1.2 RZ/G3S SMARC Evaluation Board Kit Contents

If you have purchased the RZ/G3E SMARC Evaluation Board Kit (P/N: RTK9947E57S01000BE), your contents will include:

- RZ SMARC Series Carrier Board II
- Fitted with the RZ SMARC Series Dual LVDS to HDMI Adaptor Board to DISP0 and DISP1 (hereinafter referred to as “SMARC Dual LVDS-HDMI Adaptor”)
- RZ SMARC Series Pi Camera Adaptor Board (hereinafter referred to as “SMARC Pi Camera Adaptor”)
- USB Type-A to USB Micro B cable for serial debugging
- Accessories bag:
 - 2 off M2.5 × 6 mm pan-head machine screws (for securing M.2 cards)
 - 1 off 2.5 mm spacer (for securing M.2 key B cards)
- RZ/G3E SMARC Module Board (hereinafter referred to as “G3E SMARC Module”)
- RZ SMARC Series Breakout Adaptor Board (hereinafter referred to as “SMARC Breakout Adaptor”)
- RZ SMARC Series Parallel to HDMI Adaptor Board (hereinafter referred to as “SMARC RGB-HDMI Adaptor”)
- Heat spreader*¹
- Thermal pads

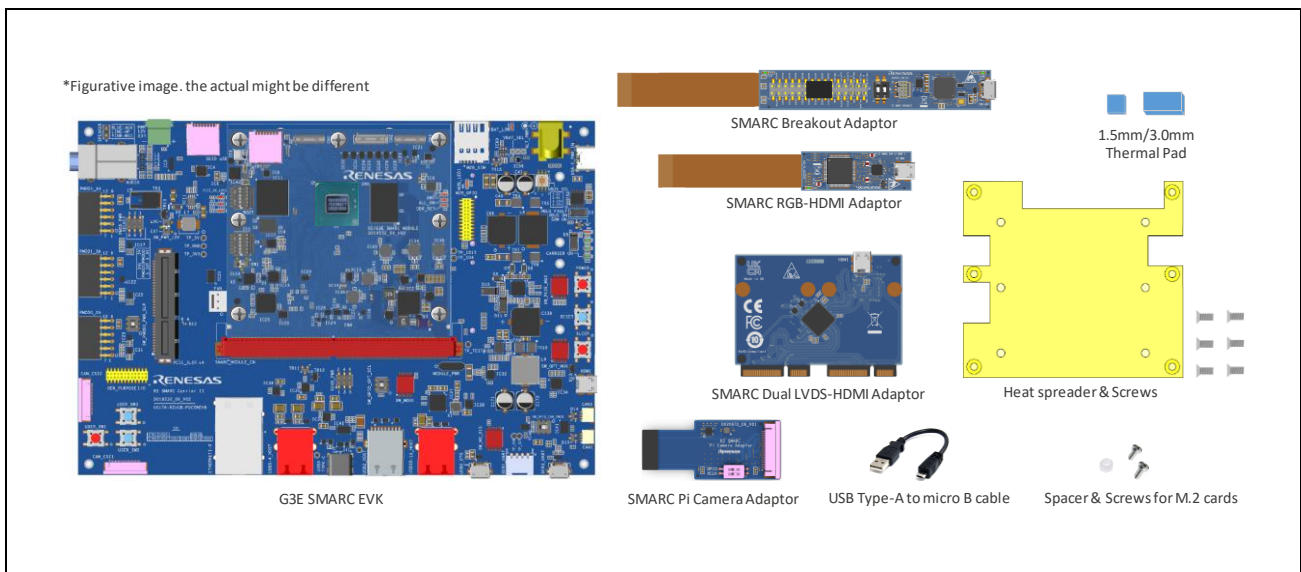


Figure 1.3 RZ/G3E SMARC Evaluation Board Kit Contents

NOTE

The heat spreader will have been fitted to the Module and Carrier Board using 6 off pozi countersunk head machine screws.

*1. For installation of the heat spreader, refer to the *RZ/G3E SMARC Module User Manual*.

1.2 Assembly

The RZ SMARC Carrier II can only be used when fitted with a SMARC compliant Module board.

Secure the Module using 7 off M2.5 × 4 mm pan-head machine screws (provided).

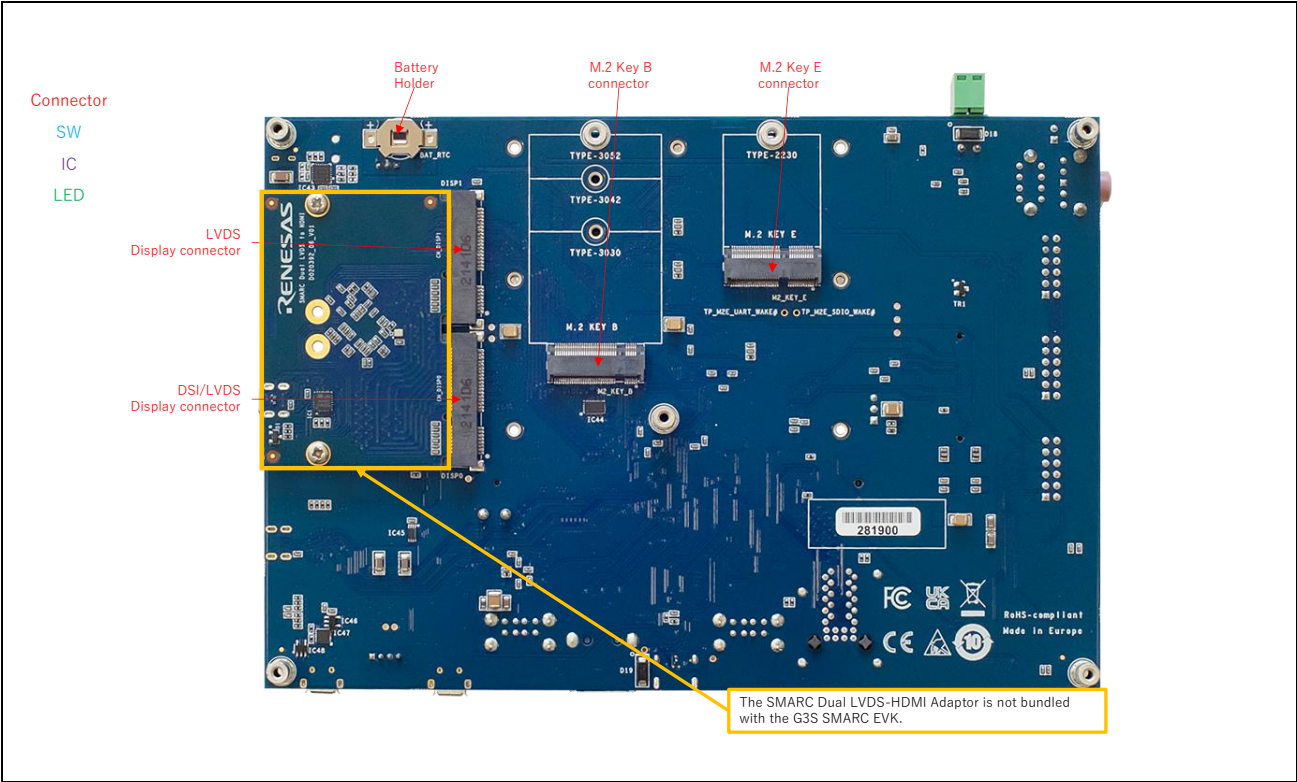


Figure 2.2 RZ SMARC Series Carrier Board II Bottom View

2.1 Functional Block

2.1.1 G3S SMARC EVK

Figure 2.3 shows the functional block diagram of the G3S SMARC EVK. ICs, connectors, and switches surrounded by red frames indicate functions used on the RZ SMARC Carrier II.

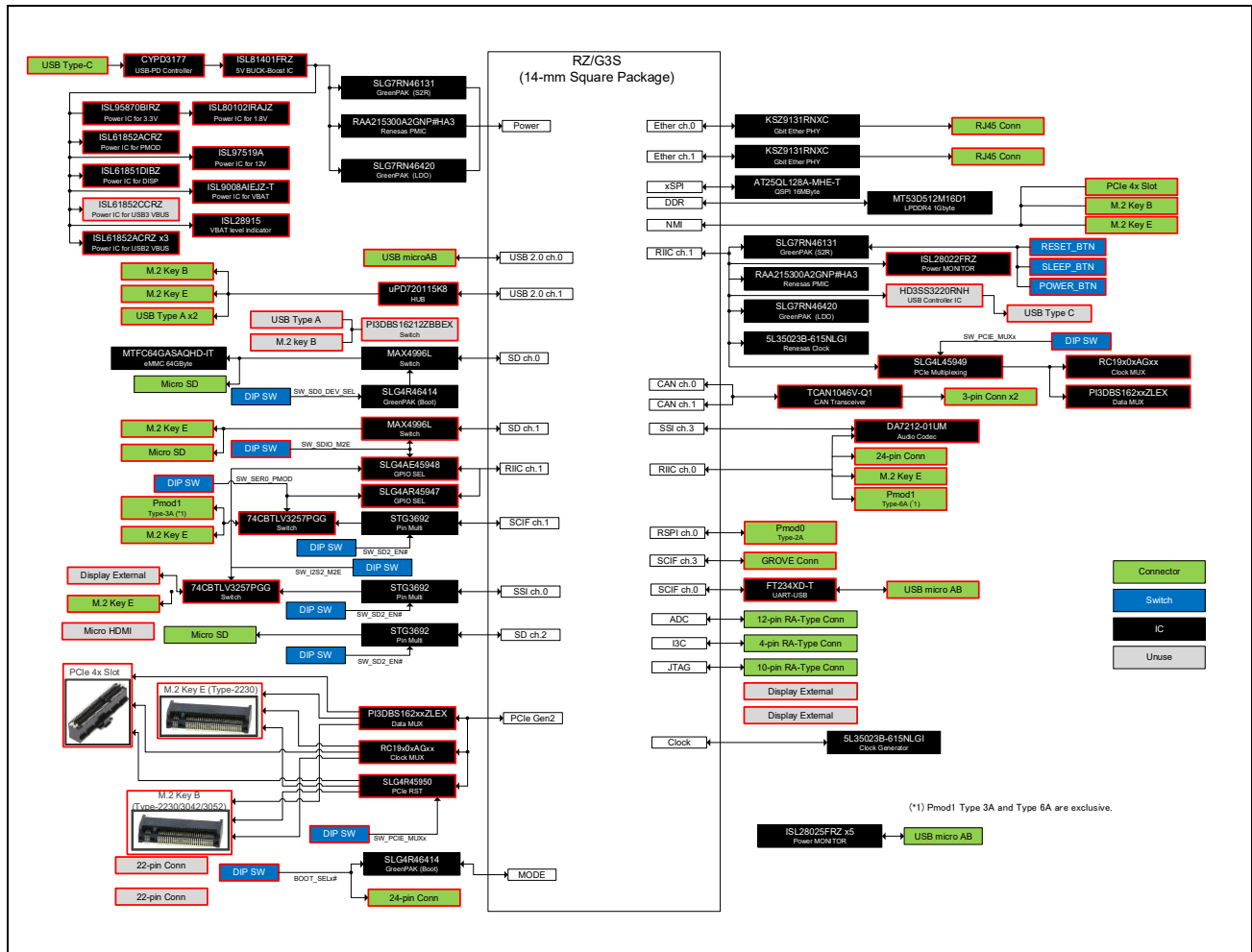


Figure 2.3 G3S SMARC EVK Block Diagram

2.1.2 G3E SMARC EVK

Figure 2.4 shows the functional block diagram of the G3E SMARC EVK. ICs, connectors, and switches surrounded by red frames indicate functions used on the RZ SMARC Carrier II.

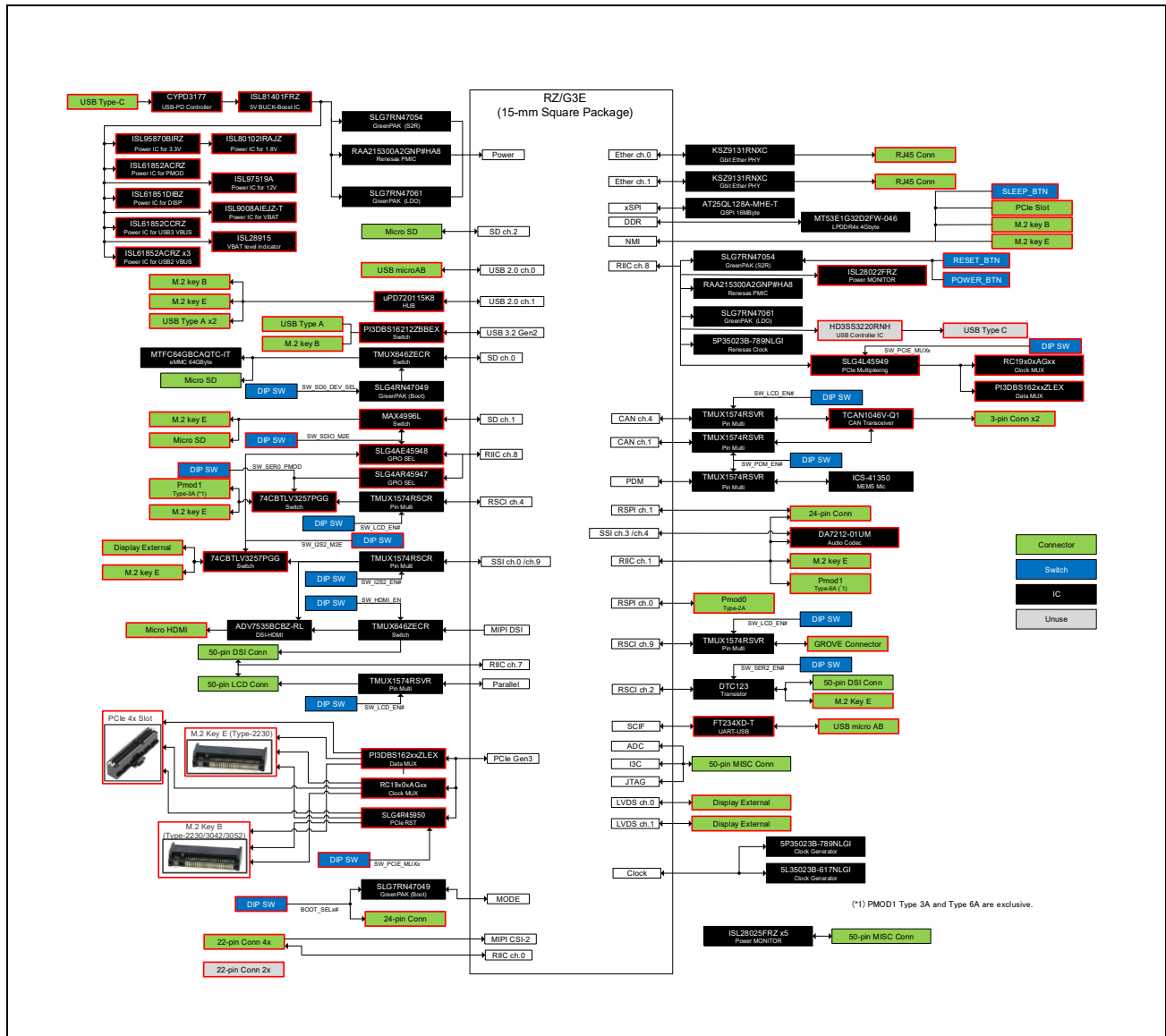


Figure 2.4 G3E SMARC EVK Block Diagram

2.2 Interface Mapping

Renesas parts are highlighted.

2.2.1 G3S SMARC EVK

Table 2.1 Interface Mapping (1/2)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description
USB0	USB2.0 ch0	629105150921	USB2.0 Type-microAB receptacle
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB2.0 Hub IC
		72309-8014BLF	USB2.0 Type-A receptacle
USB2	—	692122030100	USB3.0 Type-A receptacle
USB3	—	1054500101	USB3.0 Type-C receptacle
USB4	—	72309-8014BLF	USB2.0 Type-A receptacle
USB5	—	72309-8014BLF	USB2.0 Type-A receptacle
CAN0	CAN ch0	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
CAN1	CAN ch1	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
I2S0	SSI ch3	DA7212-01UM	Audio Codec
		STX-4335-5BGP-S1	Connector for Stereo Headphone, Stereo Mic, Aux
		M20-9990246	Pin header for speaker
I2S2	SSI ch0	MDT420E01001	M.2 Key E for I2S interface
SPI0	—	GRPB122VWQS-RC	24-pin header
SPI1	RSPI ch0	SSW-106-02-T-D-RA	PMOD Type-2A connector
SER0	SCIF ch1	SSW-106-02-T-D-RA	PMOD Type-3A connector ^(*)
		MDT420E01001	M.2 Key E ^(*)
SER1	SCIF ch3	110990037	Grove connector
SER2	—	MDT420E01001	M.2 Key E ^(*)
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC
		629105150921	USB2.0 Type-microAB receptacle for UART Debug
PCIE_A	PCIe Gen2	10061913-111PLF	PCIe 4x Slot
		MDT420B01001	M.2 Key B
		MDT420E01001	M.2 Key E
		78646-3001	SIM card for M.2 Key B
SATA	—	GRPB122VWQS-RC	GPIO pin header
HDMI	—	46765-1301	Micro HDMI connector
LVDS0	—	2041262-1	Mini PCI Express & mSATA connector
LVDS1	—	2041262-1	Mini PCI Express & mSATA connector
CSI0	—	2-1734592-2	22-pin FPC connector
CSI1	—	2-1734592-2	22-pin FPC connector
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector

Table 2.1 Interface Mapping (2/2)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description
I2C_GP	RIIC ch0	GRPB122VWQS-RC	GPIO pin header
		MDT420B01001	M.2 Key E for I2C interface
		DA7212-01UM	Audio Codec for I2C interface
		SSW-106-02-T-D-RA	PMOD Type-6A connector
I2C_PM	RIIC ch1	ISL28022FRZ	Current monitor for measuring SMARC module
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)
		SLG4R45950	GreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)
		SLG4AR45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)
		RAA215300A2GNP#HA3	PMIC
		SLG7RN46420	GreenPAK (Power Regulator)
		SLG7RN46131	GreenPAK (Power/Reset Control)
		5L35023B-615NLGI	Clock generator
I2C_LCD	—	2041262-1	Mini PCI Express & mSATA connector
I2C_CAM0	—	2-1734592-2	22-pin FPC connector
I2C_CAM1	—	2-1734592-2	22-pin FPC connector
—	SD/MMC ch0	1040310811	microSD card slot
		MTFC64GASAQHD-IT	64-GB eMMC memory
SDIO	SD ch1	1040310811	microSD card slot
—	SD ch2	1040310811	microSD card slot
—	DDR	MT53E512M16D1FW-046WT	1-GB LPDDR4 SDRAM
—	xSPI	AT25QL128A_MHE	128-Mbit Quad SPI flash memory
—	ADC	SM12B-SRSS-TB(LF)(SN)	12-pin connector
—	I3C	SM04B-SRSS-TB(LF)(SN)	4-pin connector
—	JTAG	10051922-1010EHLF	10-pin connector
—	CPG	5L35023B-615NLGI	Clock generator
		830208214909	Oscillator for AUDIO_CLK2
—	Power	ISL28025FR12Z	Current monitor for measuring five power rails on the SMARC module
		FT232HQ	USB to I2C conversion IC
		629105150921	USB2.0 Type-microAB receptacle

Note 1. Select whether to assign PMOD1 to SER0 or MDT420E01001 to SER0. M.2 Key cannot be assigned to SER2 since SER2 is not connected to the G3S SMARC module.

2.2.2 G3E SMARC EVK

Table 2.2 Interface Mapping (1/2)

SMARC Interface Name	RZ/G3E I/F	Device Part Number	Description
USB0	USB2.0 ch0	629105150921	USB2.0 Type-microAB receptacle
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB2.0 Hub IC
		72309-8014BLF	USB2.0 Type-A receptacle
USB2	USB3.2 Gen2	692122030100	USB3.0 Type-A receptacle
USB3	—	1054500101	USB3.0 Type-C receptacle
USB4	—	72309-8014BLF	USB2.0 Type-A receptacle
USB5	—	72309-8014BLF	USB2.0 Type-A receptacle
CAN0	CAN ch4	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
CAN1	CAN ch1	SM03B-SRSS-TB(LF)(SN)	3-pin connector
I2S0	SSI ch3	DA7212-01UM	Audio Codec
		STX-4335-5BGP-S1	Stereo Headphone, Stereo Mic, Aux for connector
		M20-9990246	Speaker for pin header
I2S2	SSI ch0	MDT420B01001	M.2 Key E for I2S interface
SPI0	RSPI ch1	GRPB122VWQS-RC	24-pin header
SPI1	RSPI ch0	SSW-106-02-T-D-RA	PMOD Type-2A connector
SER0	SCIF ch4	SSW-106-02-T-D-RA	PMOD Type-3A connector
SER1	SCIF ch9	110990037	Grove connector
SER2	SCIF ch2	MDT420B01001	M.2 Key B
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC
		629105150921	USB2.0 Type-microAB receptacle for UART Debug
PCIE_A	PCIe Gen3	10061913-111PLF	PCIe 4x Slot
PCIE_B		MDT420B01001	M.2 Key B
		MDT420E01001	M.2 Key E
		78646-3001	SIM card for M.2 Key B
		MDT420B01001	M.2 Key B
—	Parallel	DF40C-50DS-0.4V	LCD connector
		ADV7513BSWZ	Parallel to HDMI conversion IC(*1)
		46765-1301	Micro HDMI connector(*1)
SATA	—	GRPB122VWQS-RC	GPIO pin header
HDMI	MIPI DSI	ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC
		46765-1301	Micro HDMI connector
—	MIPI DSI	DF40C-50DP-0.4V	DSI connector
LVDS0	LVDS ch0	2041262-1	Mini PCI Express & mSATA connector
		IT2623	Dual LVDS to HDMI conversion IC(*2)
		46765-1301	Micro HDMI connector(*2)
LVDS1	LVDS ch1	2041262-1	Mini PCI Express & mSATA connector
CSI0	—	2-1734592-2	22-pin FPC connector
CSI1	MIPI CSI-2	2-1734592-2	22-pin FPC connector(*3)
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY

Table 2.2 Interface Mapping (2/2)

SMARC Interface Name	RZ/G3E I/F	Device Part Number	Description
I2C_GP	RIIC ch1	GRPB122VWQS-RC	GPIO pin header
		MDT420B01001	M.2 Key E for I2C interface
		DA7212-01UM	Audio Codec for I2C interface
		SSW-106-02-T-D-RA	PMOD Type-6A connector
I2C_PM	RIIC ch8	ISL28022FRZ	Current monitor for measuring SMARC module
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)
		SLG4R45950	GreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)
		SLG4AE45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)
		RAA215300A2GNP#HA8	PMIC
		SLG7RN47061	GreenPAK (Power Regulator)
		SLG7RN47054	GreenPAK (Power/Reset control)
		5P35023B-789NLGI	Clock generator
I2C_LCD	RIIC ch7	ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC
		DF40C-50DP-0.4V	DSI connector
		DF40C-50DS-0.4V	LCD connector
I2C_CAM1	RIIC ch0	2-1734592-2	22-pin FPC connector
—	SD/MMC ch0	1040310811	microSD card slot
		MTFC64GBCAQTC-IT	64-GB eMMC memory
SDIO	SD/MMC ch1	1040310811	microSD card slot
—	SD/MMC ch2	1040310811	microSD card slot
—	DDR	MT53E1G32D2FW-046 WT:C	4-GB LPDDR4X SDRAM
—	xSPI	AT25QL128A-MHE	128-Mbit Quad SPI Flash memory
—	ADC	DF40C-50DP-0.4V	MISC connector
		TSM-115-01-L-DV-P-TR	30-pin connector ^(*)
—	I3C	DF40C-50DP-0.4V	MISC connector
		TSM-115-01-L-DV-P-TR	30-pin connector ^(*)
—	JTAG	DF40C-50DP-0.4V	MISC connector
		10051922-1010EHLF	10-pin connector ^(*)
—	CPG	5L35023B-617NLGI	Clock generator
		5P35023B-789NLGI	Clock generator
—	Power	ISL28025FRZ	Current monitor for measuring five power rails on the SMARC module
		DF40C-50DP-0.4V	MISC connector
		FT232HQ-REEL	USB to I2C conversion IC ^(*)
		629105150921	USB2.0 Type-microAB receptacle ^(*)

Note 1. The SMARC RGB to HDMI Adaptor is required. It is bundled with the G3E SMARC EVK.

Note 2. The SMARC Dual LVDS to HDMI Adaptor is required. It is bundled with the G3E SMARC EVK.

Note 3. The SMARC Pi Camera Adaptor is required. It is bundled with the G3E SMARC EVK.

Note 4. The SMARC Breakout Adaptor is required. It is bundled with the G3E SMARC EVK.

2.3 Board Configuration and Status

The RZ SMARC Carrier II has many switched configuration options and on-board interfaces. These are described in detail in the following sections.

Default settings are highlighted.

2.3.1 VBUS_SEL – Main Power

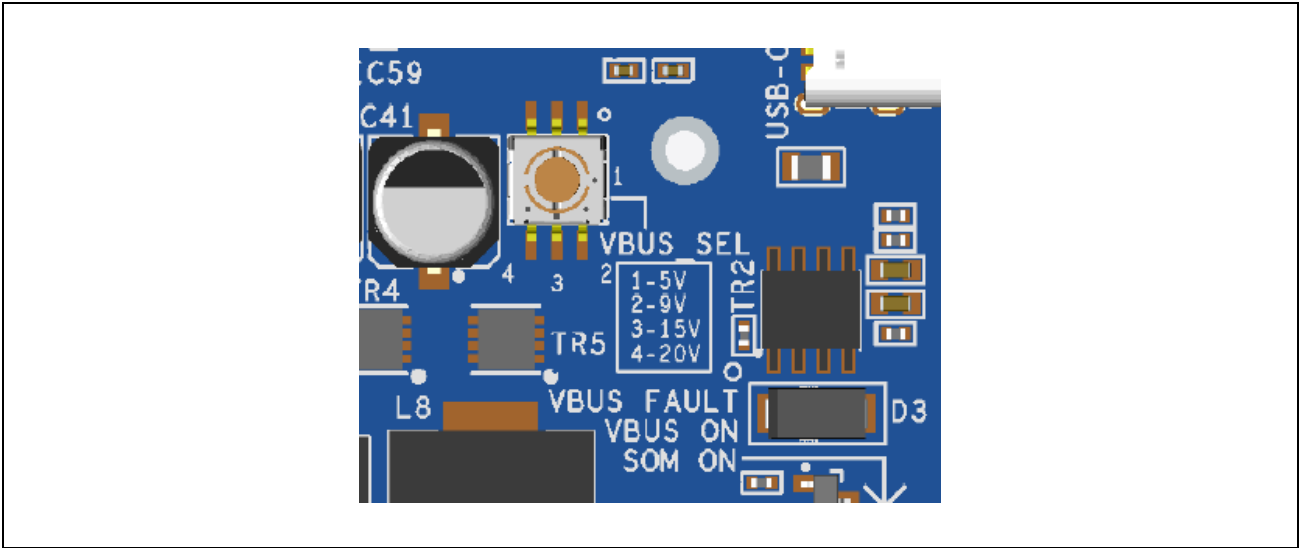


Figure 2.5 The Location and the Default Setting of the VBUS_SEL

The primary power input for the RZ SMARC Carrier II is from the USB Type-C connected to a power delivery device (not provided).

The specification for the USB Type-C power adaptor is dependent on the requirements for the SMARC Module and peripheral boards connected.

Ensure the following switch settings match the minimum power requirements and USB Type-C power adaptor capabilities.

Table 2.3 Power Requirements for Each Switch Setting

SW_MODE[4]	VBUS_SEL	Min. Voltage	Min. Current	Min. Power
ON	1	5 V	2 A	10 W
ON	2	9 V	2 A	18 W
ON	3	15 V	2 A	30 W
ON	4	20 V	2 A	40 W
OFF	1	5 V	4 A	20 W
OFF	2	9 V	4 A	36 W
OFF	3	15 V	4 A	60 W
OFF	4	20 V	4 A	80 W

2.3.2 VBAT_SEL – VDD_RTC Power

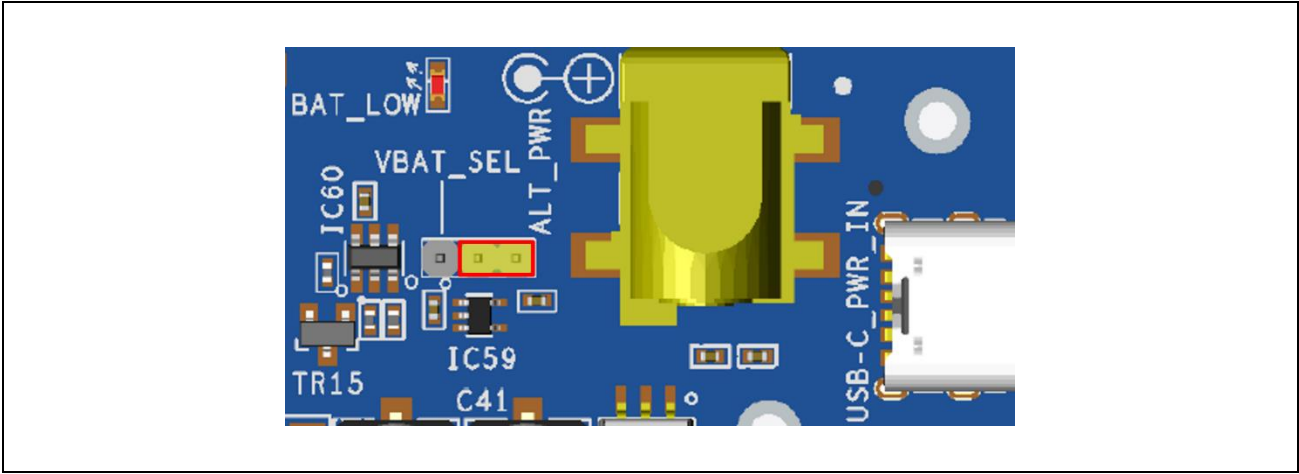


Figure 2.6 The Location and the Default Setting of the VBAT_SEL

The power to the SMARC Module required for VDD_RTC may be provided by a regulator or coin cell battery (not provided).

The power source selection is made with a 2 mm header fitted to VBAT_SEL header.

Table 2.4 Jumper Pin “VBAT_SEL” Settings

VBAT_SEL Header Link	VDD_RTC Source
Pin 1 – Pin 2	A coin cell battery must be fitted to BAT_RTC
Pin 2 – Pin 3	An on-board regulator provides 2.8 V
<i>Note:</i> Power is removed when the main power is disconnected.	

2.3.3 SW_PWR_12V – PCIe Slot Power

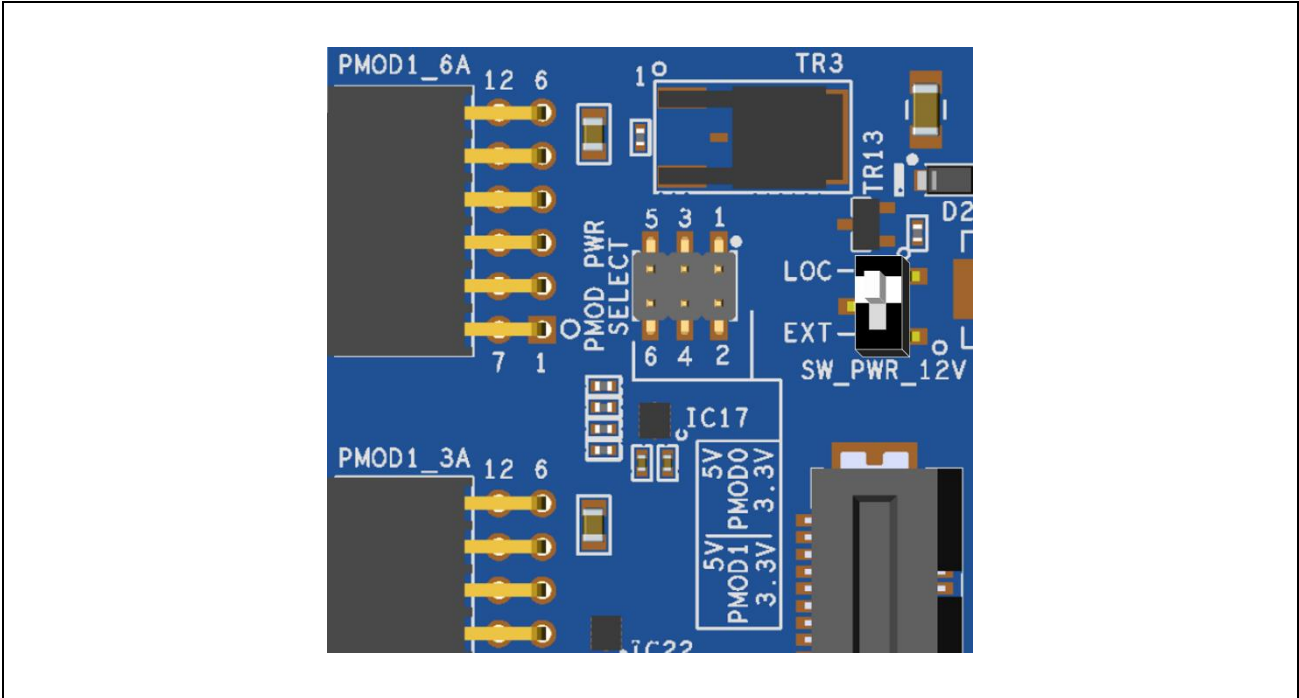


Figure 2.7 The Location and the Default Setting of the SW_PWR_12V

The 12 V power supply to the PCIe Slot may be provided by a regulator or external supply.
The power source is selected with SW_PWR_12V.

Table 2.5 Jumper Pin “SW_PWR_12V” Settings

SW_PWR_12V	PCIe Slot 12 V Source
ON	An externally 12 V supply must be connected to PWR_12V_EXT Required for PCIe cards > 10 W
OFF	An on-board regulator provides 12 V @0.5 A <i>Note:</i> PCIe plug-in card is limited to 10 W.

2.3.4 RSVD_PWR – Module Power

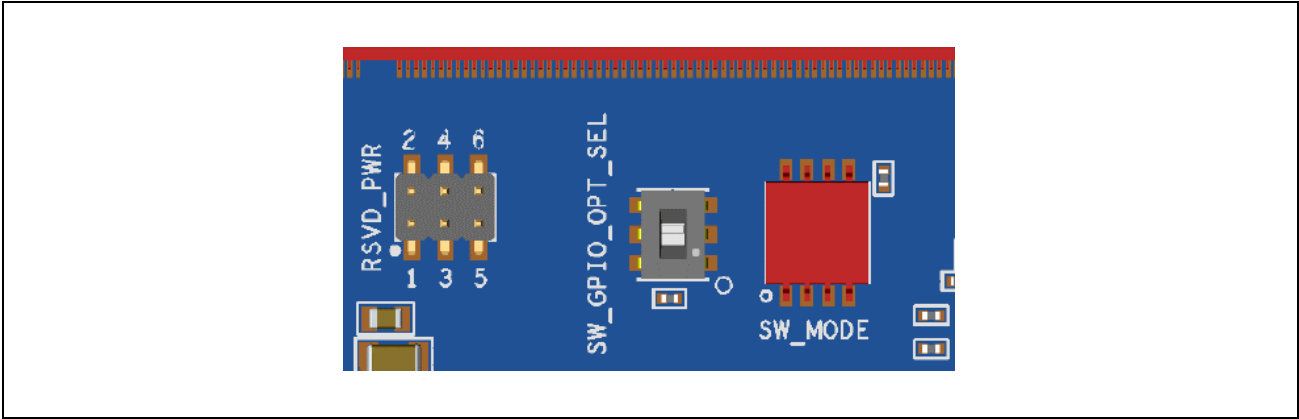


Figure 2.8 The Location and the Default Setting of the RSVD_PWR

The SMARC specification restricts the module power to 25 W (5.0 V, 10 pins @0.5 A). However, the RZ SMARC Carrier II can make use of the Module RSVD pins and increase this value.

Table 2.6 Jumper Pin “RSVD_PWR” Settings

RSVD_PWR Header Link	Max. SMARC Module Power
Pin 1 – Pin 2	32.5 W
Pin 3 – Pin 4	<i>Note:</i> For use with compatible SMARC Modules only.
Pin 5 – Pin 6	
No headers fitted	25 W

2.3.5 PMOD_PWR_SEL – PMOD Power

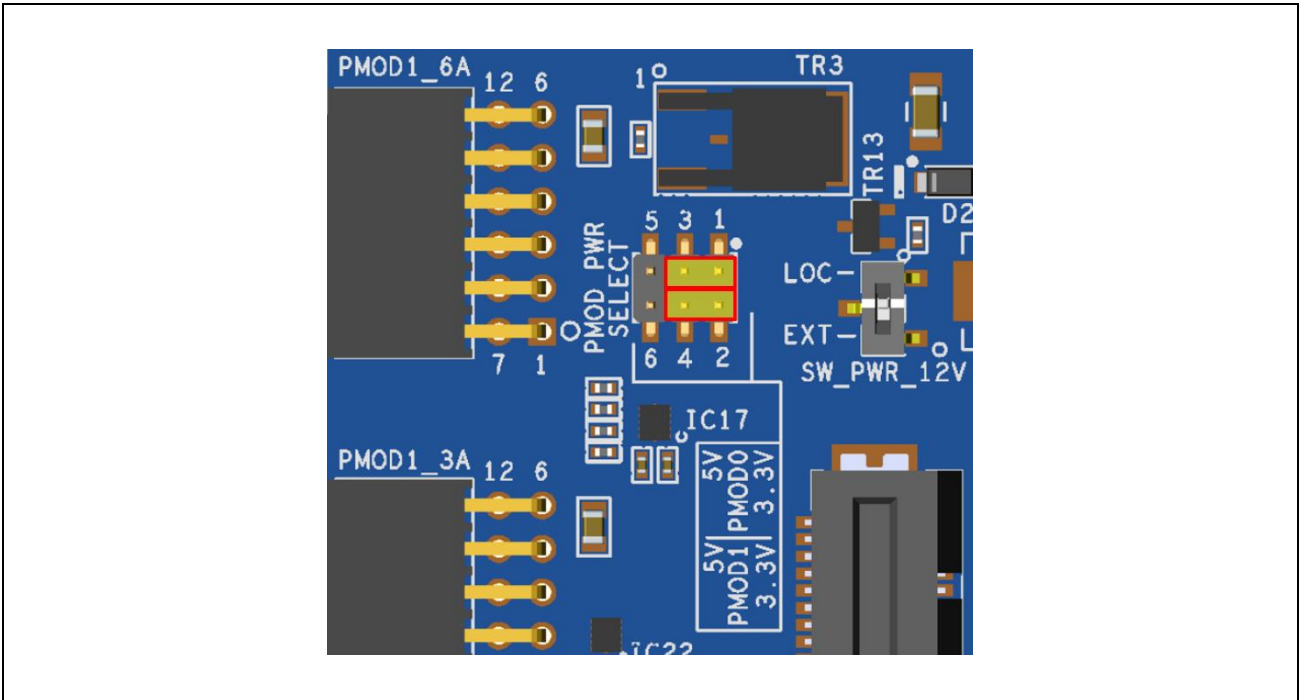


Figure 2.9 The Location and the Default Setting of the PMOD_PWR_SEL

PMOD interfaces support either 3.3 V or 5.0 V.

A 2 mm header is used to select the power level for PMOD0 (Type-2A) and another 2 mm header is used to select the power level for PMOD1 (Type-3A and Type 6A).

Table 2.7 Jumper Pin “PMOD_PWR_SEL” Settings (1/2)

PMOD_PWR_SEL Header Link	PMOD0 Power Level
Pin 1 – Pin 3	3.3 V
Pin 3 – Pin 5	5.0 V

Table 2.7 Jumper Pin “PMOD_PWR_SEL” Settings (2/2)

PMOD_PWR_SEL Header Link	PMOD1 Power Level
Pin 2 – Pin 4	3.3 V
Pin 4 – Pin 6	5.0 V

2.3.6 SW_PMOD0_PWR_SLP – PMOD Power/Sleep Control

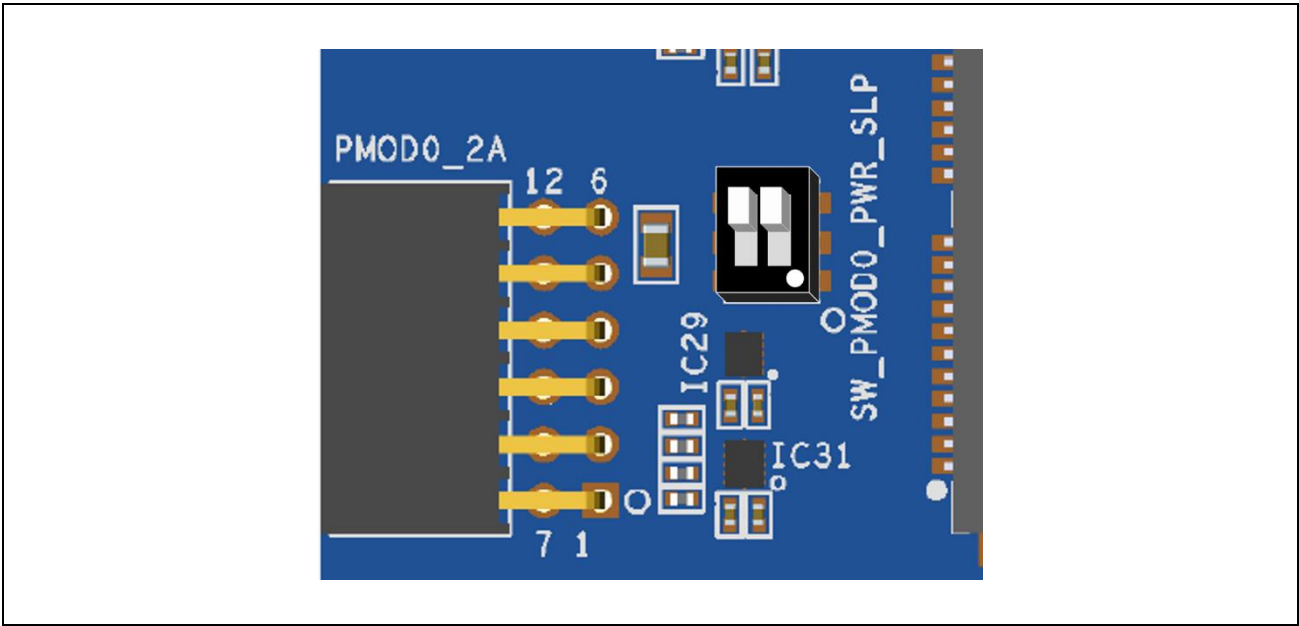


Figure 2.10 The Location and the Default Setting of the SW_PMOD0_PWR_SLP

PMOD0 has the capability to drive the POWER_BTN# and SLEEP# signals of the RZ SMARC Carrier II by configuring SW_PMOD0_PWR_SLP.

Table 2.8 DIP Switch “SW_PMOD0_PWR_SLP” Setting (1/2)

SW_PMOD0_PWR_SLP-1	PMOD0_GPIO/CS2 (Pin 9)
1 – 2	Connected to POWER_BTN#
2 – 3	Connected to GPIO6

Table 2.8 DIP Switch “SW_PMOD0_PWR_SLP” Setting (2/2)

SW_PMOD0_PWR_SLP-2	PMOD0_GPIO/CS3 (Pin 10)
4 – 5	Connected to SLEEP#
5 – 6	Connected to GPIO7

2.3.7 SW_GPIO_OPT_SEL – GPIO Options

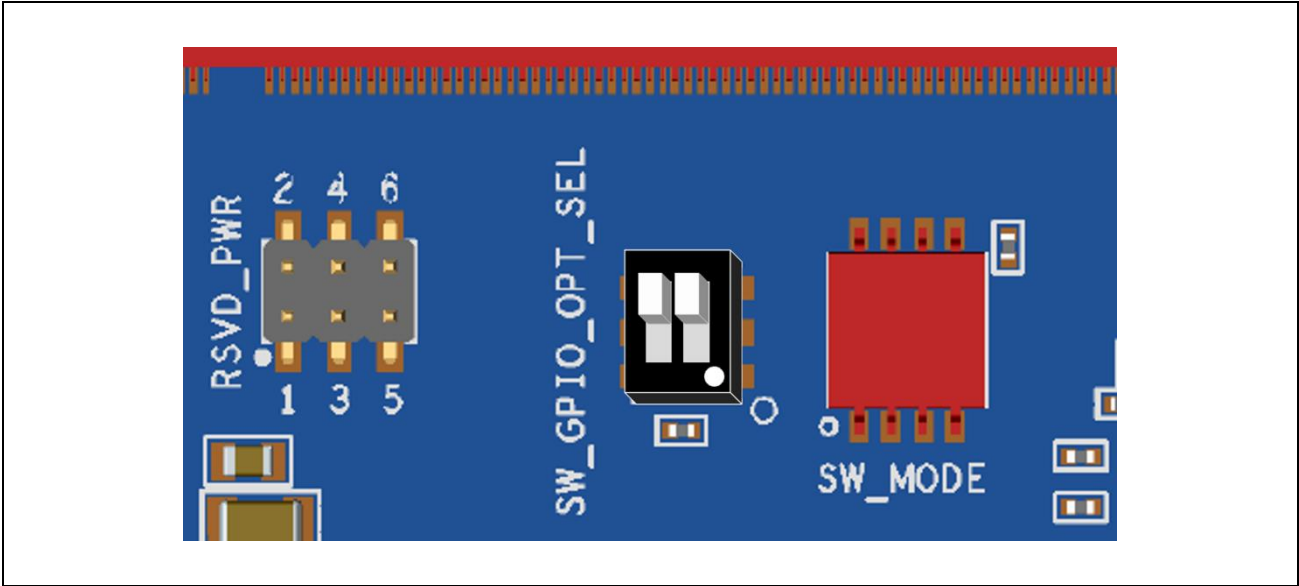


Figure 2.11 The Location and the Default Setting of the SW_GPIO_OPT_SEL

GPIO10 may be used for DISP_INT# or PMOD1. GPIO2 may be used for CAM0_RST# or DISP_INT#.

Table 2.9 DIP Switch “SW_GPIO_OPT_SEL” Setting (1/2)

SW_GPIO_OPT_SEL-1	GPIO10
1 – 2	Connected to DISP_INT#
2 – 3	Connected to PMOD1

Table 2.9 DIP Switch “SW_GPIO_OPT_SEL” Setting (2/2)

SW_GPIO_OPT_SEL-2	GPIO2
4 – 5	Connected to CAM_RST#
5 – 6	Connected to DISP_INT#
Note: CAM_RST# is pulled high.	

2.3.8 SW_GPIO_CAN_PMOD – CAN Standby

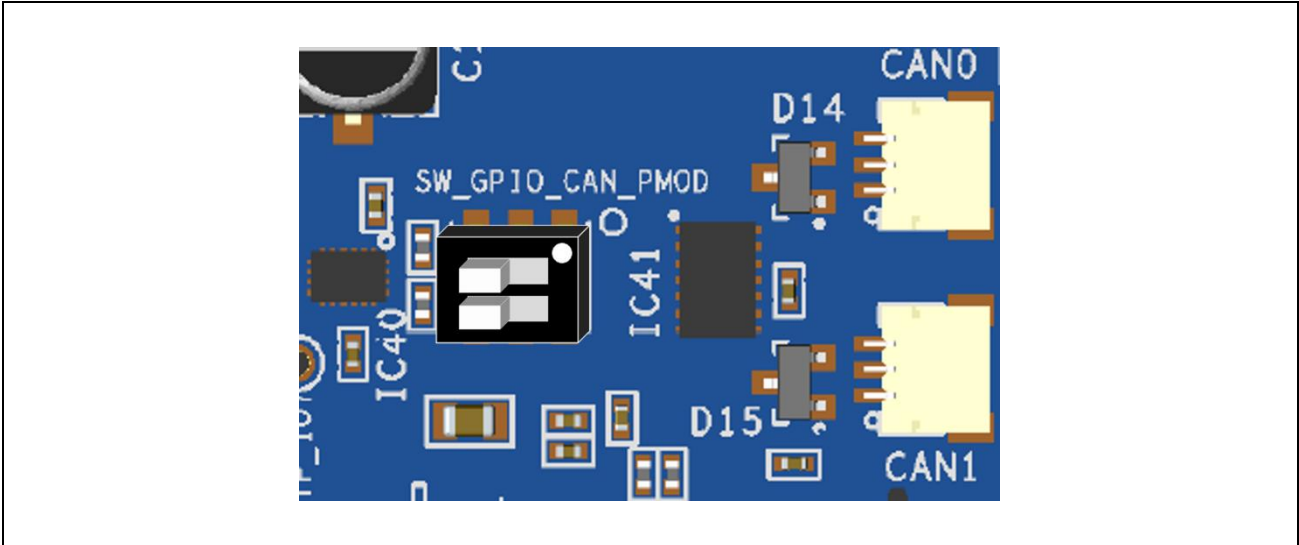


Figure 2.12 The Location and the Default Setting of the SW_GPIO_CAN_PMOD

GPIO8 and GPIO9 may be used for CAN standby or PMOD1 GPIO.

Table 2.10 DIP Switch “SW_GPIO_CAN_PMOD” Setting (1/2)

SW_GPIO_CAN_PMOD-1	GPIO8
1 – 2	Connected to CAN0_STB
2 – 3	Connected to PMOD1
Note: CAN0_STB is pulled low.	

Table 2.10 DIP Switch “SW_GPIO_CAN_PMOD” Setting (2/2)

SW_GPIO_CAN_PMOD-2	GPIO9
4 – 5	Connected to CAN1_STB
5 – 6	Connected to PMOD1
Note: CAN1_STB is pulled low.	

2.3.9 SW_MODE – Boot Mode (and Power)

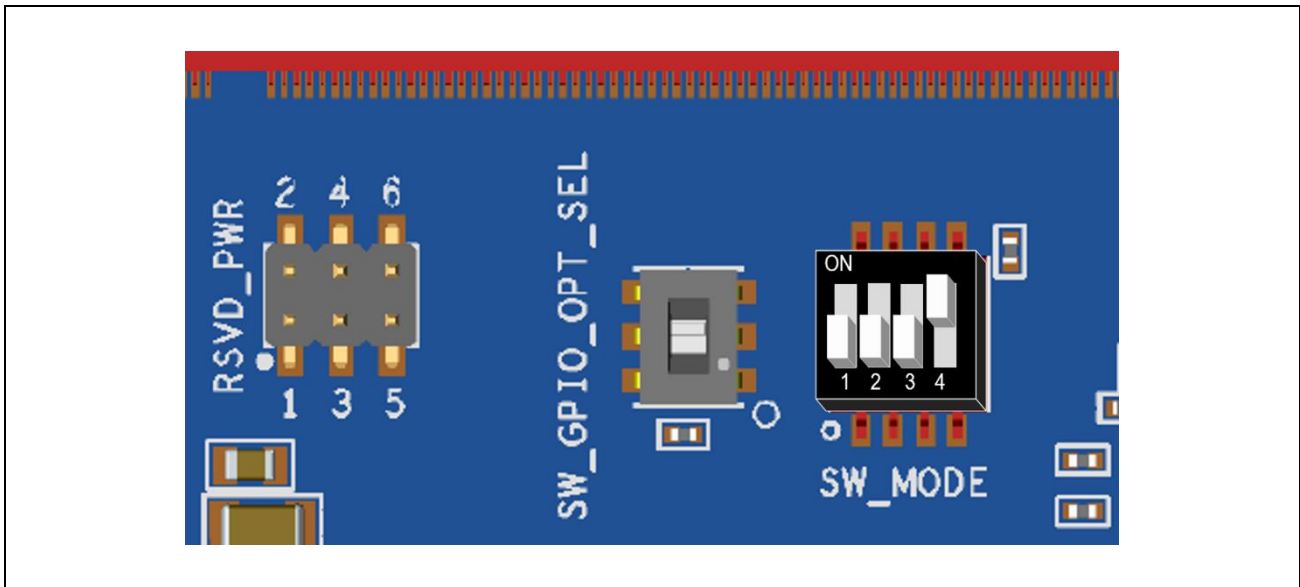


Figure 2.13 The Location and the Default Setting of SW_GPIO_OPT_SEL

As described in the SMARC specification, the Module boot mode can be configured as follows.

Table 2.11 DIP Switch “SW_MODE” Settings

Boot Mode #	SW_MODE[1] (BOOT_SEL0#)	SW_MODE[2] (BOOT_SEL1#)	SW_MODE[3] (BOOT_SEL2#)	Boot Source
0	ON	ON	ON	Carrier SATA <i>Note:</i> SATA signals are routed to the GEN_PURPOSE_IO connector.
1	OFF	ON	ON	Carrier SD card (SDIO)
2	ON	OFF	ON	Carrier eSPI (CS0#) <i>Note:</i> eSPI signals are routed to PMOD0 - Type-2A.
3	OFF	OFF	ON	Carrier SPI (CS0#) <i>Note:</i> SPI0 signals are routed to the GEN_PURPOSE_IO connector.
4	ON	ON	OFF	Module device (NAND, NOR) vendor specific E.g. Module microSD card
5	OFF	ON	OFF	Remote boot (GBE, serial) – vendor specific E.g. SCIF download using SER3_UART
6	ON	OFF	OFF	Module eMMC flash E.g. eMMC
7	OFF	OFF	OFF	Module SPI E.g. QSPI

SW_MODE[4] is not used for mode selection. It is used for selecting minimum current required from the USB-C power input. Refer to VBUS_SEL for details.

2.3.10 SW_M2_DIS – M.2 Card Control Signals

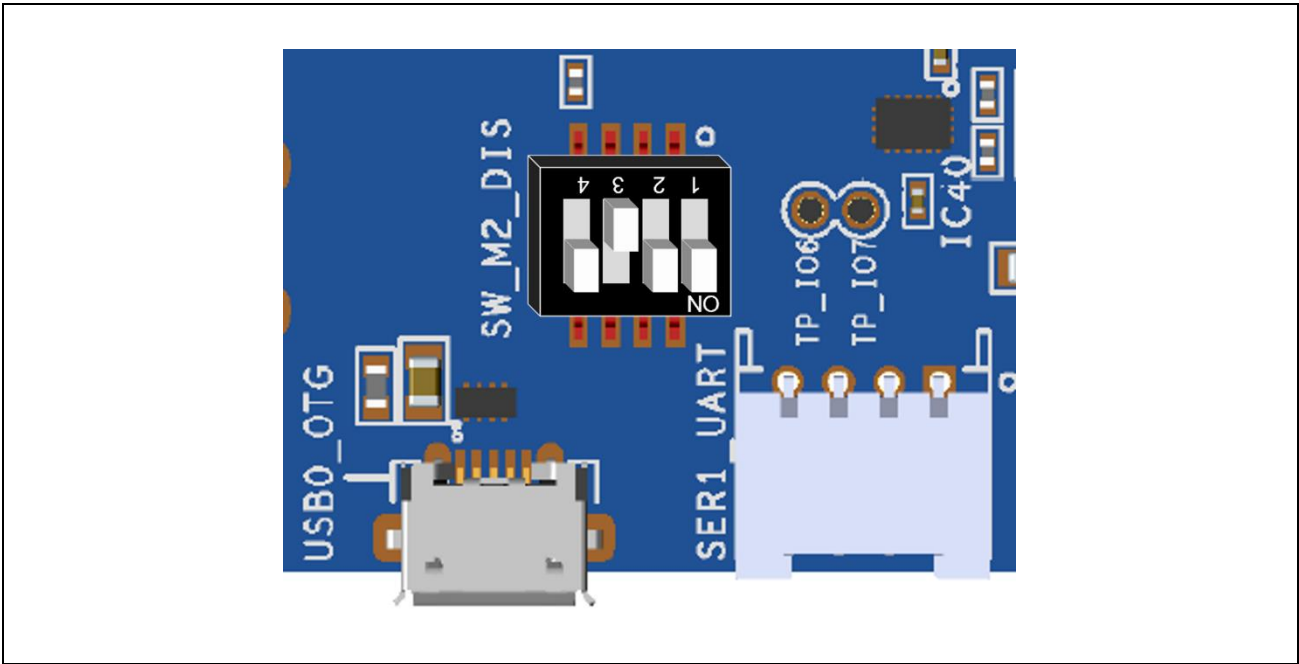


Figure 2.14 The Location and the Default Setting of the SW_M2_DIS

The M.2 cards may require control signals that are not in scope of the SMARC specification.

The RZ SMARC Carrier-II provides options for

- M.2 Key E: W_DISABLE1#, W_DISABLE2#
- M.2 key B: RESET#, FULL_CARD_POWER_OFF

These signals may be left open (usually pulled up on the M.2 card) or, for legacy modules, GPIO signals may be used, and for newer modules, these may be controlled using I2C_PM.

Table 2.12 DIP Switch “SW_M2_DIS” Settings (1/4)

SW_M2_DIS[1]	SW_M2_DIS[4]	M.2 Key E: W_DISABLE1#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 7 (toggle)
ON	OFF	Inverted GPIO12
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.12 DIP Switch “SW_M2_DIS” Settings (2/4)

SW_M2_DIS[2]	SW_M2_DIS[4]	M.2 Key E: W_DISABLE2#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 6 (toggle)
ON	OFF	Inverted GPIO13
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.12 DIP Switch "SW_M2_DIS" Settings (3/4)

SW_M2_DIS[3]	SW_M2_DIS[4]	M.2 Key B: RESET#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 5 (toggle)
ON	OFF	Inverted GPIO8
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.12 DIP Switch "SW_M2_DIS" Settings (4/4)

SW_M2_DIS[4]	M.2 Key B: FULL_CARD_POWER_OFF
ON	Controlled by I2C_PM Byte 0x7A bit 4 (toggle)
OFF	Inverted GPIO9

2.3.11 SW_OPT_MUX

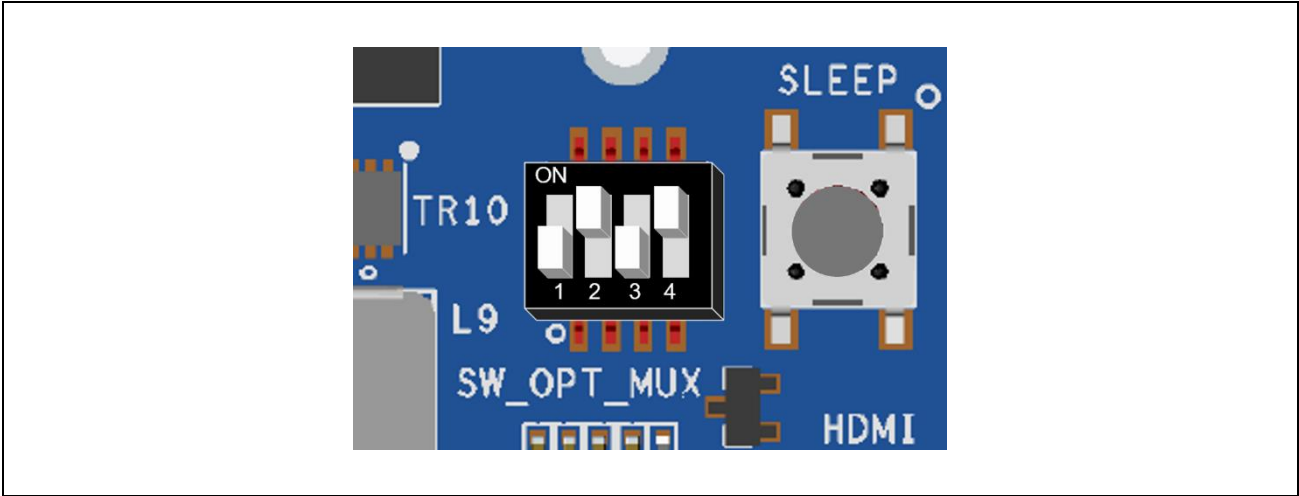


Figure 2.15 The Location and the Default Setting of the SW_OPT_MUX

To support legacy modules and provide greater flexibility, the RZ SMARC Carrier II provides multiplexing options for SDIO, I2S and SER0.

Table 2.13 DIP Switch “SW_OPT_MUX” Settings (1/4)

SW_OPT_MUX[1]	SDIO
ON	The SMARC SDIO signals are routed to the M.2 Key E interface. <i>Note:</i> The microSD interface on the Carrier cannot be used.
OFF	The SMARC SDIO signals are routed to the microSD on the Carrier. <i>Note:</i> The M.2 Key E interface cannot use SDIO.

Table 2.13 DIP Switch “SW_OPT_MUX” Settings (2/4)

SW_OPT_MUX[2]	I2S
ON	The SMARC I2S signals are routed to the M.2 Key E interface. <i>Note:</i> External display interface DISP0 has no I2S connection
OFF	The SMARC I2S signals are routed to the external display interface DISP0. <i>Note:</i> The M.2 Key E interface has no I2S connection.

Table 2.13 DIP Switch “SW_OPT_MUX” Settings (3/4)

SW_OPT_MUX[3]	SPARE
X	No function

Table 2.13 DIP Switch “SW_OPT_MUX” Settings (4/4)

SW_OPT_MUX[4]	SER0
ON	The SMARC SER0 signals are routed to PMOD1. <i>Note:</i> The SMARC SER0 signals are not routed to M.2 Key E.
OFF	The SMARC SER0 signals are routed to M.2 Key E UART. <i>Note:</i> The SMARC SER0 signals are not routed to PMOD1.

2.3.12 SW_PCIE_MUX

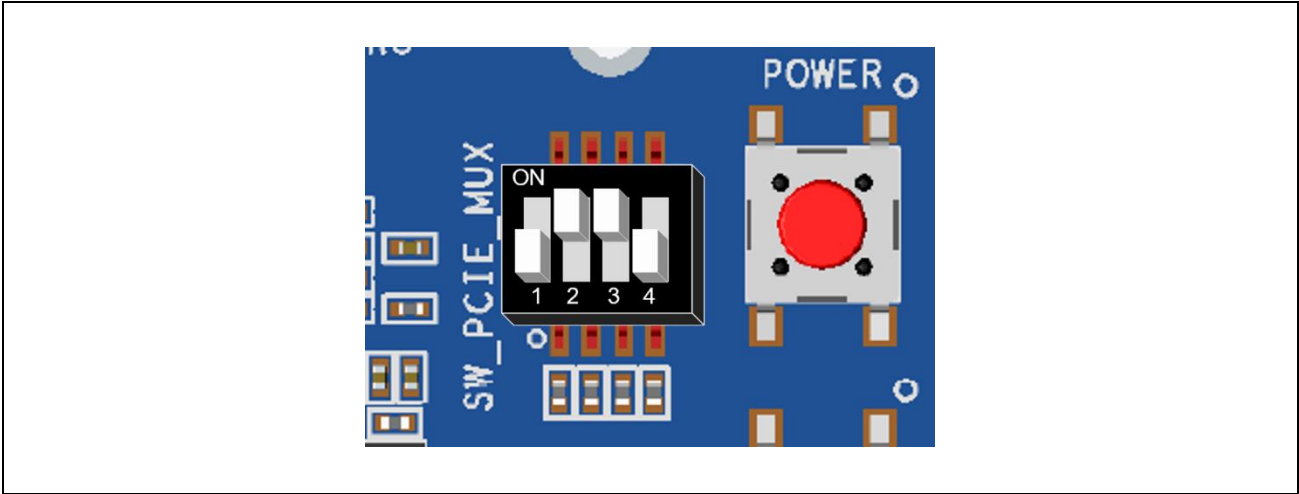


Figure 2.16 The Location and the Default Setting of the SW_PCIE_MUX

The RZ SMARC Carrier II supports SMARC Modules with the following PCIe configurations.

- 1x Channel, 1-Lane
- 2x Channel, 1-Lane
- 1x Channel, 2-Lane
- 2x Channel, 2-Lane
- 1x Channel, 4-Lane

The PCIe signals are multiplexed on the RZ SMARC Carrier II so that they can be connected to a combination of PCIe Slot, M.2 Key E and M.2 Key B interfaces.

The SMARC PCIe links are designated PCIE_A, PCIE_B, PCIE_C and PCIE_D.

Table 2.14 DIP Switch “SW_PCIE_MUX” Settings (1/4)

PCIE MUX1	
SW_PCIE_MUX[1]	Refer to Table 2.15, Usable PCIe Configurations for details
ON	High
OFF	Low

Table 2.14 DIP Switch “SW_PCIE_MUX” Settings (2/4)

PCIE MUX2	
SW_PCIE_MUX[2]	Refer to Table 2.15, Usable PCIe Configurations for details
ON	High
OFF	Low

Table 2.14 DIP Switch “SW_PCIE_MUX” Settings (3/4)

SW_PCIE_MUX[3]	PCIE MUX3 Refer to Table 2.15, Usable PCIe Configurations for details
ON	High
OFF	Low

Table 2.14 DIP Switch “SW_PCIE_MUX” Settings (4/4)

SW_PCIE_MUX[4]	USB2/M.2 Key B
ON	The SMARC USB2 signals are routed to the M.2 Key B interface. <i>Note:</i> The USB3.2 Type-A interface on the Carrier cannot be used.
OFF	The SMARC USB2 signals are routed to the USB3.2 Type-A interface. <i>Note:</i> The M.2 Key B interface on the Carrier cannot be used.

In case of the RZ/G3S, this processor supports 1lane for PCIe Interface. Only hatched "SW_PCIE_MUX" DIP switch settings are supported on the G3S SMARC EVK.

Table 2.15 Usable PCIe Configurations

Link Configuration					SW_PCIE_MUX			PCIe Slot					M.2 Key E				M.2 Key B		
	A	B	C	D	0	1	2	REFCK	Lane0	Lane1	Lane2	Lane3	REFCK0	Lane0	REFCK1	Lane1	REFCK	Lane0	Lane1
1x PCIe 1-lane	1x				1	0	0	A	A										
					0	1	1						A	A					
					1	0	1									A	A		
2x PCIe 1-lane	1x	1x			0	1	0	A	A				B	B					
					0	0	1	A	A								B	B	
					0	1	1	B					A	A	B	B			
					1	1	1						A	A			B	B	
1x PCIe 2-lane	2x				1	0	0	A	A	B									
					0	1	1						A	A		B			
					1	0	1										A	A	B
2x PCIe 2-lane	2x		2x		0	1	1	B	C	D			A	A	B	B			
					1	0	1	B	C	D							A	A	B
1x PCIe 4-lane	4x				1	0	0	A	A	B	C	D							
					0	1	1						A	A		B			
					1	0	1										A	A	B

2.4 User IO

2.4.1 Push Buttons

2.4.1.1 POWER, RESET, SLEEP

These push buttons are used to connect SMARC Module signals to ground. The SMARC Module inputs are open-drain. The operation of each push button is dependent on the connected module.

Table 2.16 Features of Each Push Button

Label	Color	SMARC Signal	Description
POWER	Red	POWER_BTN#	Power-button output to the SMARC Module
RESET	Blue	RESET_IN#	Reset output to the SMARC Module
SLEEP	Grey	SLEEP#	Sleep indicator to the SMARC Module

2.4.1.2 USER_SW1, USER_SW2, USER_SW3

These push buttons are used to connect SMARC Module GPIO signals to ground. Care must be taken to avoid signal conflicts if other peripherals are using the same GPIO signals.

Table 2.17 Features of Each Push Button

Label	Color	SMARC Signal
USER_SW1	Grey	GPIO4
USER_SW1	Blue	GPIO6
USER_SW2	Blue	GPIO7

2.4.2 LED Indicators

2.4.2.1 Power

Four LED indicators are used to provide the user with power status.

Table 2.18 Features of Each Indicator for Power Status

Label	Color	Status (when lit)
VBUS_FAULT	RED	The connected USB-C power supply is not capable of providing the minimum current and/or minimum voltage as set by VBUS_SEL and SW_MODE[4].
VBUS_ON	GREEN	USB-C power supply is ON
SOM_ON	GREEN	SMARC Module (5 V) power is ON
CARRIER_ON	GREEN	Carrier power is ON
BAT_LOW	RED	VDD_RTC is below 2.0 V. Coin cell battery voltage is low or VBAT_SEL jumper is not fitted correctly.

2.4.2.2 PCI Express

Table 2.19 Feature of Indicator for PCI Express

Label	Color	Status (when lit)
PCIE_CK_LOSS	RED	PCIE_A_REFCK is not stable

2.4.2.3 M.2

Table 2.20 Features of Each Indicator for M.2

Label	Color	Status (when lit)
M.2E_LED1	RED	Refer to datasheet of connected M.2 Key E card
M.2E_LED2	RED	Refer to datasheet of connected M.2 Key E card
M.2B_LED1	RED	Refer to datasheet of connected M.2 Key B card

2.4.2.4 Ethernet

The stacked Ethernet ports have integrated LEDs.

Table 2.21 Features of Each Indicator for Ethernet

Label	Color	Status (when lit)
ETHERNET1-0	GREEN	Link is up
ETHERNET1-0	YELLOW	Activity

2.5 Recommended Operating Condition

Table 2.22 lists operating conditions of the RZ SMARC Carrier II.

Table 2.22 Operating Conditions of RZ SMARC Carrier II

Symbol	Item	Rated Value	Note
USBC_PWR_IN	Power voltage	15 V	Reference: VSS
—	Maximum consumed current	4 A	Includes continuous G3S SMARC Module current consumption
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. The ambient temperature is the air temperature at a point as close to the board as possible.

Figure 3.2 shows a block diagram of power system of the G3E SMARC EVK.

The 5 V power supply is supplied to the PMIC (RAA215300A2GNP#HA8) installed in the G3E SMARC Module, and the PMIC generates the power supply voltage for each interface.

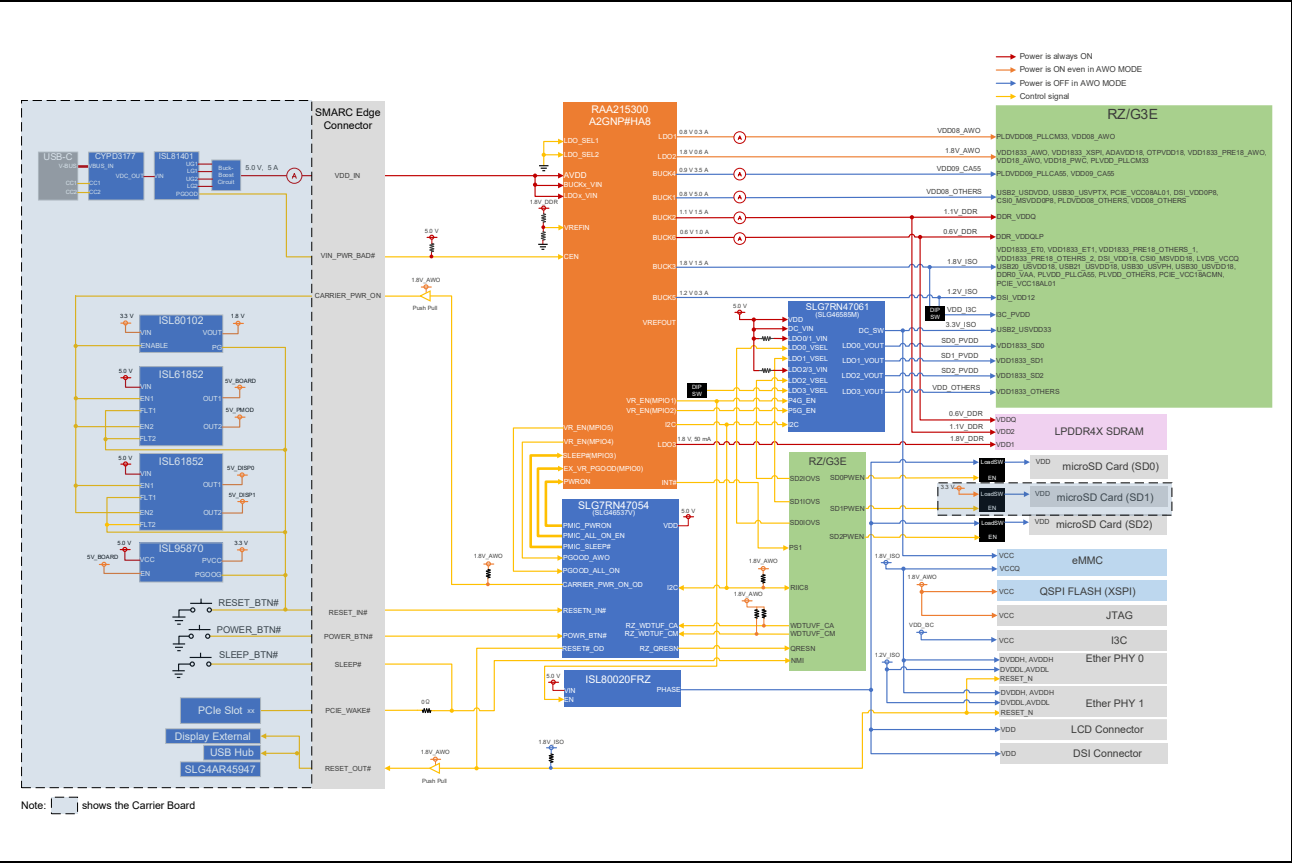


Figure 3.2 Power System Circuitry of G3E SMARC EVK

3.1.1 USB-C – Main Power

The RZ SMARC Carrier- II primary power input is from the USB -Type-C connected to a power delivery device (not provided).

3.1.2 BAT_RTC – VDD_RTC Power

A 3.0 V coin cell battery may be fitted to provide VDD_RTC power as an alternative to the on-board regulator.

The advantage of using a coin cell is that power is maintained when USB-C main power is removed.

Compatible battery sizes are CR927and CR1025.

3.1.3 PWR 12V EXT – PCIe Slot Power

To support PCIe cards that are greater than 10 W, an external 12 V supply is required.

The interface on the RZ SMARC Carrier II for this is from Wurth Electronik, part number 691305140002.

The mating part, to which power cables can be attached, is provided (Wurth Electronik, part number 691361100002) – picture below. Ensure correct polarity.

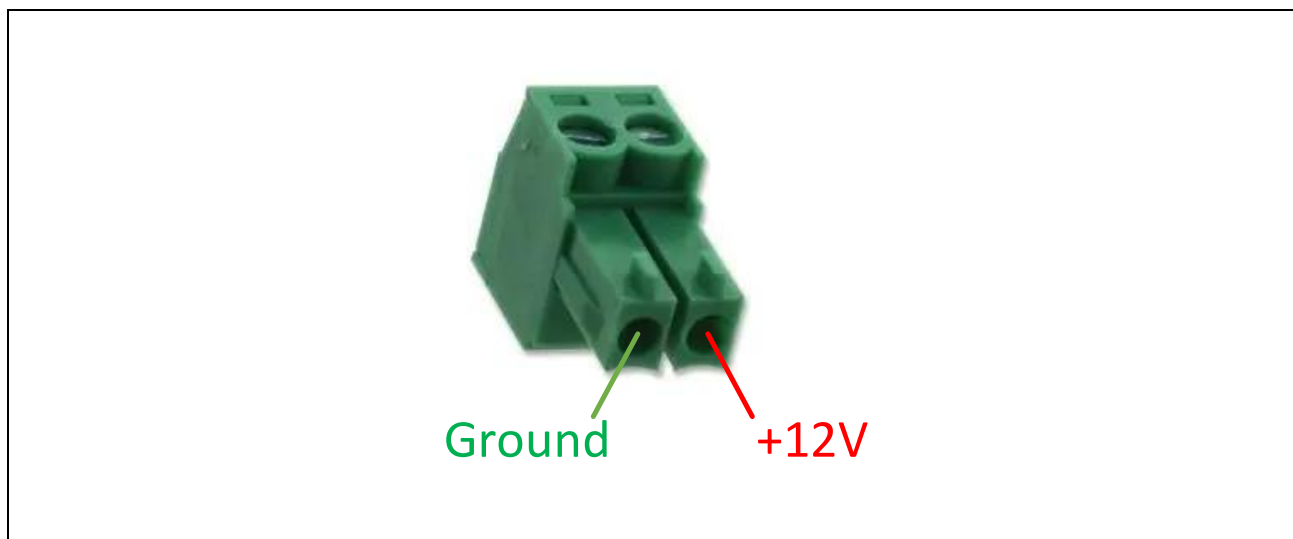


Figure 3.3 PWR_12V_EXT

3.2 Clock

RZ/G3S

RZ/G3E

Clock inputs required for peripherals such as FT232HQ, USB Hub, and M.2 Key E Card Module, are generated locally using separate crystals or oscillators. The crystals or oscillators used to provide the reference clocks for the G3S SMARC EVK peripherals are shown in the table below.

Table 3.1 Clock Table

Peripheral	Device Part Number	Frequency
FT232HQ Bridge*1 *2	FL2400022	24.000 MHz
USB Hub	FL2400022	24.000 MHz
M.2 Key E	7XZ-32.768KBE	32.768 kHz
HDMI Transmitter*3	ABM11-27.000MHZ-D2X	27.000 MHz

- Note 1. G3S SMARC Module
- Note 2. SMARC Breakout Adaptor. It is bundled with the G3E SMARC EVK.
- Note 3. SMARC Dual LVDS-HDMI Adaptor. It is bundled with the G3E SMARC EVK.

3.3 Serial UART

RZ/G3S

RZ/G3E

3.3.1 SER1_UART

A 4-pin connector (Sceed Technology, part number 110990037) provides connection to SER1.

Table 3.2 SER1 Pin Assignment

Pin Number	Signal
1	SER1_RX
2	SER1_TX
3	1.8 V
4	Ground

Note: TX and RX signals are at 1.8 V levels.

3.3.2 SER3_UART

Connection to SER3 is via a micro-USB interface. This is generally used for connection to the console/terminal.

3.4 USB

RZ/G3S

RZ/G3E

The RZ SMARC Carrier II provides interfaces for the following.

Table 3.3 Supported Interfaces of Each USB

SMARC IO	Connector Type	Description	G3S EVK	G3E EVK
USB0	USB2.0 Type-microAB	Support OTG functionality	Available	Available
USB1	USB2.0 Stacked Type-A	Support Host functionality Connected from a 4-channel USB hub IC	Available	Available
USB2	USB3.0 Type-A	Support Host functionality	Not used	Available
USB3	USB3.0 Type-C	Support OTG functionality	Not used	Not used
USB4	USB2.0 Stacked Type-A	Support Host functionality	Not used	Not used
USB5			Not used	Not used

3.5 Ethernet

RZ/G3S

RZ/G3E

A stacked RJ45 connector provides 2 ports, each capable of 1 Gbit speeds.

3.6 Camera

RZ/G3E

The SMARC specification defines two MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1 may be implemented with up to four differential data lanes (CSI1_D[0:3]+/- signals) to support higher resolution cameras.

Both camera interfaces use a 22-pin FPC connector (TYCOELECTRONICS part number 2-1734592-2) following the SMARC specification pinout.

Table 3.4 CSI0 and CSI1 Pin Assignment

Pin Number	CAM_CSI0	CAM_CSI1
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	Ground	Ground
4	CSI0_RX0+	CSI1_RX0+
5	CSI0_RX0-	CSI1_RX0-
6	Ground	Ground
7	CSI0_RX1+	CSI1_RX1+
8	CSI0_RX1-	CSI1_RX1-
9	Ground	Ground
10	Not connected	CSI1_RX2+
11	Not connected	CSI1_RX2-
12	CAM0_RST#/GPIO2 (refer to SW_GPIO_OPT_SEL)	CAM1_RST#/GPIO3
13	Not connected	CSI1_RX3+
14	Not connected	CSI1_RX3-
15	Ground	Ground
16	CSI0_CK+	CSI1_CK+
17	CSI0_CK-	CSI1_CK-
18	Ground	Ground
19	I2C_CAM0_CK	I2C_CAM1_CK
20	I2C_CAM0_DAT	I2C_CAM1_DAT
21	CAM0_PWR#/GPIO0	CAM1_PWR#/GPIO1
22	CAM_MCK	CAM_MCK

3.6.1 Pi Camera Adaptor

The G3S SMARC EVK does not support the MIPI CSI interface. On the other hand, the G3E SMARC EVK supports the MIPI CSI interface.

The SMARC Pi Camera Adaptor shown in **Figure 3.4 (a)** can be connected to the CAM_CSI1 of the G3E SMARC EVK. This enables conversion of the MIPI CSI-2 IO of the RZ/G3E to the Raspberry Pi Camera interface shown in **Figure 3.4 (c)*1**.

The pinout of the connector mounted on this adaptor board is the same as the pinout of the 22-pin Raspberry Pi camera.

This adaptor board can also be connected to the 15-pin Raspberry camera via the FPC cable: [Raspberry Pi Camera Cable](#).

NOTE

When connecting the camera module, carefully confirm each signal connection. Incorrect connections may damage the board or module.

*1. CAM_CSI0 is not available and only CAM_CSI1 is supported on the G3E SMARC EVK.

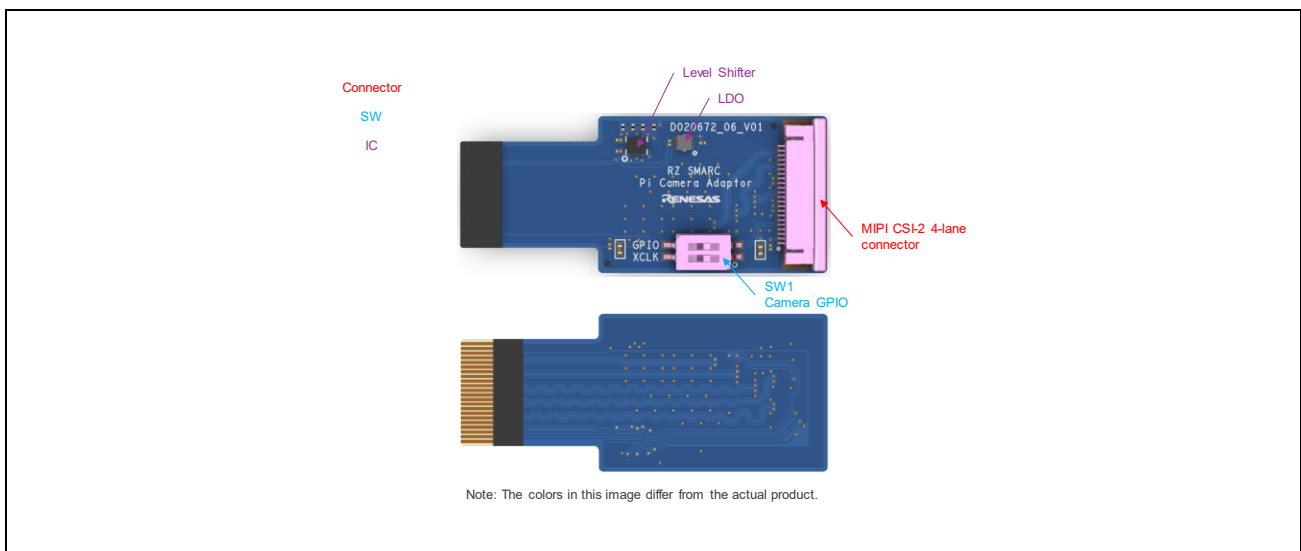


Figure 3.4 (a) SMARC Pi Camera Adaptor Top and Bottom View

A bank of two switches is used to configure the pull-up functionality of the camera interface. The default settings are **highlighted**.



Figure 3.4 (b) The Location and the Default Setting of SW1

Table 3.5 DIP Switch “SW1” Settings

SW1	Signal	ON	OFF
2	CAM_RST#_3V3	GPIO (3.3 V)	No Connect
1	CAM_MCK	MCLK (1.8 V)	No Connect

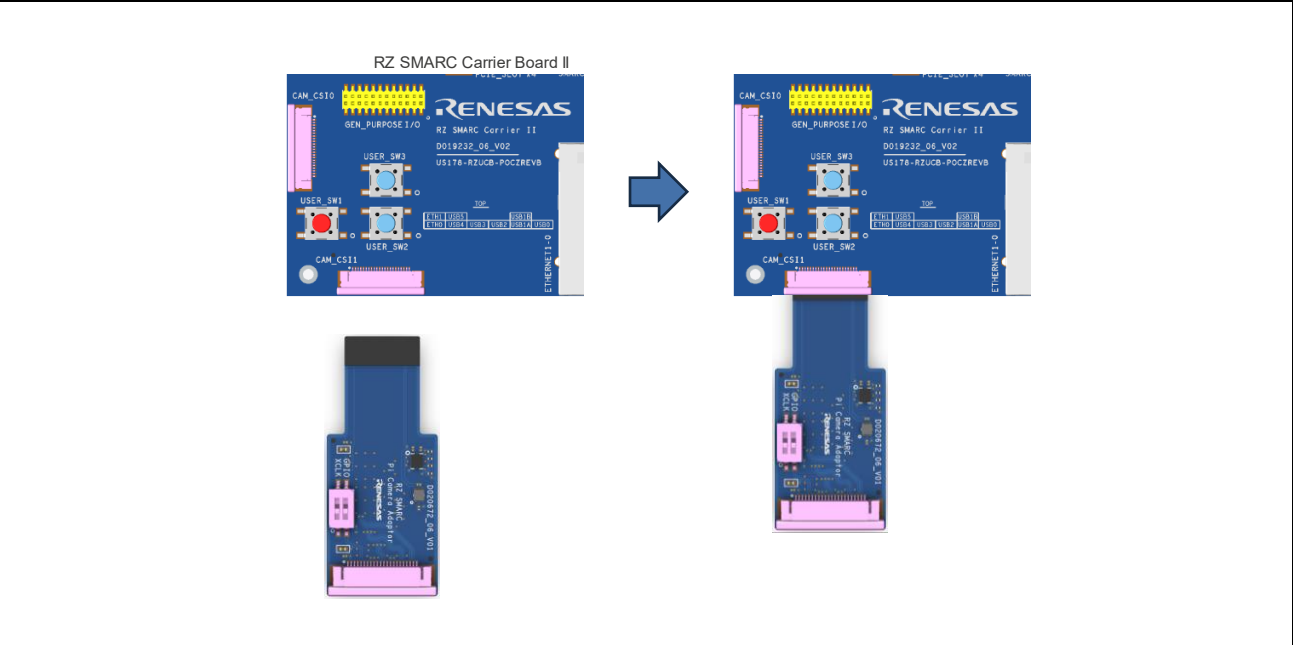


Figure 3.4 (c) SMARC Pi Camera Adaptor Connection

3.7 PMOD

RZ/G3S

RZ/G3E

The RZ SMARC Carrier II provides 3 PMOD interfaces, although there is some signal overlap, so care must be taken if both PMOD1 types are required simultaneously.

SER0 and some GPIOs are multiplexed, so refer to the relevant configuration settings to ensure the signals are available.

Table 3.6 PMOD Pin Assignment

Pin Number	PMOD0_2A (SPI)	PMOD1_3A (UART)	PMOD1_6A (I2C)
1	SPI1_CS0#	SER0_CTS#*1	GPIO10 (INT)
2	SPI1_DO	SER0_TX*1	GPIO11 (RESET)
3	SPI1_DIN	SER0_RX*1	I2C_GP_CK
4	SPI1_CK	SER0_RTS#*1	I2C_GP_DAT
5	Ground	Ground	Ground
6	PWR_PMOD0	PWR_PMOD1	PWR_PMOD1
7	GPIO4 (INT)	GPIO10 (INT)	GPIO8*2 (refer to SW_GPIO_CAN_PMOD)
8	GPIO5 (RESET)	GPIO11 (RESET)	GPIO9*2 (refer to SW_GPIO_CAN_PMOD)
9	GPIO6 / POWR_BTN# (refer to SW_PMOD0_PWR_SLP)	GPIO12*2	GPIO12*2
10	GPIO7 / SLEEP# (refer to SW_PMOD0_PWR_SLP)	GPIO13*2	GPIO13*2
11	Ground	Ground	Ground
12	PWR_PMOD0	PWR_PMOD1	PWR_PMOD1

Note 1. Refer to SW_OPT_MUX[4]

Note 2. Refer to SW_M2_DIS[4]

3.8 Audio

RZ/G3S

RZ/G3E

The mono SPEAKER connection is provided by a 2-pin header, 2.54-mm pitch.

All other audio connections are made using stereo connections to the 3.5-mm colored jack sockets. Signal lines support stereo.

Table 3.7 Functions of Each Jack

Color	Function	Direction
Blue	Auxiliary	In
Lime	Headphone	Out
Pink	Microphone	In

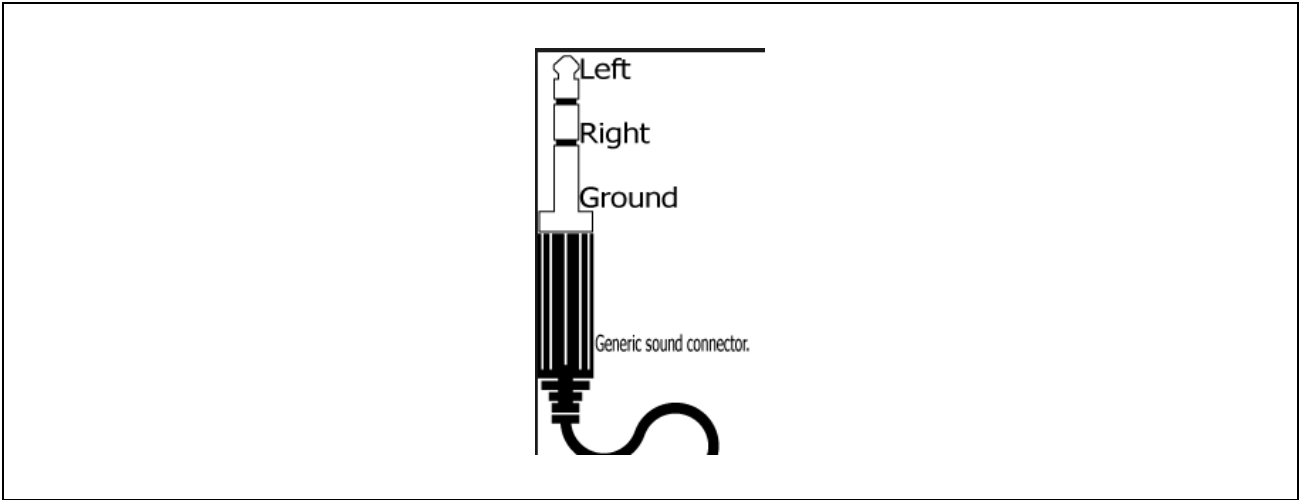


Figure 3.5 Stereo Jack

3.9 CAN

RZ/G3S

RZ/G3E

The RZ SMARC Carrier II provides 2 CAN channels, each connected through a 3-pin connector (JST, part number SM03B_SRRS-TB).

Table 3.8 CAN0 and CAN1 Pin Assignment

Pin Number	CAN0	CAN1
1	CAN0_H	CAN1_H
2	CAN0_L	CAN1_L
3	Ground	Ground
Transceiver STANDBY	GPIO8*1	GPIO9*1

Note 1. The on-board CAN transceiver has Standby functions that may be controlled using GPIO. Refer to SW_GPIO_CAN_PMOD for configuration.

3.10 microSD1 Card Interface

RZ/G3S

RZ/G3E

A microSD Card interface provides connection the SMARC SDIO signals, however, these signals are multiplexed. Refer to SW_OPT_MUX[1] for configuration.

3.11 M.2

RZ/G3S

RZ/G3E

Both Key E and Key B interfaces are provided for the RZ SMARC Carrier II.

3.11.1 M.2 Key E

A threaded spacer for Type-2230 is already inserted into the RZ SMARC Carrier II for mounting a plug-in M.2 Key E card. A $M2.5 \times 5$ mm machine screw is provided in the kit.

Table 3.9 Supported Interface for M.2 Key E

Communication Interface	SMARC Signal
USB2.0	USB1 via the 4-channel HUB
PCIe 2x Channels, 1-lane OR 1x Channel 2-lanes	PCIE_A, PCIE_B multiplexed
SDIO	SDIO multiplexed with the microSD card
I2S	I2S2 multiplexed with Display port 0
UART	SER0 (multiplexed with PMOD) or SER2
I2C	I2C_GP

Table 3.10 M.2 Key E Pin Assignment (1/2)

Pin	Signal	Signal	Pin
74	3.3 V	Ground	75
72	3.3 V	PCIE_M2E_REFCK1-	73
70	PCIE_WAKE#	PCIE_M2E_REFCK1+	71
68	PCIE_M2E_CKREQ1#	Ground	69
66	PCIE_M2E_RST1#	PCIE_M2E_RX1-	67
64	Not connected	PCIE_M2E_RX1+	65
62	Not connected	Ground	63
60	I2C_GP_CK	PCIE_M2E_TX1-	61
58	I2C_GP_DAT	PCIE_M2E_TX1+	59
56	M2E_W_DISABLE1#	Ground	57
54	M2E_W_DISABLE2#	PCIE_WAKE#	55
52	PCIE_M2E_RST0#	PCIE_M2E_CKREQ0#	53
50	M2E_SUSCLK (32.768 kHz)	Ground	51
48	Not connected	PCIE_M2E_REFCK0-	49
46	Not connected	PCIE_M2E_REFCK0+	47
44	Not connected	Ground	45
42	Not connected	PCIE_M2E_RX0-	43
40	Not connected	PCIE_M2E_RX0+	41
38	Not connected	Ground	39
36	SER0_RT#/#SER2_RT#	PCIE_M2E_TX0-	37
34	SER0_CT#/#SER2_CT#	PCIE_M2E_TX0+	35
32	SER0_TX/#SER2_TX	Ground	33
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	

Table 3.10 M.2 Key E Pin Assignment (2/2)

Pin	Signal	Signal	Pin
22	SER0_RX/SER2_RX	SDIO_RESET#	23
20	TP_M2E_UART_WAKE#	TP_M2E_SDIO_WAKE#	21
18	Not connected	SDIO_D3	19
16	M2E_LED2 (Red)	SDIO_D2	17
14	I2S2_SDOUT	SDIO_D1	15
12	I2S2_SDIN	SDIO_D0	13
10	I2S2_LRCK	SDIO_CMD	11
8	I2S2_CK	SDIO_CK	9
6	M2E_LED1 (Red)	Ground	7
4	3.3 V	USB1_M2E-	5
2	3.3 V	USB1_M2E+	3
		Ground	1

3.11.2 M.2 Key B

A threaded spacer for Type-3052 is already inserted into the RZ SMARC Carrier II for mounting a plug-in M.2 Key B card. A M2.5 × 5 mm machine screw is provided in the kit.

Type-xx42 or Type-xx30 plug-in M.2 Key B card can also be mounted using the threaded inserts and 2.5-mm spacer provided.

Table 3.11 Supported Interface for M.2 Key B

Communication Interface	SMARC Signal
USB2.0	USB1 via the 4-channel HUB
PCIe 1x Channel, 1-lane or 2-lanes	PCIE_A, PCIE_B multiplexed
USB3.0	USB2 multiplexed with USB-C
SIM card	N/A

Table 3.12 M.2 Key B Pin Assignment (1/2)

Pin	Signal	Signal	Pin
74	3.3 V	M2B_CONFIG2	75
72	3.3 V	Ground	73
70	3.3 V	Ground	71
68	M2B_SUSCLK* ¹	M2B_CONFIG1	69
66	Not connected	M2B_RESET#	67
64	M2B_COEX_RXD* ¹	M2B_ANTCTL3* ¹	65
62	M2B_COEX_TXD* ¹	M2B_ANTCTL2* ¹	63
60	M2B_COEX3* ¹	M2B_ANTCTL1* ¹	61
58	M2B_RFFE_DATA* ¹	M2B_ANTCTL0* ¹	59
56	M2B_RFFE_CLK* ¹	Ground	57
54	PCIE_WAKE#	PCIE_M2B_REFCK+	55
52	PCIE_M2B_CKREQ#	PCIE_M2B_REFCK-	53
50	PCIE_M2B_RST#	Ground	51
48	M2B_GPIO_4* ¹	PCIE_M2B_TX0+	49

Table 3.12 M.2 Key B Pin Assignment (2/2)

Pin	Signal	Signal	Pin
46	M2B_GPIO_3*1	PCIE_M2B_TX0-	47
44	M2B_GPIO_2*1	Ground	45
42	M2B_GPIO_1*1	PCIE_M2B_RX0+	43
40	M2B_GPIO_0*1	PCIE_M2B_RX0-	41
38	M2B_DEVSLP*1	Ground	39
36	SIM_PWR	PCIE_M2B_TX1+/USB2_SSTX_M2B+	37
34	SIM_DATA	PCIE_M2B_TX1-/USB2_SSTX_M2B-	35
32	SIM_CLK	Ground	33
30	SIM_RESET	PCIE_M2B_RX1+/USB2_SSRX_M2B+	31
28	M2B_GPIO_8*1	PCIE_M2B_RX1-/USB2_SSRX_M2B-	29
26	Pull-up 10k (W_DISABLE2#)	Ground	27
24	M2B_GPIO_7*1	M2B_DPR*1	25
22	M2B_GPIO_6*1	PCIE_WAKE#	23
20	M2B_GPIO_5*1	M2B_CONFIG0	21
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
10	M2B_LED1#	Ground	11
8	Pull-up 10k (W_DISABLE1#)	USB1_M2B-	9
6	M2B_FULL_CARD_POWER_OFF#	USB1_M2B+	7
4	3.3 V	Ground	5
2	3.3 V	Ground	3
		M2B_CONFIG3	1

Note 1. Connected to the M2B_GPIO header.

3.12 Display

RZ/G3E

The RZ SMARC Carrier II provides a micro-HDMI port for direct connection to the SMARC HDMI display interface and two further interfaces (DISP0 and DISP1) for LVDS/MIPI-DSI channels 0 and 1.

3.12.1 HDMI

A micro-HDMI is provided for direct connection the SMARC Module HDMI signals.

The G3E SMARC EVK supports this port via the MIPI DSI to HDMI conversion IC from Analog Devices (part number ADV7535BCBZ-RL) on the G3E SMARC Module.

3.12.2 DISP0 and DISP1

Two mini-PCIe connectors (not to be used for mini-PCIe cards) are provided for interfacing to SMARC LVDS/DSI signals.

Table 3.13 DISP0 Pin Assignment

Pin Number	DISP0 Signal	DISP0 Signal	Pin Number
1	5V_DISP0	3.3 V	2
3	5V_DISP0	3.3 V	4
5	5V_DISP0	3.3 V	6
7	5V_DISP0	3.3 V	8
9	Not connected	1.8 V	10
11	Not connected	1.8 V	12
13	Not connected	1.8 V	14
15	Not connected	1.8 V	16
	KEY	KEY	
17	Ground	Ground	18
19	LVDS0_CK+/DSI0_CLK+	I2S2_DISP0_CK	20
21	LVDS0_CK-/DSI0_CLK-	I2S2_DISP0_LRCK	22
23	Ground	I2S2_DISP0_SDIN	24
25	LVDS0_0+/DSI0_D0+	I2S2_DISP0_SDOUT	26
27	LVDS0_0-/DSI0_D0-	I2C_LCD_CK	28
29	Ground	I2C_LCD_DAT	30
31	LVDS0_1+/DSI0_D1+	Ground	32
33	LVDS0_1-/DSI0_D1-	LCD0_BKLT_PWM	34
35	Ground	Ground	36
37	LVDS0_2+/DSI0_D2+	DSI0_TE	38
39	LVDS0_2-/DSI0_D2-	LCD0_VDD_EN	40
41	Ground	LCD0_BKLT_EN	42
43	LVDS0_3+/DSI0_D3+	RESET_OUT#	44
45	LVDS0_3-/DSI0_D3-	DISP_INT#	46
47	Ground	Ground	48
49	Not connected	Not connected	50
51	Not connected	Not connected (DISP_ID)	52

Table 3.14 DISP1 Pin Assignment

Pin Number	DISP1 Signal	DISP1 Signal	Pin Number
1	5V_DISP1	3.3 V	2
3	5V_DISP1	3.3 V	4
5	5V_DISP1	3.3 V	6
7	5V_DISP1	3.3 V	8
9	Not connected	1.8 V	10
11	Not connected	1.8 V	12
13	Not connected	1.8 V	14
15	Not connected	1.8 V	16
	KEY	KEY	
17	Ground	Ground	18
19	LVDS1_CK+/DSI1_CLK+	Not connected	20
21	LVDS1_CK-/DSI1_CLK-	Not connected	22
23	Ground	Not connected	24
25	LVDS1_0+/DSI1_D0+	Not connected	26
27	LVDS1_0-/DSI1_D0-	I2C_LCD_CK	28
29	Ground	I2C_LCD_DAT	30
31	LVDS1_1+/DSI1_D1+	Ground	32
33	LVDS1_1-/DSI1_D1-	LCD1_BKLT_PWM	34
35	Ground	Ground	36
37	LVDS1_2+/DSI1_D2+	DSI1_TE	38
39	LVDS1_2-/DSI1_D2-	LCD1_VDD_EN	40
41	Ground	LCD1_BKLT_EN	42
43	LVDS1_3+/DSI1_D3+	RESET_OUT#	44
45	LVDS1_3-/DSI1_D3-	DISP_INT#	46
47	Ground	Ground	48
49	Not connected	Not connected	50
51	Not connected	Ground (DISP_ID)	52

3.12.2.1 Dual LVDS-HDMI Adaptor

The SMARC Dual LVDS-HDMI Adaptor is required to convert the RZ/G3E LVDS IO to HDMI output via the LVDS to HDMI conversion IC from ITE Tech (part number IT6263).

This adaptor board can be connected to the mini PCI Express & mSATA connectors which are DISP0 and DISP1 from TYCOELECTRONICS (part number 2041262-1) shown in **Figure 3.6 (b)**.

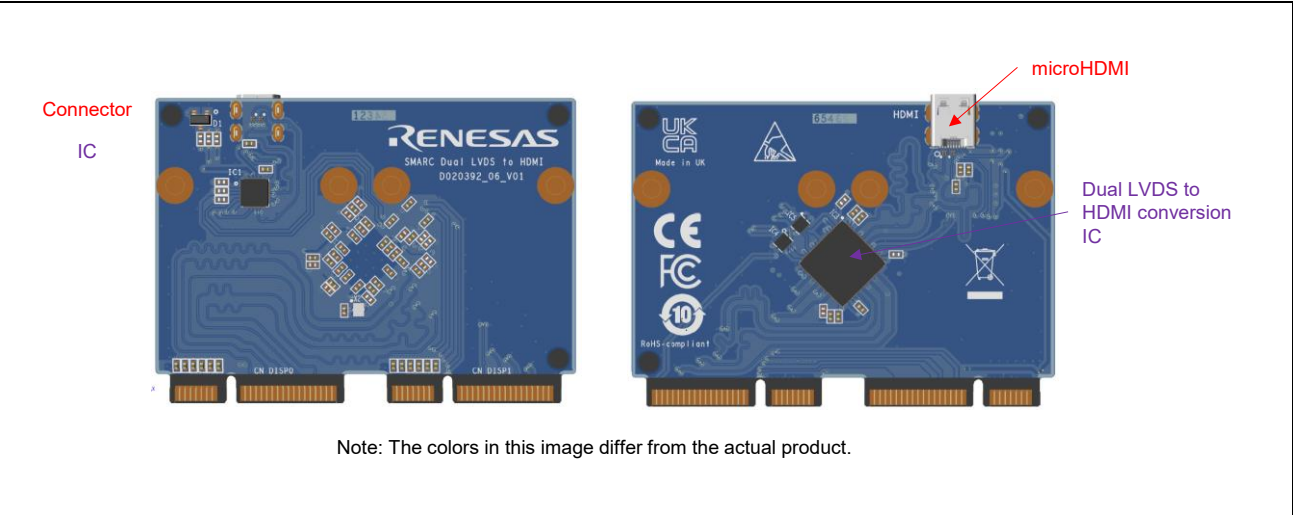


Figure 3.6 (a) SMARC Dual LVDS-HDMI Adaptor Top and Bottom View

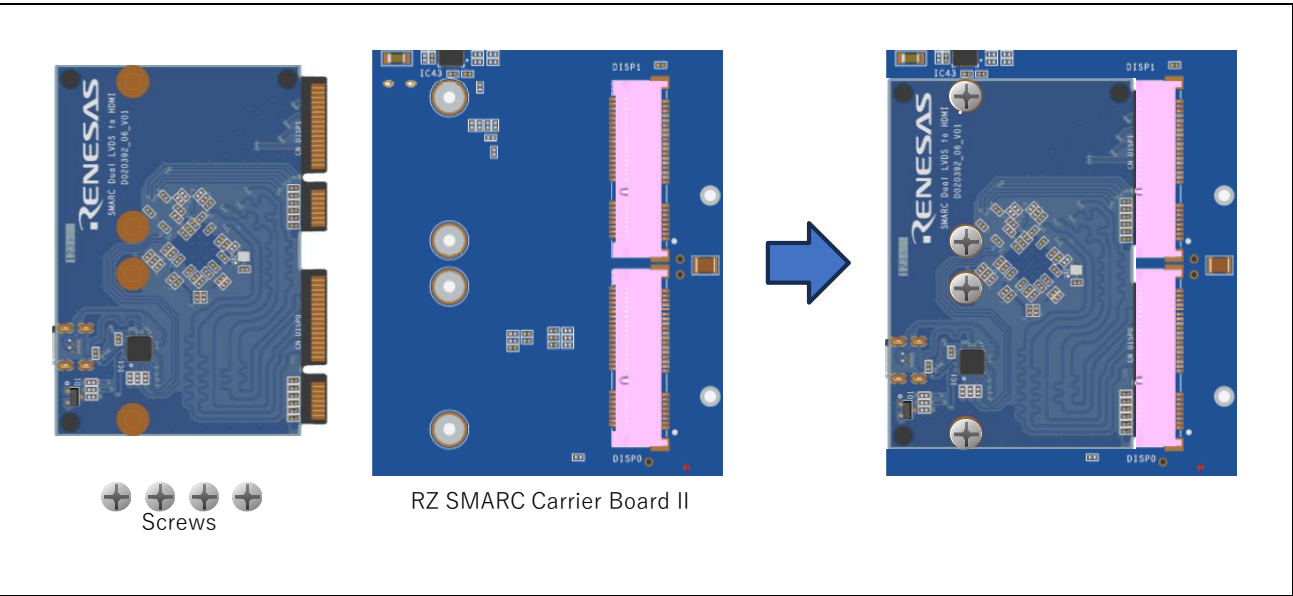


Figure 3.6 (b) SMARC Dual LVDS-HDMI Adaptor Connection

3.13 I2C

RZ/G3S

RZ/G3E

There are six I2C interfaces connected to the SMARC Module.

Table 3.15 Supported Interface for I2C

I2C Bus	Signal Names
Power management	I2C_PM_CK, I2C_PM_DAT
General purpose	I2C_GP_CK, I2C_GP_DAT
Camera interface 0	I2C_CAM0_CK, I2C_CAM0_DAT
Camera interface 1	I2C_CAM1_CK, I2C_CAM1_DAT
LCD display ID	I2C_LCD_CK, I2C_LCD_DAT
HDMI interface	HDMI_CTRL_CK, HDMI_CTRL_DAT

3.13.1 I2C_PM

This I2C bus is designed to support power management and system configuration management.

Table 3.16 Address Mapping for I2C_PM

I2C_PM Device	7-bit Address
Renesas ISL28022FRZ (current monitor)	0x44
Renesas GreenPAK SLG4AR45947 (logic)	0x08
Renesas GreenPAK SLG4AE45948 (logic)	0x10
Renesas GreenPAK SLG4L45949 (PCIe mixing)	0x18
HD3SS3220RNH (USB-C port controller)	0x47

3.13.2 I2C_GP

This I2C bus is intended for general purpose use.

Table 3.17 Address Mapping for I2C_GP

I2C_GP Device	7-bit Address
Renesas DA7212-01UM (audio codec)	0x1A
PMOD1 – Type-6A	
M.2 Key E	
GEN_PURPOSE IO	

3.13.2.1 Current Monitoring

The SMARC Module current can be measured by using I2C_PM to read the Renesas ISL28022FRZ.

3.13.2.2 Board Configuration

Using the I2C_PM bus, it is possible to read back the board configuration from many of the switches and M2B_CONFIG.

Table 3.18 Board Configuration

Switch Configuration Read	Linux Command	Bit
SW_GPIO_PMOD	i2cget -y 1 0x8 0x74	2
SW_SER0_PMOD	i2cget -y 1 0x8 0x74	6
SW_SDIO_M2E	i2cget -y 1 0x10 0xF0	7
SW_I2S2_M2E	i2cget -y 1 0x10 0xF0	6
SW_SPARE	i2cget -y 1 0x10 0xF0	4
SW_USB2_M2B	i2cget -y 1 0x10 0xF0	3
M2B_CONFIG3	i2cget -y 1 0x10 0xF6	4
M2B_CONFIG2	i2cget -y 1 0x10 0xF6	3
M2B_CONFIG1	i2cget -y 1 0x10 0xF6	1
M2B_CONFIG0	i2cget -y 1 0x10 0xF6	0
SW_PCIE_MUX0	i2cget -y 1 0x18 0xF0	6
SW_PCIE_MUX1	i2cget -y 1 0x18 0xF0	4
SW_PCIE_MUX2	i2cget -y 1 0x18 0xF0	2
PCIE_SLOT_PRNT#	i2cget -y 1 0x18 0xF0	1

3.13.2.3 M.2 Key E Controls

W_DISABLE1# and W_DISABLE2# control signals may be activated using the I2C_PM providing SW_M2_DIS[1], SW_M2_DIS[2] and SW_M2_DIS[4] are all ON.

After power on or reset, both W_DISABLE1# and W_DISABLE2# control signals are driven low. Setting the relevant bit to '1' and then to '0' toggles the state of the control signal.

Table 3.19 M.2 Key E Controls

M.2 Key E Control Signal	Linux Command	Bit
W_DISABLE1#	i2cset -y 1 0x08 0x7a	7
W_DISABLE2#	i2cset -y 1 0x08 0x7a	6

3.13.2.4 M.2 Key B Controls

M2B_RESET# control signal may be activated using the I2C_PM providing SW_M2_DIS[3] and SW_M2_DIS[4] are both ON.

M2B_FULL_CARD_POWER_OFF control signal may also be activated using the I2C_PM.

After power on or reset, both M2B_RESET# and M2B_FULL_CARD_POWER_OFF control signals are driven low. Setting the relevant bit to '1' and then to '0' toggles the state of the control signal.

Table 3.20 M.2 Key B Controls

M.2 Key B Control Signal	Linux Command	Bit
M2B_RESET#	i2cset -y 1 0x08 0x7a	5
M2B_FULL_CARD_POWER_OFF	i2cset -y 1 0x08 0x7a	4

3.13.3 I2C_CAM0, I2C_CAM1

This I2C bus is intended for camera support.

3.13.4 I2C_LCD

This I2C bus is intended for LCD display support and connects the SMARC Module directly to DISP0 and DISP1.

3.13.5 HDMI_CTRL

This I2C bus is intended for HDMI control and connects the SMARC Module to the micro-HDMI connector with level shifting and protection.

3.14 Miscellaneous

RZ/G3S

RZ/G3E

3.14.1 FAN

A 3-pin header is provided for connection to a standard fan IO.

Table 3.21 FAN Pin Assignment

Pin Number	CAN0
1	Not connected (Sense)
2	Power (12 V*1)
3	Ground

Note 1. If 5 V is required, resistor fitting options are available.

3.14.2 GEN_PURPOSE I/O

A 24-pin, 0.27 mm pitch header from Sullins, part number GRPB122VWQS-RC, provides access to general purpose IO.

NOTE

Take care connecting to some pins that are already used on the RZ SMARC Carrier II.

Table 3.22 GEN_PURPOSE I/O Pin Assignment

Pin Number	Signal	Signal	Pin Number
2	5.0 V	1.8 V	1
4	POWER_BTN#	BOOT_SEL0#	3
6	RESET_IN#	BOOT_SEL1#	5
8	SLEEP#	BOOT_SEL2#	7
10	5.0 V	Ground	9
12	Ground	SPI0_CS0#	11
14	SATA_TX+	SPI0_CK	13
16	SATA_TX-	SPI0_DIN	15
18	Ground	SPI0_DO	17
20	SATA_RX+	I2C_GP_CK	19
22	SATA_RX-	I2C_GP_DAT	21
24	Ground	Ground	23

3.14.3 M2B_GPIO

A 24-pin, 0.27-mm pitch header from Sullins, part number GRPB122VWQS-RC, provides access to general purpose IO for M.2 Key B.

Table 3.23 M2B_GPIO Pin Assignment

Pin Number	Signal	Signal	Pin Number
2	M2B_REFE_CLK	1.8 V	1
4	M2B_REFE_DATA	M2B_DEVSLP	3
6	CLK_32K	M2B_SUSCLK	5
8	M2B_GPIO_8	M2B_GPIO_0	7
10	M2B_ANTCTL0	M2B_GPIO_1	9
12	M2B_ANTCTL1	M2B_GPIO_2	11
14	M2B_ANTCTL2	M2B_GPIO_3	13
16	M2B_ANTCTL3	M2B_GPIO_4	15
18	M2B_COEX_RXD	M2B_GPIO_5	17
20	M2B_COEX_TXD	M2B_GPIO_6	19
22	M2B_COEX3	M2B_GPIO_7	21
24	M2B_DPR	Ground	23

3.14.4 M2B_SIM

A push-pull type, 1.27 mm pitch connector from Molex, part number 78646-3001, provides access to SIM card for M.2 Key B.

Table 3.24 M2B_SIM Pin Assignment

Pin Number	Signal
1	SIM_PWR
2	SIM_RESET
3	SIM_CLK
5	Ground
6	SIM_PWR
7	SIM_DATA

3.15 SMARC Module Connector

RZ/G3S

RZ/G3E

The 314 pin, 0.5 mm pitch, R/A memory socket style connector is used to interface the SMARC Module.

3.15.1 Display Interfaces

The RZ SMARC Carrier II provides two interfaces that may be used for LVDS, MIPI-DSI, or eDP signal and a secondary HDMI.

These signals are routed to DISP0:

Table 3.25 DISP0 Signals

LVDS Signal Name	MIPI DSI Signal Name	eDP Signal Name	Pin #	RZ Port Pin	Signal
LVDS0_0+	DSI0_D0+	eDP0_TX0+	S125	*1	*1
LVDS0_0-	DSI0_D0-	eDP0_TX0-	S126		
LVDS0_1+	DSI0_D1+	eDP0_TX1+	S128		
LVDS0_1-	DSI0_D1-	eDP0_TX1-	S129		
LVDS0_2+	DSI0_D2+	eDP0_TX2+	S131		
LVDS0_2-	DSI0_D2-	eDP0_TX2-	S132		
LVDS0_3+	DSI0_D3+	eDP0_TX3+	S137		
LVDS0_3-	DSI0_D3-	eDP0_TX3-	S138		
LVDS0_CLK+	DSI0_CLK+	eDP0_AUX+	S134	*1	*1
LVDS0_CLK-	DSI0_CLK-	eDP0_AUX-	S135		
LCD0_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN	S133	*1	*1
LCD0_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN	S127	*1	*1
LCD0_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM	S141	*1	*1
—	DSI0_TE	eDP0_HPD	S144	*1	*1
I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT	S140	*1	*1
I2C_LCD_CLK	I2C_LCD_CLK	I2C_LCD_CLK	S139	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

These signals are routed to DISP1.

Table 3.26 DISP1 Signals

LVDS Signal Name	MIPI DSI Signal Name	eDP Signal Name	Pin #	RZ Port Pin	Signal
LVDS1_0+	DSI1_D0+	eDP1_TX0+	S111	*1	*1
LVDS1_0-	DSI1_D0-	eDP1_TX0-	S112		
LVDS1_1+	DSI1_D1+	eDP1_TX1+	S114		
LVDS1_1-	DSI1_D1-	eDP1_TX1-	S115		
LVDS1_2+	DSI1_D2+	eDP1_TX2+	S117		
LVDS1_2-	DSI1_D2-	eDP1_TX2-	S118		
LVDS1_3+	DSI1_D3+	eDP1_TX3+	S120		
LVDS1_3-	DSI1_D3-	eDP1_TX3-	S121		
LVDS1_CLK+	DSI1_CLK+	eDP1_AUX+	S108	*1	*1
LVDS1_CLK-	DSI1_CLK-	eDP1_AUX-	S109		
LCD1_VDD_EN	LCD1_VDD_EN	LCD1_VDD_EN	S116	*1	*1
LCD1_BKLT_EN	LCD1_BKLT_EN	LCD1_BKLT_EN	S107	*1	*1
LCD1_BKLT_PWM	LCD1_BKLT_PWM	LCD1_BKLT_PWM	S122	*1	*1
—	DSI1_TE	eDP1_HPD	S113	*1	*1
I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT	S140	*1	*1
I2C_LCD_CLK	I2C_LCD_CLK	I2C_LCD_CLK	S139	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

These signals are routed to the HDMI connector.

Table 3.27 HDMI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
HDMI_D2+	P92	*1	*1
HDMI_D2-	P93		
HDMI_D1+	P95		
HDMI_D1-	P96		
HDMI_D0+	P98		
HDMI_D0-	P99		
HDMI_CLK+	P101	*1	*1
HDMI_CLK-	P102		
HDMI_CTRL_CLK	P105	*1	*1
HDMI_CTRL_DAT	P106	*1	*1
HDMI_HPD	P104	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.2 Camera Interfaces

The RZ SMARC Carrier II provides two interfaces that may be used for MIPI-CSI.

Table 3.28 CAM0 and CAM1 Signals

SMARC Signal Name	Pin #	Description	RZ Port Pin	Signal
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input	*1	*1
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock input (point to point)	*1	*1
I2C_CAM0_DAT/CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	*1	*1
I2C_CAM0_CK/CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	*1	*1
CAM0_PWR#	P108	Camera 0 Power Enable, active low output.	*1	*1
CAM0_RST#	P110	Camera 0 reset, active low output	*1	*1
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	*1	*1
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	*1	*1
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	*1	*1
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	*1	*1
CAM1_PWR#	P109	Camera 1 Power Enable, active low output	*1	*1
CAM1_RST#	P111	Camera 1 reset, active low output	*1	*1
CAM_MCK	S6	Master clock output	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.3 SDIO Card (4-bit) Interface

The SDIO signal is routed to the USB card slot.

Table 3.29 SDIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SDIO_D0	P39	*1	*1
SDIO_D1	P40	*1	*1
SDIO_D2	P41	*1	*1
SDIO_D3	P42	*1	*1
SDIO_WP	P33	*1	*1
SDIO_CMD	P34	*1	*1
SDIO_CD#	P35	*1	*1
SDIO_CK	P36	*1	*1
SDIO_PWR_EN	P37	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.4 SPI Interfaces

These signals are routed to the 24-pin header and the PMOD Type-2A connector.

Table 3.30 SPI0 and SPI1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SPI0_CS0#	P43	*1	*1
SPI0_CS1#	P31	*1	*1
SPI0_CK	P44	*1	*1
SPI0_DIN	P45	*1	*1
SPI0_DO	P46	*1	*1
SPI1_CS0#	P54	*1	*1
SPI1_CS1#	P55	*1	*1
SPI1_CK	P56	*1	*1
SPI1_DIN	P57	*1	*1
SPI1_DO	P58	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.5 Audio

These signals are routed to the Audio Codec and M.2 Key E.

Table 3.31 I2S0 and I2S2 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S0_LRCK	S39	*1	*1
I2S0_SDOUT	S40	*1	*1
I2S0_SDIN	S41	*1	*1
I2S0_CK	S42	*1	*1
AUDIO_MCK	S38	*1	*1
I2S2_LRCK	S50	*1	*1
I2S2_SDOUT	S51	*1	*1
I2S2_SDIN	S52	*1	*1
I2S2_CK	S53	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.6 I2C Interfaces

The I2C_GP signals are routed to the GPIO pin header, M.2 Key E, Audio Codec, and PMOD1 Type6A connector.

The I2C_PM signals are routed to the ISL28022FRZ, SLG4L45949, SLG4R45950, SLG4AE45947, and SLG4AE45948.

The I2C_CAM0 and I2C_CAM1 signals are routed to the 22-pin FPC connectors.

The I2C_LCD signal is routed to connected to the Mini PCI Express & mSATA connectors.

Table 3.32 I2C_GP and I2C_PM Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2C_GP_CK	S48	*1	*1
I2C_GP_DAT	S49	*1	*1
I2C_PM_CK	P121	*1	*1
I2C_PM_DAT	P122	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.7 Asynchronous Serial Ports

The RZ SMARC Carrier II provides four interfaces that may be used for asynchronous serial ports.

These signals are routed to the PMOD1 Type-3A connector, GROVE connector, M.2 Key E and DEBUG UART.

Table 3.33 SER0, SER2, and SER3 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SER0_TX	P129	*1	*1
SER0_RX	P130	*1	*1
SER0_RTS#	P131	*1	*1
SER0_CTS#	P132	*1	*1
SER1_TX	P134	*1	*1
SER1_RX*1	P135	*1	*1
SER2_TX	P136	*1	*1
SER2_RX	P137	*1	*1
SER2_RTS#	P138	*1	*1
SER2_CTS#	P139	*1	*1
SER3_TX	P140	*1	*1
SER3_RX	P141	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.8 CAN Bus

These signals are routed to the CAN connectors.

Table 3.34 CAN0 and CAN1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CAN0_TX	P143	*1	*1
CAN0_RX	P144	*1	*1
CAN1_TX	P145	*1	*1
CAN1_RX	P146	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.9 USB Interfaces

These signals are routed to the USB Type micro-AB and USB hub IC.

The USB channel 3, 4, and 5 signals are not connected to the Renesas SMARC Module

Table 3.35 USB0 and USB1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
USB0+	P60	*1	*1
USB0-	P61	*1	*1
USB0_EN_OC#	P62	*1	*1
USB0_VBUS_DET	P63	*1	*1
USB0_OTG_ID	P64	*1	*1
USB1+	P65	*1	*1
USB1-	P66	*1	*1
USB1_EN_OC#	P67	*1	*1
USB2+	P69	*1	*1
USB2-	P70	*1	*1
USB2_SSRX+	S74	*1	*1
USB2_SSRX-	S75	*1	*1
USB2_SSTX+	S71	*1	*1
USB2_SSTX-	S72	*1	*1
USB2_EN_OC#	P71	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.10 PCI Express

The PCIe signals are routed to the PCIe slot, M.2 Key E, and M.2 Key B.

Table 3.36 PCIe_A Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
PCIE_A_TX+	P89	*1	*1
PCIE_A_TX-	P90	*1	*1
PCIE_A_RX+	P86	*1	*1
PCIE_A_RX-	P87	*1	*1
PCIE_A_REFCK+	P83	*1	*1
PCIE_A_REFCK-	P84	*1	*1
PCIE_A_RST#	P75	*1	*1
PCIE_A_CKREQ#	P78	*1	*1
PCIE_B_TX+	S90	*1	*1
PCIE_B_TX-	S91	*1	*1
PCIE_B_RX+	S87	*1	*1
PCIE_B_RX-	S88	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.11 SATA

The RZG3S and RZ/G3E do not support SATA interfaces. None of the SATA signals are connected.

3.15.12 Ethernet

These signals are routed to the RJ45 connectors.

Table 3.37 GBE0 and GBE1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GBE0_MDI0+	P30	*1	*1
GBE0_MDI0-	P29		
GBE0_MDI1+	P27		
GBE0_MDI1-	P26		
GBE0_MDI2+	P24		
GBE0_MDI2-	P23		
GBE0_MDI3+	P20		
GBE0_MDI3-	P19		
GBE0_LINK100#	P21	*1	*1
GBE0_LINK1000#	P22	*1	*1
GBE0_LINK_ACT#	P25	*1	*1
GBE0_CTREF	P28	*1	*1
GBE0_SDP	P6	*1	*1
Ethernet PHY0 Interrupt	N/A	*1	*1
GBE1_MDI0+	S17	*1	*1
GBE1_MDI0-	S18		
GBE1_MDI1+	S20		
GBE1_MDI1-	S21		
GBE1_MDI2+	S23		
GBE1_MDI2-	S24		
GBE1_MDI3+	S26		
GBE1_MDI3-	S27		
GBE1_LINK100#	S19	*1	*1
GBE1_LINK1000#	S22	*1	*1
GBE1_LINK_ACT#	S31	*1	*1
GBE1_CTREF	S28	*1	*1
GBE1_SDP	P5	*1	*1
Ethernet PHY1 Interrupt	N/A	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

3.15.13 GPIO

Table 3.38 GPIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GPIO0	P108	*1	*1
GPIO1	P109	*1	*1
GPIO2	P110	*1	*1
GPIO3	P111	*1	*1
GPIO4	P112	*1	*1
GPIO5	P113	*1	*1
GPIO6	P114	*1	*1
GPIO7	P115	*1	*1
GPIO8	P116	*1	*1
GPIO9	P117	*1	*1
GPIO10	P118	*1	*1
GPIO11	P119	*1	*1
GPIO12	S142	*1	*1
GPIO13	S123	*1	*1

Note 1. Refer to the RZ/G3S and RZ/G3E SMARC Module Board Kit User's Manuals.

4. Certifications

The RZ SMARC Carrier II comprising the G3S and G3E SMARC EVKs meets the following certification/standards. See page 3 of this user's manual for the disclaimer and precautions.

4.1 EMC/EMI Standards

- FCC Notice (Class A)



This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

[NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)



This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)



This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

4.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013



For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.



This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at:

<https://www.renesas.com/en/support/regional-customer-support/weee>

4.3 Safety Standards

- UL 94V-0

REVISION HISTORY	RZ Family / RZ/G Series RZ SMARC Series Carrier Board II
------------------	---

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 14, 2023	—	First edition issued
1.10	July 07, 2025	All	RZ/G3E SMARC EVK, added
		11	1.1 Kit Contents The following boards were added. • RZ/G3E SMARC Carrier Board II Kit • RZ/G3E SMARC Module Board Kit
		12	2. System Description Figure 2.1 RZ SMARC Series Carrier Board II Top View, modified
		13	2. System Description Figure 2.2 RZ SMARC Series Carrier Board II Bottom View, modified
		14	2.1 G3S SMARC EVK Functional Block Figure 2.3, modified
		16, 17	2.2 Interface Mapping Table 2.1, modified
		29, 30	2.3.10 SW_M2_DIS – M.2 Card Control Signals Table 2.12: The table title was modified from “DIP Switch “SW_OPT_MUX” Settings” to “DIP Switch “SW_M2_DIS” Settings”.
		31, 32	2.3.11 SW_OPT_MUX Table 2.13: The table title was modified from “DIP Switch “SW_PCIE_MUX” Settings” to “DIP Switch “SW_OPT_MUX” Settings”.
		39	3.1 Power Figure 3.1, modified
		45, 46	Section 3.6.1 Pi Camera Adaptor, added
		55	Section 3.12.2.1 Dual LVDS-HDMI Adaptor, added
1.11	Oct. 29, 2025	All	Some sentences and tables have been reorganized for improved readability. The content of the document remains unchanged.
		13	2. System Description Figure 2.1 RZ SMARC Series Carrier Board II Top View, modified
		14	2. System Description Figure 2.2 RZ SMARC Series Carrier Board II Bottom View, modified
		16	2.1.2 G3E SMARC EVK Figure 2.4, modified
		17 to 20	2.2 Interface Mapping Tables 2.1 and 2.2, modified
		29	2.3.9 SW_MODE – BOOT Mode (and Power) Table 2.11, modified
		45	3.4 USB Table 3.3, modified
		55	3.12.1 HDMI, 3.12.2 DISP0 and DISP1 Descriptions, modified
		57	3.12.2.1 Dual LVDS-HDMI Adaptor Figure 3.6(a), modified
		63 to 71	3.15 SMARC Module Connector Tables 3.25 to 3.38, modified
		69	3.15.9 USB interfaces, 3.15.11 SATA Descriptions, modified

Rev.	Date	Description	
		Page	Summary
1.11	Oct. 29, 2025	72, 73	Section 4 Certifications, added

RZ SMARC Series Carrier Board II
User's Manual: Hardware

Publication Date:	Rev.1.00	Nov. 14, 2023
	Rev.1.11	Oct. 29, 2025

Published by:	Renesas Electronics Corporation
---------------	---------------------------------

RZ Family / RZ/G Series