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User's Manual

μPD788001A, 788002A, 78F8002A

8-Bit Single-Chip Microcontroller With LIN Transceiver & Power Supply

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μPD788001A
μPD788002A
μPD78F8002A

Document No. U17742EJ3V0UD00 (3rd edition)
Date Published September 2006 NS CP(K)

Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD788001A, 78F8002A, 78F8002A, and to design and develop application systems and programs for these devices.

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD788001A, 78F8002A, 78F8002A's manuals are separated into three manuals: this manual, 78K0/KB1 User's Manual, and the Instructions edition (common to the 78K/0 microcontrollers).

μPD788001A, 78F8002A, 78F8002A User's Manual (This Manual)	**78K0/KB1 User's Manual**	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- To know details of the microcontroller part:
  → Refer to the separate document **78K0/KB1 User's Manual (U15836E)**.

78K0/KB1 products	The products corresponding to the 78K0/KB1 products
μPD780101	–
μPD780102	μPD788001A
μPD780103	μPD788002A
μPD78F0103	μPD78F8002A

- To know details of the 78K/0 microcontrollers instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

- To know electrical specifications of the μPD788001A(A1) and 788002A(A1):
  → Refer to the separate document **μPD788001A(A1), 788002A(A1) Data Sheet (U18334E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Differences between μPD788001A, 788002A, 78F8002A and μPD788001, 788002, 78F8002

Item \ Product Name	μPD788001A, 788002A, 78F8002A	μPD788001, 788002, 78F8002
Minimum instruction execution time	0.166 μs (at 12 MHz operation)	0.2 μs (at 10 MHz operation)
Voltage Regulator output voltage	5 V ± 2% (I_{CM} = 100 mA)	5V ± 5% (I_{CM} = 100 mA)
LINO Dominant level output voltage	0.3 V (V_{SUP} = 7.3 V, I_{lino} = 15 mA)	0.2 V (V_{SUP} = 7.3 V, I_{lino} =15 mA) 0.4 V (V_{SUP} = 18 V, I_{lino} =36 mA)
Other	Improved EMS for voltage regulator circuit and LIN transceiver circuit	–

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD788001A, 788002A, 78F8002A User's Manual	This Manual
μPD788001A(A1), 788002A(A1) Data Sheet	U18334E
78K0/KB1 User's Manual	U15836E
78K/0 Series Instructions User's Manual	U12326E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Ver. 3.80 Assembler Package	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
CC78K0 Ver. 3.70 C Compiler	Operation	U17201E
	Language	U17200E
ID78K0-QB Ver. 2.81 Integrated Debugger	Operation	U16996E
PM plus Ver. 5.20		U16934E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0KX1H In-Circuit Emulator	U17081E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE − Product and Packages −	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Review of Quality and Reliability Handbook Information	C12769E

Note See the "Semiconductor Device Mount Manual" website (http://www.necel.com/pkg/en/mount/index.html)

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CONTENTS

CHAPTER 1 OUTLINE

μPD788001A, 788002A, and 78F8002A are MCP (Multi-Chip Package) which combined 2 chips in 1 package: an analog chip (including LIN transceiver, power supply, and several drivers) and a microcontroller chip.

8-bit microcontroller block is 78K0/KB1.

1.1 Features

○ ROM, RAM capacities

Item \ Part Number	Program Memory (ROM)		Data Memory (Internal High-Speed RAM)
μPD788001A	Mask memory	16 KB	768 bytes
μPD788002A		24 KB	
μPD78F8002A	Flash memory	24 KB[Note]	

Note The internal flash memory and internal high-speed RAM capacities can be changed using the internal memory size switching register (IMS).

○ On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
○ Short startup is possible via the CPU default start using the on-chip internal oscillator
○ On-chip clock monitor function using on-chip internal oscillator
○ On-chip watchdog timer (operable with internal oscillator clock)
○ I/O ports: 21
○ Timer: 5 channels
○ Serial interface: 2 channels
  UART (supporting LIN bus): 1 channel
  CSI/UART[Note] : 1 channel
○ 10-bit resolution A/D converter: 3 channels
○ On-chip power supply circuit (power transistors are external)
  Output voltage: 5 V ± 2%
  On-chip overcurrent protection circuit
○ LIN transceiver
  The LIN transceiver complies with LIN Specifications Rev.2.0
  On-chip wakeup function
  Low power consumption achieved with on-chip sleep function
  On-chip pull-up resistors for slave applications
  On-chip LIN driver current limiter
  On-chip LIN driver thermal shutdown circuit
○ Package: 38-pin plastic SSOP (7.62 mm (300))
○ Operation ambient temperature: T_A = −40 to +85 °C

Note Select either of the functions of these alternate-function pins.

1.2 Applications

○ Automotive equipment

System control for body electronic control units

- Power windows
- Keyless entry reception
- Immobilizer
- Mirror control, etc.

1.3 Ordering Information

Part Number	Package	Internal ROM
μPD788001AMC(A)-xxx-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	MASK memory
μPD788002AMC(A)-xxx-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	MASK memory
μPD78F8002AM5MC(A)-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	FLASH memory
μPD78F8002AM6MC(A)-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	FLASH memory

Remark ××× indicates ROM code suffix.

Mask ROM versions (μPD788001A, and 788002A) include mask options. When ordering, it is possible to select whether “Internal oscillator clock can be stopped/cannot be stopped by software”.

Flash memory versions supporting the mask options of the mask ROM versions are as follows.

Table 1-1. Flash Memory Versions Supporting Mask Options of Mask ROM Versions

Mask Option		Flash Memory Versions (Part Number)
POC Circuit	Internal Oscillator	
POC used (V_{POC} = 3.5 ± 0.2 V)	Cannot be stopped	μPD78F8002AM5MC(A)-GAA-AX
	Can be stopped by software	μPD78F8002AM6MC(A)-GAA-AX

1.4 Quality Grade

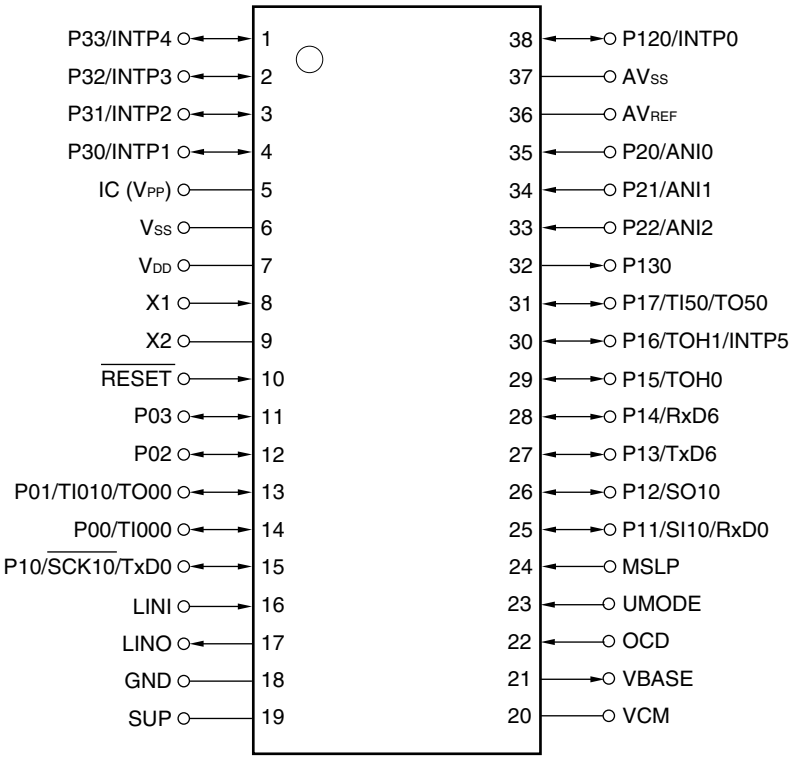
Part Number	Package	Quality Grade
μPD788001AMC(A)-xxx-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	Special
μPD788002AMC(A)-xxx-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	Special
μPD78F8002AM5MC(A)-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	Special
μPD78F8002AM6MC(A)-GAA-AX	38-pin plastic SSOP (7.62 mm (300))	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of quality grade on the devices and its recommended applications.

1.5 Pin Configuration (Top View)

- 38-pin plastic SSOP (7.62 mm (300))



Cautions 1. Connect the IC (Internally Connected) pin directly with V_{SS}.

2. Connect the AV_{REF} pin to V_{DD} respectively.

3. Connect the AV_{SS} pin to V_{SS} respectively.

4. Make sure the potential of V_{SS} and GND is the same.

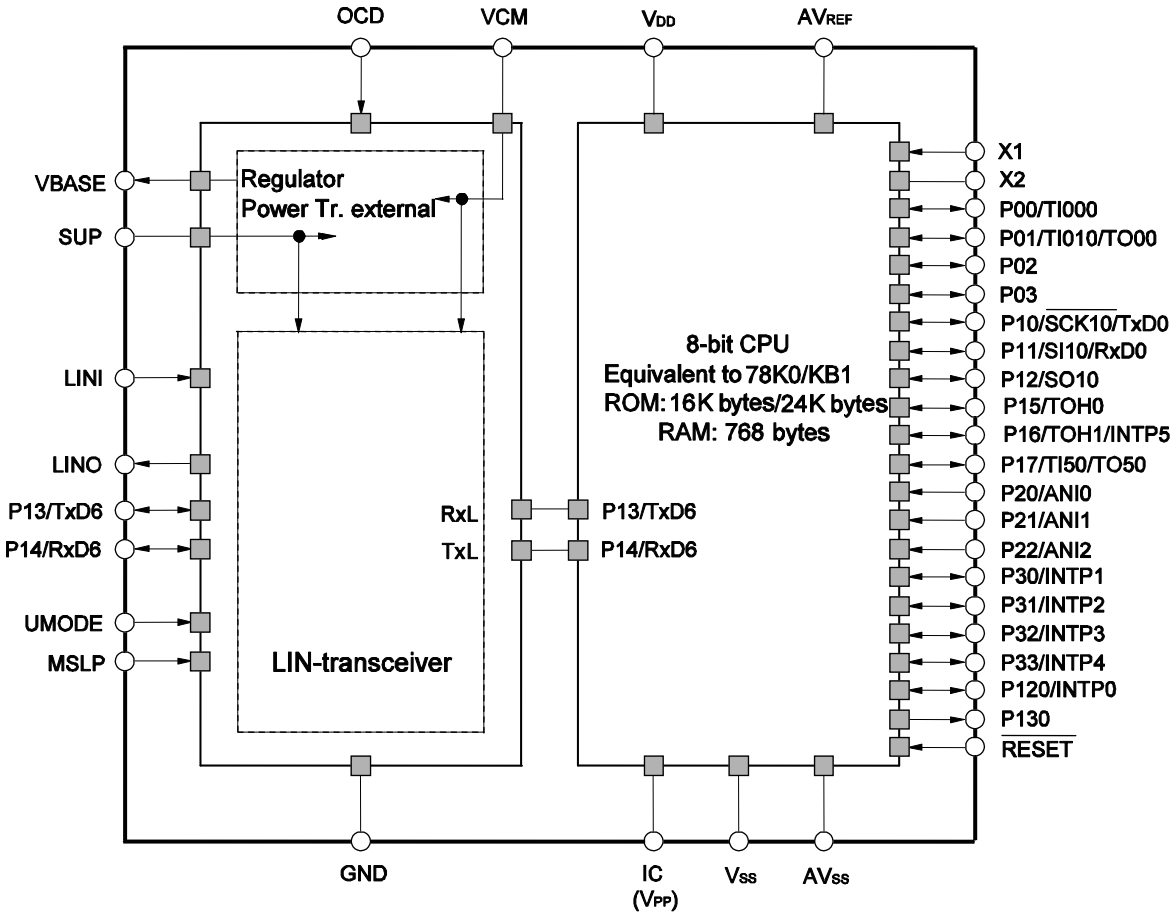
5. Make sure the potential of V_{CM} and V_{DD} is the same.

Remark Figures in parentheses apply only to the μPD78F8002A.

Pin Identification

ANI0 to ANI3:	Analog input
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
GND:	Ground
IC:	Internally connected
INTP0 to INTP5:	External interrupt input
LINI:	LIN bus data input
LINO:	LIN bus data output
MSLP:	Mode select port
OCD:	Over current detect
P00 to P03:	Port 0
P10 to P17:	Port 1
P120:	Port 12
P130:	Port 13
P20 to P22:	Port 2
P30 to P33:	Port 3
$\overline{\text{RESET}}$:	Reset
RxD0, RxD6:	Receive data
$\overline{\text{SCK10}}$:	Serial clock input/output
SI10:	Serial data input
SO10:	Serial data output
SUP:	Power supply
TI000, TI010, TI50:	Timer input
TO00, TO50, TOH0, TOH1:	Timer output
TxD0, TxD6:	Transmit data
UMODE:	Uart/LIN mode select port
VBASE:	base control
VCM:	Vcc controller
V_{DD}:	Power supply for Micro
V_{PP}:	Programming power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (X1 input clock)

1.6 Block Diagram



Cautions 1. The A/D input of the μPD788001A, 788002A, 78F8002A consists of 3 channels (ANI0 to ANI2). This differs from the number of A/D channels (4 channels) of 78K0/KB1 products.

2. Make sure the potential of V_{SS} and GND is the same.

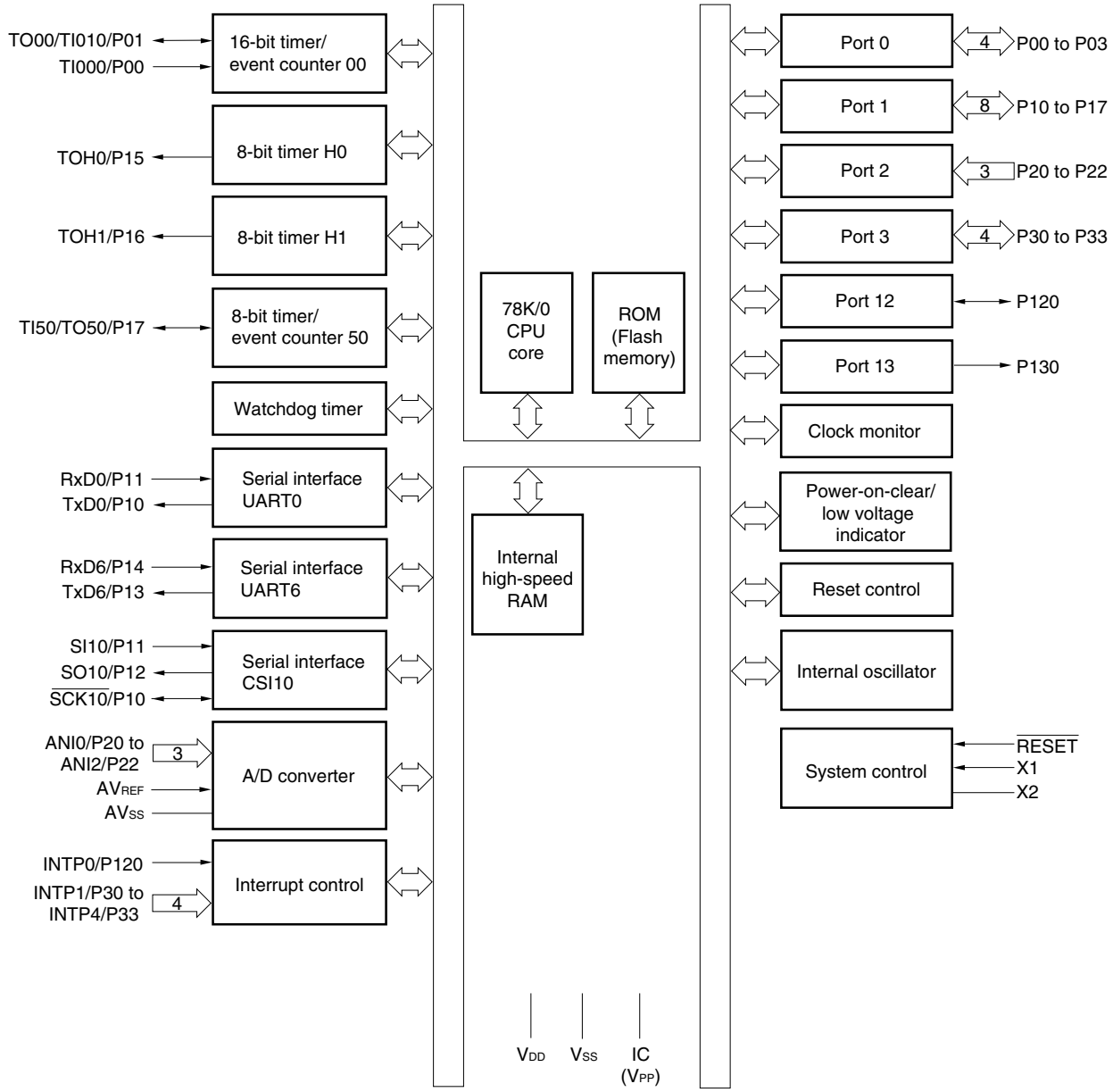
3. Make sure the potential of V_{CM} and V_{DD} is the same.

4. μPD788001A, 788002A, 78F8002A are MCP (Multi Chip Package) which have the built-in 2 chips (Voltage Regulator, LIN Transceiver).

5. P13/TxD6 and P14/RxD6 terminal are connected with LIN transceiver circuit in package.

Remark Figures in parentheses apply only to the μPD78F8002A.

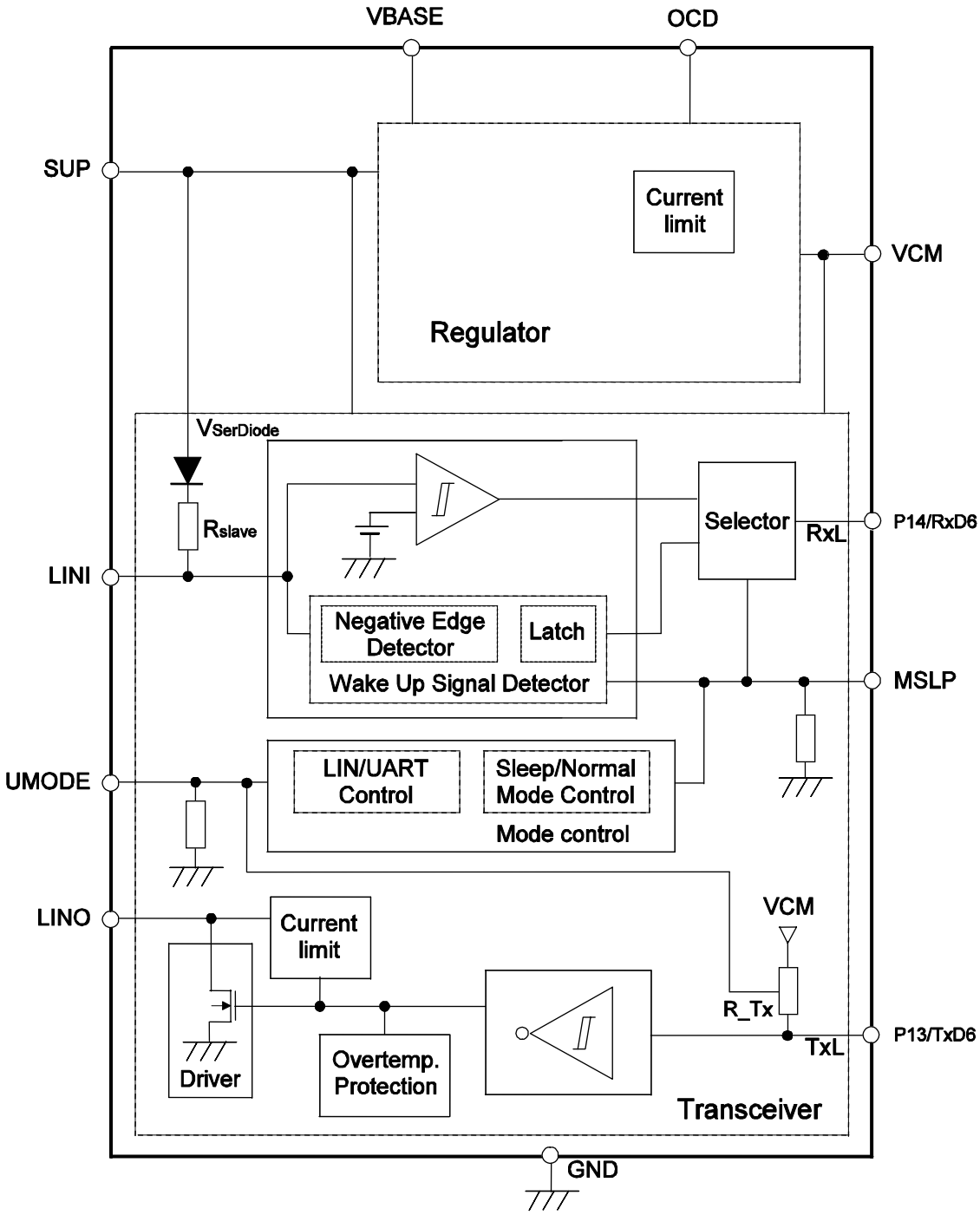
1.6.1 Microcontroller block diagram



Caution The A/D input of the μPD788001A, 788002A, and 78F8002A consists of 3 channels (ANI0 to ANI2). This differs from the number of A/D channels (4 channels) of 78K0/KB1 products.

Remark Items in parentheses are available only in the μPD78F8002A.

1.6.2 Analog block diagram



1.7 Outline of Functions

(1/2)

Item		μPD788001A	μPD788002A	μPD78F8002A
Internal memory	ROM	16 KB	24 KB	24 KB (flash memory)
	High-speed RAM	768 bytes		
Memory space		64 KB		
X1 input clock (oscillation frequency)		Ceramic/crystal clock oscillation (12 MHz: V_{DD} = 4.0 to 5.1 V)		
Internal oscillator clock (oscillation frequency)		On-chip internal oscillation (240 kHz (TYP.) V_{DD} = 2.5 to 5.1 V)		
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Minimum instruction execution time		0.166 μs/0.333 μs/0.666 μs/1.333 μs/2.666 μs (X1 input clock: @ f_{XP} = 12 MHz operation)		
		8.3 μs/16.6 μs/33.2 μs/66.4 μs/132.8 μs (TYP.) (Internal oscillator clock: @ f_R = 240 kHz (TYP.) operation)		
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, and Boolean operation) • BCD adjust, etc.		
I/O ports		Total: 21 CMOS I/O 17 CMOS input 3 CMOS output 1		
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 1 channel • 8-bit timer: 2 channels • Watchdog timer: 1 channel		
Timer outputs		4 (PWM outputs: 3)		
A/D converter		10-bit resolution × 3 channels		
Serial interface		• UART mode supporting LIN-bus: 1 channel • 3-wire serial I/O mode/UART mode[Note]: 1 channel		
Vectored interrupt sources	Internal	12		
	External	6		
Reset		• Reset using $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by clock monitor • Internal reset by power-on-clear • Internal reset by low-voltage detector		
LIN transceiver		• The LIN transceiver complies with LIN Specifications Rev.2.0 • On-chip wakeup function • On-chip sleep function • On-chip pull-up resistors for slave applications • On-chip LIN driver current limiter • On-chip LIN driver thermal shutdown circuit		

Note Select either of the functions of these alternate-function pins.

(2/2)

Item	μPD788001A	μPD788002A	μPD78F8002A
Power supply	• Output voltage: 5 V ± 2% • On-chip over current protection circuit		
Operating ambient temperature	T_A = –40 to +85°C		
Package	38-pin plastic SSOP (7.62 mm (300))		

An outline of the timer is shown below.

		16-Bit Timer/ Event Counter 00	8-Bit Timer/ Event Counters 50	8-Bit Timers H0 and H1		Watchdog Timer
		TM00	TM50	TMH0	TMH1	
Operation mode	Interval timer	1 channel	1 channel	1 channel	1 channel	–
	External event counter	1 channel	1 channel	–	–	–
	Watchdog timer	–	–	–	–	1 channel
Function	Timer output	1 output	1 output	1 output	1 output	–
	PPG output	1 output	–	–	–	–
	PWM output	–	1 output	1 output	1 output	–
	Pulse width measurement	2 inputs	–	–	–	–
	Square-wave output	1 output	1 output	1 output	1 output	–
	Interrupt source	2	1	1	1	–

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P22
V_{DD}	Pins other than P20 to P22

(1) Port functions

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	TI000
P01				TI010/TO00
P02				–
P03				
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	$\overline{SCK10}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P22	Input	Port 2. 3-bit input-only port.	Input	ANI0 to ANI2
P30 to P33	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP1 to INTP4
P120	I/O	Port 12. 1-bit I/O port. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP0
P130	Output	Port 13. 1-bit output-only port.	Output	–

(2) Non-port functions (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P120
INTP1 to INTP4				P30 to P33
INTP5				P16/TOH1
SI10	Input	Serial data input to serial interface	Input	P11/RxD0
SO10	Output	Serial data output from serial interface	Input	P12
$\overline{SCK10}$	I/O	Clock input/output for serial interface	Input	P10/TxD0
RxD0	Input	Serial data input to asynchronous serial interface	Input	P11/SI10
RxD6				P14
TxD0	Output	Serial data output from asynchronous serial interface	Input	P10/$\overline{SCK10}$
TxD6				P13
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input	P00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
TO00	Output	16-bit timer/event counter 00 output	Input	P01/TI010
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P17/TO50
TO50	Output	8-bit timer/event counter 50 output	Input	P17/TI50
TOH0	Output	8-bit timer H0 output	Input	P15
TOH1		8-bit timer H1 output		P16/INTP5
ANI0 to ANI2	Input	A/D converter analog input	Input	P20 to P22
<R> AV_{REF}	Input	A/D converter reference voltage input	–	–
AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting resonator for X1 input clock	–	–
X2	–		–	–

(2) Non-port functions (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC	–	Internally connected. Connect directly to V_{SS}.	–	–
V_{PP}	–	Flash memory programming mode setting. High-voltage application for program write/verify. Connect to V_{SS} in normal operation mode.	–	–
LINI	Input	LIN bus connection pin[Note]	–	–
LINO	Output	LIN driver pin[Note]	–	–
VBASE	Output	Base current control pin for power supply external transistor	–	–
OCD	Input	Power supply overcurrent monitor pin	–	–
VCM	–	Power supply voltage monitor and power supply pin	–	–
MSLP	Input	Sleep mode selection pin	–	–
UMODE	Input	LIN transceiver function enable/disable selection pin Low: Enable LIN transceiver High: Disable LIN transceiver	–	–
SUP	–	Supply power connection pin	–	–
GND	–	Ground potential of LIN transceiver block	–	–

Note An external diode is required for negative charge protection between the LINI and LINO pins.

Caution Make sure the potential of V_{SS} and GND is the same.

2.2 Description of Pin Functions

2.2.1 P00 to P03 (port 0)

4-bit I/O port. These pins also function as timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

4-bit I/O port. P00 to P03 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P03 function as timer I/O.

(a) TI000

This is the pins for inputting an external count clock to 16-bit timer/event counter 00 and is also for inputting a capture trigger signal to the capture registers (CR000, CR010) of 16-bit timer/event counter 00.

(b) TI010

This is the pin for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counter 00.

(c) TO00

This is a timer output pin of 16-bit timer/event counters 00 .

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as pins for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

Note that the UMODE pin must also be set when setting P13 and P14.

(a) P13

When the LIN transceiver function is enabled (UMODE = Low), the LIN bus transmit signal from the microcontroller is output as is.

When the LIN transceiver function is disabled (UMODE = High), this pin is used as the P13 I/O pin.

(b) P14

When the LIN transceiver function is enabled (UMODE = Low), the LIN bus receive signal from the LIN transceiver is output as is.

When the LIN transceiver function is disabled (UMODE = High), this pin is used as the P14 I/O pin.

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

(a) SI10, SO10

These are the serial data I/O pins of the serial interface.

(b) $\overline{\text{SCK10}}$

This is the serial clock I/O pin of the serial interface.

(c) RxD0, TxD0

These are the serial data I/O pins of the asynchronous serial interface.

(d) TI50

This is the pin for inputting an external count clock to 8-bit timer/event counter 50.

(e) TO50, TOH0, and TOH1

These are timer output pins.

(f) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(g) TxD6

When the LIN transceiver function is enabled (UMODE = Low), the LIN bus transmit signal from the microcontroller is output as is.

When the LIN transceiver function is disabled (UMODE = High), this pin is used as the serial data output pin of the asynchronous serial interface.

(h) RxD6

When the LIN transceiver function is enabled (UMODE = Low), the LIN bus receive signal from the LIN transceiver is output as is.

When the LIN transceiver function is disabled (UMODE = High), this pin is used as the serial data input pin of the asynchronous serial interface.

2.2.3 P20 to P22 (port 2)

P20 to P22 function as a 3-bit input only port. These pins also function as pins for A/D converter analog input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P22 function as a 3-bit input only port.

(2) Control mode

P20 to P22 function as A/D converter analog input pins (ANI0 to ANI2).

2.2.4 P30 to P33 (port 3)

P30 to P33 function as a 4-bit I/O port. These pins also function as pins for external interrupt request input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as a 4-bit I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input pins (INTP1 to INTP4) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified..

2.2.5 P120 (port 12)

P120 functions as a 1-bit I/O port. This pin also functions as a pin for external interrupt request input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as a 1-bit I/O port. P120 can be set to input or output in 1-bit units using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

(2) Control mode

P120 functions as an external interrupt request input pin (INTP0) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.6 P130 (port 13)

P130 functions as a 1-bit output-only port.

2.2.7 AV_{REF}

This is the A/D converter reference voltage input pin.

When the A/D converter is not used, connect this pin directly to V_{DD}.

2.2.8 AV_{SS}

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

2.2.9 $\overline{RESET}$

This is the active-low system reset input pin.

2.2.10 X1 and X2

These are the pins for connecting a resonator for high-speed system clock.

When supplying an external clock, input a signal to the X1 pin and input the inverse signal to the X2 pin.

2.2.11 V_{DD}

V_{DD} is the positive power supply pin for other than ports.

2.2.12 V_{SS}

V_{SS} is the ground potential pin for other than ports.

2.2.13 V_{PP} (flash memory versions only)

This is a pin for flash memory programming mode setting and high-voltage application for program write/verify.

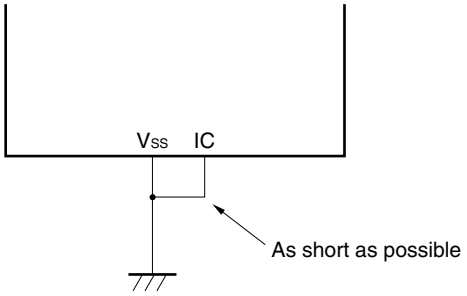
Connect to V_{SS} in the normal operation mode.

2.2.14 IC (mask ROM versions only)

The IC (Internally Connected) pin is provided to set the test mode to check the 78K0/KB1 at shipment. Connect it directly to V_{SS} with the shortest possible wire in the normal operation mode.

When a potential difference is produced between the IC pin and the V_{SS} pin because the wiring between these two pins is too long or external noise is input to the IC pin, the user's program may not operate normally.

- **Connect the IC pin directly to V_{SS}.**



2.2.15 LINI

This is the LIN bus data input pin.

It is pulled up with a diode and 30 kΩ (TYP.) resistor inside the IC for the slave system. When using this IC as the master, it must be pulled up externally with a diode and 1 kΩ resistor.

An external diode is required for negative charge protection between the LINI and LINO pins.

2.2.16 LINO

This is the LIN bus data output pin.

When TxD6 is high-level output, the LIN driver switches off (LIN bus: Recessive status).

When TxD6 is low-level output, the LIN driver switches on (LIN bus: Dominant status).

An external diode is required for negative charge protection between the LINI and LINO pins.

2.2.17 MSLP

This is the pin that receives mode transition instructions.

In the normal mode, the LIN transceiver goes into the sleep mode when MSLP = Low.

In the sleep mode, the LIN transceiver goes into the normal mode when MSLP = High.

Moreover, this pin is pulled down within the IC.

2.2.18 UMODE

This is a mode pin for enabling/disabling the LIN transceiver function. This pin is pulled down within the IC.

UMODE	LIN Transceiver Circuit Status	P13/TxD6 Pin Status	P14/RxD6 Pin Status
Low	Active	Output[Note] (TxL: Pull up input)	Output[Note] (RxL: Output)
High	Non active (Driver OFF)	Input /Output	Input /Output

Note When the LIN transceiver function is enabled, leave the P13/TxD6 and P14/RxD6 pins open. Clear PM13 to 0 (P13/TxD6 output setting) and set PM14 to 1 (P14/RxD6 input setting)

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-2 shows the types of pin I/O circuit and the recommended connections of unused pins.
Refer to Figure 2-1 for the configuration of the I/O circuits of each type.

Table 2-2. Pin I/O Circuit Types

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P02			
P03			
P10/$\overline{SCK10}$/TxD0			
P11/SI10/RxD0			
P12/SO10	5-A		
P13/TxD6 Note			
P14/RxD6 Note	8-A		
P15/TOH0	5-A		
P16/TOH1/INTP5	8-A		
P17/TI50/TO50			
P20/ANI0 to P22/ANI2	9-C	Input	Connect to V_{DD} or V_{SS}.
P30/INTP1 to P33/INTP4	8-A	I/O	Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P120/INTP0			Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P130	3-C	Output	Leave open.
$\overline{RESET}$	2	Input	Connect to V_{DD}.
AV_{REF}	–	Input	Connect directly to V_{DD}.
AV_{SS}		–	Connect directly to V_{SS}.
IC			
V_{PP}			Connect to V_{SS}.
LINI	LIN-1	Input	Leave open.
LINO	LIN-2	Output	Leave open.
VBASE	LIN-3	Output	–
OCD	LIN-4	Input	Connect directly to SUP
VCM	LIN-5	–	–
MSLP	LIN-6	Input	Leave open.
UMODE	LIN-7	Input	When using LIN transceiver: Leave open. When not using LIN transceiver: Connect directly to V_{DD}.

Note This pin also has an alternate function as the LIN transceiver function pin. When using this pin as the LIN transceiver function pin, leave it open.
When used as a microcontroller function pin, the UMODE pin must be externally pulled up.

Caution An external diode is required for negative charge protection between the LINI and LINO pins.

Figure 2-1. Pin I/O Circuit List (1/2)

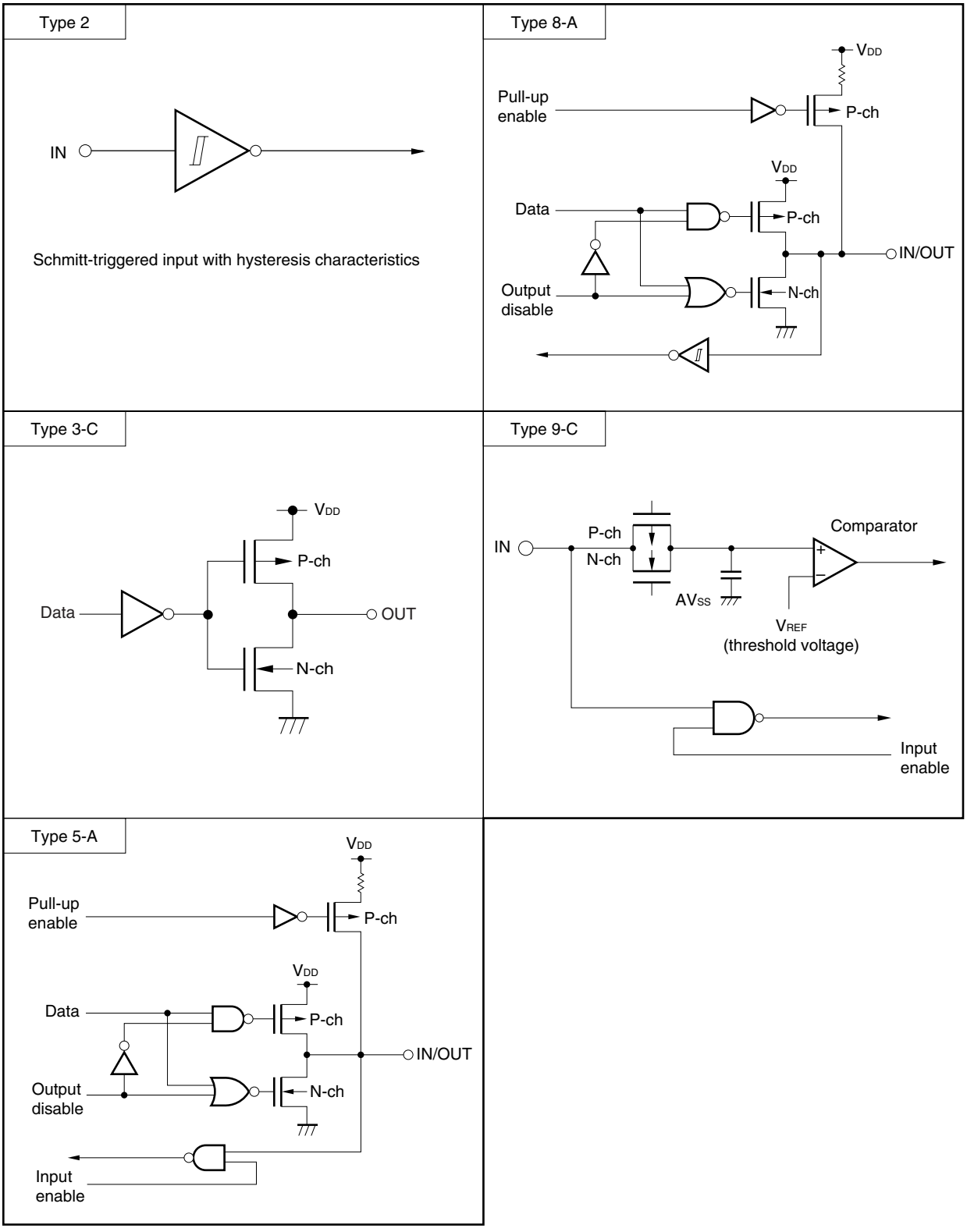
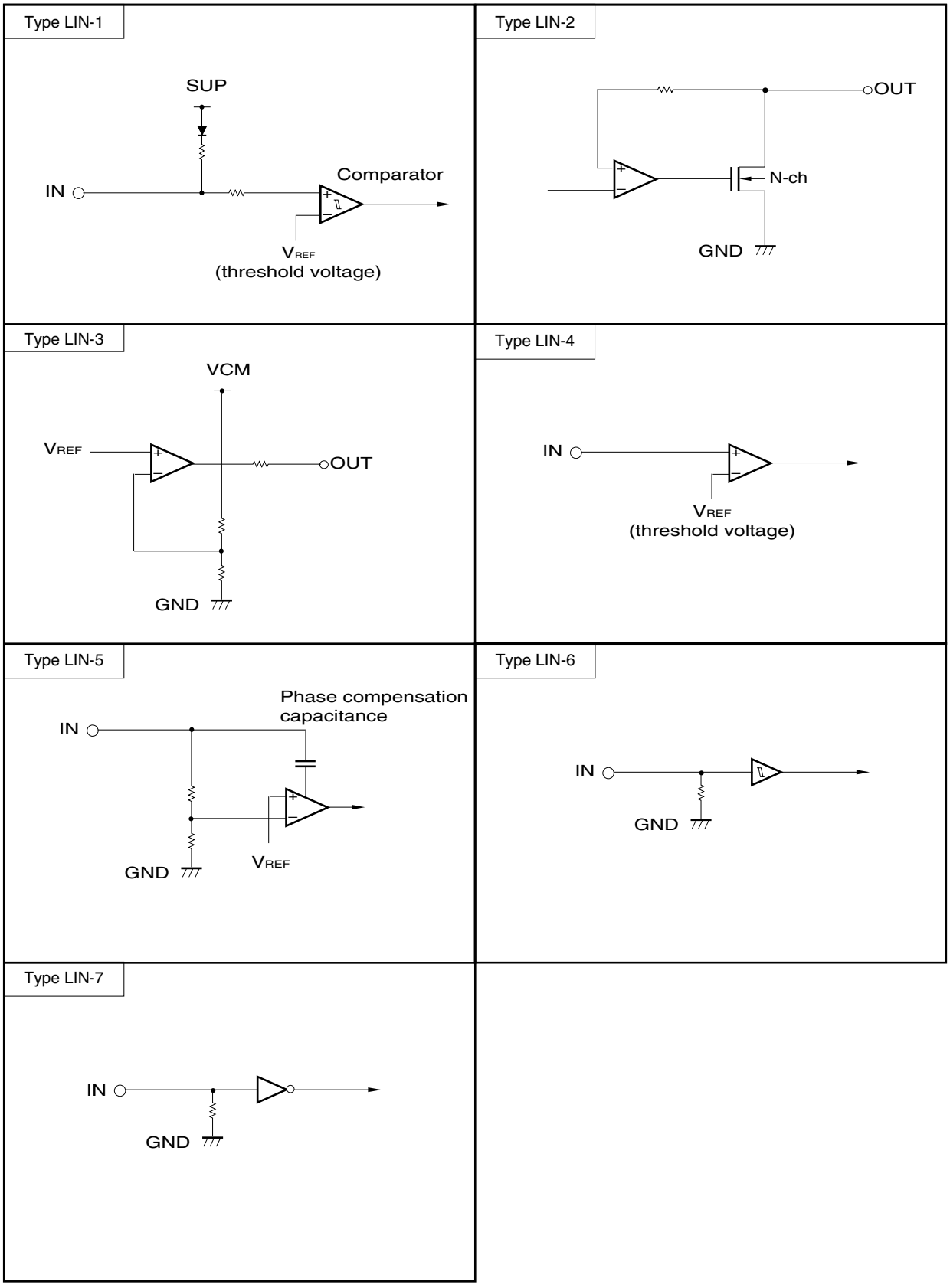


Figure 2-1. Pin I/O Circuit List (2/2)



CHAPTER 3 MICROCONTROLLER FUNCTIONS

The 8-bit microcontroller block is equipped with functions equivalent to those of the 78K0/KB1.
The differences in microcontroller functions between the μPD788001A, 788002A, and 78F8002A and the 78K0/KB1 are as follows.

Item	μPD788001A, 788002A, 78F8002A	78K0/KB1
A/D converter	10-bit resolution × 3 channels	10-bit resolution × 4 channels
I/O port	21	22

Except for number of A/D converter channels and ports, the μPD788001A, 788002A, and 78F8002A have the same functions as the 78K0/KB1.

The μPD788001A, 788002A, and 78F8002A do not have the P23/ANI3 pin.

3.1 Port Functions

The μPD788001A, 788002A, and 78F8002A have the ports shown in Figure 3-1, allowing for a variety of control. The functions of these ports are listed in Table 3-1.

In addition to functions as digital I/O ports, various alternate functions are provided. For a description of the alternate functions, refer to **CHAPTER 2 PIN FUNCTIONS**.

The differences in ports functions between the μPD788001A, 788002A, and 78F8002A, and the 78K0/KB1 are as follows.

Item	μPD788001A, 788002A, 78F8002A	78K0/KB1
Port 2	P20 to P22 (3)	P20 to P23 (4)
I/O port	21	22

Figure 3-1. Port Types

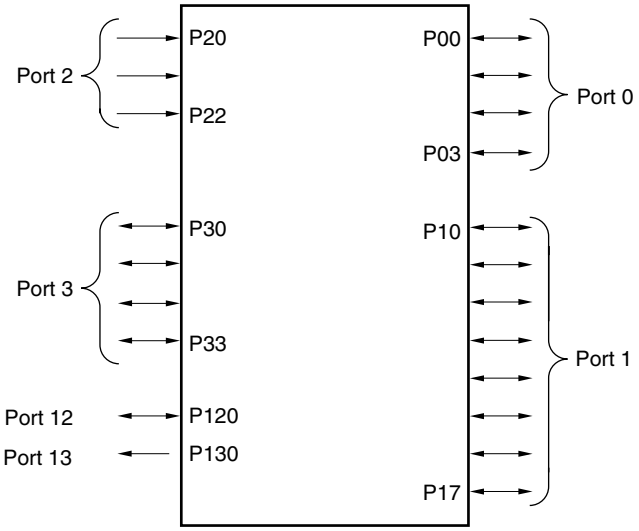


Table 3-1. Port Functions

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	TI000
P01				TI010/TO00
P02				–
P03				
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	$\overline{\text{SCK10}}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P22	Input	Port 2. 3-bit input-only port.	Input	ANI0 to ANI2
P30 to P33	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP1 to INTP4
P120	I/O	Port 12. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP0
P130	Output	Port 13. 1-bit output-only port.	Output	–

Caution When Port 2 is used as an input port, bit 3 (P23) is undefined.

3.1.1 Detailed function descriptions

For descriptions of the following, refer to **78K0/KB1 User's Manual (U15836E)**.

- Port configuration
- Registers controlling port functions
- Operation of port functions

3.2 A/D Converter

The A/D converter is a 10-bit resolution converter that converts analog input into digital values, and is configured to enable control of up to three analog input channels (ANI0 to ANI2).

The A/D converter has the following functions.

(1) 10-bit resolution A/D conversion

Selects a channel for analog input from among ANI0 to ANI2 and performs 10-bit resolution A/D conversion on a repeated basis. Each time one A/D conversion is performed, an interrupt request (INTAD) is output.

(2) Power file detection function

This function is used to detect low battery voltage. It compares the A/D conversion result (ADCR register value) and the power fail comparison threshold register (PFT), and outputs INTAD if the comparison conditions are met.

(3) Differences with 78K0/KB1 products

The differences between the μPD788001A, 788002A, and 78F8002A and the 78K0/KB1 with regard to A/D converter functions are as follows.

<table>
<tr><th>Item</th><th>μPD788001A, 788002A, 78F8002A</th><th>78K0/KB1</th></tr>
<tr><td>Number of A/D channels</td><td>P20 to P22 (3)</td><td>P20 to P23 (4)</td></tr>
<tr><td>Specification of analog input channel specification register (ADS)</td><td>
<table>
<tr><th>ADS2</th><th>ADS1</th><th>ADS0</th><th>Specification of analog input channel</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ANI0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ANI1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ANI2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table>
</td><td>
<table>
<tr><th>ADS2</th><th>ADS1</th><th>ADS0</th><th>Specification of analog input channel</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ANI0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ANI1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ANI2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ANI3</td></tr>
</table>
</td></tr>
</table>

3.2.1 Detailed function descriptions

For descriptions of the following, refer to **78K0/KB1 User's Manual (U15836E)**.

- Function of A/D Converter
- A/D Converter Configuration
- Registers Controlling A/D Converter
- A/D Converter Operations
- Basic operations of A/D converter
- Input voltage and conversion results
- A/D converter operation mode
- How to Read A/D Converter Characteristics Table
- Cautions for A/D Converter

3.3 Description of Functions Other than Port Functions and A/D Converter

For descriptions of the following, refer to **78K0/KB1 User's Manual (U15836E)**.

- CPU architecture
- Clock generator
- 16-bit timer/event counter 00
- 8-bit timer/event counter 50
- 8-bit timers H0 and H1
- Watchdog timer
- Serial interface UART0
- Serial interface UART6
- Serial interface CSI10
- Interrupt functions
- Standby function
- Reset function
- Clock monitor
- Power-on-clear circuit
- Low-voltage detector
- Mask options
- Instruction set

Remark Regarding the above-listed functions, only the product names differ from those in the **78K0/KB1 User's Manual (U15836E)**.

78K0/KB1 Product Names	Product Names Corresponding to 78K0/KB1 Product Names
μPD780101	–
μPD780102	μPD788001A
μPD780103	μPD788002A
μPD78F0103	μPD78F8002A

CHAPTER 4 POWER SUPPLY CIRCUIT

4.1 Power Supply Function

The power supply circuit is a stabilization power supply circuit that generates a 5 V (TYP.) voltage from 12 V battery supply voltage (6 to 18 V) via an external PNP transistor. Connect the collector pin voltage (V_{CCout}) of the external PNP transistor to the VCM pin and V_{DD} pin.

An overcurrent protection circuit for protecting the external PNP transistor is provided on chip.

4.2 Power Supply Overcurrent Protection

This circuit protects the external transistor by limiting the current if an overcurrent occurs in the power supply line due to a cause such as a load short.

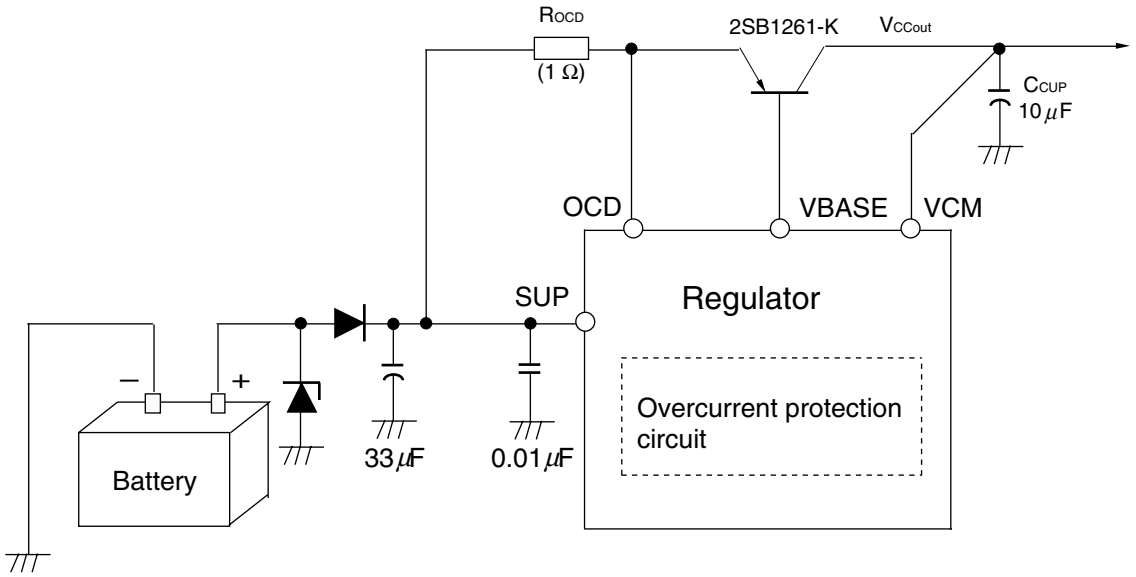
Overcurrent is detected using the difference in potential between the edges of the resistors connected between the SUP pin and OCD pin. The external resistance can be adjusted according to the user system.

When this function is not used, directly connect the OCD pin to the SUP pin.

Current limit = Overcurrent detect voltage (V_{SUPlim}) / R_{OCD}

Overcurrent detect voltage (V_{SUPlim}) = $V_{SUP} - V_{OCD}$ = 150 mV (Min.)

4.3 Power Supply Block Configuration Example



Remarks 1. Place the external transistor for the power supply adjacent to the VBASE, VCM, and SUP pins and use the shortest possible wiring for the base, collector, and emitter.

2. Place the ceramic capacitor between the SUP and GND pins adjacent to the SUP pin and use the shortest possible wiring.

CHAPTER 5 LIN TRANSCEIVER FUNCTION

5.1 LIN Transceiver Function

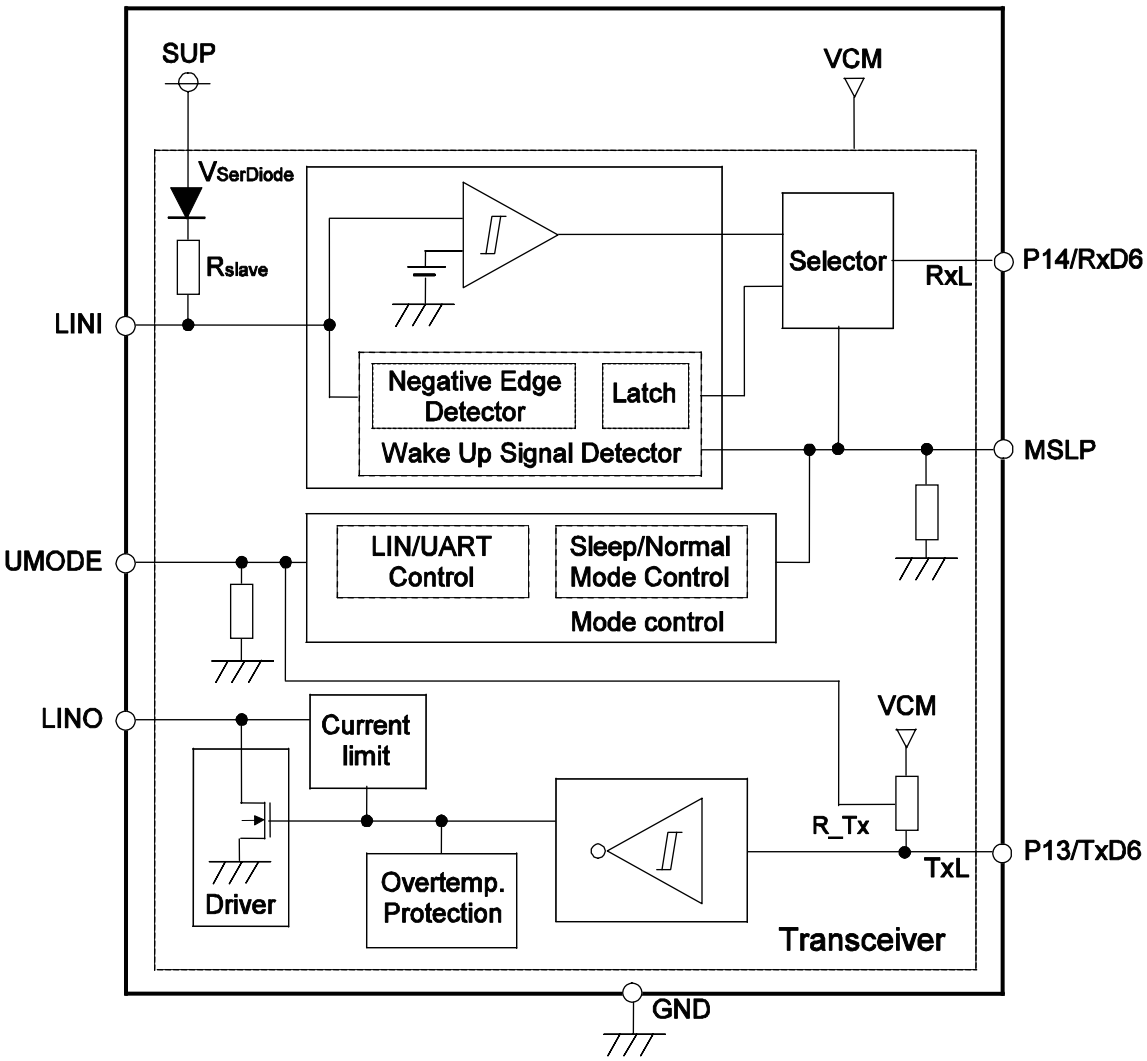
The LIN transceiver complies with LIN Specification Rev. 2.0.
An overcurrent limiter and a thermal shutdown circuit are provided on chip as the protection functions.
The LIN transceiver has the following two types of modes.

- Sleep mode
- Normal mode

5.2 LIN Transceiver Configuration

The LIN transceiver consists of the following hardware.

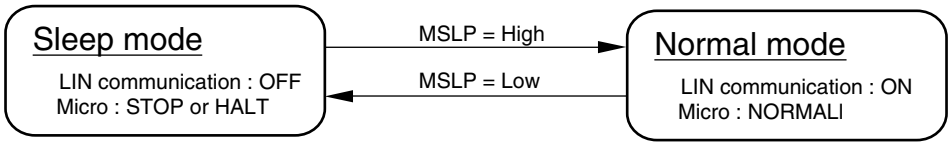
Figure 5-1. LIN Transceiver Block Diagram



5.3 Operation Mode (UMODE = Low)

The LIN transceiver has the following two modes.

Figure 5-2. Mode Transition Diagram



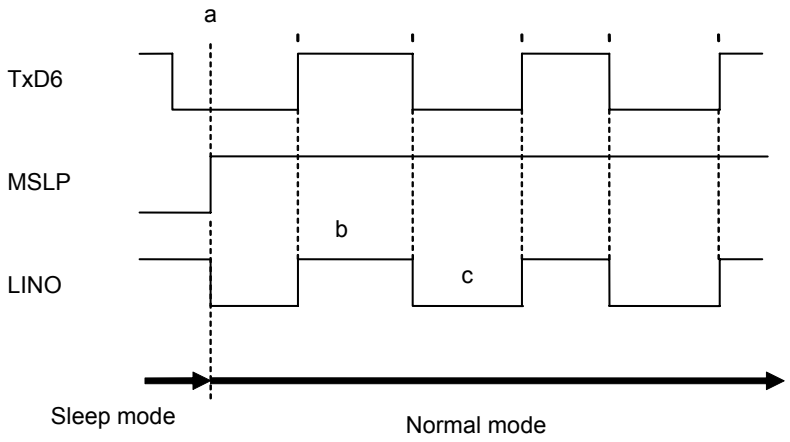
- Sleep mode
  When MSLP becomes Low, the sleep mode is entered.
  In the sleep mode, the LIN driver output becomes OFF (recessive) regardless of the Tx pin input state.
  To reduce the current consumption, set the microcontroller's operation mode either to the HALT or the STOP mode.

- Normal mode
  When MSLP becomes high, the normal mode is entered. In the normal mode, the Tx input data can be output to the LIN bus.

Cautions 1. When using the LIN transceiver function, leave the UMODE pin open.
(The UMODE pin is pulled down within the IC.)
2. When not using the LIN transceiver function, directly connect the UMODE pin to V_{DD} and set it to high level. When the UMODE pin is set to high level, the pull-up resistor of the LIN transceiver circuit (R_Tx) becomes unconnected.
3. The MSLP pin is pulled down within the IC.

Figure 5-3. Normal Mode Timing

(a) Normal mode transmitter operation (TxD6 to LINO)

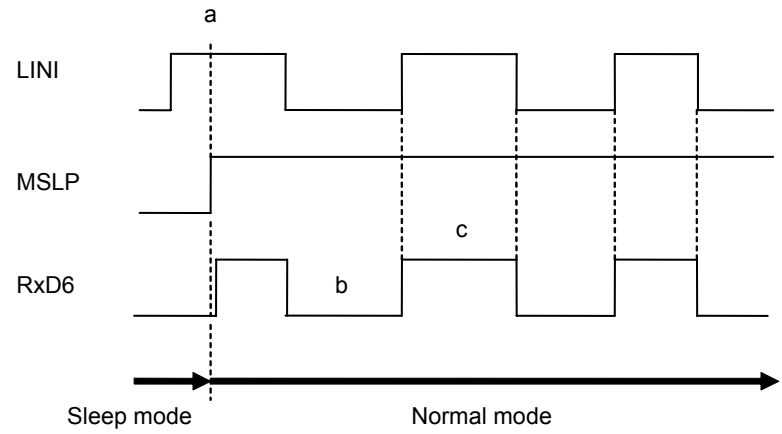


a: Normal mode request

b: Normal mode
LIN driver is OFF when TxD6 is high level.
(LIN bus: Recessive)

c: Normal mode
LIN driver is ON when TxD6 is low level.
(LIN bus: Dominant)

(b) Normal mode receiver operation (LINI to RxD6)



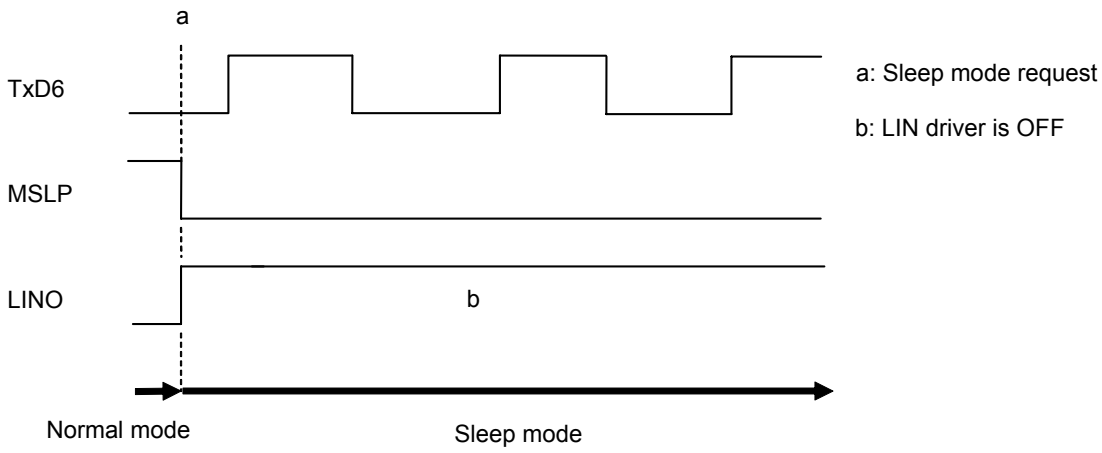
a: Normal mode request

b: Normal mode
RxD6 output low level when LIN bus is dominant.

c: Normal mode
RxD6 output high level when LIN bus is recessive

Figure 5-4. Sleep Mode Timing

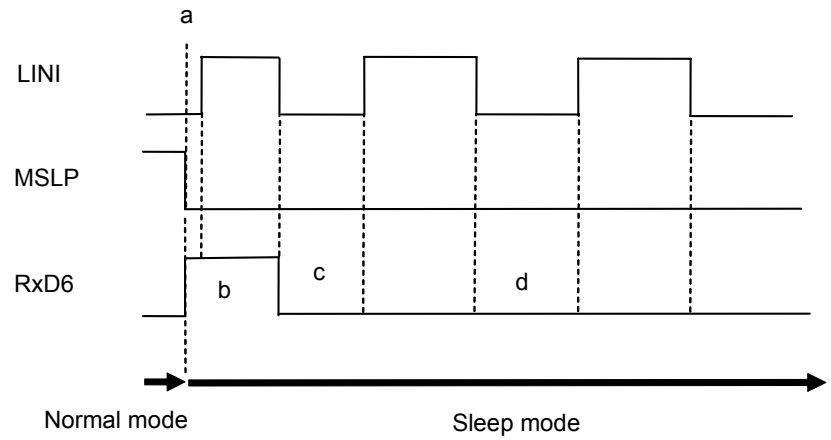
(a) Sleep mode transmitter operation (TxD6 to LINO)



a: Sleep mode request

b: LIN driver is OFF

(b) Sleep mode transmitter operation (LINI to RxD6)



a: Sleep mode request

b: Sleep mode
RxD6 output high level.

c: Sleep mode
RxD6 output low level when LINI detect negative edge.

d: Sleep mode
RxD6 hold low level until receive normal mode request from Micro.

5.4 Protection Function

5.4.1 Overcurrent limiter

The overcurrent limiter prevents destruction caused by overcurrent during a load short.

If a current that exceeds the overcurrent detection value flows to the LIN driver due to a load short, etc., the output current is limited by inhibiting the gate voltage of the LIN driver.

5.4.2 Thermal shutdown circuit

This is a protection circuit for preventing destruction due to overtemperature.

The temperature of the LIN driver is monitored and when a temperature that exceeds the overheating detection temperature is detected, the LIN driver is forcibly switched off.

After the LIN driver is forcibly switched off, it automatically switches back on after the temperature declines.

5.4.3 Protection circuit operation

Table 5-1 shows the operating status of the protection circuits in the various modes of the LIN transceiver.

Table 5-1. Protection Circuit Operation Status Transitions

Trigger		Power Supply Protection (UMODE = High/Low)	LIN driver protection (UMODE = Low)	
		Overcurrent status $V_{SUP} - V_{OCD} > 150$ mV (Min.)	Overcurrent status Ibus_lim > 40 mA (Min.)	Overtemperature status LINth > 150°C (Min.)
Status	Sleep mode	Power supply current limit: 0.15 V/R_{OCD} [A]	–	–
	Normal mode	Power supply current limit: 0.15 V/R_{OCD} [A]	LIN driver current limit: 40 mA (Min.)	LIN driver OFF

CHAPTER 6 FLASH MEMORY

The μPD78F8002A is provided as the flash memory version.

The μPD78F8002A replaces the internal mask ROM of the μPD788002A with flash memory to which a program can be written, erased, and overwritten while mounted on the board. Table 6-1 lists the differences between the μPD78F8002A and the mask ROM versions.

Table 6-1. Differences between μPD78F8002A and Mask ROM

Item	μPD78F8002A	Mask ROM Versions
Internal ROM configuration	Flash memory	Mask ROM
Internal ROM capacity	24 KB[Note]	μPD788001A : 16 KB μPD788002A : 24 KB
Internal high-speed RAM capacity	768 bytes[Note]	768 bytes
IC pin	None	Available
V_{PP} pin	Available	None
Electrical specifications	Refer to **CHAPTER 7 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS**	

Note The same capacity as the mask ROM versions can be specified by means of the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM versions.

6.1 Internal Memory Size Switching Register

The μPD78F8002A allows users to select the internal memory capacity using the internal memory size switching register (IMS) so that the same memory map as that of the mask ROM versions with a different internal memory capacity can be achieved.

IMS is set by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Caution The initial value of IMS is "setting prohibited (CFH)". Be sure to set the value of the relevant mask ROM version at initialization.

Figure 6-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
0	1	0	512 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	1	0	8 KB
0	1	0	0	16 KB
0	1	1	0	24 KB
Other than above				Setting prohibited

The IMS settings required to obtain the same memory map as mask ROM versions are shown in Table 6-2.

Table 6-2. Internal Memory Size Switching Register Settings

Target Mask ROM Versions	IMS Setting
μPD788001A	04H
μPD788002A	06H

Caution When using a mask ROM version, be sure to set IMS to the value indicated in Table 6-2.

6.2 Writing with Flash Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the μPD78F8002A has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the μPD78F8002A is mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Table 6-3. Wiring between μPD78F8002A and Dedicated Flash Programmer (1/2)

(1) 3-wire serial I/O (CSI10)

Pin Configuration of Dedicated Flash Programmer			With CSI10		With CSI10+HS	
Signal Name	I/O	Pin Function	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SO10/P12	26	SO10/P12	26
SO/TxD	Output	Transmit signal	SI10/RxD0/P11	25	SI10/RxD0/P11	25
SCK	Output	Transfer clock	$\overline{\text{SCK10}}$/TxD0/P10	15	$\overline{\text{SCK10}}$/TxD0/P10	15
CLK	Output	Clock to μPD78F8002A	X1	8	X1	8
			X2[Note]	9	X2[Note]	9
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	10	$\overline{\text{RESET}}$	10
V_{PP}	Output	Write voltage	V_{PP}	5	V_{PP}	5
H/S	Input	Handshake signal	Not needed	Not needed	HS/P15/TOH0	29
V_{DD}	I/O	V_{DD} voltage generation/voltage monitor	V_{DD}	7	V_{DD}	7
			AV_{REF}	36	AV_{REF}	36
GND	–	Ground	V_{SS}	6	V_{SS}	6
			AV_{SS}	37	AV_{SS}	37

Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Table 6-3. Wiring between μPD78F8002A and Dedicated Flash Programmer (2/2)

(2) UART (UART0, UART6)

Pin Configuration of Dedicated Flash Programmer			With UART0		With UART0+HS		With UART6	
Signal Name	I/O	Pin Function	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	$\overline{\text{TxD0}}$/$\overline{\text{SCK10}}$/P10	15	$\overline{\text{TxD0}}$/$\overline{\text{SCK10}}$/P10	15	TxD6/P13	27
SO/TxD	Output	Transmit signal	RxD0/SI10/P11	25	RxD0/SI10/P11	25	RxD6/P14	28
SCK	Output	Transfer clock	Not needed	Not needed	Not needed	Not needed	Not needed	Not needed
CLK	Output	Clock to μPD78F002A	X1	8	X1	8	X1	8
			X2[Note]	9	X2[Note]	9	X2[Note]	9
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	10	$\overline{\text{RESET}}$	10	$\overline{\text{RESET}}$	10
V_{PP}	Output	Write voltage	V_{PP}	5	V_{PP}	5	V_{PP}	5
H/S	Input	Handshake signal	Not needed	Not needed	HS/P15/TOH0	29	Not needed	Not needed
V_{DD}	I/O	V_{DD} voltage generation/voltage monitor	V_{DD}	7	V_{DD}	7	V_{DD}	7
			AV_{REF}	36	AV_{REF}	36	AV_{REF}	36
GND	–	Ground	V_{SS}	6	V_{SS}	6	V_{SS}	6
			AV_{SS}	37	AV_{SS}	37	AV_{SS}	37

Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Examples of the recommended connection when using the adapter for flash memory writing are shown below.

Figure 6-2. Example of Wiring Adapter for Flash Memory Writing in 3-Wire Serial I/O (CSI10) Mode

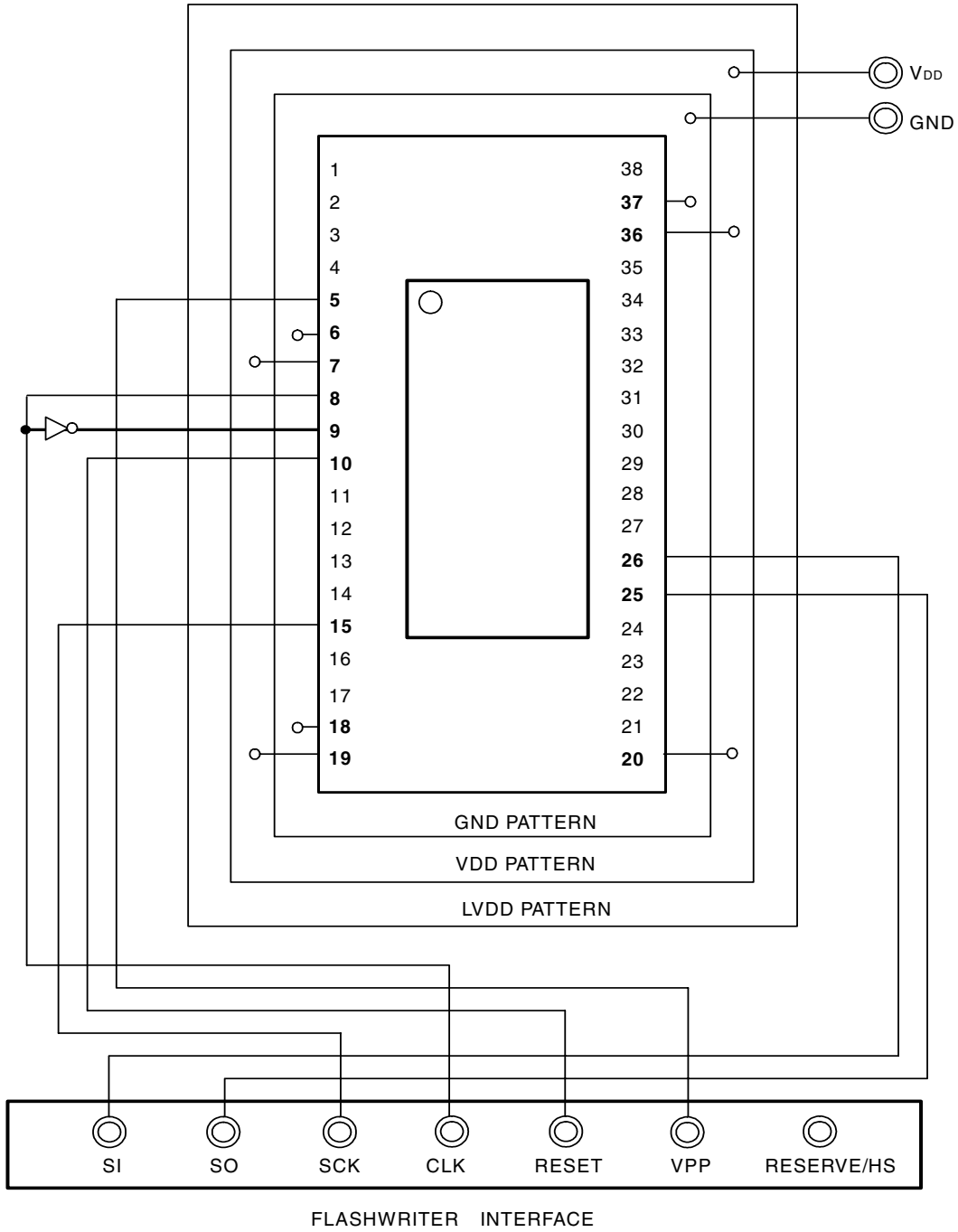


Figure 6-3. Example of Wiring Adapter for Flash Memory Writing in 3-Wire Serial I/O (CSI10 + HS) Mode

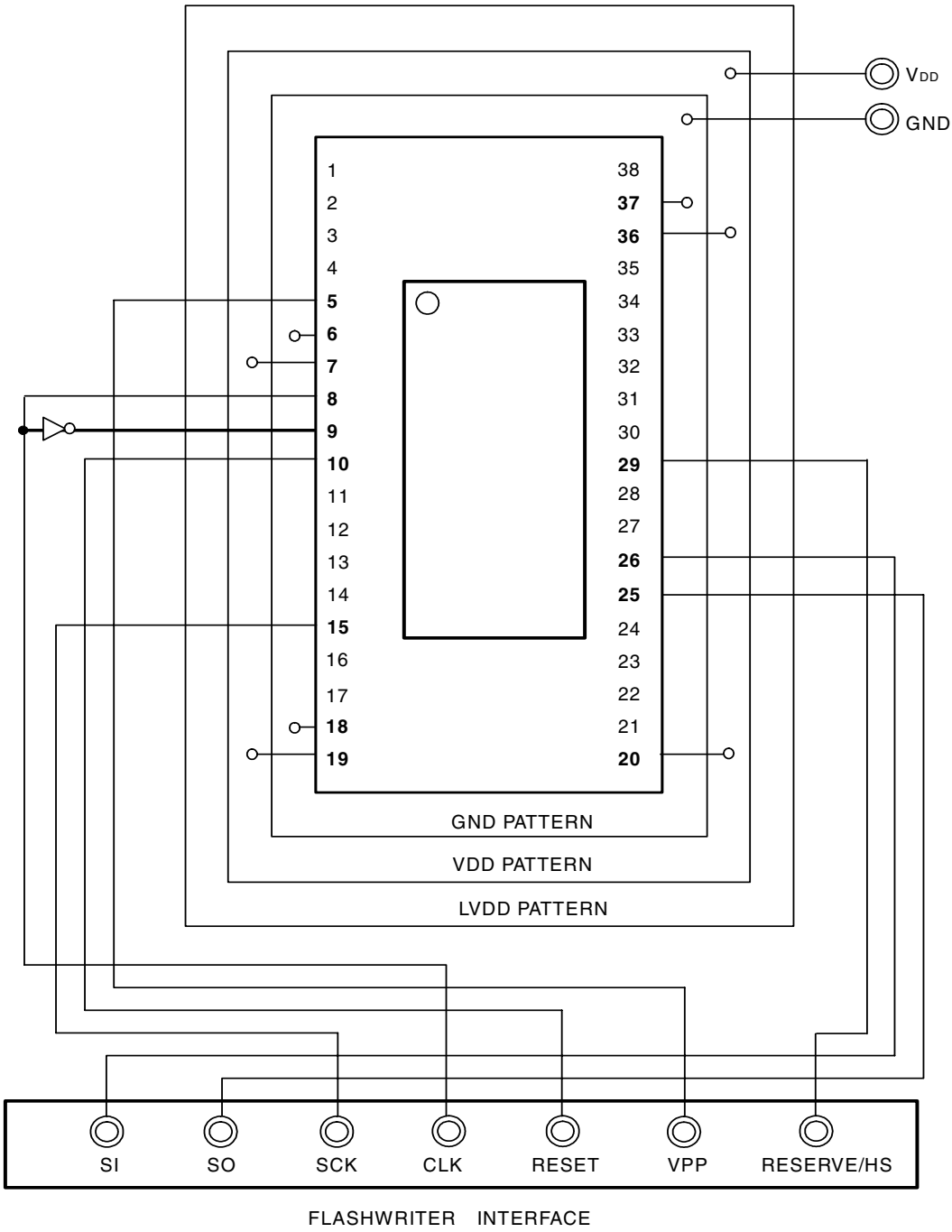


Figure 6-4. Example of Wiring Adapter for Flash Memory Writing in UART (UART0) Mode

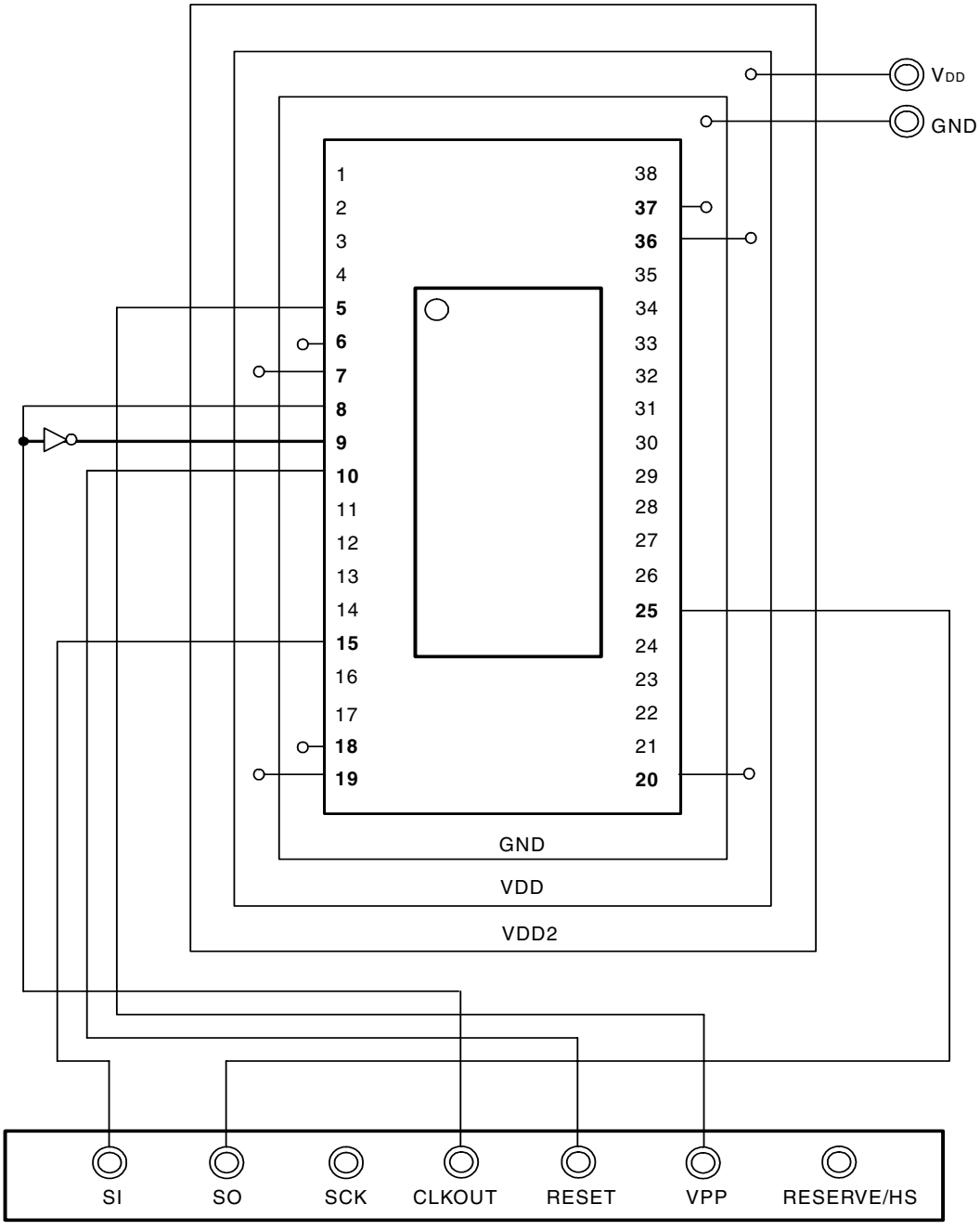


Figure 6-5. Example of Wiring Adapter for Flash Memory Writing in UART (UART0 + HS) Mode

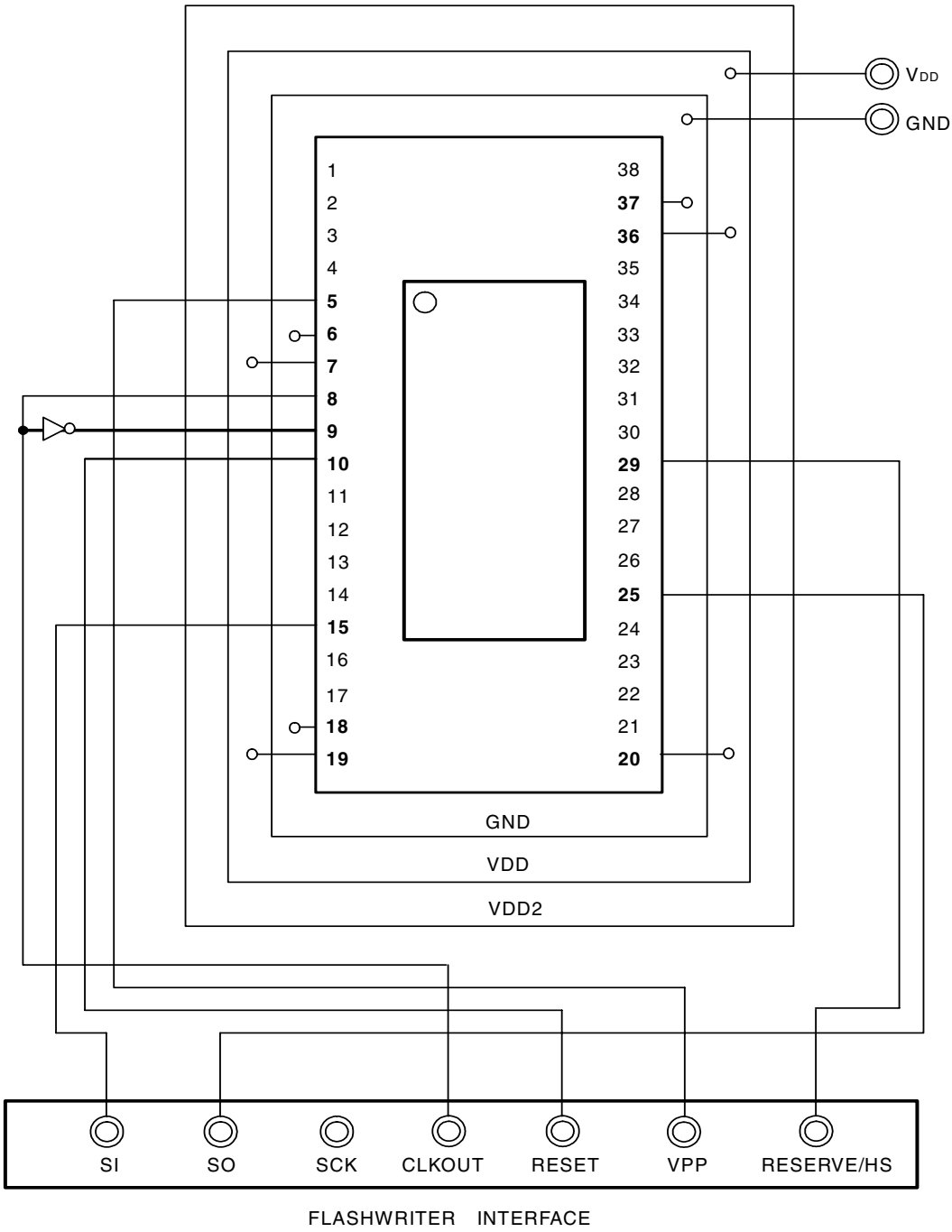
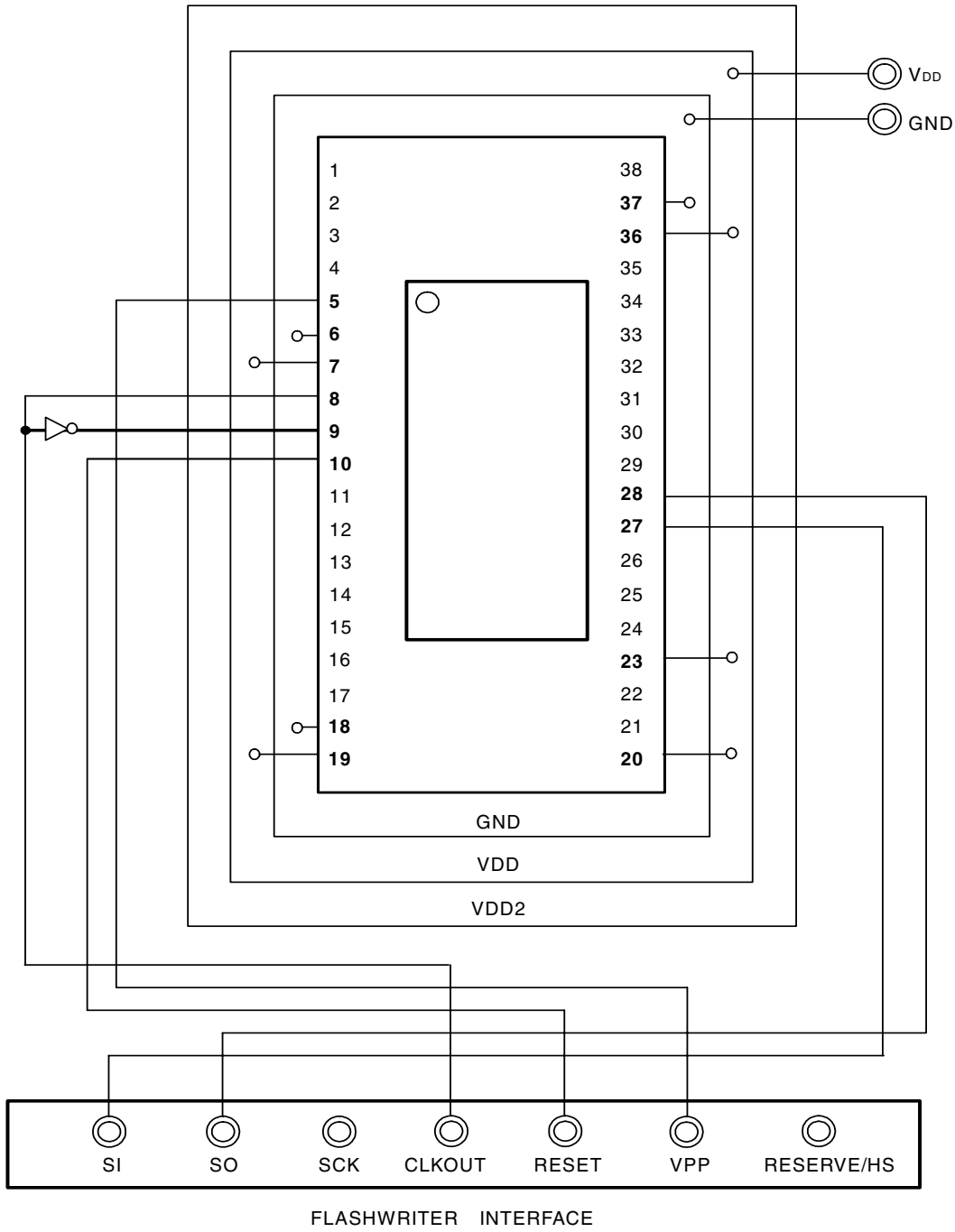


Figure 6-6. Example of Wiring Adapter for Flash Memory Writing in UART (UART6) Mode



For descriptions of the following, refer to **78K0/KB1 User's Manual (U15836E)**.

- Programming Environment
- Communication Mode
- Handling of Pins on Board
- Programming Method

CHAPTER 7 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS

7.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{SUP1}	SUP, 400 ms		–0.3 to +40	V
	V_{SUP2}	SUP, 2 min		–0.3 to +28	V
	V_{SUP3}	SUP		–0.3 to +20	V
	V_{CM}	V_{CM}		–0.3 to +6.5	V
	V_{DD}	V_{DD}		–0.3 to +6.5 Note 1	V
	AV_{REF}	AV_{REF}		–0.3 to V_{DD} + 0.3 Note 2	V
Voltage between ground pins	GND	|GND – V_{SS}|, |GND – AV_{SS}|, | V_{SS} – AV_{SS}|		0 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P22, P30 to P33, P120, X1, X2, $\overline{\text{RESET}}$, MSLP, UMODE		–0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	V_{PP} in flash programming mode (μPD78F8002A only) Note 3		–0.3 to +10.5	V
	V_{I3}	OCD, 400 ms		–0.3 to +40	V
	V_{I4}	OCD, 2 min		–0.3 to +28	V
	V_{I5}	OCD		–0.3 to +20	V
	$V_{IHlini1}$	LINI, 400 ms		–0.3 to +40	V
	$V_{IHlini2}$	LINI, 2 min		–0.3 to +28	V
	$V_{IHlini3}$	LINI		–0.3 to +20	V
	V_{ILlini}	LINI, 7 V ≤ V_{SUP} ≤ 18 V, 1 s		V_{SUP} – 40 Note 4	V
Output voltage	V_{o1}	P00 to P03, P10 to P17, P30 to P33, P120, P130		–0.3 to V_{DD} + 0.3 Note 2	V
	V_{olin1}	LINO, 400 ms		–0.3 to +40	V
	V_{olin2}	LINO, 2 min		–0.3 to +28	V
	V_{olin3}	LINO		–0.3 to +20	V
A/D input voltage	V_{AN}	P20 to P22		AV_{SS} – 0.3 to AV_{REF} + 0.3 Note 2 and –0.3 to V_{DD} + 0.3 Note 2	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total of all pins	P00 to P03, P10 to P17, P130	–30	mA
			P30 to P33, P120	–30	mA
Output current, low	I_{OL1}	Per pin		+20	mA
		Total of all pins	P00 to P03, P10 to P17, P130	+35	mA
			P30 to P33, P120	+35	mA
	I_{OL2}	LINO		+200	mA
VBASE current	I_{BASE}	VBASE		–10 to +10	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode		–10 to +85	°C
Storage temperature	T_{stg}	μPD788001A, μPD788002A		–65 to +150	°C
		μPD78F8002A		–40 to +125	°C

Notes 1. However, $|V_{CM} - V_{DD}| < 0.3$ V is required.

2. Must be 6.5 V or lower.

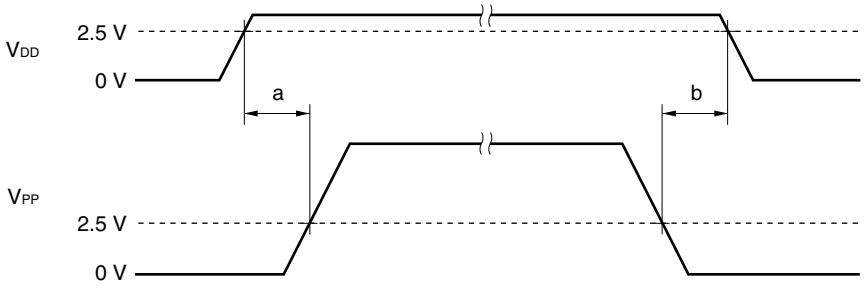
3. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash Memory is written.

- **When supply voltage rises.**

  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (2.5 V) of the operating voltage range (see a in the below).

- **When supply voltage drops.**

  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (2.5 V) of the operating voltage range of V_{DD} (see b in the figure below).



4. An external diode is required for negative charge protection between the LINI and LINO pins.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

7.2 Power Supply Block Characteristics

DC characteristics (T_A = –40 to +85°C, 6 V ≤ V_{SUP} ≤ 18 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{bat1}	$I_{bat1} = I_{SUP} + I_{CM} + I_{DD}$, LIN: Sleep Mode, Micro: STOP mode, (Internal oscillator = ON)			100	μA
	I_{bat2}	$I_{bat2} = I_{SUP} + I_{CM} + I_{DD}$ LIN: Sleep Mode Micro: STOP mode, (Internal oscillator = OFF)			80	μA
<R>	I_{bat3}	T_A = +25°C, V_{SUP} = 14 V $I_{bat3} = I_{SUP} + I_{CM} + I_{DD}$ LIN: Sleep Mode Micro: STOP mode, (Internal oscillator = OFF)			(50)	μA
	I_{bat4}	$I_{bat4} = I_{SUP} + I_{CM} + I_{DD}$[Note 2] LIN: Normal Mode (Driver: OFF) Micro: Crystal/ ceramic oscillation operating mode, A/D operation, fxp = 10 MHz Flash ROM			29	mA
	I_{bat5}	$I_{bat5} = I_{SUP} + I_{CM} + I_{DD}$[Note 2] LIN: Normal Mode (Driver: OFF) Micro: Crystal/ ceramic oscillation operating mode, A/D operation, fxp = 10 MHz Mask ROM			18	mA
	I_{bat6}	$I_{bat6} = I_{SUP} + I_{CM}$ LIN: Sleep Mode			50	μA
	I_{bat7}	$I_{bat7} = I_{SUP} + I_{CM}$ LIN: Normal Mode (Driver: OFF)			5	mA
REG output voltage[Note 3]	V_{CCout}	$V_{CCout} = V_{CM}$, I_{CM} = 100 mA	4.9	5	5.1	V
Power supply overcurrent detect voltage[Note 3]	V_{SUPlim}		150		300	mV
Load regulation[Note 3]	REGL	V_{SUP} = 14 V, 10 mA ≤ I_{CM} ≤ 150 mA	–50		+50	mV
<R> Input regulation[Note 3]	REGIN1	I_C = 100 mA, T_A ≤ 25°C	–70		+70	mV
	REGIN2	I_C = 100 mA, T_A ≤ 85°C	–80		+80	mV
VBASE output current[Note 4]	I_{BASE}	$V_{BASE} = V_{SUP} - 0.6$ V, V_{SUP} = 7 V	(480)			μA

Notes 1. This is the total current flowing to the V_{SUP}, V_{CM}, V_{DD} internal power supply. The peripheral operating current is included. (However, the current flowing to the port pull-up resistor is not included.)

2. I_{DD} includes the peripheral operating current.
When set to PCC = 00H.
Including the current that flows through the AV_{REF} pin.
When crystal/ceramic oscillation is selected as the high-speed system clock using the option byte.

3. 2SB1261-K is used for the external transistors [h_{FE} (Max.) = 400] .

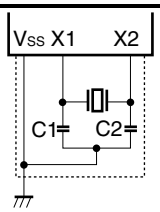
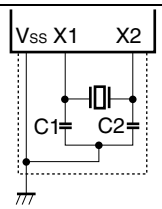
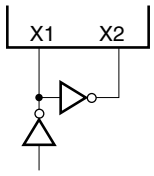
4. VBASE output current is current capability on VBASE pin. VBASE pin can apply the current more than minimum value on the BASE pin of external transistor.

Remark The values in parentheses are design guaranteed values for which no shipping test has been performed.

7.3 Microcontroller Block Characteristics

High-Speed System Clock (Crystal/Ceramic) Oscillator Characteristics

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} =V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_{XP})[Note]	4.0 V ≤ V_{DD} ≤ 5.1 V	2.0		12	MHz
			3.5 V ≤ V_{DD} < 4.0 V	2.0		10	
			3.0 V ≤ V_{DD} < 3.5 V	2.0		8.38	
			2.5 V ≤ V_{DD} < 3.0 V	2.0		5.0	
Crystal resonator		Oscillation frequency (f_{XP})[Note]	4.0 V ≤ V_{DD} ≤ 5.1 V	2.0		12	MHz
			3.5 V ≤ V_{DD} < 4.0 V	2.0		10	
			3.0 V ≤ V_{DD} < 3.5 V	2.0		8.38	
			2.5 V ≤ V_{DD} < 3.0 V	2.0		5.0	
External clock		X1 input frequency (f_{XP})[Note]	4.0 V ≤ V_{DD} ≤ 5.1 V	2.0		12	MHz
			3.5 V ≤ V_{DD} < 4.0 V	2.0		10	
			3.0 V ≤ V_{DD} < 3.5 V	2.0		8.38	
			2.5 V ≤ V_{DD} < 3.0 V	2.0		5.0	
		X1 input high-/low-level width (t_{XPH}, t_{XPL})	4.0 V ≤ V_{DD} ≤ 5.1 V	38		250	ns
			3.5 V ≤ V_{DD} < 4.0 V	46		250	
			3.0 V ≤ V_{DD} < 3.5 V	56		250	
			2.5 V ≤ V_{DD} < 3.0 V	96		250	

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the Internal oscillator after reset is released, check the oscillation stabilization time of the crystal/ceramic oscillation clock using the oscillation stabilization time status register (OSTC). Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Internal Oscillator Characteristics

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} =V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
On-chip internal oscillator	Oscillation frequency (f_R)		120	240	480	kHz

DC Characteristics (1/4)

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	4.0 V ≤ V_{DD} ≤ 5.1 V			–5	mA
		Total of P30 to P33, P120	4.0 V ≤ V_{DD} ≤ 5.1 V			–25	mA
		Total of P00 to P03, P10 to P17, P130	4.0 V ≤ V_{DD} ≤ 5.1 V			–25	mA
<R>		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.1 V			–40	mA
			2.5 V ≤ V_{DD} < 4.0 V			–10	mA
Output current, low	I_{OL}	Per pin	4.0 V ≤ V_{DD} ≤ 5.1 V			10	mA
		Total of P30 to P33, P120	4.0 V ≤ V_{DD} ≤ 5.1 V			30	mA
		Total of P00 to P03, P10 to P17, P130	4.0 V ≤ V_{DD} ≤ 5.1 V			30	mA
<R>		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.1 V			50	mA
			2.5 V ≤ V_{DD} < 4.0 V			10	mA
Input voltage, high	V_{IH1}	P12, P13, P15	2.7 V ≤ V_{DD} ≤ 5.1 V	0.7 V_{DD}		V_{DD}	V
			2.5 V ≤ V_{DD} < 2.7 V	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P10, P11, P14, P16, P17, P30 to P33, P120, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.1 V	0.8 V_{DD}		V_{DD}	V
			2.5 V ≤ V_{DD} < 2.7 V	0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P22[Note]	2.7 V ≤ V_{DD} ≤ 5.1 V	0.7 AV_{REF}		AV_{REF}	V
			2.5 V ≤ V_{DD} < 2.7 V	0.8 AV_{REF}		AV_{REF}	V
	V_{IH4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.1 V	V_{DD} – 0.5		V_{DD}	V
			2.5 V ≤ V_{DD} < 2.7 V	V_{DD} – 0.2		V_{DD}	V
Input voltage, low	V_{IL1}	P12, P13, P15	2.7 V ≤ V_{DD} ≤ 5.1 V	0		0.3 V_{DD}	V
			2.5 V ≤ V_{DD} < 2.7 V	0		0.2 V_{DD}	V
	V_{IL2}	P00 to P03, P10, P11, P14, P16, P17, P30 to P33, P120, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.1 V	0		0.2 V_{DD}	V
			2.5 V ≤ V_{DD} < 2.7 V	0		0.15 V_{DD}	V
	V_{IL3}	P20 to P22[Note]	2.7 V ≤ V_{DD} ≤ 5.1 V	0		0.3 AV_{REF}	V
			2.5 V ≤ V_{DD} < 2.7 V	0		0.2 AV_{REF}	V
	V_{IL4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.1 V	0		0.4	V
			2.5 V ≤ V_{DD} < 2.7 V	0		0.2	V
Output voltage, high	V_{OH}	Total of P30 to P33, P120 pins I_{OH} = –25 mA	4.0 V ≤ V_{DD} ≤ 5.1 V, I_{OH} = –5 mA	V_{DD} – 1.0			V
		Total of P00 to P03, P10 to P17, P130 pins I_{OH} = –25 mA	4.0 V ≤ V_{DD} ≤ 5.1 V, I_{OH} = –5 mA	V_{DD} – 1.0			V
		I_{OH} = –100 μA	2.5 V ≤ V_{DD} < 4.0 V	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	Total of P30 to P33, P120 pins I_{OL} = 30 mA	4.0 V ≤ V_{DD} ≤ 5.1 V, I_{OL} = 10 mA			1.3	V
		Total of P00 to P03, P10 to P17, P130 pins I_{OL} = 30 mA	4.0 V ≤ V_{DD} ≤ 5.1 V, I_{OL} = 10 mA			1.3	V
		I_{OL} = 400 μA	2.5 V ≤ V_{DD} < 4.0 V			0.4	V

Note When used as a digital input port, set AV_{REF} = V_{DD}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/4)

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	P00 to P03, P10 to P17, P30 to P33, P120, $\overline{\text{RESET}}$			3	μA
		$V_I = AV_{REF}$	P20 to P23			3	μA
	I_{LIH2}	$V_I = V_{DD}$	X1, X2[Note]			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	P00 to P03, P10 to P17, P20 to P23, P30 to P33, P120, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2[Note]			–20	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Pull-up resistance value	R	V_I = 0 V		10	30	100	kΩ
V_{PP} supply voltage (μPD78F8002A only)	V_{PP1}	In normal operation mode		0		0.2 V_{DD}	V

Note When the inverse level of X1 is input to X2.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/4): μPD78F8002A

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

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Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	X1 crystal oscillation operating mode[Note 2]	f_{XP} = 12 MHz, V_{DD} = 5.0 V ±2%[Note 3]	When A/D converter is stopped		14	23.4	mA
				When A/D converter is operating[Note 4]		15	25.4	mA
			f_{XP} = 10 MHz, V_{DD} = 5.0 V ±2%[Note 3]	When A/D converter is stopped		11.6	19.5	mA
				When A/D converter is operating[Note 4]		12.6	21.5	mA
			f_{XP} = 5 MHz, V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		4	6.4	mA
				When A/D converter is operating[Note 4]		4.6	7.6	mA
	I_{DD2}	X1 crystal oscillation HALT mode	f_{XP} = 12 MHz, V_{DD} = 5.0 V ±2%	When peripheral functions are stopped		1.6	3.2	mA
				When peripheral functions are operating			6.4	mA
			f_{XP} = 10 MHz, V_{DD} = 5.0 V ±2%	When peripheral functions are stopped		1.4	2.8	mA
				When peripheral functions are operating			5.5	mA
			f_{XP} = 5 MHz, V_{DD} = 3.0 V ±10%	When peripheral functions are stopped		0.32	0.64	mA
				When peripheral functions are operating			1.9	mA
	I_{DD3}	Internal oscillation operating mode[Note 5]	V_{DD} = 5.0 V ±2%			0.37	1.51	mA
			V_{DD} = 3.0 V ±10%			0.29	1.16	mA
	I_{DD4}	Internal oscillation mode[Note 5]	V_{DD} = 5.0 V ±2%			0.19	0.76	mA
			V_{DD} = 3.0 V ±10%			0.16	0.64	mA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±2%	POC: ON, Internal oscillator: OFF		3.5	35.5	μA
				POC: ON, Internal oscillator: ON		17.5	63.5	μA
			V_{DD} = 3.0 V ±10%	POC: ON, Internal oscillator: OFF		3.5	15.5	μA
				POC: ON, Internal oscillator: ON		11	30.5	μA

Notes 1. Total current flowing through the internal power supply (V_{DD}). Peripheral operation current is included (however, the current that flows through the pull-up resistors of ports is not included).

2. I_{DD1} includes peripheral operation current.

3. When PCC = 00H.

4. Total current flowing through V_{DD} and AV_{REF} pins.

5. When X1 oscillator is stopped.

DC Characteristics (4/4): μPD788001A, 788002A

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

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Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	X1 crystal oscillation operating mode[Note 2]	f_{XP} = 12 MHz, V_{DD} = 5.0 V ±2%[Note 3]	When A/D converter is stopped		7.2	13.1	mA
				When A/D converter is operating[Note 4]		8.2	15.1	mA
			f_{XP} = 10 MHz, V_{DD} = 5.0 V ±2%[Note 3]	When A/D converter is stopped		6	10.9	mA
				When A/D converter is operating[Note 4]		7	12.9	mA
			f_{XP} = 5 MHz, V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		1.7	3.1	mA
				When A/D converter is operating[Note 4]		2.3	4.3	mA
	I_{DD2}	X1 crystal oscillation HALT mode	f_{XP} = 12 MHz, V_{DD} = 5.0 V ±2%	When peripheral functions are stopped		1.5	3.0	mA
				When peripheral functions are operating			5.5	mA
			f_{XP} = 10 MHz, V_{DD} = 5.0 V ±2%	When peripheral functions are stopped		1.3	2.6	mA
				When peripheral functions are operating			4.8	mA
			f_{XP} = 5 MHz, V_{DD} = 3.0 V ±10%	When peripheral functions are stopped		0.25	0.5	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	Internal oscillation operating mode[Note 5]	V_{DD} = 5.0 V ±2%			0.18	0.72	mA
			V_{DD} = 3.0 V ±10%			0.11	0.44	mA
	I_{DD4}	Internal oscillation HALT mode[Note 5]	V_{DD} = 5.0 V ±2%			0.05	0.20	mA
			V_{DD} = 3.0 V ±10%			0.03	0.12	mA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±2%	POC: ON[Note 6], Internal oscillator: OFF		3.5	35.5	μA
				POC: ON[Note 6], Internal oscillator: ON		17.5	63.5	μA
			V_{DD} = 3.0 V ±10%	POC: ON[Note 6], Internal oscillator: OFF		3.5	15.5	μA
				POC: ON[Note 6], Internal oscillator: ON		11	30.5	μA

Notes 1. Total current flowing through the internal power supply (V_{DD}). Peripheral operation current is included (however, the current that flows through the pull-up resistors of ports is not included).

2. I_{DD1} includes peripheral operation current.

3. When PCC = 00H.

4. Total current flowing through V_{DD} and AV_{REF} pins.

5. When X1 oscillator is stopped.

AC Characteristics

(1) Basic operation

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	X1 input clock	4.0 V ≤ V_{DD} ≤ 5.1 V	0.166		16	μs
			3.5 V ≤ V_{DD} < 4.0 V	0.2		16	μs
			3.0 V ≤ V_{DD} < 3.5 V	0.238		16	μs
			2.5 V ≤ V_{DD} < 3.0 V	0.4		16	μs
		Internal oscillation clock		4.17	8.33	33.3	μs
TI000, TI010 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.1 V		$2/f_{sam}$+ 0.1 Note			μs
		2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$+ 0.2 Note			μs
		2.5 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+ 0.5 Note			μs
TI50 input frequency	f_{TI5}	4.0 V ≤ V_{DD} ≤ 5.1 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.5 V ≤ V_{DD} < 2.7 V				2.5	MHz
TI50 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	4.0 V ≤ V_{DD} ≤ 5.1 V		50			ns
		2.7 V ≤ V_{DD} < 4.0 V		100			ns
		2.5 V ≤ V_{DD} < 2.7 V		200			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	2.7 V ≤ V_{DD} ≤ 5.1 V		1			μs
		2.5 V ≤ V_{DD} < 2.7 V		2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 5.1 V		10			μs
		2.5 V ≤ V_{DD} < 2.7 V		20			μs

Note Selection of f_{sam} = f_{XP}, f_{XP}/4, f_{XP}/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, f_{sam} = f_{XP}.

(2) Serial interface

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

(a) UART mode (UART6, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(b) UART mode (UART0, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(c) 3-wire serial I/O mode (master mode, $\overline{SCK10}$... internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.1 V	200			ns
		3.3 V ≤ V_{DD} < 4.0 V	240			ns
		2.7 V ≤ V_{DD} < 3.3 V	400			ns
		2.5 V ≤ V_{DD} < 2.7 V	800			ns
$\overline{SCK10}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.1 V	t_{KCY1}/2 – 10			ns
		2.5 V ≤ V_{DD} < 2.7 V	t_{KCY1}/2 – 50			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.1 V	30			ns
		2.5 V ≤ V_{DD} < 2.7 V	70			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.1 V	30			ns
		2.5 V ≤ V_{DD} < 2.7 V	70			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO1}	C = 100 pF[Note] 2.7 V ≤ V_{DD} ≤ 5.1V			30	ns
		C = 100 pF[Note] 2.5 V ≤ V_{DD} < 2.7 V			120	ns

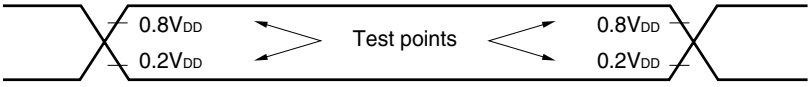
Note C is the load capacitance of the $\overline{SCK10}$ and SO10 output lines.

(d) 3-wire serial I/O mode (slave mode, $\overline{SCK10}$... external clock input)

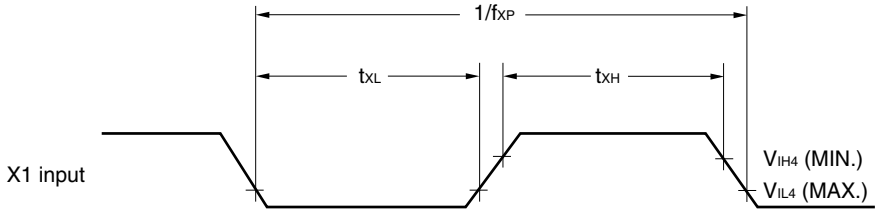
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.1 V	400			ns
		2.5 V ≤ V_{DD} < 2.7 V	800			ns
$\overline{SCK10}$ high-/low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK2}		80			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI2}		50			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO2}	C = 100 pF[Note]			120	ns

Note C is the load capacitance of the SO10 output line.

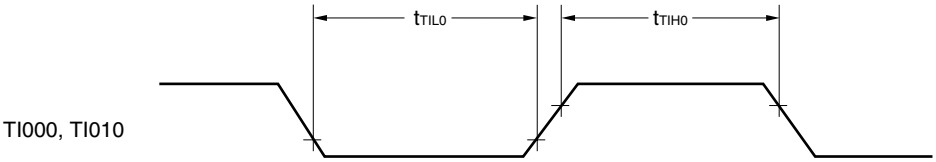
AC Timing Test Points (Excluding X1 Input)

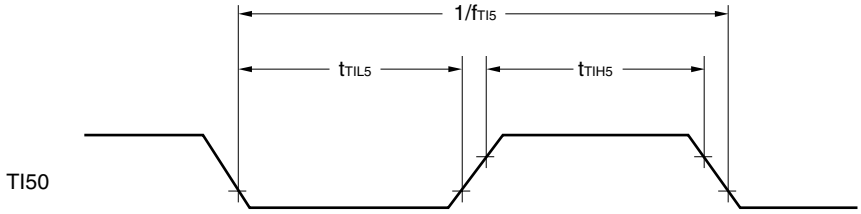


Clock Timing

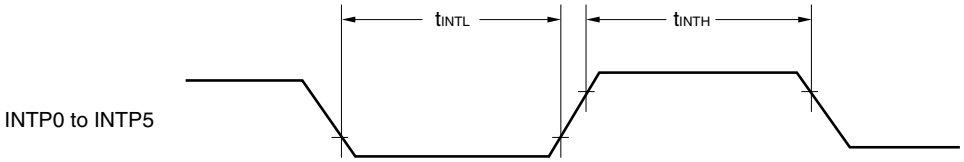


TI Timing

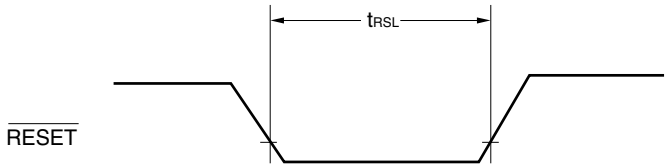




Interrupt Request Input Timing

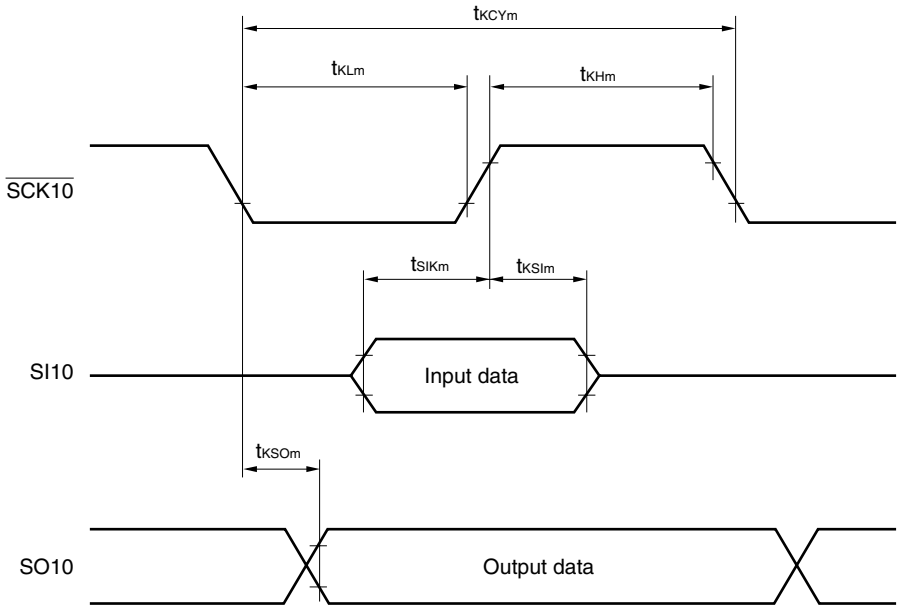


$\overline{\text{RESET}}$ Input Timing



Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1, 2

A/D Converter Characteristics

(T_A = –40 to +85°C, 2.5 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.5 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		10	10	10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.1 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		2.5 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.1 V	14		100	μs
		2.7 V ≤ AV_{REF} < 4.0 V	17		100	μs
		2.5 V ≤ AV_{REF} < 2.7 V	48		100	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.1 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.5 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.1 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.5 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral non-linearity error[Note 1]	I_{LE}	4.0 V ≤ AV_{REF} ≤ 5.1 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.5 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential non-linearity error[Note 1]	D_{LE}	4.0 V ≤ AV_{REF} ≤ 5.1 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		2.5 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input voltage	V_{AIN}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

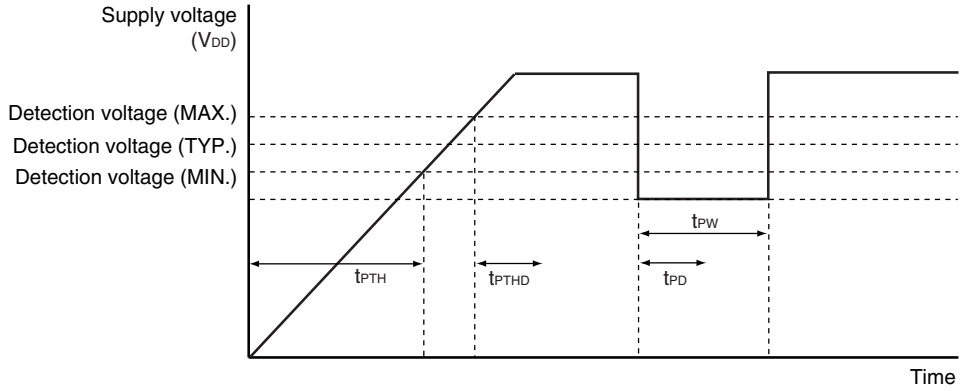
POC Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.3	3.5	3.7	V
Power supply rise time	t_{PTH}	V_{DD}: 0 V → 2.7 V	0.0015			ms
		V_{DD}: 0 V → 3.3 V	0.002			ms
Response delay time 1 Note 1	t_{PTHD}	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2 Note 2	t_{PD}	When V_{DD} falls			1.0	ms
Minimum pulse width	t_{PW}		0.2			ms

Notes 1. Time required from voltage detection to reset release.

2. Time required from voltage detection to internal reset output.

POC Circuit Timing



LVI Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.1	4.3	4.5	V
	V_{LVI1}		3.9	4.1	4.3	V
	V_{LVI2}		3.7	3.9	4.1	V
	V_{LVI3}		3.5	3.7	3.9	V
	V_{LVI4}		3.3	3.5	3.7	V
	V_{LVI5}		3.15	3.3	3.45	V
	V_{LVI6}		2.95	3.1	3.25	V
	V_{LVI7}		2.7	2.85	3.0	V
Response time[Note 1]	t_{LD}			0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Reference voltage stabilization wait time	t_{LWAIT0}			0.5	2.0	ms
Operation stabilization wait time[Note 2]	t_{LWAIT1}			0.1	0.2	ms

Notes 1. Time required from voltage detection to interrupt output or internal reset output.

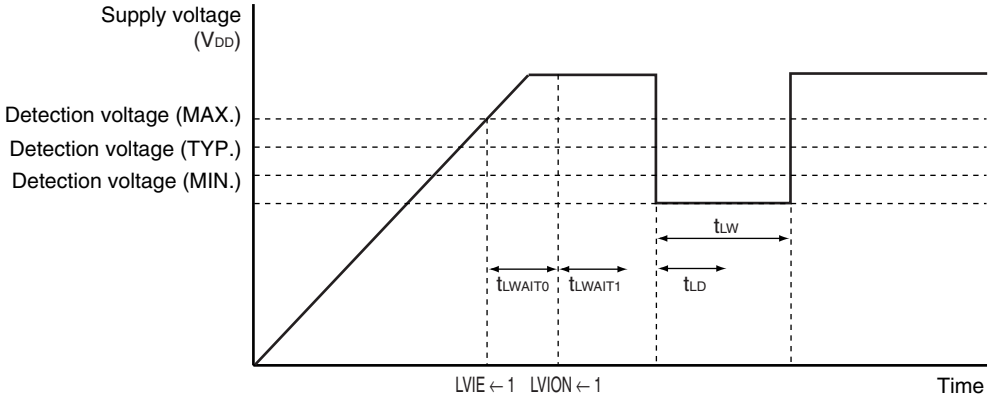
2. Time required from setting LVION to 1 to operation stabilization.

Caution Do not set V_{LVI3} to V_{LVI7}. Since the POC detection voltage is set to 3.5 V ± 0.2 V, low voltage is not detected even if V_{LVI3} to V_{LVI7} are set.

Remarks 1. $V_{LVI0} > V_{LVI1} > V_{LVI2} > V_{LVI3} > V_{LVI4} > V_{LVI5} > V_{LVI6} > V_{LVI7}$

2. $V_{POC} < V_{LVIm}$ (m = 0 to 7)

LVI Circuit Timing



Flash Memory Programming Characteristics: μPD78F8002A

(T_A = +10 to +60°C, 2.7 V ≤ V_{CM} = V_{DD} ≤ 5.1 V, 2.7 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

(1) Write erase characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} supply voltage	V_{PP2}	During flash memory programming	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When V_{PP} = V_{PP2}, f_{XP} = 10 MHz, V_{DD} = 5.1 V			37	mA
V_{PP} supply current	I_{PP}	V_{PP} = V_{PP2}			100	mA
Step erase time[Note 1]	T_{er}		0.199	0.2	0.201	s
Overall erase time[Note 2]	T_{era}	When step erase time = 0.2 s			20	s/chip
Writeback time[Note 3]	T_{wb}		49.4	50	50.6	ms
Number of writebacks per 1 writeback command[Note 4]	C_{wb}	When writeback time = 50 ms			60	Times
Number of erases/writebacks	C_{erwb}				16	Times
Step write time[Note 5]	T_{wr}		48	50	52	μs
Overall write time per word[Note 6]	T_{wrw}	When step write time = 50 μs (1 word = 1 byte)	48		520	μs
Number of rewrites per chip[Note 7]	C_{erwr}	1 erase + 1 write after erase = 1 rewrite			20	Times/ area

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. The recommended setting value of the writeback time is 50 ms.

4. Writeback is executed once by the issuance of the writeback command. Therefore, the number of retries must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step write time is 50 μs.

6. The actual write time per word is 100 μs longer. The internal verify time during or after a write is not included.

7. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P → E → P: 3 rewrites

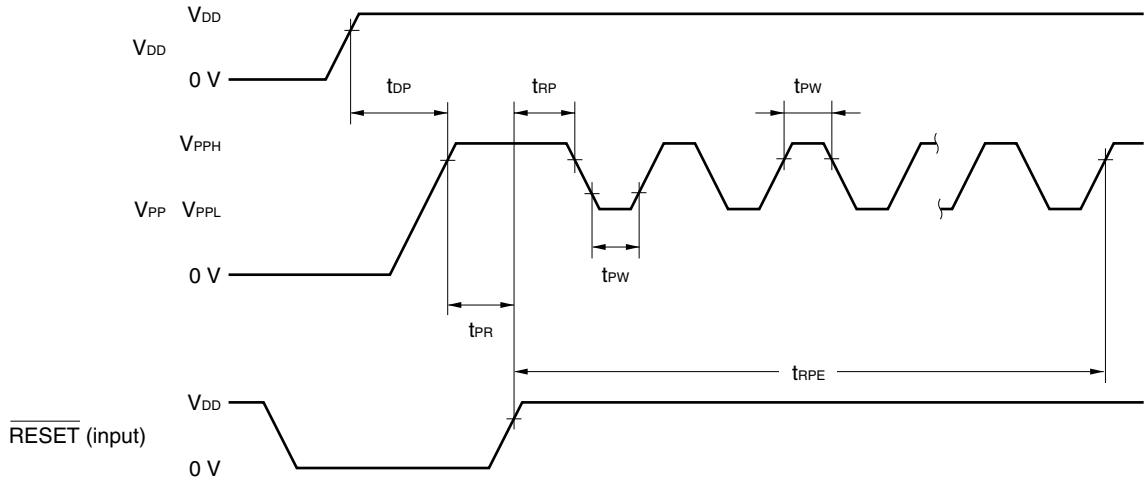
Shipped product → E → P → E → P → E → P: 3 rewrites

Remark The range of the operating clock during flash memory programming is the same as the range during normal operation.

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Set time from $V_{DD}\uparrow$ to $V_{PP}\uparrow$	t_{DP}		10			μs
Release time from $V_{PP}\uparrow$ to $\overline{RESET}\uparrow$	t_{PR}		10			μs
V_{PP} pulse input start time from $\overline{RESET}\uparrow$	t_{RP}		2			ms
V_{PP} pulse high-/low-level width	t_{PW}		8			μs
V_{PP} pulse input end time from $\overline{RESET}\uparrow$	t_{RPE}				14	ms
V_{PP} pulse low-level input voltage	V_{PPL}		0.8 V_{DD}		1.2 V_{DD}	V
V_{PP} pulse high-level input voltage	V_{PPH}		9.7	10.0	10.3	V

Flash Write Mode Setting Timing



7.4 LIN Transceiver Block Characteristics

DC Characteristics (T_A = –40 to +85°C, 7 V ≤ V_{DD} ≤ 18 V, 4.9 V ≤ V_{CM} = V_{DD} ≤ 5.1 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LIN Bus dominant leak current	$I_{BUS\_PAS\_dom}$	Driver off (V_{TxD} = VCM), V_{BUS} = 0 V, V_{SUP} = 12 V	–1			mA
LIN Bus recessive leak current	$I_{BUS\_PAS\_rec}$	Driver off (V_{TxD} = VCM), 8 V < V_{SUP} < 18 V, 8 V < V_{BUS} <18 V, V_{BUS} ≥ V_{SUP}			20	μA
LIN Bus current 1	$I_{BUS\_NO\_GND}$	GND_{Device} = V_{SUP}, 0 V < V_{BUS} < 18 V, V_{SUP} = 12 V	(–1)		(+1)	mA
LIN Bus current 2	I_{BUS}	V_{SUP_Device} = GND, 0 V < V_{BUS} < 18 V		(1)	(10)	μA
Receive dominant-level input voltage	V_{BUSdom}	7 V ≤ V_{SUP} ≤ 18 V			0.4 V_{SUP}	V
Receive recessive-level Input voltage	V_{BUSrec}	7 V ≤ V_{SUP} ≤ 18 V	0.6 V_{SUP}			V
Receive center-level threshold	V_{BUS_CNT}	7 V ≤ V_{SUP} ≤ 18 V, (V_{th_dom} + V_{th_rec})/2	0.475 V_{SUP}	0.5 V_{SUP}	0.525 V_{SUP}	V
Receive hysteresis	V_{HYS}	7 V ≤ V_{SUP} ≤ 18 V			0.175 V_{SUP}	V
LINO dominant-level output voltage 1	$V_{BUSdom\_DRV\_LoSUP}$	V_{SUP} = 7.3V, I_{lino} = 15 mA			0.3	V
LINO dominant-level output voltage 2	$V_{BUSdom\_DRV\_HiSUP}$	V_{SUP} = 18V, I_{lino} = 36 mA			0.4	V
LIN serial diode drop voltage	$V_{SerDiode}$	V_{TxD} = VCM, I_{lino} = 10 μA	(0.4)	(0.7)	(1.0)	V
LIN pull-up resistance	R_{slave}		(20)	(30)	(60)	kΩ
MSLP high level input voltage	V_{slph}		3.5			V
MSLP low level input voltage	V_{slpL}				1.5	V
MSLP pull-down resistance	R_{mslp}		50		200	kΩ
UMODE high level input voltage	V_{umh}		0.7 V_{CM}			V
UMODE low level input voltage	V_{uml}				0.3 V_{CM}	V
UMODE pull-down resistance	R_{umode}		0.5		2	MΩ
LIN overcurrent limitation	I_{bus_lim}	Driver ON	40		200	mA
LIN thermal shutdown	LIN_{th}		(150)			°C

Caution An external diode is required for negative charge protection between the LINI and LINO pins.

Remark The values in parentheses are design guaranteed values for which no shipping test has been performed.

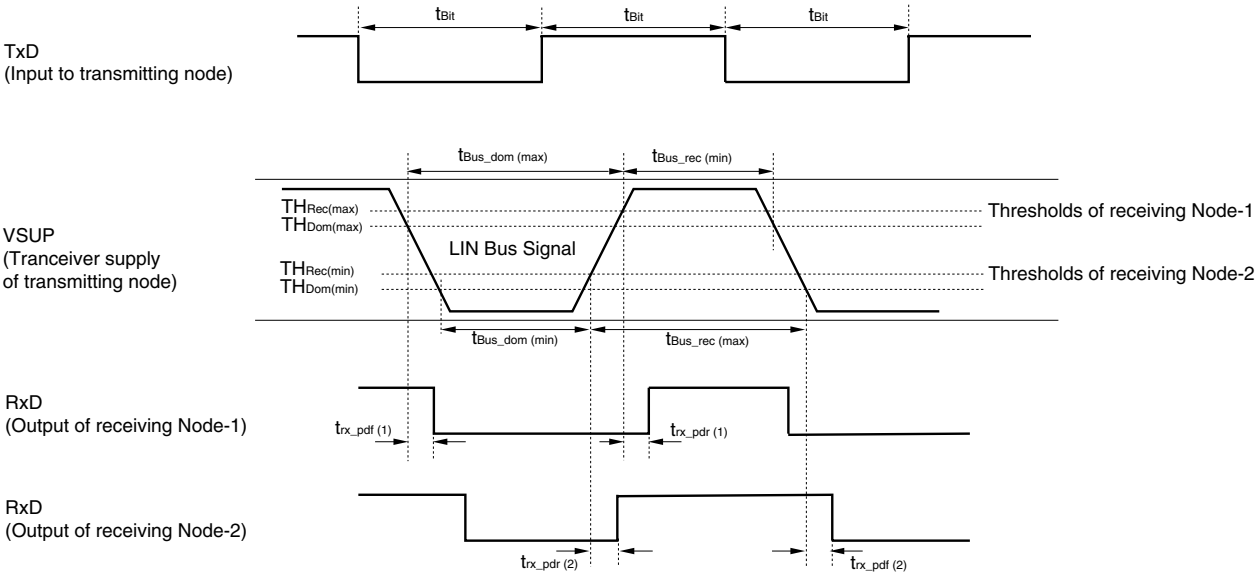
AC Characteristics

(T_A = –40 to +85°C, 7 V ≤ V_{DD} ≤ 18 V, 4.9 V ≤ V_{CM} = V_{DD} ≤ 5.1 V)

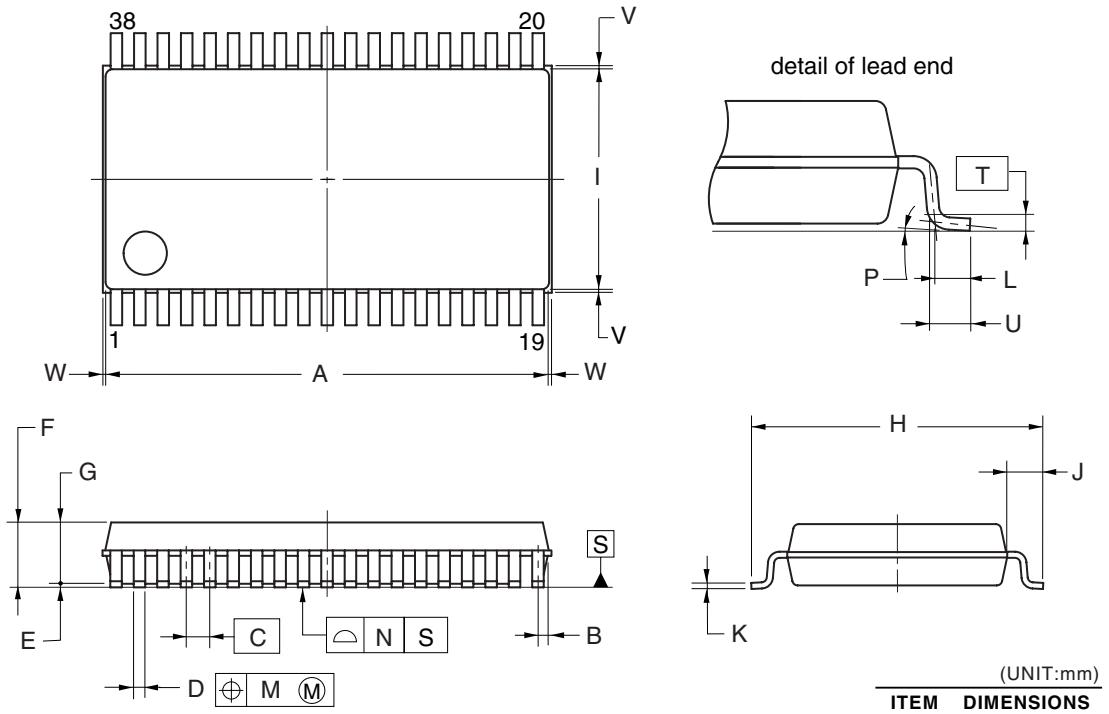
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Duty_Cycle1	D1	$TH_{Res\ (max)} = 0.744 \times V_{SUP}$, $TH_{Dom\ (max)} = 0.581 \times V_{SUP}$, V_{SUP} = 7.0 V to 18 V; t_{Bit} = 50 μs, $D1 = t_{Bus\_res\ (min)} / (2 \times t_{Bit})$ C_{BUS} = 1 nF, R_{BUS} = 1 kΩ	0.396			
Duty_Cycle2	D2	$TH_{Res\ (min)} = 0.422 \times V_{SUP}$, $TH_{Dom\ (min)} = 0.284 \times V_{SUP}$, V_{SUP} = 7.6 V to 18 V; t_{Bit} = 50 μs, $D2 = t_{Bus\_res\ (max)} / (2 \times t_{Bit})$ C_{BUS} = 1 nF, R_{BUS} = 1 kΩ			0.581	
Duty_Cycle3	D3	$TH_{Res\ (max)} = 0.778 \times V_{SUP}$, $TH_{Dom\ (max)} = 0.616 \times V_{SUP}$, V_{SUP} =7.0 V to 18 V; t_{Bit} = 96 μs, $D3 = t_{Bus\_res\ (min)} / (2 \times t_{Bit})$ C_{BUS} = 1 nF, R_{BUS} = 1 kΩ	0.417			
Duty_Cycle4	D4	$TH_{Res\ (min)} = 0.389 \times V_{SUP}$, $TH_{Dom\ (min)} = 0.251 \times V_{SUP}$, V_{SUP} = 7.6 V to 18 V; t_{Bit} =96 μs, $D4 = t_{Bus\_res\ (max)} / (2 \times t_{Bit})$ C_{BUS} = 1 nF, R_{BUS} = 1 kΩ			0.590	
Propagation delay	t_{rx_pd}	$t_{rx\_pdf\ (1)}$, $t_{rx\_pdf\ (2)}$, $t_{rx\_pdr\ (1)}$, $t_{rx\_pdr\ (2)}$			6	μs
LIN rising and falling transmitter delay symmetry	t_{rx_sym}	$t_{rx\_sym} = t_{rx\_pdf\ (1)} - t_{rx\_pdr\ (1)}$, $t_{rx\_sym} = t_{rx\_pdf\ (2)} - t_{rx\_pdr\ (2)}$,	–2		+2	μs

Definition of Bus Timing Parameters

Timing diagram:



38-PIN PLASTIC SSOP (7.62mm (300))



(UNIT:mm)

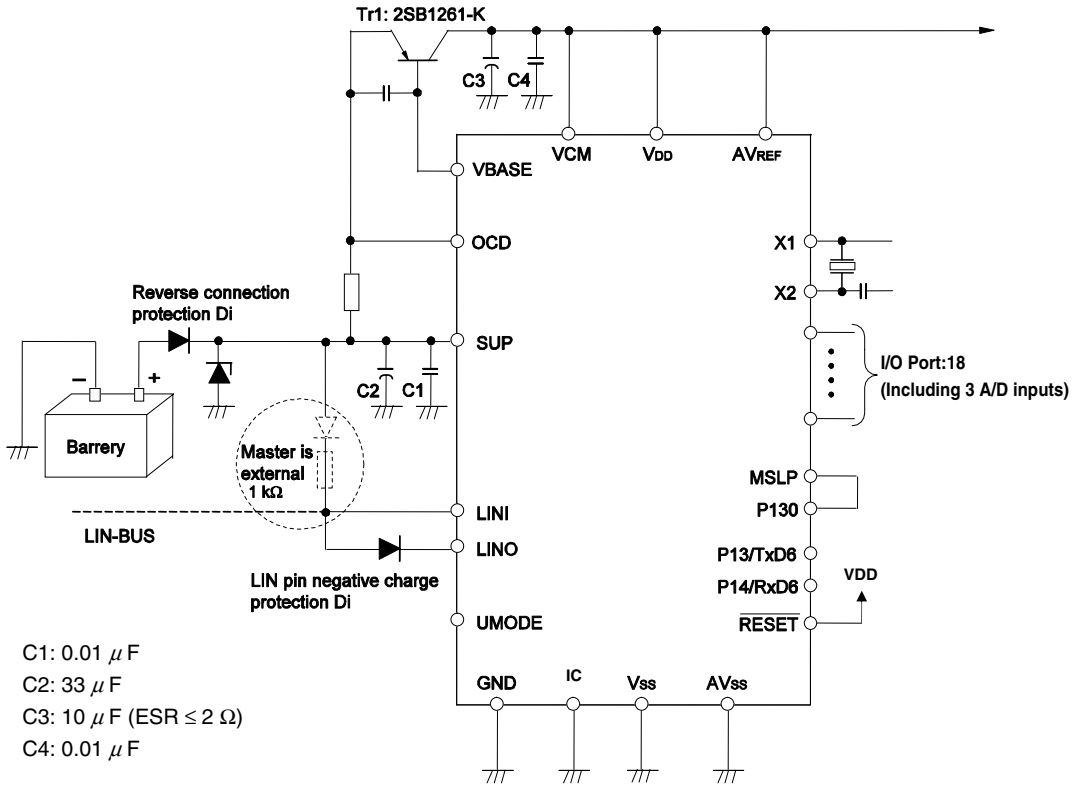
ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.30^{+0.10}_{-0.05}$
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.10}_{-0.05}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P38MC-65-GAA

NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

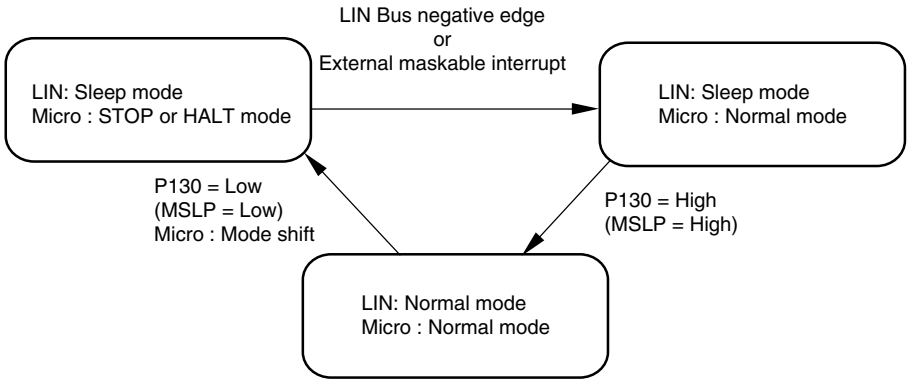
Figure 9-1. Circuit Example



Remarks 1. Place the external transistor of Tr1 for the power supply adjacent to the VBASE, VCM, and SUP pins and use the shortest possible wiring for the base, collector, and emitter.

2. Place the ceramic capacitor of C1 between the SUP and GND pins adjacent to the SUP pin and use the shortest possible wiring.

Figure 9-2. State Chart Example



APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD788001A, 788002A, and 78F8002A.

Figure A-1 shows the development tool configuration.

- **Support for PC98-NX series**

  Unless otherwise specified, products supported by IBM PC/AT™ compatibles are compatible with PC98-NX series computers. When using PC98-NX series computers, refer to the explanation for IBM PC/AT compatibles.

- **Windows™**

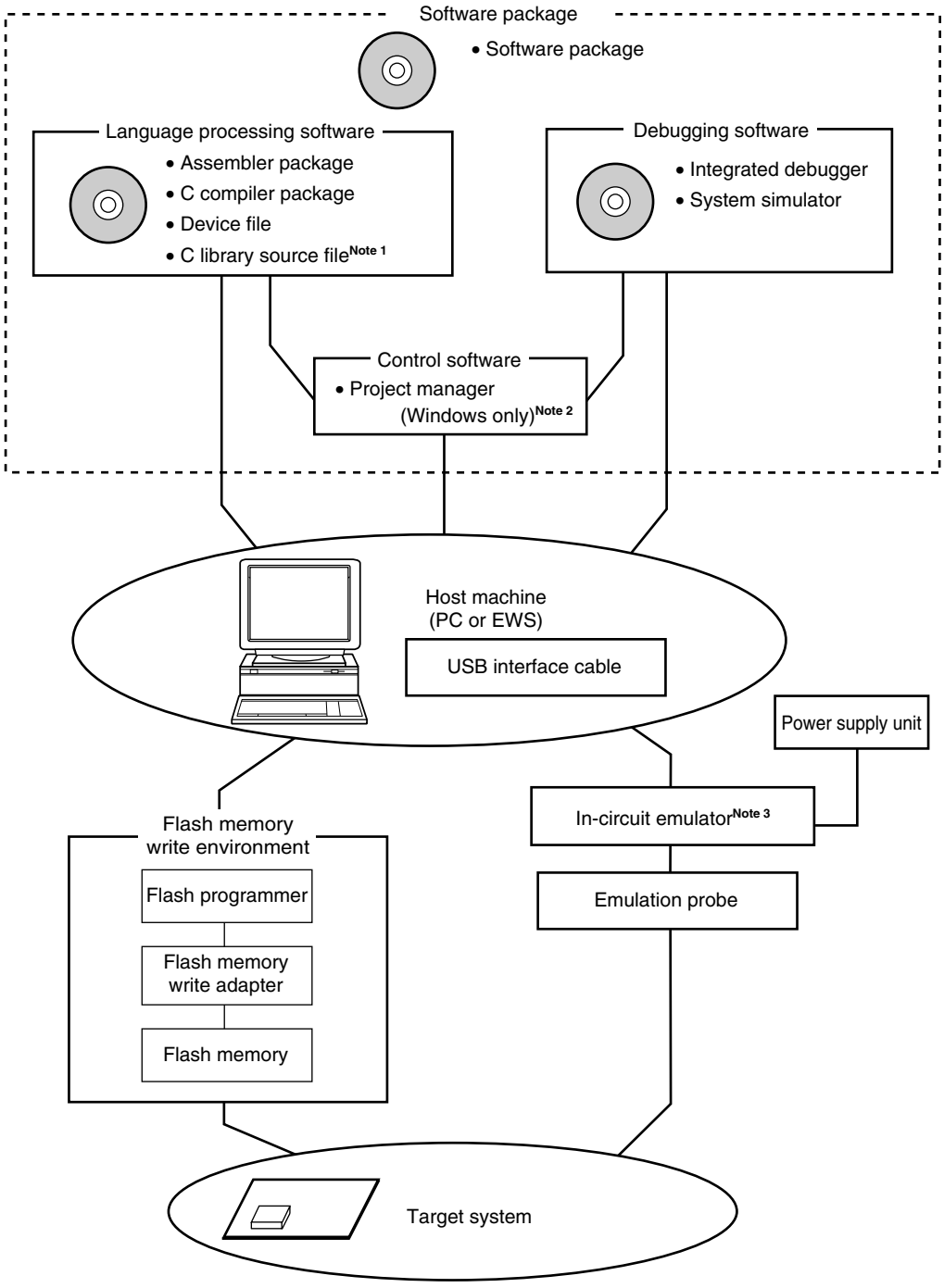
  Unless otherwise specified, “Windows” means the following OS.

  - Windows 98
  - Windows NT™
  - Windows 2000
  - Windows XP

Caution For the development tools, contact an NEC Electronics sales representative.

Figure A-1. Development Tool Configuration

(1) When using the in-circuit emulator QB-78K0KX1H



Notes 1. The C library source file is not included in the software package.

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. In-circuit emulator QB-78K0KX1H is supplied with integrated debugger ID78K0-QB, flash memory programmer PG-FPL (unsupported in the 78K0/Kx1 products), power supply unit, and USB interface cable. Any other products are sold separately.

A.1 Software Package

SP78K0 78K/0 microcontrollers software package	Development tools (software) common to the 78K/0 microcontrollers are combined in this package.
	Part number: μS××××SP78K0

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SP78K0

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

A.2 Language Processing Software

RA78K0 Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF788002) (sold separately). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the project manager (included in assembler package) on Windows.
	Part number: μS××××RA78K0
CC78K0 C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file (both sold separately). **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××CC78K0
DF788002[Note 1] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, and ID78K0-QB) (all sold separately). The corresponding OS and host machine differ depending on the tool to be used.
	Part number: μS××××DF788002
CC78K0-L[Note 2] C library source file	This is a source file of the functions that configure the object library included in the C compiler package. This file is required to match the object library included in the C compiler package to the user's specifications. Since this is a source file, its working environment does not depend on any particular operating system.
	Part number: μS××××CC78K0-L

Notes 1. The DF788002 can be used in common with the RA78K0, CC78K0, and ID78K0-QB.

2. The CC78K0-L is not included in the software package (SP78K0).

Remark ××××in the part number differs depending on the host machine and OS used.

μS××××RA78K0
μS××××CC78K0
μS××××CC78K0-L

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	
3P17	HP9000 series 700™	HP-UX™ (Rel. 10.10)	
3K17	SPARCstation™	SunOS™ (Rel. 4.1.4) Solaris™ (Rel. 2.5.1)	

μS××××DF788002

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	

A.3 Control Software

PM+ Project manager	This is control software designed to enable efficient user program development in the Windows environment. All operations used in development of a user program, such as starting the editor, building, and starting the debugger, can be performed from the project manager. **<Caution>** The project manager is included in the assembler package (RA78K0). It can only be used in Windows.

A.4 Flash Memory Writing Tools

FlashPro4 (part number: FL-PR4, PG-FP4) Flash programmer	Flash programmer dedicated to microcontrollers with on-chip flash memory.
FA-38GS-300B-A Flash memory writing adapter	Flash memory writing adapter used connected to the FlashPro4.

Remark FL-PR4,and FA-38GS-300B-A are products of Naito Densei Machida Mfg. Co., Ltd.
TEL: +81-42-750-4172 Naito Densei Machida Mfg. Co., Ltd.

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator QB-78K0KX1H

QB-78K0KX1H[Note] In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0/Kx1 and 78K0/Kx1+. It corresponds to the integrated debugger (ID78K0-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-788002-EA-01T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. Adapter has LIN transceiver and voltage regulator function.
QB-38MC-YS-01T Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator.
QB-38MC-YQ-01T YQ connector	This YQ connector is used to connect the target connector and exchange adapter.
QB-38MC-HQ-01T Mount adapter	This mount adapter is used to mount the target device with socket.
QB-38MC-NQ-01T Target connector	This target connector is used to mount on the target system.

Note The QB-78K0KX1H is supplied with a power supply unit, USB interface cable, and flash memory programmer PG-FPL (78K0/Kx1 products are not supported). As control software, integrated debugger ID78K0-QB is supplied.

Remark The packed contents differ depending on the part number, as follows.
QB-78K0KX1H-ZZZ: In-circuit emulator only

A.6 Debugging Tools (Software)

ID78K0-QB (supporting in-circuit emulator QB-78K0KX1H) Integrated debugger	This debugger supports the in-circuit emulators for the 78K0/Kx1 and 78K0/Kx1+. ID78K0-QB is Windows-based software. It has improved C-compatible debugging functions and can be display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (sold separately).
	Part number: μS××××ID78K0-QB

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××ID78K0-QB

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

<R>

APPENDIX B REVISION HISTORY

B.1 Major Revisions in This Edition

Page	Description
p. 20	Deletion of description for Function of AV_{REF} in **(2) Non-port functions (1/2)**
p. 51	**DC characteristics** in **7.2 Power Supply Block Characteristics** • Modification of LIN for I_{bat3} in Supply current • Modification of Input regulation
p. 53	**DC Characteristics (1/4)** in **7.3 Microcontroller Block Characteristics** • Addition of Total of all pins in Output current, high and Output current, low
pp. 55, 56	**DC Characteristics (3/4), (4/4)** in **7.3 Microcontroller Block Characteristics** • Modification of V_{DD} in f_{XP} = 5 MHz of X1 crystal oscillation operating mode
p. 75	Addition of **APPENDIX B REVISION HISTORY**

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