

# Linux Interface Specification Device Driver SPI Multi IO

User's Manual: Software  
RZ/G2L Group, RZ/V2L Group, and RZ/Five

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## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group and RZ/Five Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description  Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
User's manual for Software	Description of SPI Multi IO Linux interface Specification	Linux interface Specification – SPI Multi IO	This user's manual
Application Note	Information on using peripheral functions and application examples  Sample programs  Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

#### 4. List of Abbreviations and Acronyms

Abbreviation	Full Form
SPIBSC	Serial Peripheral Interface Bus Serial Controller

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# 1. Overview

## 1.1 Overview

This manual explains the driver module (this module) that controls the SPIBSC Interfaces or SPI Multi I/O Bus Controller on RZ/G2L Group, RZ/G2LC Group, RZ/V2L Group, RZ/G2UL Group, and RZ/Five.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L group and RZ/Five.
- v6.1: RZ/G2L and RZ/G2LC.

## 1.2 Function

This module allows the connected serial flash, Octa Flash, Hyper Flash memory devices to be accessed by reading the external address space or using Manual mode to transmit and receive data.

The following table lists the features of this module.

**Table 1.1 Driver Features**

Feature	Support status (RZ/G2L, RZ/G2LC and RZ/V2L)	Support status (RZ/G2UL, RZ/Five)
Master Mode	Support	
Serial-Flash Memory Interface	RZ/G2LC: QSPIO_SPCLK: 66MHz (SDR); Others: QSPIO_SPCLK: 66MHz; two serial flash memory are connected parallel	QSPIO_SPCLK: 66MHz (SDR); one serial flash memory is connected.
Octa-Flash memory Interface	No support	No support
Hyper-Flash Interface	No support	No support
External Address Space Read Mode	Read access from the bus master to SPI multi I/O is automatically converted to a read command; normal read and burst read operation	
Manual Mode	Read and write commands are available for serial flash or Hyper-Flash memory; a write buffer is provided; cache is not usable for reading	

## 1.3 Connected device

This module can connect Serial flash memory devices on RZ/G2L Series, RZ/V2L and RZ/Five.

## 1.4 Reference

### 1.4.1 Standard

There are no reference documents on standards.

### 1.4.2 Related documents

The following table shows the document related to this module.



**Table 1.2**      **Related documents (RZ)**

Number	Issue	Title	Edition	Data
-	-	-	-	-

## 1.5      Restrictions

There is no restriction in this module.

## 1.6      Notice

## 2. Terminology

The following table shows the terminology related to this kernel.

**Table 2-1 Terminology**

Terms	Explanation
SPIBSC	<b>S</b> erial <b>P</b> eripheral Interface <b>B</b> us <b>S</b> erial <b>C</b> ontroller

## 3. Operating Environment

### 3.1 Hardware Environment

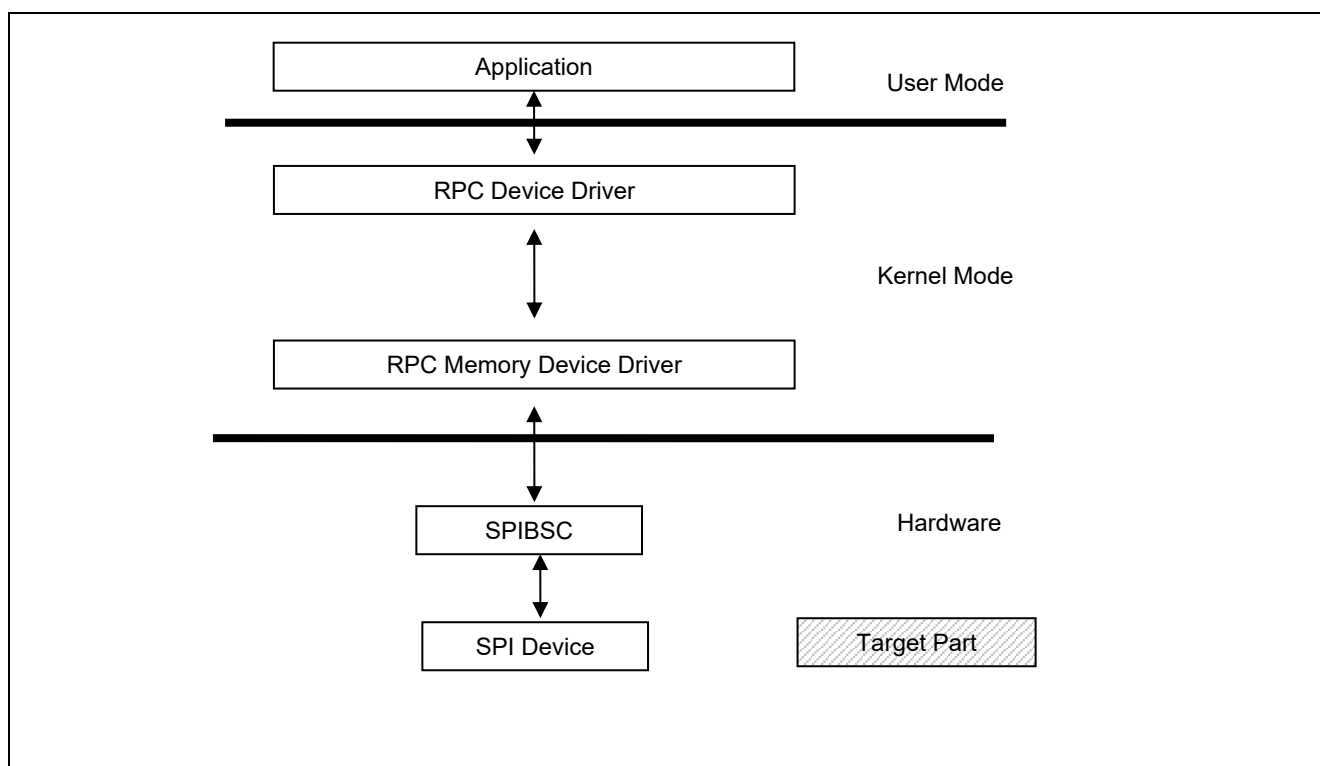
The following table lists the hardware needed to use this module.

**Table 3.1 Hardware specification**

Name	Version	Manufacturer
RZ/G2L Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/V2L Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/G2UL Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/G2LC Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/Five Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH

### 3.2 Module Configuration

The following figure shows the configuration of this module.



**Figure 3.1 Module configuration**

### 3.3 State Transition Diagram

The following figure shows the software flowchart of this module.

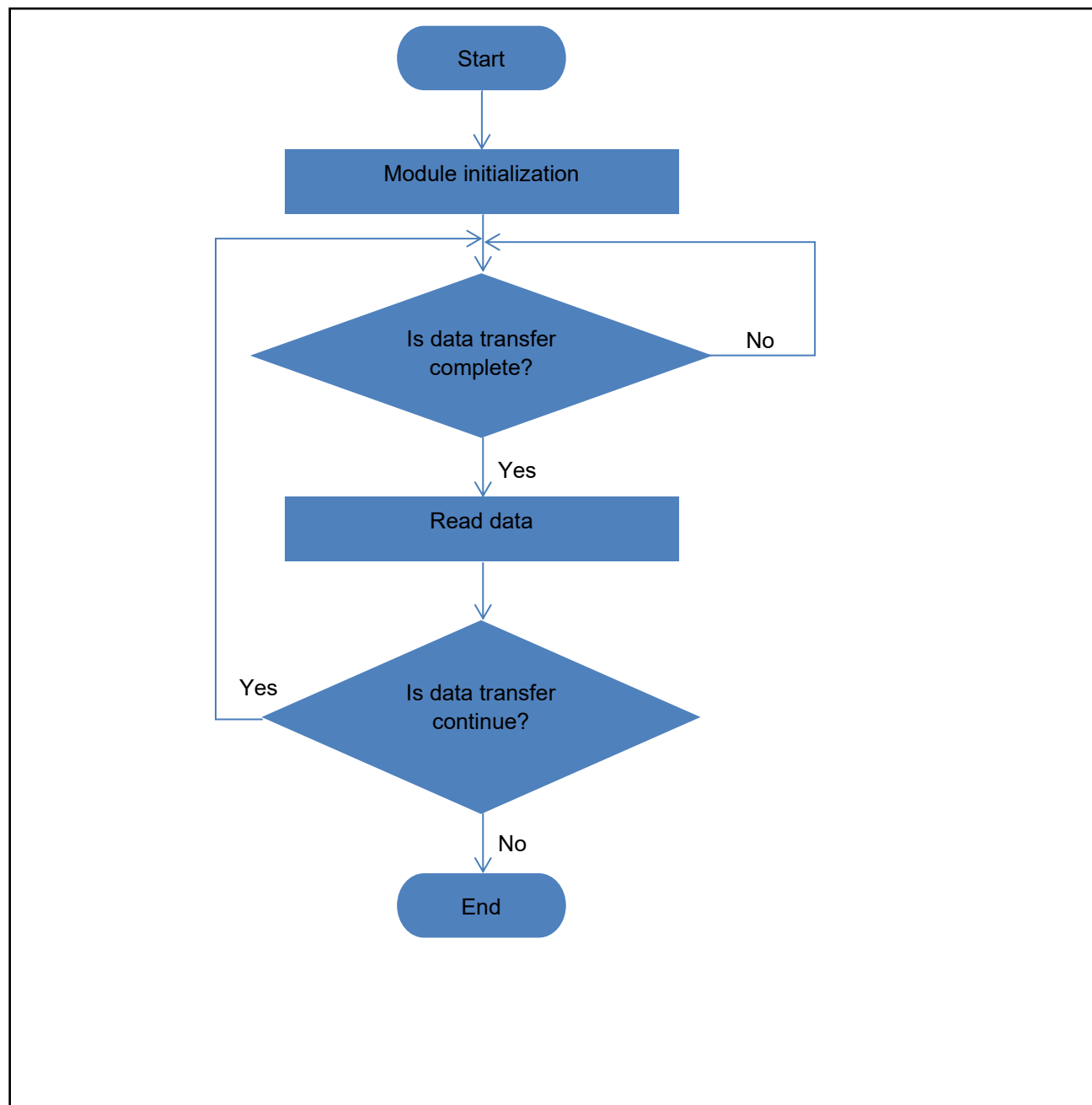


Figure 3.2 Module configuration

## 4. External Interface

### 4.1 Sysfs Interface

Table 4.1 Hardware specification

SPI Multi IO Interfaces	Notes
/sys/class/spi_master/spi3/spi3.0	-

### 4.2 External Function

Detailed explanation is skipped because the external interface of this module is based on Linux.

## 5. Integration

### 5.1 Directory Configuration

The directory configuration is shown below.

drivers/spi/	drivers/spi/spi-rpc-if.c	: RPC driver source file
drivers/memory/	drivers/memory/renesas-rpc-if.c	: RPC memory source file

**Figure 5-1 Directory Configuration (RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five)**

### 5.2 Integration Procedure

Add the setting of the channel to be used by modifying the settings in Device tree.

#### 5.2.1 Device tree settings

The target file by board is as follows.

Directory: arch/arm64/boot/dts/renesas

- r9a07g044.dtsi for RZ/G2{L,LC}, r9a07g054.dtsi for RZ/V2L and r9a07g044.dtsi for RZ/G2UL, RZ/Five
- r9a07g044l{1,2}.dtsi, rzg2l-smarc.dtsi, rzg2l-smarc-som.dtsi for RZ/G2L specific parts
- r9a07g044c{1, 2}.dtsi, rzg2lc-smarc.dtsi, rzg2lc-smarc-som.dtsi for RZ/G2LC specific parts
- r9a07g054l{1,2}.dtsi for RZ/V2L specific parts
- r9a07g043u11.dtsi, rzg2ul-smarc.dtsi, rzg2ul-smarc-som.dtsi for RZ/G2UL specific parts.
- r9a07g044l2-smarc.dts for RZ/G2L smarc, r9a07g044c2-smarc.dts for RZ/G2LC smarc, r9a07g054l2-smarc.dts for RZ/V2L smarc and r9a07g043u11-smarc.dts for RZ/G2UL smarc.

Directory: arch/riscv/boot/dts/renesas

- r9a07g043f.dtsi for RZ/Five
- rzfive-smarc.dtsi, rzfive-smarc-som.dtsi for RZ/Five specific parts
- r9a07g043f01-smarc.dts for RZ/Five smarc.

#### 5.2.1.1 Settings in file .dtsi

Create node of module spibsc

```
sbc: spi@10060000 {
    compatible = "renesas,r9a07g044-rpc-if",
                "renesas,rzg2l-rpc-if";
    reg = <0 0x10060000 0 0x10000>,
          <0 0x20000000 0 0x10000000>,
          <0 0x10070000 0 0x10000>;
    reg-names = "regs", "dirmap", "wbuf";
    interrupts = <GIC_SPI 41 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G044_SPI_CLK2>,
             <&cpg CPG_MOD R9A07G044_SPI_CLK>;
    resets = <&cpg R9A07G044_SPI_RST>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5-2 Add settings in file .dtsi (RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five)**

Note: All of the information in above device tree is used for both RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five except:

compatible: "renesas,r9a07g044-rpc-if" for RZ/G2L and RZ/G2LC. "renesas,r9a07g054-rpc-if" for RZ/V2L. "renesas,r9a07g043-rpc-if" for RZ/G2UL and RZ/Five.

clocks: R9A07G044\_SPI\_CLK2 and R9A07G044\_SPI\_CLK for RZ/G2L and RZ/G2LC, R9A07G054\_SPI\_CLK2 and R9A07G054\_SPI\_CLK for RZ/V2L, R9A07G043\_SPI\_CLK2 and R9A07G043\_SPI\_CLK for RZ/G2UL and RZ/Five.

resets: R9A07G044\_SPI\_RST for RZ/G2L and RZ/G2LC, R9A07G054\_SPI\_RST for RZ/V2L and R9A07G043\_SPI\_RST for RZ/Five and RZ/G2UL

### 5.2.1.2 Settings in file .dts

- Device setting:

```
&sb{
    pinctrl-0 = <&qspi0_pins>;
    pinctrl-names = "default";
    status = "okay";

    flash@0 {
        compatible = "micron,mt25qu512a", "jedec,spi-nor";
        reg = <0>;
        m25p,fast-read;
        spi-max-frequency = <50000000>;
        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x0001c000>;
            };

            partition@1d000 {
                /* fip is at offset 0x200 */
                label = "fip";
                reg = <0x0001d000 0x1fe3000>;
            };

            partition@2000000 {
                label = "user";
                reg = <0x02000000 0x2000000>;
            };
        };
    };
};
```

**Figure 5-3 Add settings in file .dtsi (RZ/G2L, RZ/G2LC and RZ/V2L)**

```

&sbcs {

    pinctrl-0 = <&qspi0_pins>;
    pinctrl-names = "default";

    status = "okay";

    flash@0 {
        compatible = "atmel,at25ql128a", "jedec,spi-nor";
        reg = <0>;
        m25p,fast-read;
        spi-max-frequency = <50000000>;
        spi-tx-bus-width = <4>;
        spi-rx-bus-width = <4>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x0001c000>;
            };

            partition@01d00 {
                /* fip is at offset 0x200 */
                label = "fip";
                reg = <0x0001d000 0x7e3000>;
            };

            partition@800000 {
                label = "user";
                reg = <0x800000 0x800000>;
            };
        };
    };
};

```

Figure 5-4 Add settings in file .dtsi (RZ/G2UL)

```

#include <arm64/renesas/rzg2ul-smarc-som.dtsi>

&sbcs {
    spi-tx-bus-width = <1>;
    spi-rx-bus-width = <1>;
};

```

Figure 5-5 Add settings in file .dtsi (RZ/Five)

**-Note:** if you are **not** using mount command for mtd partition in JFFS2 format, you can set spi-tx-bus-width to <4>.



### 5.2.2 Kernel and build-root configuration

To enable the function of this module, make the following setting with Kernel Configuration. The changes affect after re-building the kernel.

```
Device Drivers --->
  [*] SPI support -->
    --- SPI support
        ...
    <*> Renesas RPC-IF SPI driver
  [*] Memory Controller drivers
    <*> Renesas RPC-IF driver
```

**Figure 5-5: Kernel configuration for SPIBSC Driver (RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five)**

To use file system driver JFF2, make the following setting with Kernel Configuration. The changes affect after re-building the file system build-root.

```
File Systems --->
  <*> Miscellaneous filesystems -->
    <*> Journaling Flash File System v2 (JFFS2) support
    [*] JFFS2 write-buffering support
```

**Figure 5-6: File system configuration for SPIBSC Driver (RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five)**

## 5.3 Option Setting

### 5.3.1 Module Parameters

There are no module parameters.

### 5.3.2 Kernel Parameters

There is no module parameter.

Revision History	Linux Interface Specification Device Driver SPI Multi IO User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 21	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents.
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	—	Update device tree and driver
1.4	May. 31, 2022	—	No modification, change version to keep consistent with other documents
1.5	June. 24, 2022	—	Add RZ/Five
1.6	Sep. 15, 2022	—	Update information
1.7	Dec. 15, 2022	—	Update information
1.8	Mar. 31, 2023	—	No modification, change version to keep consistent with other documents
1.9	Mar. 31, 2025	1, 2, 7-9	Correct device tree node for RZ/G2L group and RZ/Five, correct connected device, remove content in "1.6 Notice" because cannot support 8 bits bus interface
1.10	May 30, 2025	1, 11	<ul style="list-style-type: none"> <li>- Add MPU information support for both kernel versions v5.10 and v6.1.</li> <li>- Remove note build-root</li> </ul>

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