

Linux Interface Specification Device Driver SCIFA

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/G3E Group and RZ/Five

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General Precautions in the Handling of Micro processing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Micro processing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a micro processing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group and RZ/G3E Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
User's manual for Software	Software specifications (basic function of Linux kernel, memory maps, interrupt, clock, pins mux, device tree)	Linux interface Specification - Device Driver SCIFA	This User's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
bps	bits per second
DMA	Direct Memory Access
UART	Universal Asynchronous Receiver/Transmitter

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1. Overview

1.1 Overview

This manual explains the driver module that controls the SCIFA on RZ/G and RZ/V2L Series, 2nd Generation, RZ/Five, RZ/V2N and RZ/G3E. Detailed explanation is skipped because the interface of this module is based on Linux.

Note: Currently, the devices that support this function are RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five RZ/V2N and RZ/G3E.

It supports two kernel versions v5.10 and v6.1 as shown below:

- v5.10: RZ/G2L Group, RZ/V2L group and RZ/Five.
- v6.1: RZ/G2L, RZ/G2LC, RZ/V2N and RZ/G3E.

1.2 Function

This module controls the Serial Communications Interface with FIFO (SCIFA) on RZ/G2L, RZ/V2L, RZ/Five, RZ/V2N and RZ/G3E. This module supports the following functions.

- Data transmission and reception for RS232C
- 1 channel support asynchronous communication for RZ/V2N and RZ/G3E
- Control of communication settings
 - Baud rate 9600, 19200, 38400, 57600, 115200[bps]
 - Parity bit (none/ODD/EVEN)
 - Stop bit (1bit or 2bit)
 - Data transfer bit length (7bit or 8bit)

Each setting can be changed from the standard ioctl for tty.

- Hardware Flow Control of RZ/G2L, RZ/V2L, RZ/Five
 - Support: SCIF2
 - Not support: SCIF0

1.3 Connected Port

Table 1.1 describes port connected to SCIFA on the RZ/G2L and RZ/V2L Evaluation Board Kit.

Table 1-1 Connected port (RZ/G2L group, RZ/V2L and RZ/Five) Evaluation Board Kit

Channel	Connector	Support status	Remark
SCIF0	SMARC module: CN4 Carrier board: CN14	Yes	Output as DEBUG UART
SCIF1	-	No	-
SCIF2	SMARC module: CN4 Carrier board: SW1, SW2, SW3, SW4, CN7	Yes	Output as PMOD1
SCIF3	-	No	-
SCIF4	-	No	-

Note: G2UL, RZ/Five only supports SCIF0.

Table 1.2 describes port connected to SCIFA on the RZ/V2N Evaluation Board Kit

Table 1-2 Connected port (RZ/V2N) Evaluation Board Kit

Channel	Connector	Support status	Remark
SCIF0	Expansion board: USB Serial	Yes	Default output at USB Serial

Table 1.3 describes port connected to SCIFA on the RZ/G3E Evaluation Board Kit

Table 1-3 Connected port (RZ/G3E) Evaluation Board Kit

Channel	Connector	Support status	Remark
SCIF0	RZ SMARC Carrier II: SER3_UART	Yes	Output as DEBUG UART

1.4 Reference

1.4.1 Standard

There is no reference document on standards.

1.4.2 Related Documents

None.

1.5 Restrictions

None.

1.6 Notice

- This driver isn't evaluated with the baud rate of 1Mbps and more.

2. Terminology

The following table shows the terminology related to this module.

Table 2-1 Terminology

Terms	Explanation
SCIF	Serial Communications Interface with FIFO

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this module.

Table 3-1 Hardware Environment (RZ/G2L, RZ/V2L and RZ/Five)

Name	Version	Manufacturer
RZ/G2L Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/G2LC Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/G2UL Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/V2L Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH
RZ/Five Evaluation Board Kit	SMARC module: v01 Carrier board: v03	Renesas Electronics Europe GmbH

Table 3-2 Hardware Environment RZ/V2N and RZ/G3E

Name	Product number
RZ/V2N Evaluation Board Kit	RTK0EF0186C03000BJ
RZ/G3E SMARC Evaluation Board Kit	RTK9947E57S01000BE

3.2 Module Configuration

The following figure shows the configuration of this module.

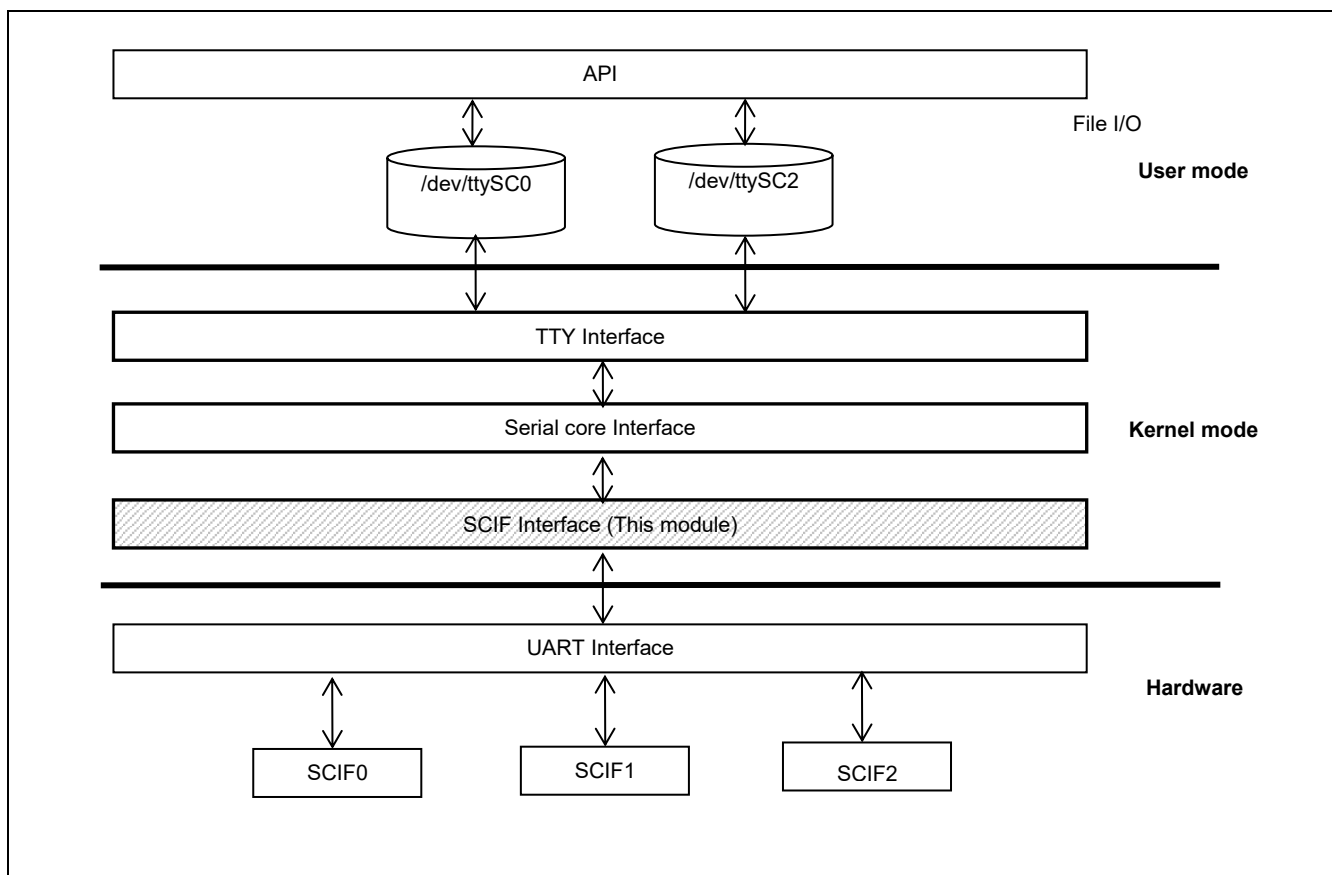


Figure 3-1 Module Configuration

Note: RZ/G2UL, RZ/Five, RZ/V2N, RZ/G3E only supports SCIF0.

3.3 State Transition Diagram

There is no state transition diagram for this module.

4. External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

4.1 Device Node

Device node of this module is shown below.

Table 4-1 Device Node

Channel	Device node	Supported
SCIF0	/dev/ttySC0	RZ/G2{L, LC, UL}, V2L, RZ/Five RZ/V2N and RZ/G3E
SCIF1	/dev/ttySC1	RZ/G2LC
SCIF2	/dev/ttySC1	RZ/G2L, RZ/V2L

4.2 Clock source setting

4.2.1 Select clock source

The following clock source can be used.

Table 4-2 Clock Source

Clock source	Frequency	Description
fck	100 MHz	Functional Clock Source

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.

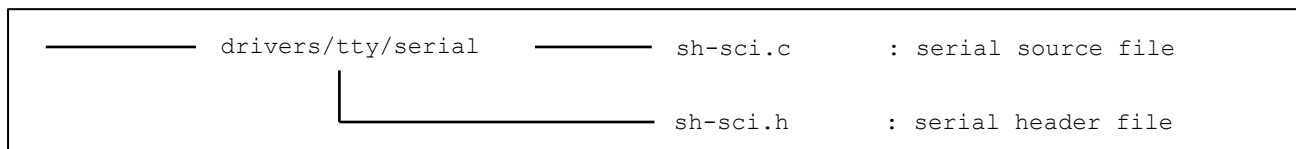


Figure 5-1 Directory Configuration

5.2 Integration Procedure

5.2.1 Enable scif0 and scif2.

The following description explains how to enable scif0 and scif2 channel in RZ/G2L and RZ/V2L.

The following description indicates a difference from the default setting. ("−": Delete a description (default setting), "+": Setting after the modification))

file: arch/arm64/boot/dts/renesas/rzg2l-smarc.dtsi

```
aliases {
    i2c0 = &i2c0;
    i2c1 = &i2c1;
    i2c3 = &i2c3;
+   serial0 = &scif0;
+   serial2 = &scif2;
    ethernet0 = &eth0;
    ethernet1 = &eth1;
};

&scif0 {
    pinctrl-0 = <&scif0_pins>;
    pinctrl-names = "default";
+   status = "okay";
};

&scif2 {
    pinctrl-0 = <&scif2_pins>;
    pinctrl-names = "default";
+   status = "okay";
};
```

Figure 5-2 Enable SCIF0 and SCIF2

Note: RZ/G2UL, RZ/Five, RZ/V2N, RZ/G3E only supports SCIF0.

5.2.2 Enable hardware flow control

The following description explains how to enable hardware flow control function. To use the hardware flow control function, add "uart-has-rtscts" property. The following description indicates a difference from the default setting. ("+": Setting after the modification)

file: arch/arm64/boot/dts/renesas/rzg2l-smarc.dtsi

The editing contents are shown in Figure 5-3

```

&scif2 { *1
    pinctrl-0 = <&scif2_pins>; *1
    pinctrl-names = "default";
+    uart-has-rtsccts;
    ...
};

```

*1: Replace with the channel number of the scif to be used.

Figure 5-3 Enable Hardware Flow Control for SCIF2

5.2.3 Pin configuration settings

In RZ/V2N, add "renesas,output-impedance = <1>;" property to set enable the drive strength of SCIF pin.

```

scif0_pins: scif0 {
    pins = "SCIF_TXD", "SCIF_RXD";
    renesas,output-impedance = <1>;
};

```

Figure 5-4 Enable the drive strength of SCIF0 pin

5.2.4 Kernel configuration settings

To enable the functions of this module, make the following setting with Kernel Configuration.

```

General setup --->
  [ ] Embedded system *1

Device Drivers --->
  Character devices --->
    Serial drivers --->
      <*> SCI(F) serial port support
      (11) Maximum number of SCI(F) serial ports *2
      [*] Support for console on SCI(F) *2
      [*] Support for early console on SCI(F) *2
      [*] DMA support *2 *3

```

Figure 5-5 Kernel configuration

Notes: *1 Please set if you want to enable option selection.

*2 This menu is option. To use it, enable the configuration of *1.

*3 The default is DMA transfer mode. When this configuration is disabled, selects the PIO transfer mode.

5.3 Device Tree Setting

5.3.1 SCIF node

Basic configuration information of SCIF is defined at device tree file (r9a07g044l.dtsi for RZ/G2L and r9a07g044c.dtsi for RZ/G2LC and r9a07g043u.dtsi for RZ/G2UL and r9a07g054l.dtsi for RZ/V2L). It exists at arch/arm64/boot/dts/renesas directory. This module uses these described contents in device tree file.

The initial reference information is shown below.

```

scif0: serial@1004b800 {
    compatible = "renesas,scif-r9a07g044";
    reg = <0 0x1004b800 0 0x400>;
    interrupts = <GIC_SPI 380 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 382 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 383 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 381 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 384 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 384 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "eri", "rx", "tx",
                    "bri", "dri", "tei";
    clocks = <&cpg CPG_MOD R9A07G044_SCIF0_CLK_PCK>;
    clock-names = "fck";
    power-domains = <&cpg>;
    resets = <&cpg R9A07G044_SCIF0_RST_SYSTEM_N>;
    status = "disabled";
};

```

Figure 5-6 Device tree initial references information of SCIF (RZ/G2L and RZ/V2L)

Required properties:

- **compatible:**
must be "renesas,scif-r9a07g04{4,3}" for (RZ/G2{[L,C], UL}) or "renesas,scif-r9a07g044"
- **reg:**
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- **interrupts:**
interrupt specifier for the SCIF
- **clocks, resets:**
phandle + clock/reset specifier pairs

Note) All the information in the above device tree is used for RZ/G2L, also the same as RZ/V2L. To config for RZ/V2L, only replace r9a07g044l with r9a07g054l. For RZ/G2LC, replace r9a07g044l with r9a07g044c. And for RZ/G2UL, replace r9a07g044l with r9a07g043u.

- RZ/Five: SCIF nodes: arch/riscv/boot/dts/renesas/r9a07g043f.dtsi

```

scif0: serial@1004b800 {
    compatible = "renesas,scif-r9a07g043f";
    reg = <0 0x1004b800 0 0x400>;
    interrupts = <412 IRQ_TYPE_LEVEL_HIGH>,
                <414 IRQ_TYPE_LEVEL_HIGH>,
                <415 IRQ_TYPE_LEVEL_HIGH>,
                <413 IRQ_TYPE_LEVEL_HIGH>,
                <416 IRQ_TYPE_LEVEL_HIGH>,
                <416 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "eri", "rx", "tx",
                    "bri", "dri", "tei";
    clocks = <&cpg CPG_MOD R9A07G043F_SCIF0_CLK_PCK>;
    clock-names = "fck";
    power-domains = <&cpg>;
    resets = <&cpg R9A07G043F_SCIF0_RST_SYSTEM_N>;
    status = "disabled";
};

```

Figure 5-7 Device tree initial references information of SCIF (RZ/Five)

- RZ/V2N: SCIF nodes: arch/arm64/boot/dts/renesas/r9a09g056.dtsi
- RZ/G3E: SCIF nodes: arch/arm64/boot/dts/renesas/r9a09g047.dtsi

```

scif0: serial@1004b800 {
    compatible = "renesas,scif-r9a09g056", "renesas,scif-
r9a07g044";

    reg = <0 0x11c01400 0 0x400>;
    interrupts = <GIC_SPI 529 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 532 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 533 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 530 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 534 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 531 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 535 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 536 IRQ_TYPE_EDGE_RISING>,
        <GIC_SPI 537 IRQ_TYPE_EDGE_RISING>;
    interrupt-names = "eri", "rx", "tx", "bri", "dri",
        "tei", "tei-dri", "rx-edge", "tx-edge";
    clocks = <&cpg CPG_MOD 0x8f>;
    clock-names = "fck";
    power-domains = <&cpg>;
    resets = <&cpg 0x95>;
    status = "disabled";
};

```

Figure 5-8 Device tree initial references information of SCIF (RZ/V2N and RZ/G3E)

Required properties:

- compatible:
must be compatible "renesas,scif-r9a09g056", "renesas,scif-r9a07g044" for RZ/V2N

must be compatible "renesas,scif-r9a09g047", "renesas,scif-r9a07g044" for RZ/G3E
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
interrupt specifier for the SCIF
- clocks, resets:
phandle + clock/reset specifier pairs (clock index 0x8f, reset index 0x95 for RZ/V2N)

phandle + clock/reset specifier pairs (clock index 143, reset index 149 for RZ/G3E)

5.3.2 Documentation file in the kernel

Please follow guideline in Documentation/devicetree/bindings/serial/serial.yaml

5.4 Option Setting

5.4.1 Module Parameters

There are no module parameters.

5.4.2 Kernel Parameters

To ensure proper initialization and debugging capabilities over the serial console during early boot stages, it is recommended to add the following kernel parameters:

- `earlycon`: Enables early console output for debugging messages during the early boot process, before the full console driver is initialized.
- `console=<serial_device>`: Specifies the UART device to be used as the primary console.
For example, `console=ttySC0`.
- `no_console_suspend`: Prevents the serial console from being suspended during system suspend.

REVISION HISTORY	Linux Interface Specification Device Driver SCIFA User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 2021	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	12	Update information for Devicetree
1.4	May. 31, 2022	—	No modification, keep version to keep consistent with other documents
1.5	Jun. 24, 2022	—	Add RZ/Five device
1.6	Sep. 15, 2022	—	Update information
1.7	Dec. 15, 2022	—	No modification, keep version to keep consistent with other documents
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents
1.9	May. 30, 2025	1	Add MPU information support for both kernel versions v5.10 and v6.1. Update list of abbreviations and acronyms
1.10	Jun. 30, 2025	—	Add RZ/V2N information
1.11	Jul. 22, 2025	—	Add RZ/G3E information
		11	Add "5.2.3 Pin configuration settings"

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