

RICBox GUI Software for VersaClock® 8

This guide assists those using the Renesas IC Toolbox (RICBox) software to configure and control a VersaClock® 8 (VC8) device. This includes (but is not limited to) the RC31312A, RC31309A, RC31305A, RC31312AQ, RC31309AQ devices.

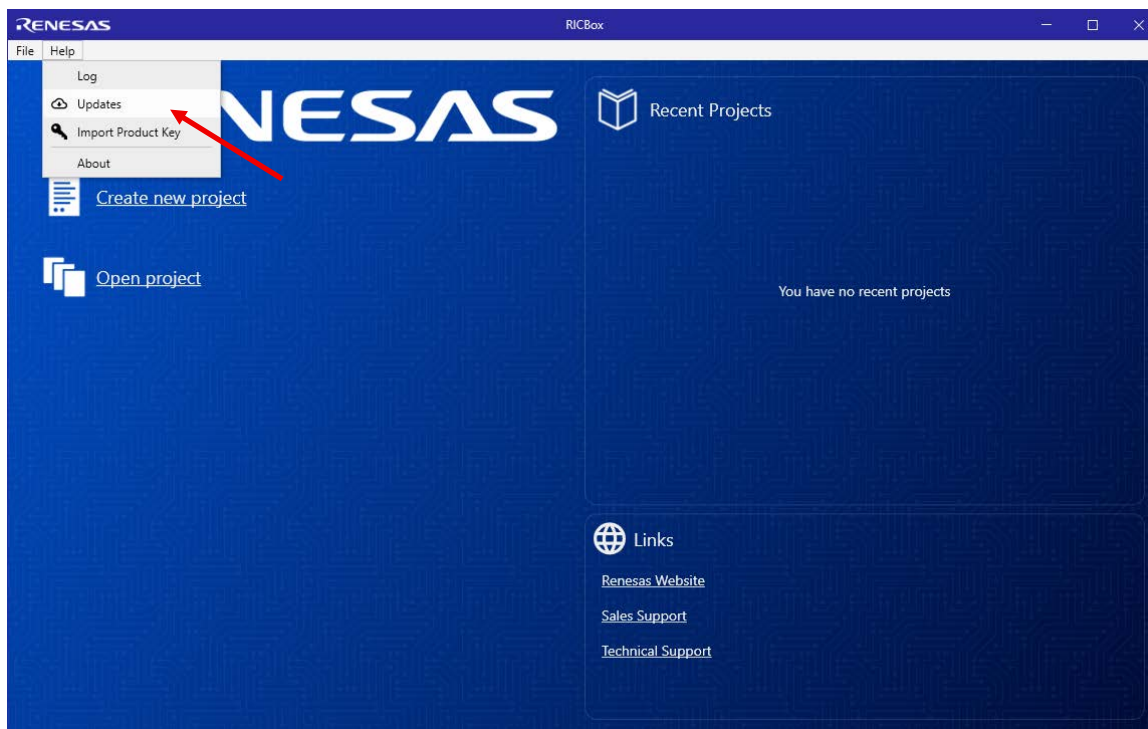
Contents

1. Installation and Setup	2
1.1 Manual installation	4
2. Loading and Creating Configurations	5
2.1 Creating a New Configuration	5
2.2 Loading a Settings File	6
3. Wizard Setup	7
3.1 Inputs	8
3.2 DPLL	9
3.3 Spread Spectrum	10
3.4 Outputs	11
4. Side Panel Buttons	12
5. Overview	12
6. Power View	13
7. Fields View	13
8. Register View	14
9. Diagram View	15
9.1 XIN Block	15
9.2 Clock Inputs Section	15
9.3 APLL Block	16
9.4 DPLL Block	17
9.5 Outputs Block	18
9.6 GPI/GPIO Block	20
10. Device Connection	20
11. Using the Emulator to Capture Register Writes	21
12. Python	24
12.1 Example Script	24
13. Errors and Warnings	25
14. Other Configurable Settings	25
14.1 Changing the I ² C Device Address	25
14.2 DCO mode	26
14.3 Device Startup	26
14.4 EEPROM	27
14.5 OTP	27
15. Revision History	28

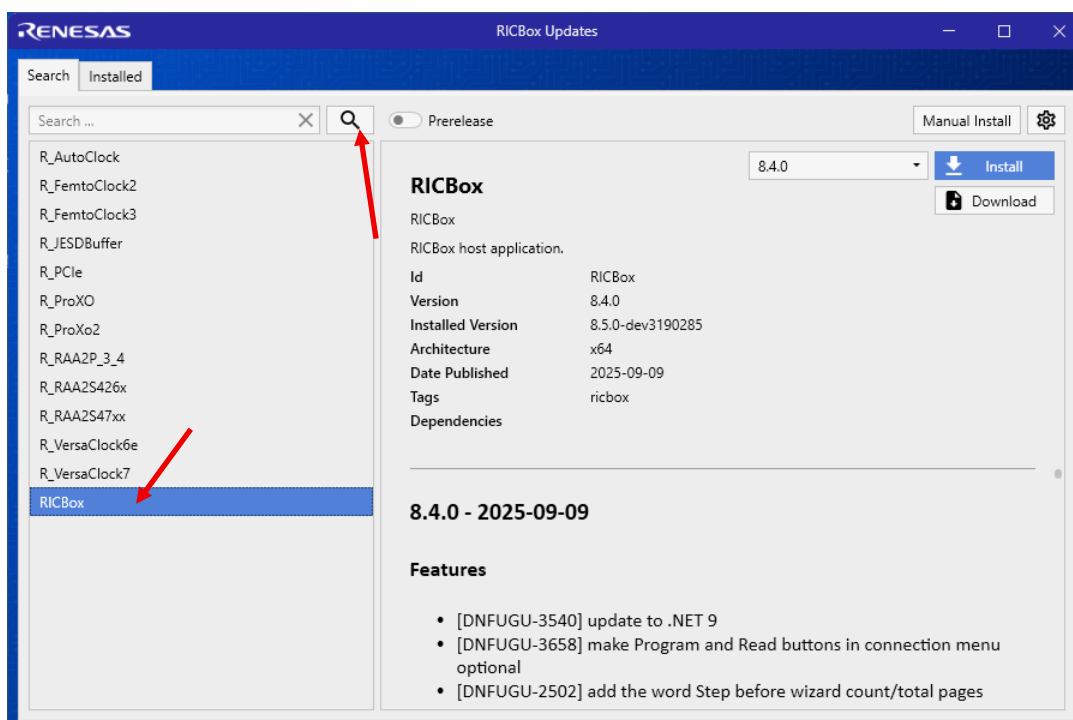
1. Installation and Setup

Ensure that the latest version of the Renesas IC Toolbox software is installed. New versions are released frequently and can provide a better experience with new functionality. The Renesas IC Toolbox software can be downloaded at [RICBox](#) software page. Download the installer and run it. Once installed, the tool will need to be updated thru the built-in updater tool. Prior to updating any RICBox software and/or plugins, please make sure that all instances of RICBox have been shut down. Only **one instance** must be running at the time of update.

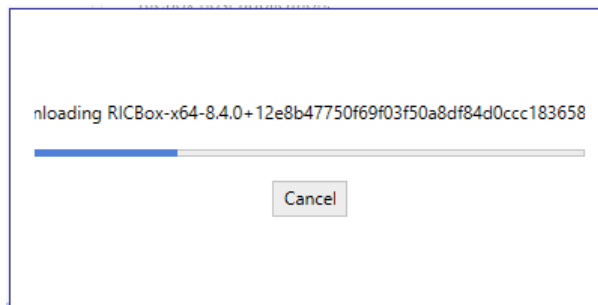
Click on the Help → Updates



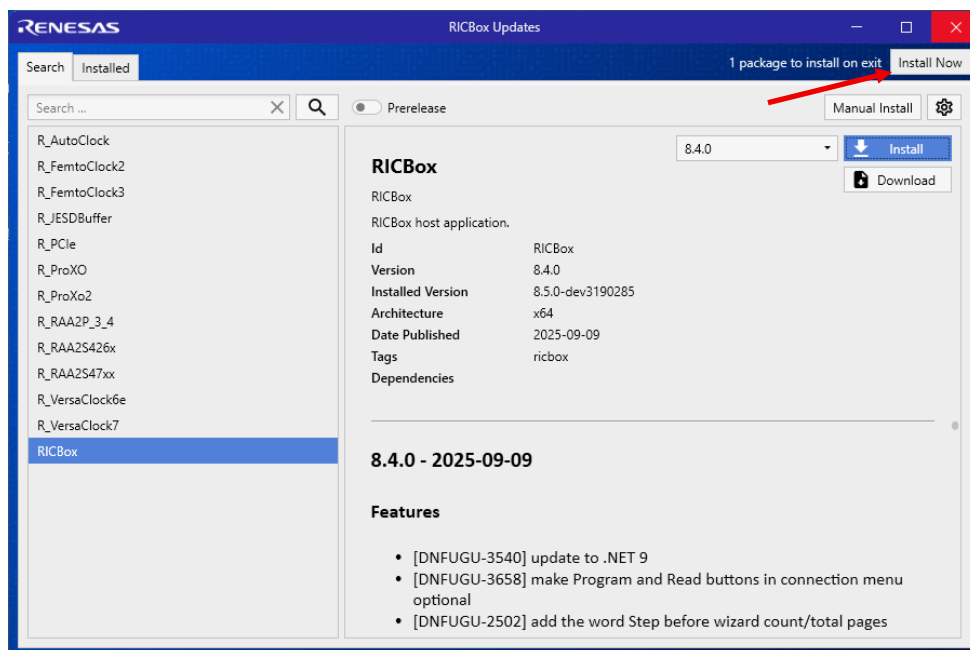
The RICBox Updates window is now visible. Search for “RICBox” on the left side of the search results. Push the  to refresh the list if needed.



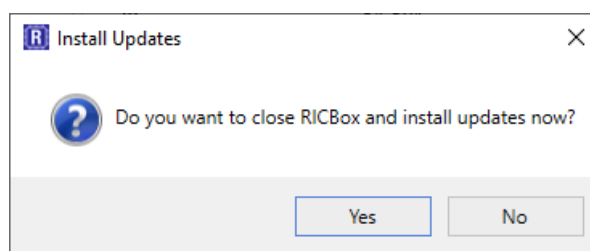
Push the blue  **Install** button to add the latest RICBox software to the download queue.



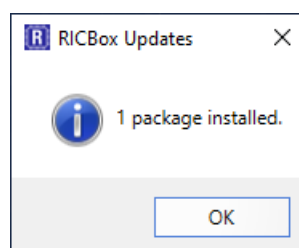
Push the  **Install Now** button to install the update.



RICBox will ask, “Do you want to close RICBox and install updates now?”. Answering Yes will cause RICBox to shut down in order to install the update. RICBox should automatically close and install the update.



If the installation is successful, you will see that the package installed.

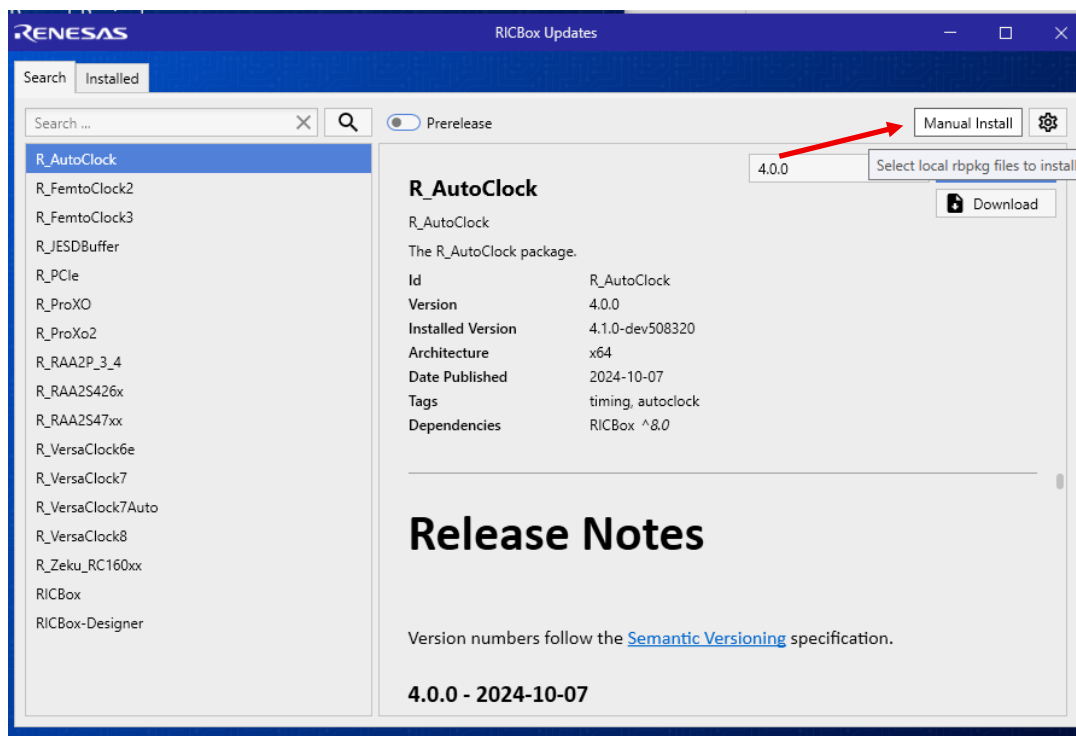


Repeat this process for any of the plugins listed.

1.1 Manual installation

There may come a time when new development versions of RICBox and/or plugins are available but not released yet. Renesas can supply a secure link to download the development software. Once obtained, these files can be manually installed.

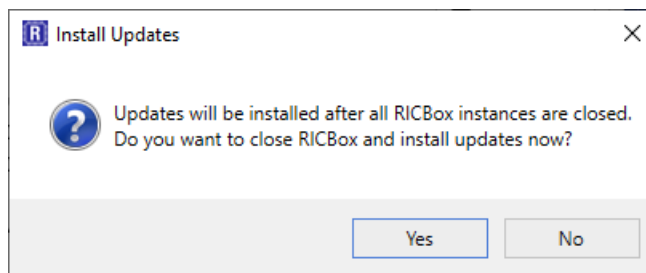
Open the Updates tool by clicking Help → Updates. Next push Manual Install



Navigate to where the development version of the software has been downloaded, select the package, and push Open.

Name	Date modified	Type	Size
Today (2)			
R_VersaClock8-x64-2.1.0-dev510820.rbpkg	7/17/2025 12:42 PM	RBPKG File	25,201 KB
RICBox-x64-8.4.0-dev508228.rbpkg	7/17/2025 12:42 PM	RBPKG File	119,537 KB

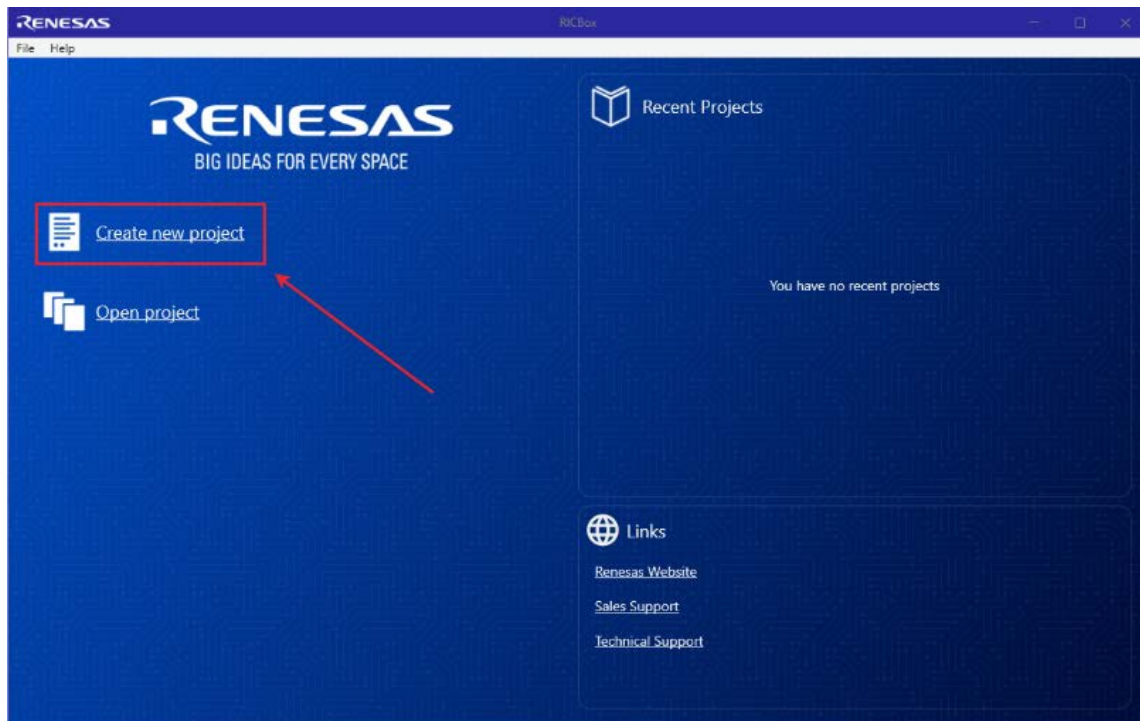
Click Yes and the package file will be installed. Repeat this process for all other rbpkg files. Keep in mind that RICBox packages should always be installed first as there are RICBox version dependencies for plugins.



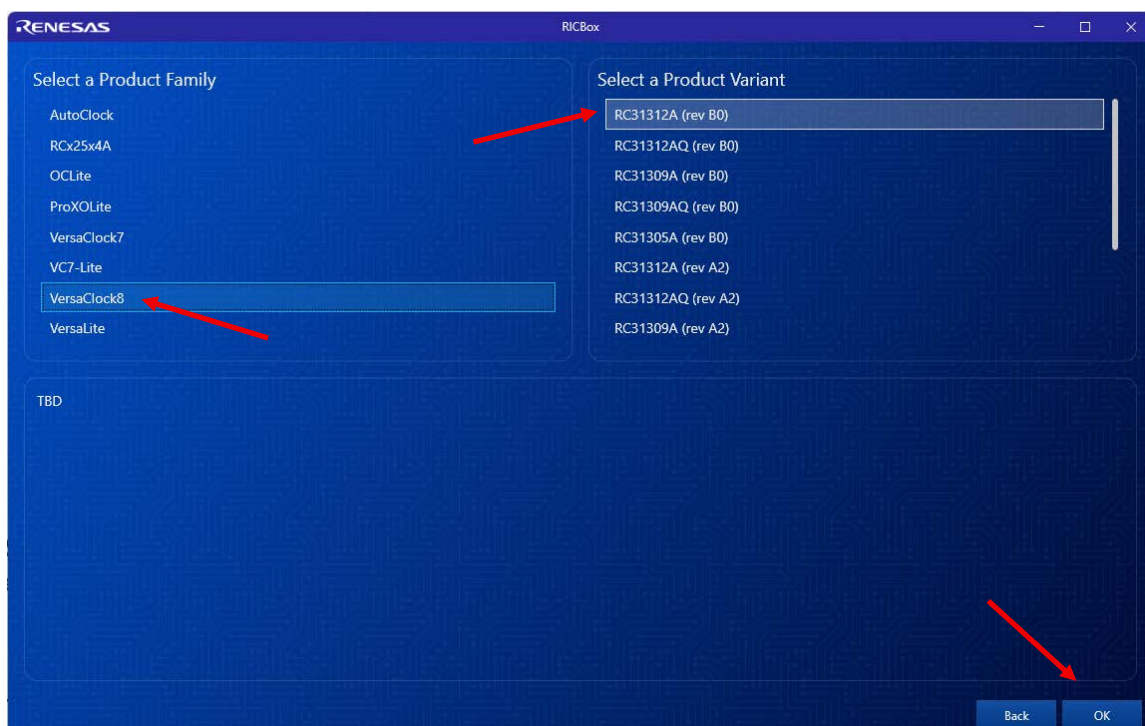
2. Loading and Creating Configurations

2.1 Creating a New Configuration

To create a new configuration, open the Renesas IC Toolbox software and click the *Create new project* button.



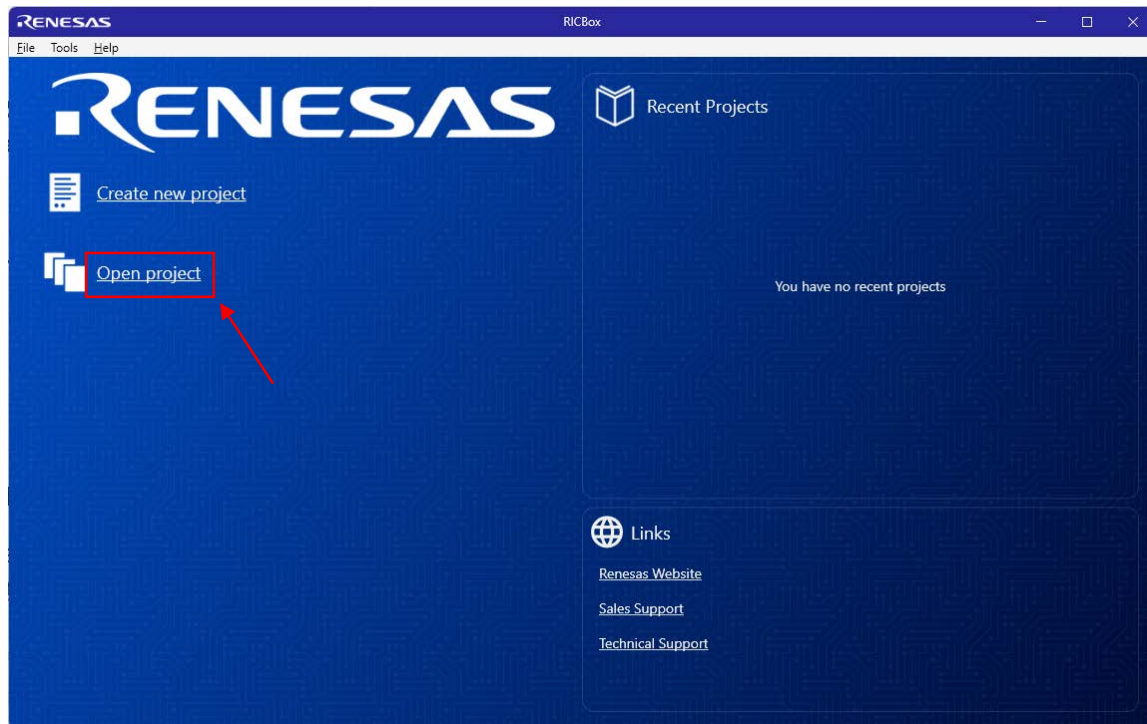
In the “Select Product Family” section, select VersaClock8. From the “Select Product” section, select the working device. Click the *OK* button to open up the new configuration. It may take a couple of minutes to open for the first time.



Note: Some variations between devices may show up in this guide. The intent of this guide is to encompass an overview of the entire device family.

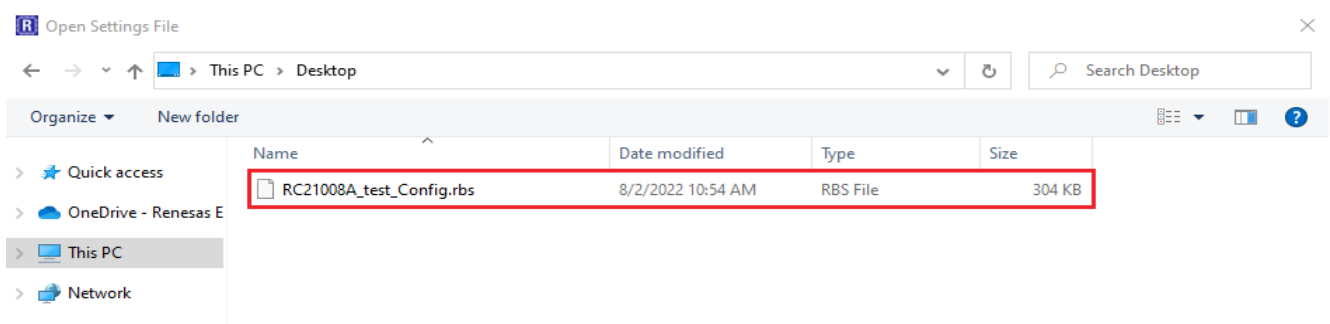
2.2 Loading a Settings File

Loading a settings file is similar to creating a new one. To load an existing settings file, click on the *Open project* button just after opening the Renesas IC Toolbox software. This will open a file browser.



Note: Recently used settings files are under the “Recent Projects” section.

Navigate to the directory that stores the settings file and select it. Renesas IC Toolbox settings files have the file type ‘.rbs’.



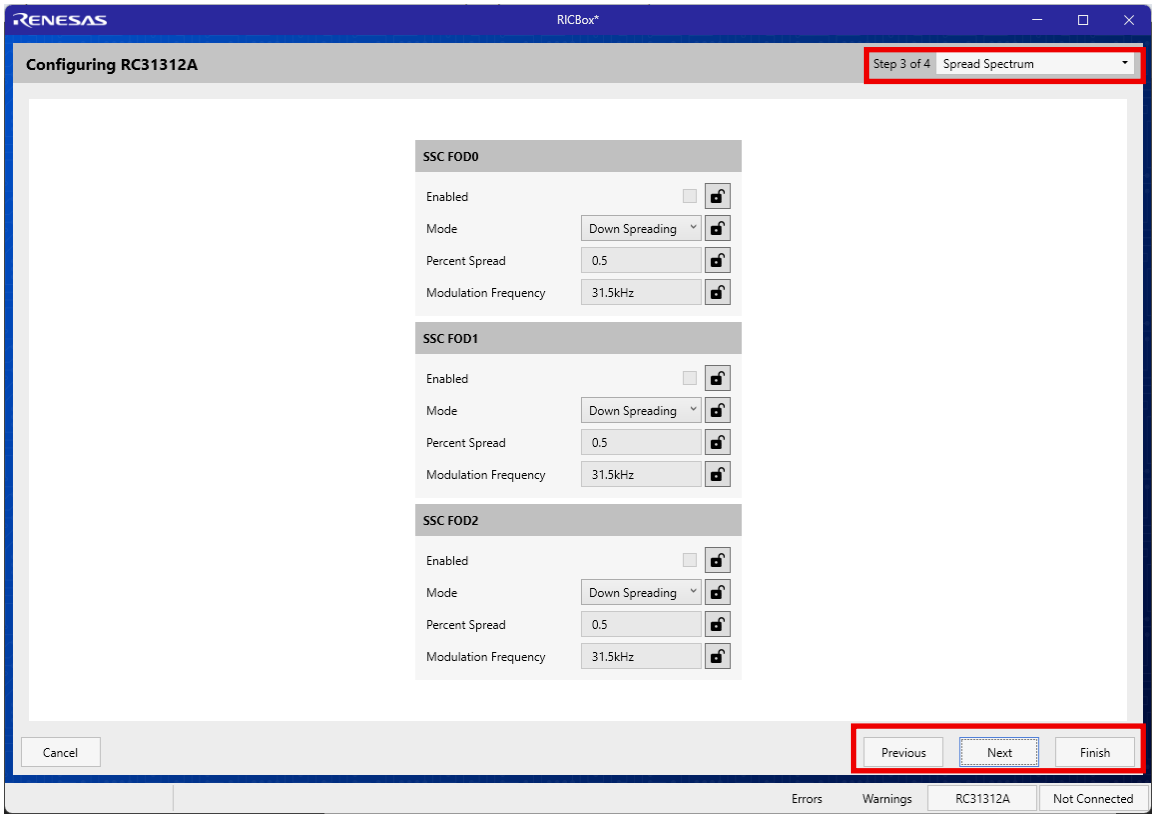
After pushing ‘Open’, you will come to an interim window. By clicking the triangle next to the Advanced text you will see the Part Number and the Hardware Revision. If you have an A2 rev rbs file and want to **migrate** to B0 rev, update the Hardware Revision to ‘B0’. Push ‘Open’ when ready.



3. Wizard Setup

When creating a new configuration, the wizard page will be the first screen to appear. For VersaClock 8 devices, there are four separate wizard pages: **Inputs**, **DPLL**, **Spread Spectrum**, and **Outputs**. Each section pertains to a different portion of the device that needs to be configured for proper functionality.

Navigation to individual sections can be performed by using the *Next* and *Previous* buttons in the lower right corner of the screen or the drop-down menu in the upper right. Select the *Finish* button to enter the control panel page.



3.1 Inputs

There are two sections to make note of when configuring the inputs: **Crystal** and **Reference Clocks**. The Crystal section is used when creating a configuration that is either in synthesizer mode and uses a clock at the XIN pin, or in any Jitter Attenuator mode. The same applies for the CLKIN section. Device mode is through the “Operation Mode” dropdown menu. Device modes include **Synthesizer**, **Jitter Attenuator**, and **DCO**.

Descriptions of each mode can be found on the right-side panel of the page.

The screenshot displays the configuration interface for the VersaClock 8, divided into two main sections: **Crystal** and **Reference Clocks**.

Crystal Section:

- Operation Mode:** A dropdown menu set to "Synthesizer" with a lock icon. A red arrow points to this dropdown with the label "Change Operation Mode".
- Frequency:** A text field set to "54MHz" with a lock icon.
- XIN Pin Overdriven:** A checkbox that is currently unchecked with a lock icon.
- XIN Cap:** A dropdown menu set to "0.75pF" with a lock icon.
- XOUT Cap:** A dropdown menu set to "0.75pF" with a lock icon.

A red bracket groups the Frequency, XIN Cap, and XOUT Cap fields with the label "Set XIN frequency and crystal load capacitance".

Reference Clocks Section:

- CLKIN0:** A dropdown menu set to "None" with a lock icon.
- CLKIN0b:** A dropdown menu set to "None" with a lock icon.
- CLKIN1:** A dropdown menu set to "None" with a lock icon.
- CLKIN1b:** A dropdown menu set to "None" with a lock icon.

Each of these four dropdowns has a "DISABLED" status indicator and a lock icon to its right. A red bracket groups these four fields with the label "Set CLKIN type and frequency".

3.2 DPLL

If the device is configured for jitter attenuator mode, the DPLL section will become available. The DPLL section enables manual adjustment of the bandwidth, decimator, gain peaking, and phase slope limit values. Alternatively, there's the option to select a predefined SyncE profile that will automatically populate the adjustable settings. Descriptions of each section and the SyncE profiles are on the right of the page.

DPLL Profile Synchronizer 

Typical Jitter Attenuation settings

Bandwidth

Normal Bandwidth Goal 25Hz 

Actual: ~24.8045Hz (-0.7822% from goal of 25Hz)

Acquire Bandwidth Goal 250Hz 

Actual: ~248.0446Hz (-0.7822% from goal of 250Hz)

Decimator

Decimator Bandwidth Goal 2.5kHz 

Actual: None

Gain Peaking

Normal Gain Peaking Goal 0.2 

Actual: ~0.1935 (-3.2523% from goal of 0.2)

Acquire Gain Peaking Goal 0.2 

Actual: ~0.1896 (-5.1977% from goal of 0.2)

Phase Slope Limit

Normal Phase Slope Limit Goal None  ns/sec

Actual: ~67.8158μs

Acquire Phase Slope Limit Goal None  ns/sec

Actual: ~67.8158μs

3.3 Spread Spectrum

The spread spectrum section enables spectrum spreading on either **FOD0**, **FOD1**, **FOD2**, or **simultaneously**. The mode for the spread spectrum engine can be set to down spreading or center spreading. The modulation frequency and the percent spread can also be configured in this section.

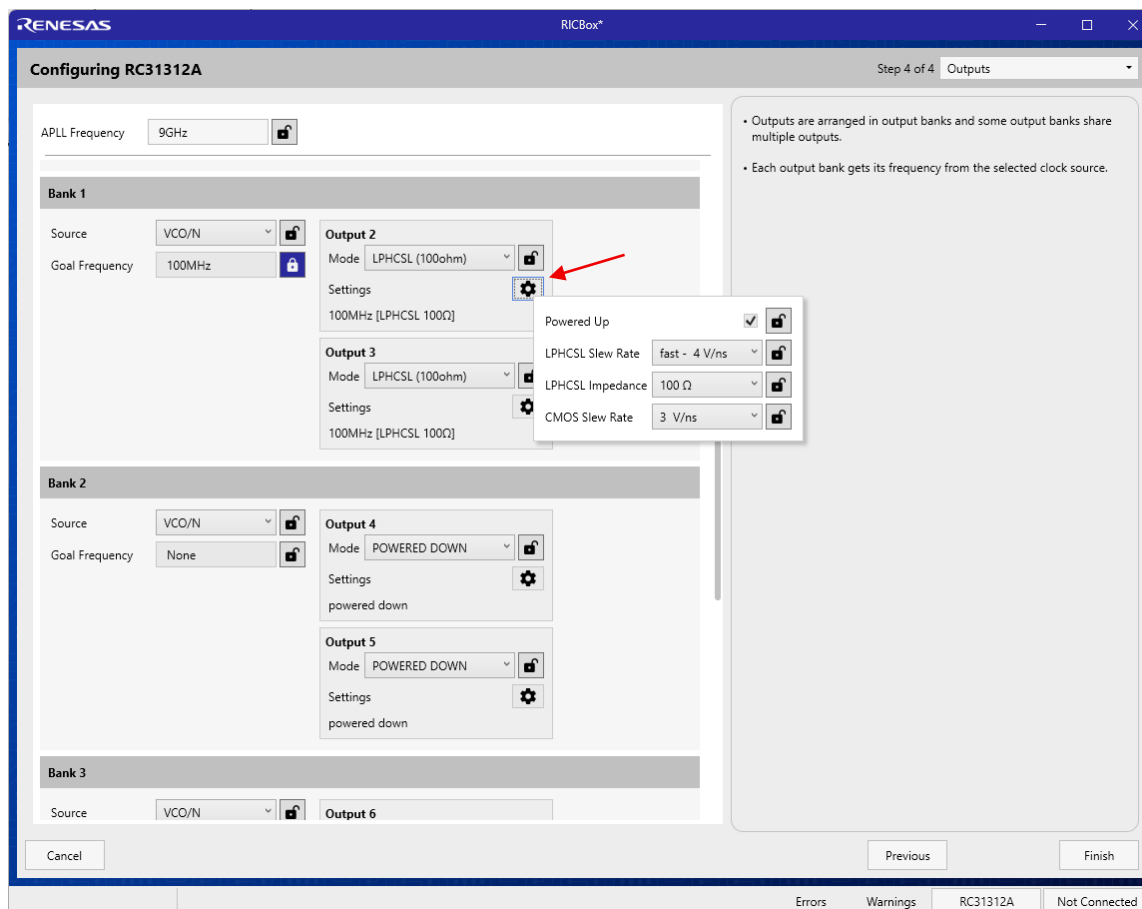
SSC FOD0	
Enabled	☒ 
Mode	Center Spreading... 
Percent Spread	0.5 
Modulation Frequency	31.5kHz 

SSC FOD1	
Enabled	☐ 
Mode	Down Spreading... 
Percent Spread	0.5 
Modulation Frequency	31.5kHz 

SSC FOD2	
Enabled	☐ 
Mode	Down Spreading... 
Percent Spread	0.5 
Modulation Frequency	31.5kHz 

3.4 Outputs

The outputs section enables setting the output frequencies and adjusting the overall VCO frequency. Outputs can be further configured by clicking on the symbol next to the output field. This gives the ability to enable/disable the output, select the output type, and adjust the signal settings.



4. Side Panel Buttons

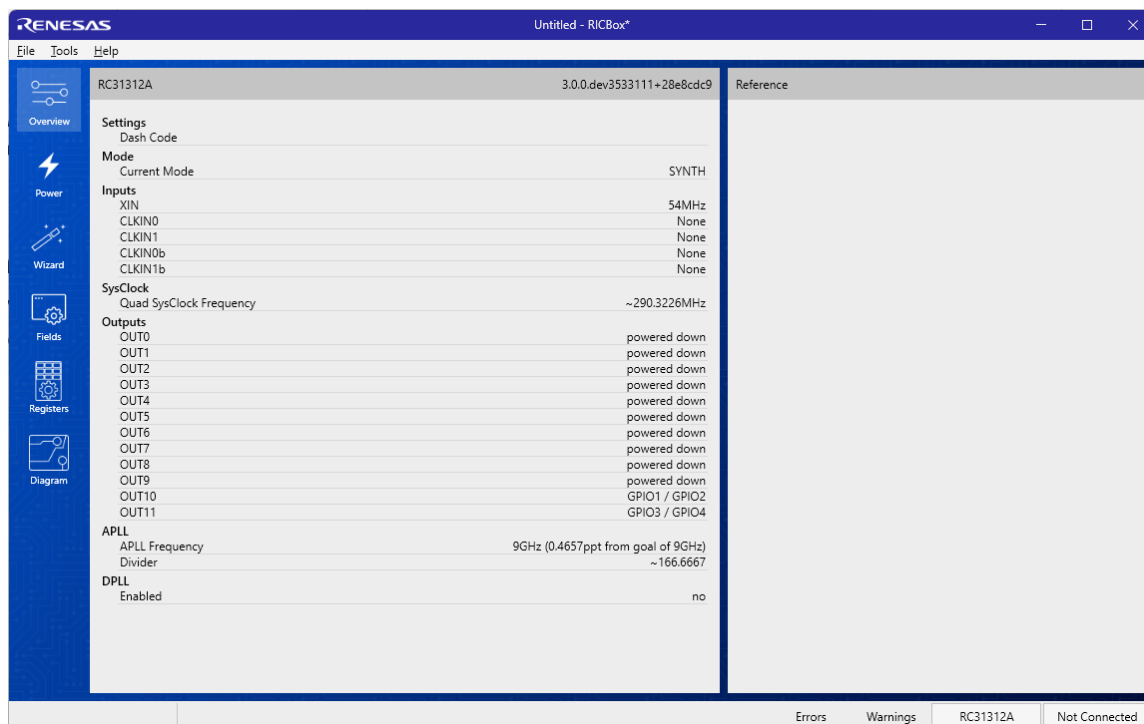
The side panel consists of five separate buttons. Each button opens a separate page. Each page has a unique view, allowing the configuration of the device from different perspectives.

- **Overview** button opens the device overview page.
- **Power** button displays the estimated power drawn from the currently selected config.
- **Wizard** button opens the initial wizard page.
- **Fields** button displays the register settings in a readable text format with a search engine.
- **Registers** button shows a graphic of the registers in the device.
- **Diagram** button opens a configurable block diagram view.



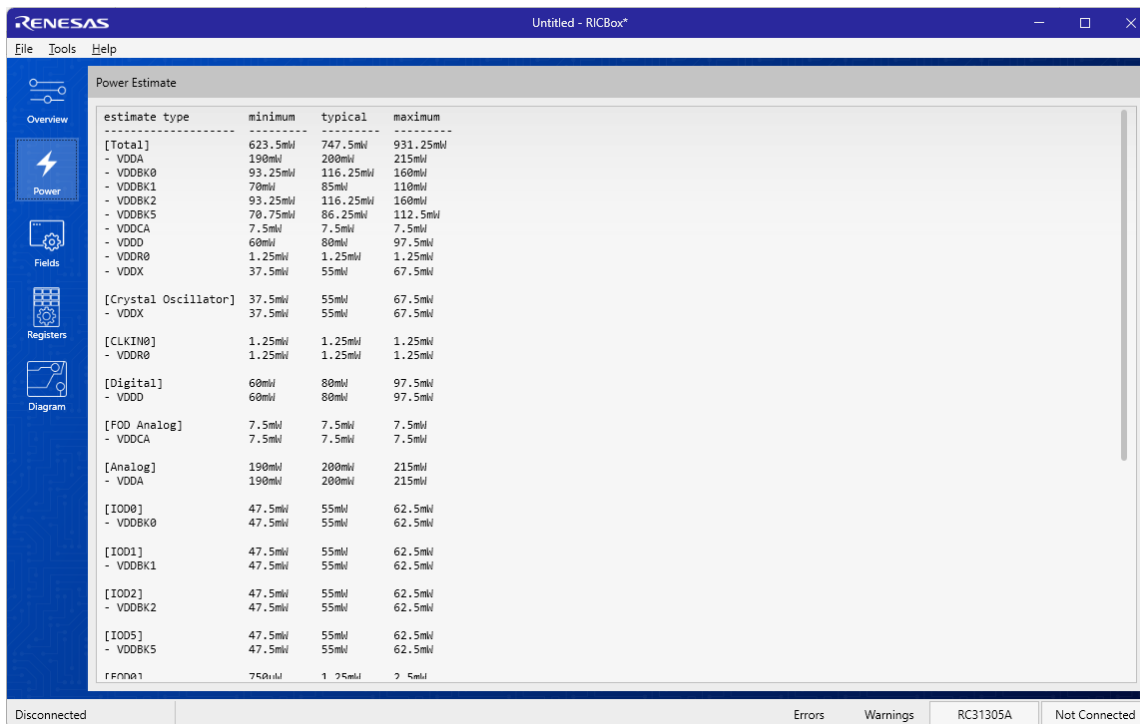
5. Overview

The overview displays a summary page depicting the major settings for the device. This page can be used as an important reference for the overall device configuration.



6. Power View

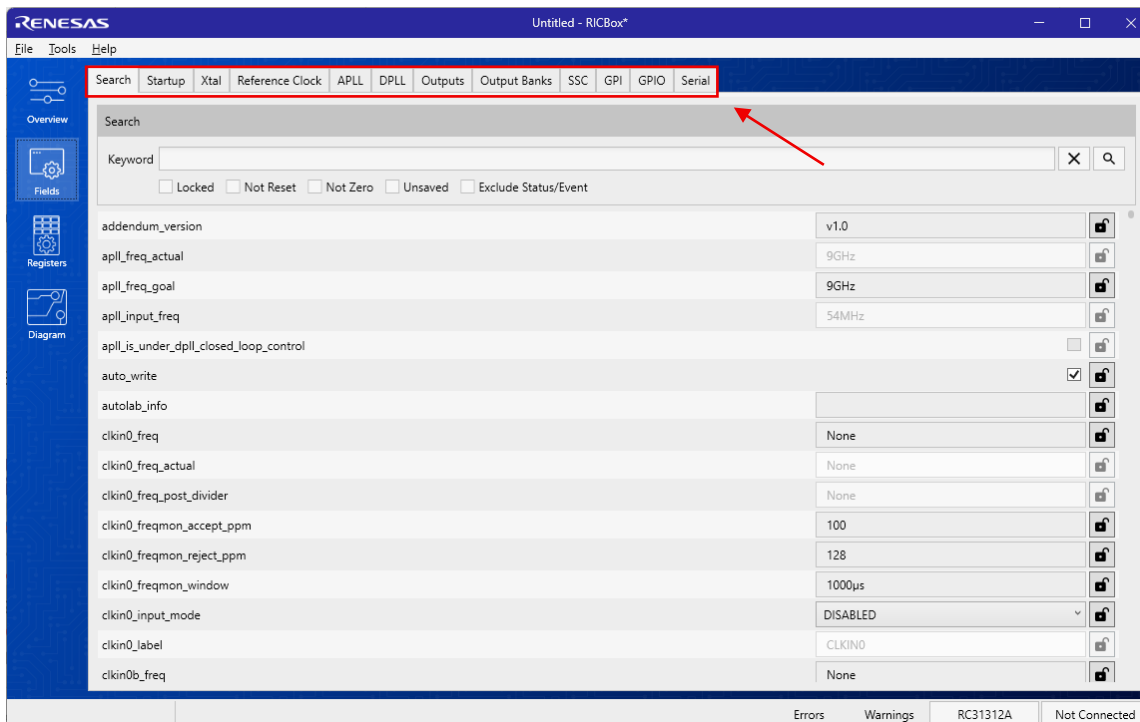
The Power View provides an estimate how much power the current configuration will draw. Expected VDD must be known ahead of time for the estimator to work.



estimate type	minimum	typical	maximum
[Total]	623.5mW	747.5mW	931.25mW
- VDDA	190mW	200mW	215mW
- VDDBK0	93.25mW	116.25mW	160mW
- VDDBK1	70mW	85mW	110mW
- VDDBK2	93.25mW	116.25mW	160mW
- VDDBK5	70.75mW	86.25mW	112.5mW
- VDDCA	7.5mW	7.5mW	7.5mW
- VDD	60mW	80mW	97.5mW
- VDDR0	1.25mW	1.25mW	1.25mW
- VDDX	37.5mW	55mW	67.5mW
[Crystal Oscillator]	37.5mW	55mW	67.5mW
- VDDX	37.5mW	55mW	67.5mW
[CLKIN0]	1.25mW	1.25mW	1.25mW
- VDDR0	1.25mW	1.25mW	1.25mW
[Digital]	60mW	80mW	97.5mW
- VDD	60mW	80mW	97.5mW
[FDD Analog]	7.5mW	7.5mW	7.5mW
- VDDCA	7.5mW	7.5mW	7.5mW
[Analog]	190mW	200mW	215mW
- VDDA	190mW	200mW	215mW
[I000]	47.5mW	55mW	62.5mW
- VDDBK0	47.5mW	55mW	62.5mW
[I001]	47.5mW	55mW	62.5mW
- VDDBK1	47.5mW	55mW	62.5mW
[I002]	47.5mW	55mW	62.5mW
- VDDBK2	47.5mW	55mW	62.5mW
[I005]	47.5mW	55mW	62.5mW
- VDDBK5	47.5mW	55mW	62.5mW
RFNN01	750mW	1.25mW	2.5mW

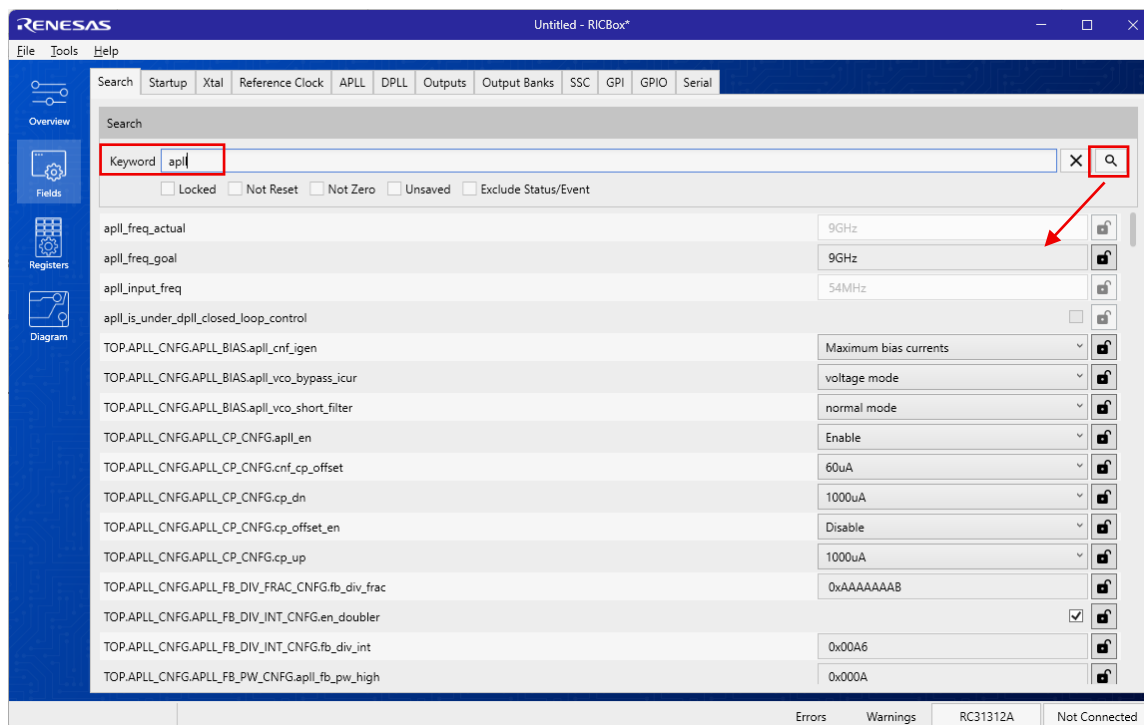
7. Fields View

The Fields view enables easy movement through register settings via the tabs at the top of the page. Each section has all of the critical registers and data fields listed to configure the device block.



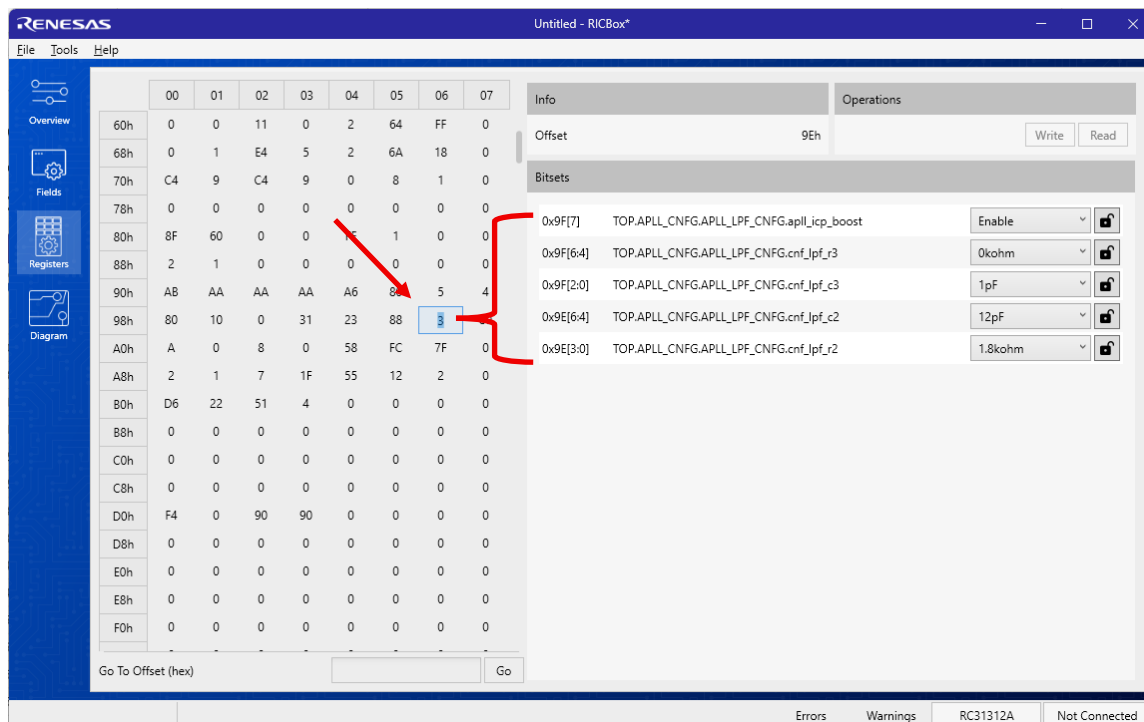
Field	Value
addendum_version	v1.0
apll_freq_actual	9GHz
apll_freq_goal	9GHz
apll_input_freq	54MHz
apll_is_under_dpll_closed_loop_control	☐
auto_write	☒
autolab_info	
clk0_freq	None
clk0_freq_actual	None
clk0_freq_post_divider	None
clk0_freqmon_accept_ppm	100
clk0_freqmon_reject_ppm	128
clk0_freqmon_window	1000µs
clk0_input_mode	DISABLED
clk0_label	CLKIN0
clk0b_freq	None

The search tab provides access to the configurable fields through a search bar. The search engine can be used to find any specific configurable field.



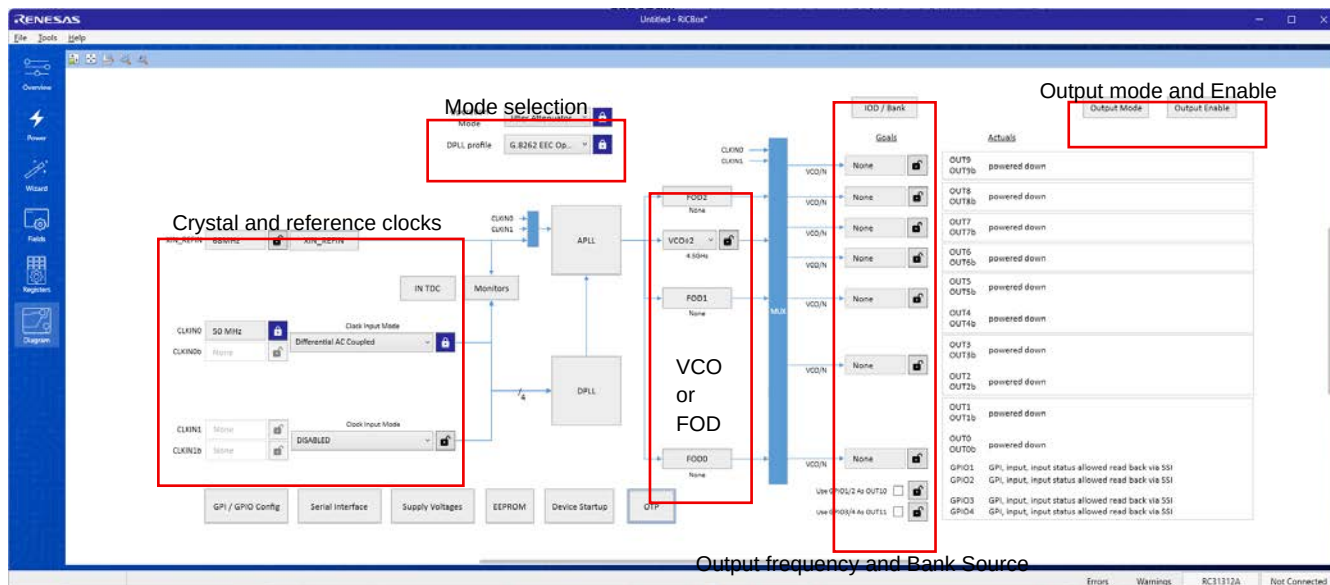
8. Register View

The register view shows a graphical diagram of the registers and enables reading or writing any of the individual registers. By clicking on the individual register block, the given registers for that block will appear to the right. They can either be adjusted by writing directly to the diagram or entering values into the data fields on the right.



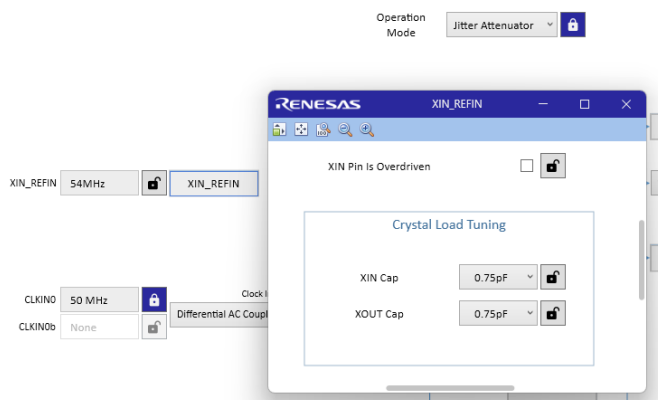
9. Diagram View

The block diagram view reflects the datasheet representation of the VersaClock8 devices. The main diagram enables adjustment of the operation mode, setting the output frequency and type, changing the output divider, setting the Xin frequency and the input frequency, and viewing the output frequency estimate. Each block has its own pop-out page. This can be accessed by clicking on the block.



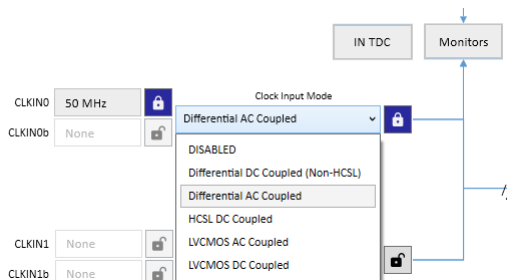
9.1 XIN Block

Clicking on the *XIN_REFIN* block gives access to the settings that configure the Xin frequency and internal tuning capacitors.

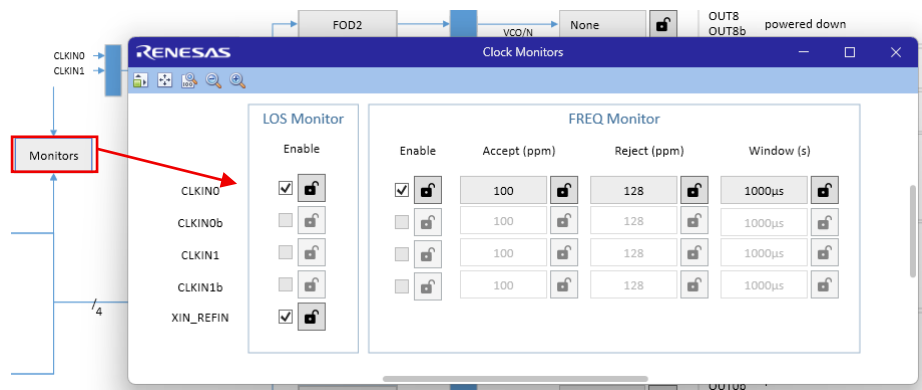


9.2 Clock Inputs Section

Clicking on the Clock Input Mode box allows setting the input signal type.

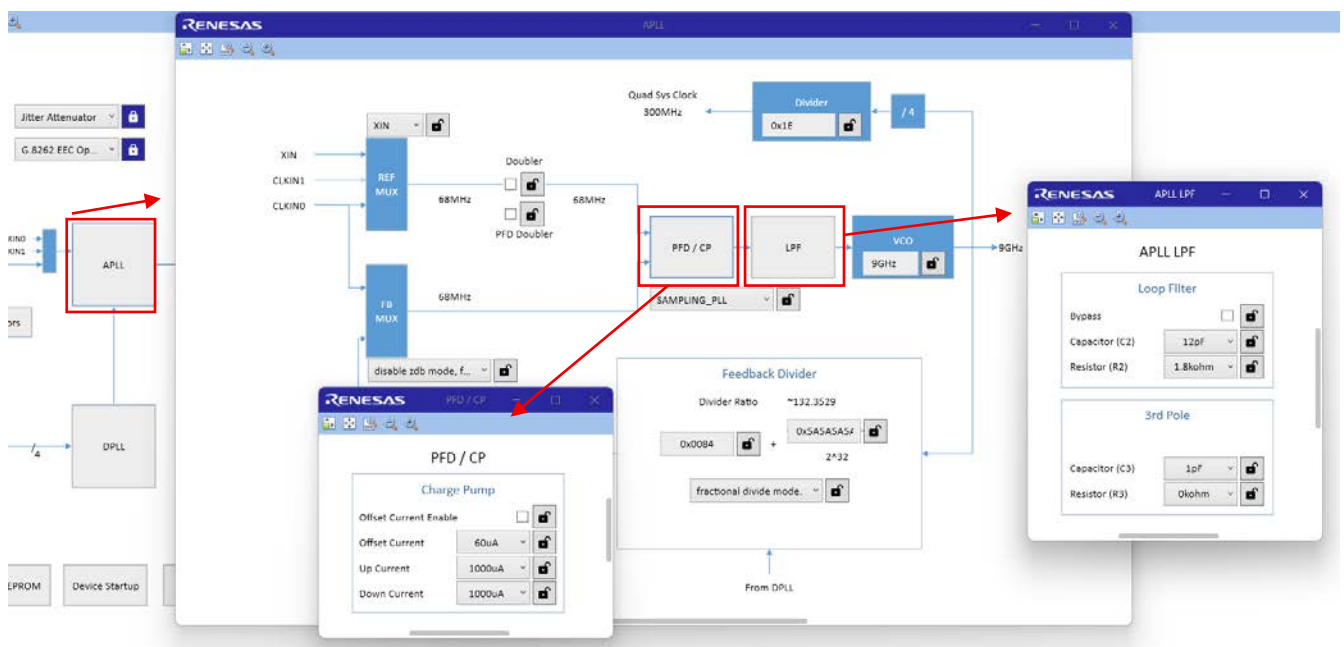


The monitors block can be used to configure the LOS and Frequency monitors.



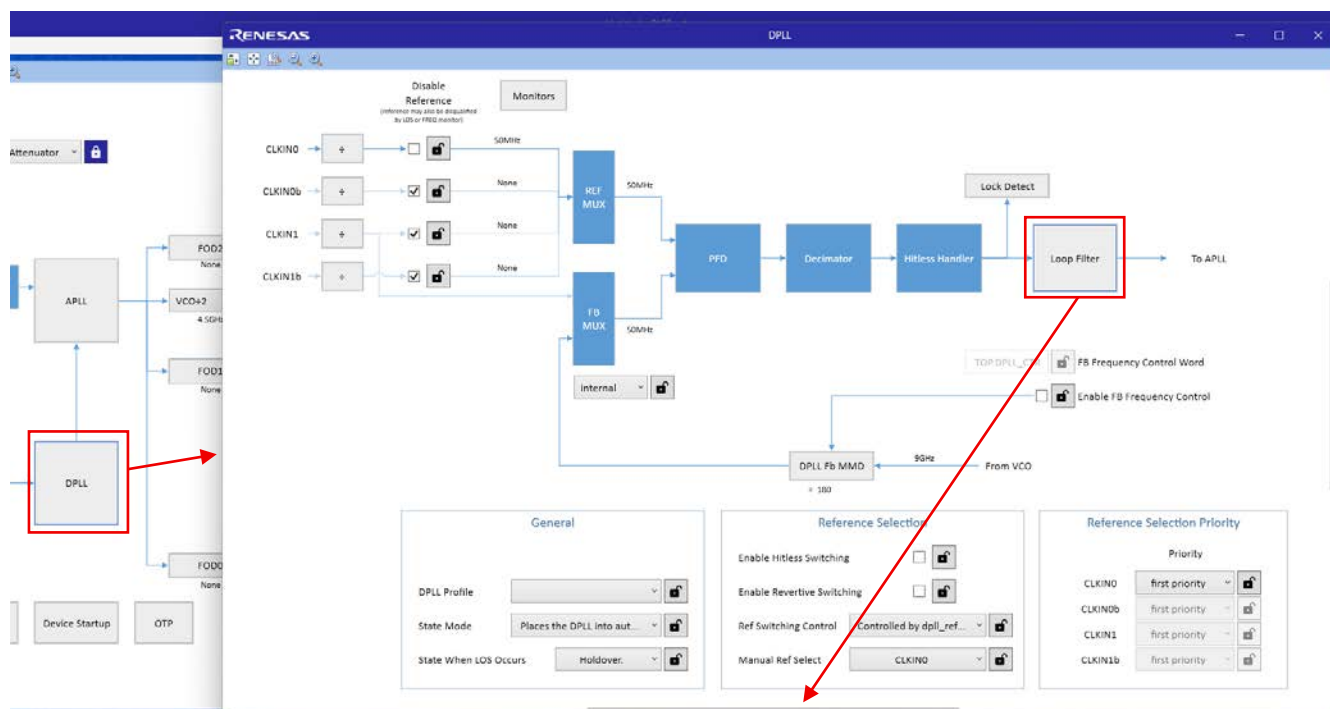
9.3 APLL Block

Clicking on the APLL block enables configuration of the input mux, charge pump settings, and internal loop filter settings. The VCO frequency and the Feedback Divider value can also be changed from here.



9.4 DPLL Block

The *DPLL* block is only accessible when the device operation mode is set to “Jitter Attenuator”. This block contains all features pertaining to the DPLL. Clicking on the *DPLL* block enables revertive or hitless switching, adjustment of the phase offset, and the ability to change the digital loop filter settings.

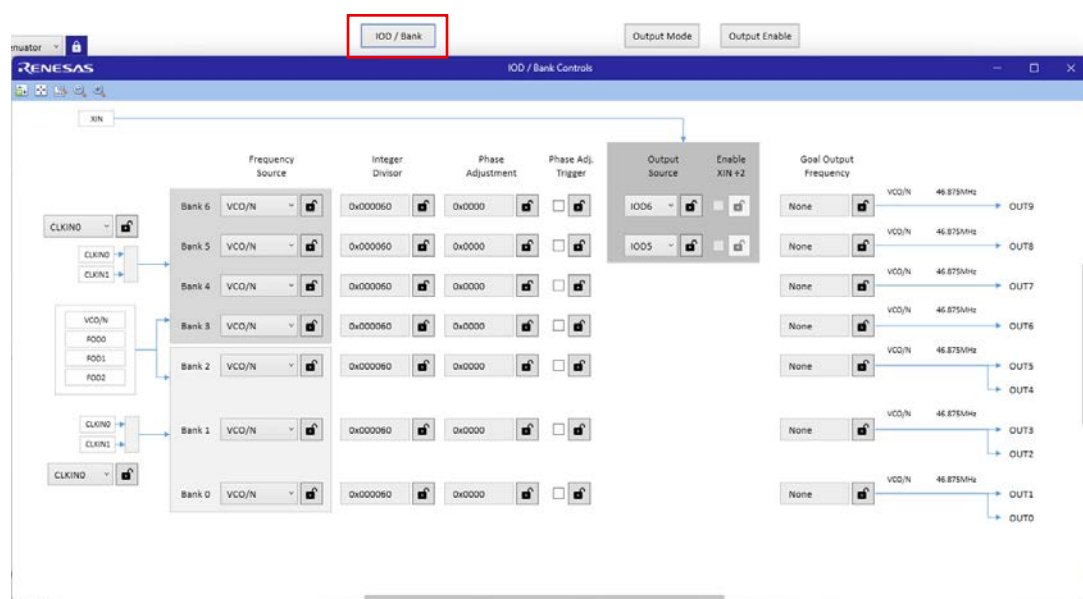


The screenshot displays the DPLL Loop Filter configuration window. It shows two tabs: 'Normal' and 'Acquire'. Each tab has three sections: 'Bandwidth', 'Gain Peaking', and 'Phase Slope Limit (ns/s)'. The 'Normal' tab shows goals and actual values for these parameters. The 'Acquire' tab shows the same parameters with different values. A checkbox 'Use Acquire setting when DPLL is in acquire state' is checked.

Parameter	Goal	Actual
Bandwidth	25 Hz	~24.4926Hz
Gain Peaking	0.2	~0.1957
Phase Slope Limit (ns/s)	7000	~7.0004μs

9.5 Outputs Block

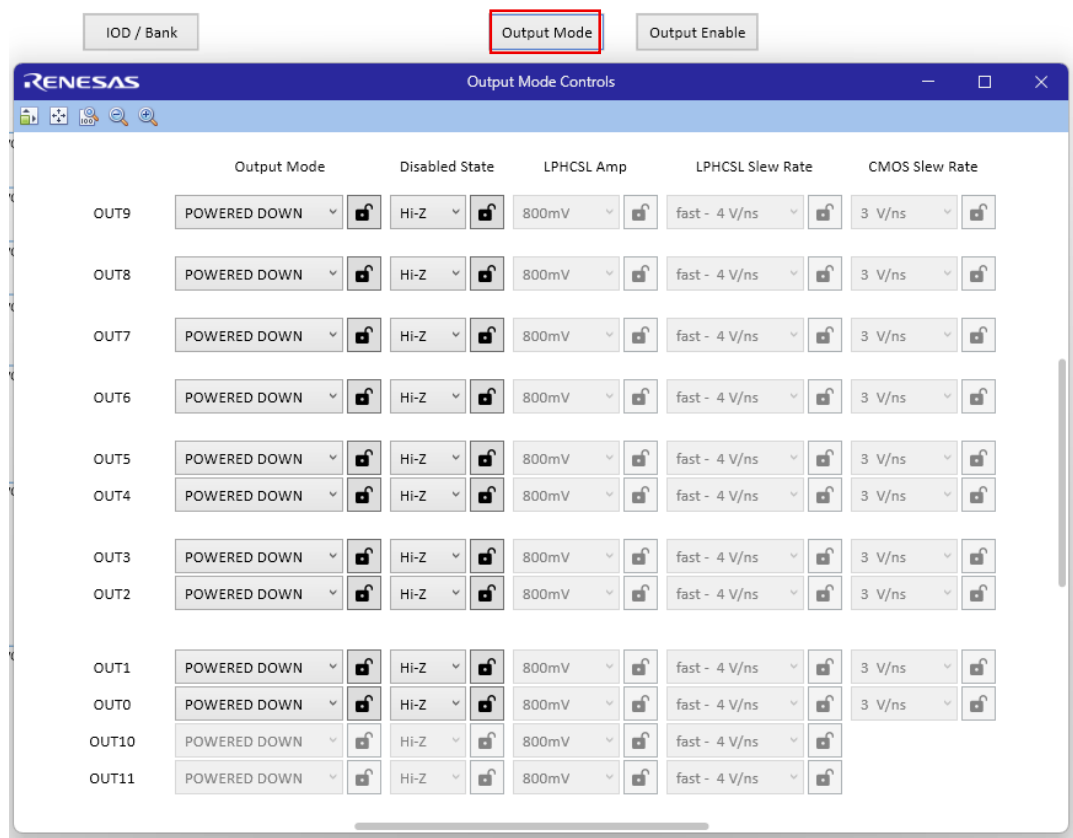
Each output can be configured for frequency and source by clicking on the *IOD/Bank* button on the main diagram.



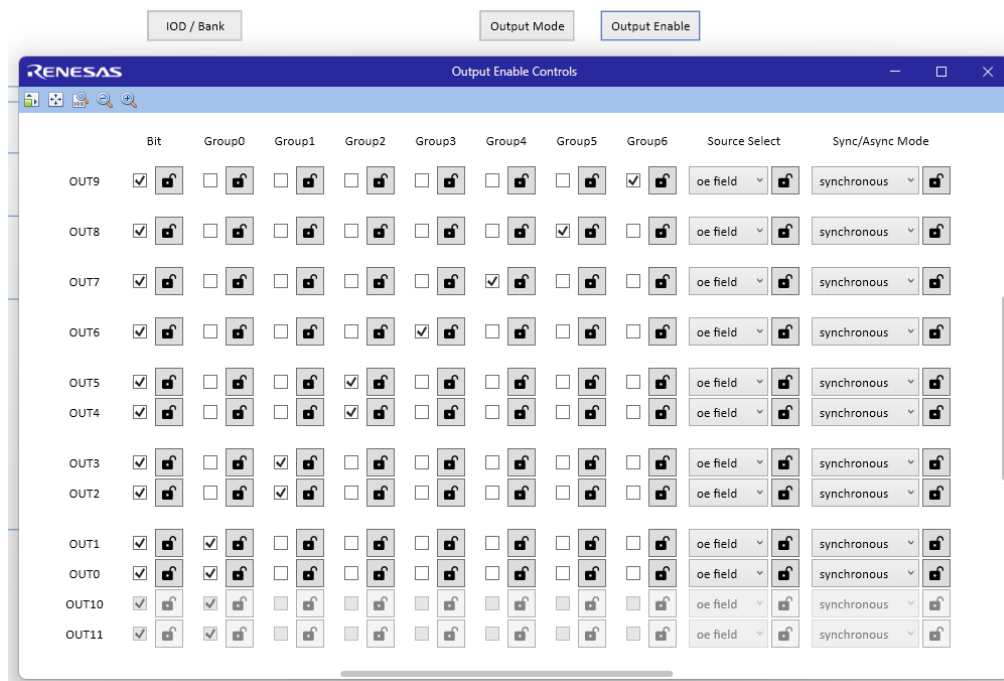
If a source is selected to be from an FODx, be sure to also configure the respective FOD block.



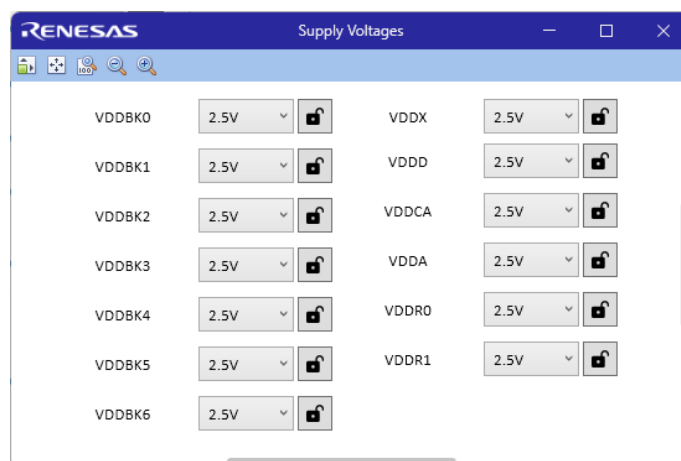
Each output mode can be set by pushing the Output Mode button on the main diagram.



Each output enable can be configured by pushing the Output Enable button on the main diagram.

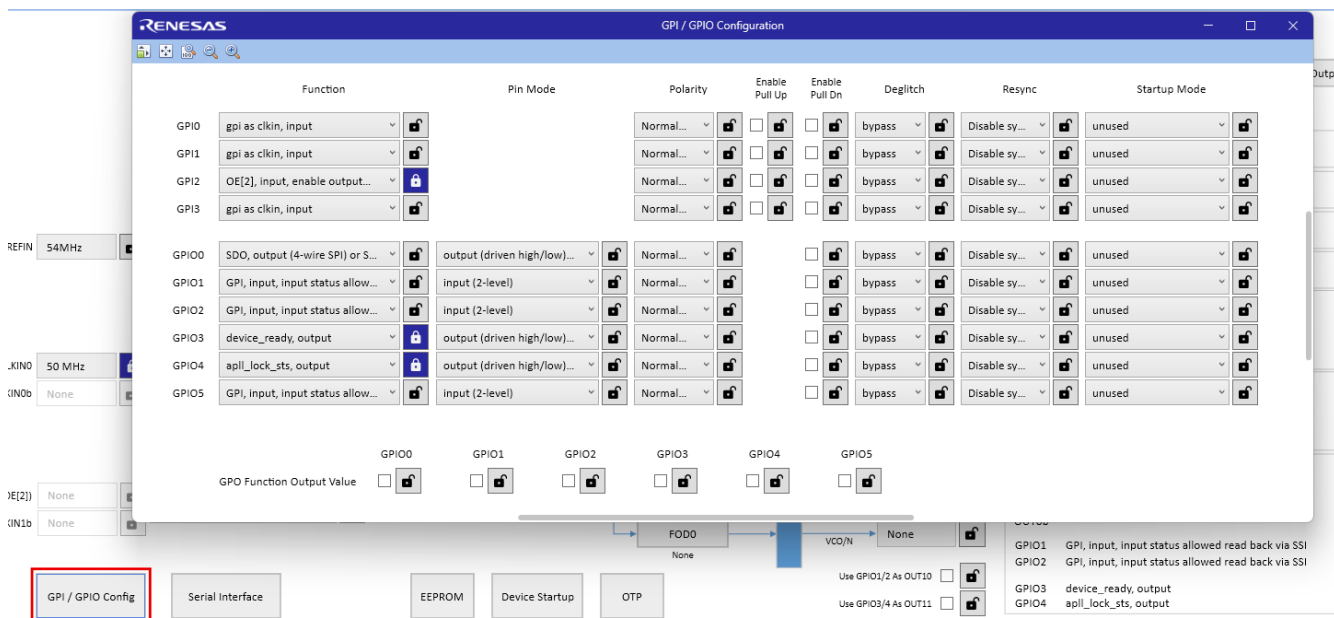


Be sure to set the expected VDD voltage. VersaClock 8 supports 1.8V, 2.5V, and 3.3V operation.



9.6 GPI/GPIO Block

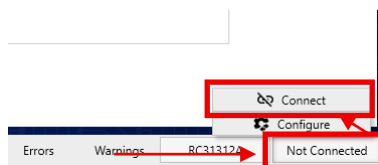
Clicking on the *GPI/GPIO* block enables configuration of the input functionality, enable/disable pull-up/pull-down, and enable/disable inversion.



10. Device Connection

Device connection can be achieved through the bottom right corner of every page. To connect one of the Renesas evaluation boards, ensure the device is powered and connected to the working computer. Then, click the *Not Connected* button in the corner of the screen. This will lead to a small pop-out page. Click the connect symbol in the corner of the page to establish a connection to the device.

See the *Evaluation Board User Manual* for more information regarding device connection. This manual is located on the **VersaClock 8 Evaluation Kit** page.

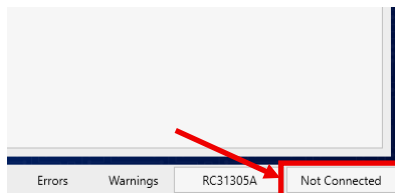


By Default, all VC8 devices are configured as SPI 3W, 2 byte addressing. GPIO0 is setup as SDIO. When configured as I2C, default address is 0x58.

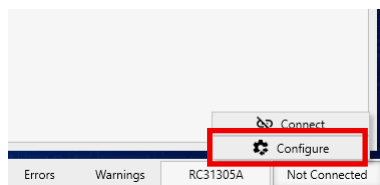
11. Using the Emulator to Capture Register Writes

RICBox has an emulator feature that is used to simulate a connection the device. This feature is useful for capturing register write sequences when combined with the use of the RICBox log.

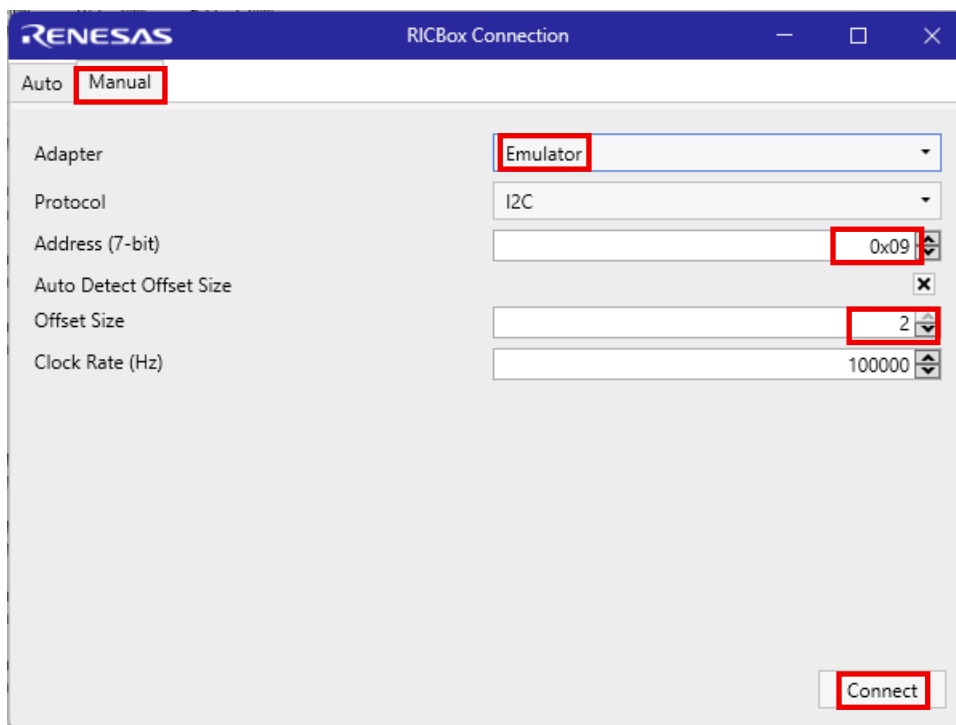
Click the “Not Connected” button in the corner of the screen. The Connect/Configure pop-out page appears



Click on the “Configure” button to open the RICBox Connection settings sub diagram



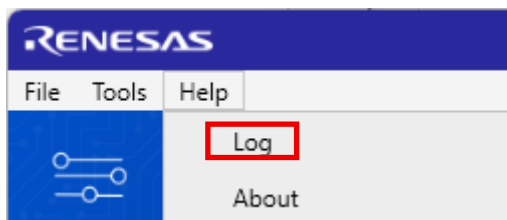
Select the “Manual” tab to see all the emulator settings. Set the “Adapter” field to Emulator, set address to 0x09, and offset size to 2. Push “Connect” when ready.



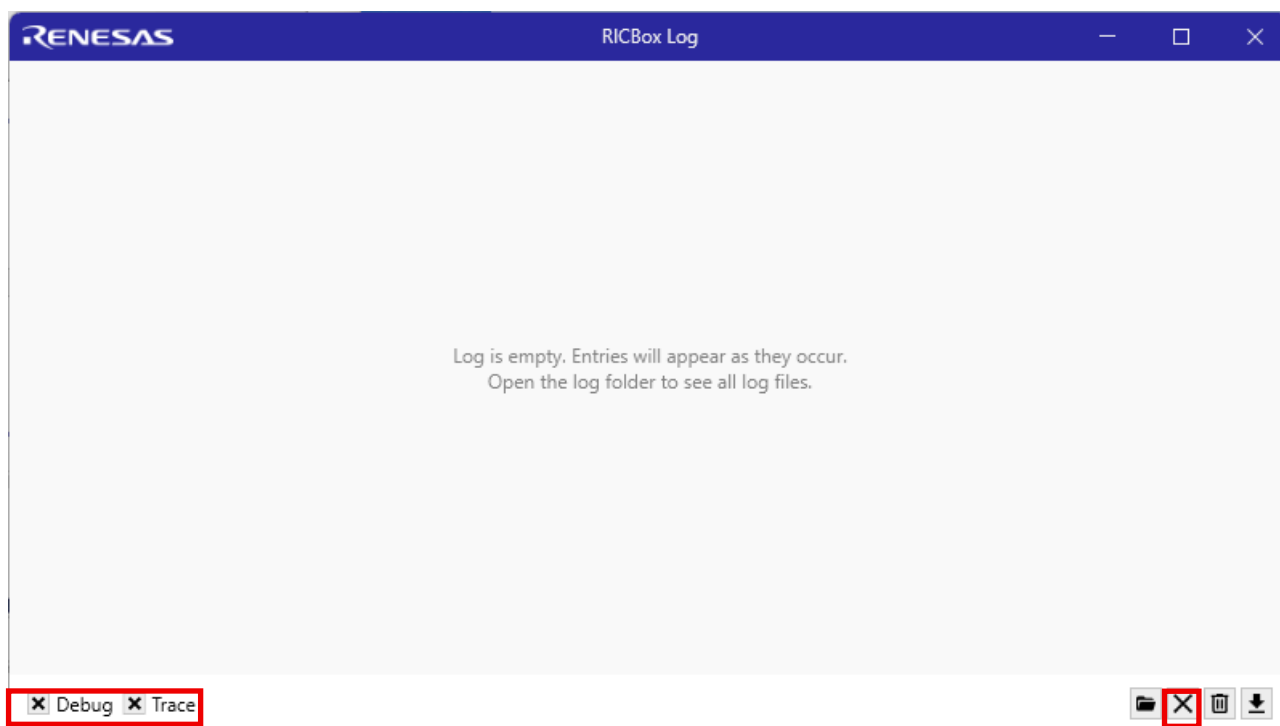
RICBox now shows that it is connect to a device. However, when using the Emulator, RICBox only thinks it is connected to a device.



Go to the Help menu and click the Log



Ensure that the Debug and Trace checkboxes are selected in the bottom left corner of the log window. The log window can be cleared by pushing the “X” in the bottom right corner.



When a change is made to the GUI while the log window is open, the necessary register writes to make the changes are printed to the log. This is due to RICBox being connected to a device and any changes are written to that device in real-time. When using the emulator, RICBox thinks that there is a device to write to, so it sends the necessary write sequences that would be used to program the changes to a device. Use the mouse to select the log contents, then cop/paste them into a text editor.

For this example, bank1 frequency was changed to 156.25MHz. The frequency into the divider is 5 GHz, therefore the divider is now set to 32 (0x20). Looking at the log window, we see that address is 0x58. This value is the VC8 I2C address. The offset is 0x188. The register that contains the IOD divider can be found at 0x188. The data is 20 00 00 00 and of length 4 bytes. The values listed are byte reversed. The data to write is 0x00000020.

- WRITE 0x188 0x00000020



When adjusting other fields, it is possible that multiple I2C transactions will be needed to achieve the end goal. All those register writes will be shown in the log window.

If the emulator was started with offset size set to 1 byte, then the log would display an extra write to the page register (offset – 0xFC), followed by the offset and intended value (0x00000100).

- WRITE 0xFC 0x00000100
- WRITE 0x88 0x00000020



Please take note of the register name **TOP.IOD_CNFG[1].IOD_DIV_CNFG.iod_divider**. This is called a **bitset**. Bitsets can be used in Python scripts to update register values.

12. Python

An alternative way to configure the device is to use Python. Using an RBS as a starting point, the following script can be used to write and read the device.

12.1 Example Script

In order for this example to work, you will need to install RICBox with the latest VC8 plugin. You will need to open a command prompt. The location where the command prompt opens is where the script and RBS file will need to be saved. To run the python script, use the following command in the command prompt

```
%AppData%\RICBox\pyenvs\R_VersaClock8-x64\python.exe myscript.py RC31312AQ_test.rbs
```

myscript.py

```
from rbcore.settings import SettingsData
from r_drv_vc8.device_abstraction.versaclock8 import VersaClock8

import sys

rbs_file = sys.argv[1]

print("")
print("Loading RBS file : %s" % (rbs_file))
data = SettingsData.load(rbs_file)

vc8 = VersaClock8(VersaClock8.create_device(data.info.part_number,
data.info.hardware_revision))
vc8.load_settings(rbs_file)

print("Connecting to DUT")
vc8.connect() # connection will be made as specified in the rbs e.g. i2c, 2 byte addressing

print("Writing RBS to DUT")
vc8.writeall()

# changing TOP.IOD_CNFG[1].IOD_DIV_CNFG.iod_divider to 0x20
vc8.device.programmer.write(0x20, 0x188)
print(vc8.device.programmer.read(0x188))

# the names can be copied directly from RICBox Fields view. Right click on field and copy
# talk directly to vc8 registers
vc8.device.programmer.write(7, vc8.bitsets.TOP.TRIM.X0_DIGICAP_X1.xo_digcap_x1())
vc8.device.programmer.write(7, vc8.bitsets.TOP.TRIM.X0_DIGICAP_X2.xo_digcap_x2())

print(vc8.device.programmer.read(vc8.bitsets.TOP.TRIM.X0_DIGICAP_X1.xo_digcap_x1()))
print(vc8.device.programmer.read(vc8.bitsets.TOP.TRIM.X0_DIGICAP_X2.xo_digcap_x2()))

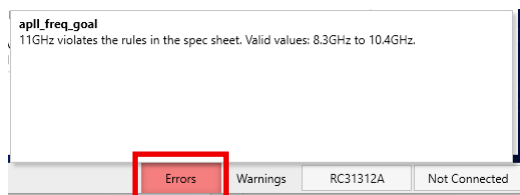
# only fields that are set with set_and_lock() will get saved
vc8.bitsets.TOP.TRIM.X0_DIGICAP_X1.xo_digcap_x1().set_and_lock(8)
vc8.bitsets.TOP.TRIM.X0_DIGICAP_X2.xo_digcap_x2().set_and_lock(8)

print("Saving RBS")
vc8.save_settings("new.rbs")
```

13. Errors and Warnings

When adjusting the values in the configuration, errors or warnings may arise. These are used to help users stay within the limitations of the device and give recommendations to how to configure it. Errors must be cleared before writing to the device.

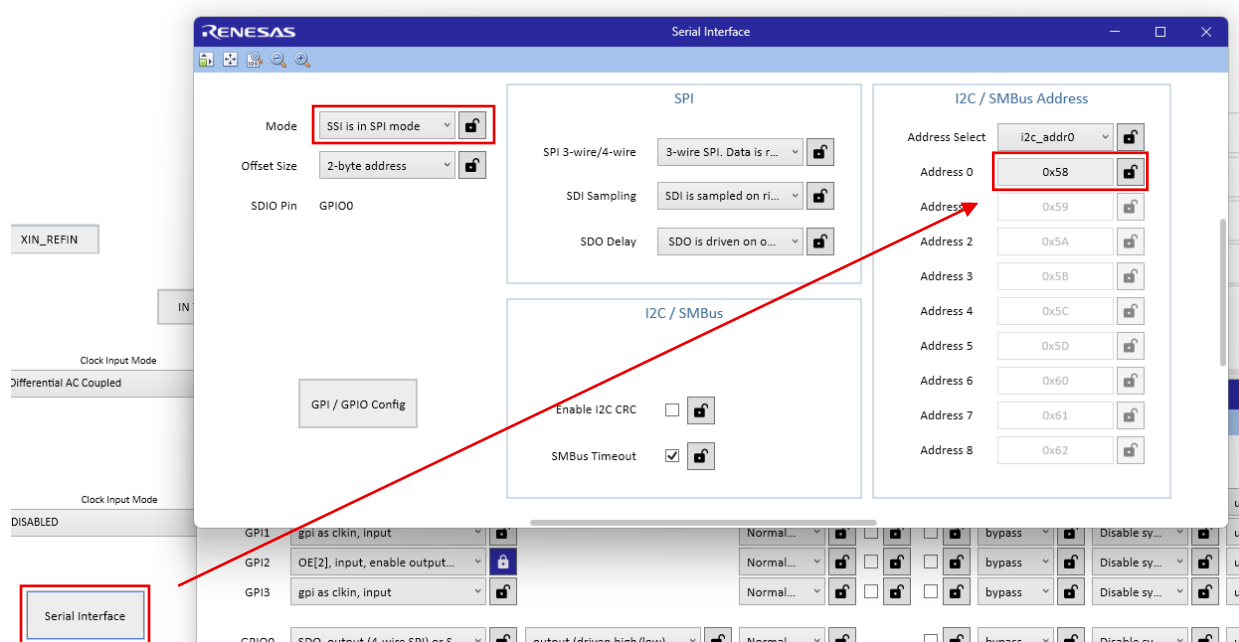
The bottom right corner of the screen shows how many errors or warnings have occurred. Click on one to view the contents.



14. Other Configurable Settings

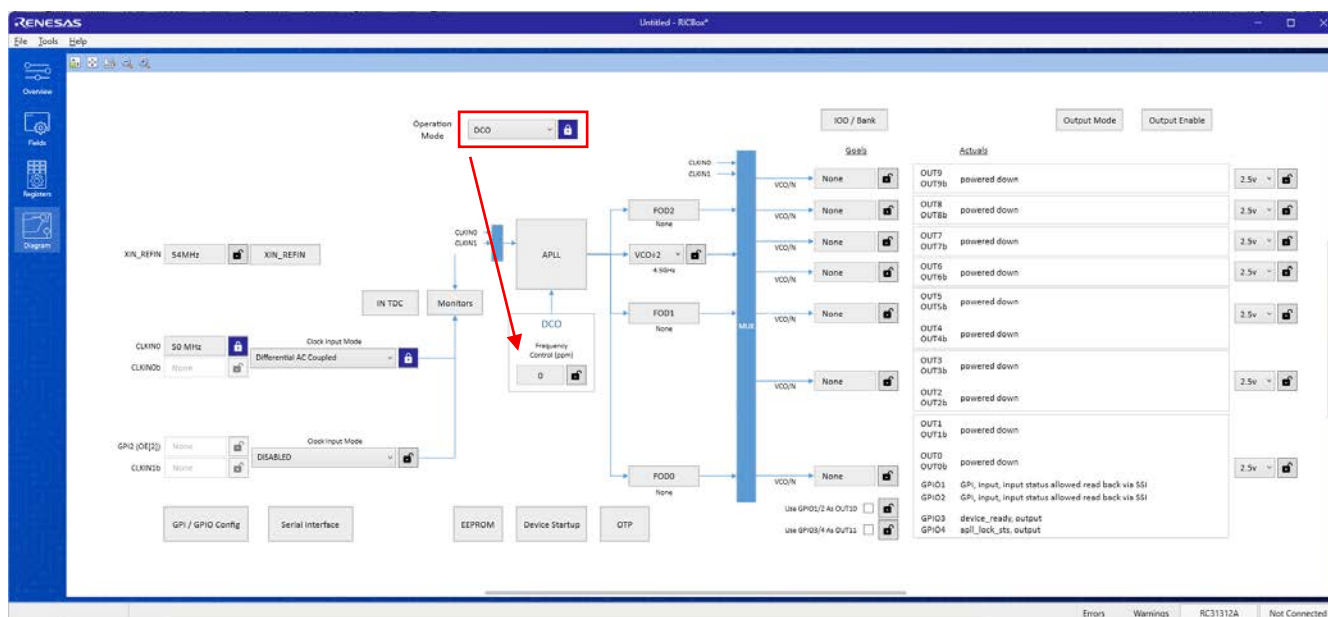
14.1 Changing the I²C Device Address

1. Click on the main Diagram and push the Serial Interface button.
2. Default Serial mode is SPI 3 wire with GPIO0 as SDIO.
3. Update Address 0 to the desired address.
4. Change Mode to I2C mode.



14.2 DCO mode

1. Go to the block diagram view.
2. Change the Operation Mode to “DCO”.
3. Adjust the Frequency Control value.



14.3 Device Startup

1. Go to the block diagram view and push Device Startup button.
2. Select how each config select bit will function.
 - a. For a single config, the defaults are good to use.
3. Fill in each config slot with their respective configuration.

The screenshot shows the RENESAS Device Startup window. It contains the following sections:

- Startup Config Selection:**
 - Config Select (bit 2): Static Value (High)
 - Config Select (bit 1): Static Value (Low)
 - Config Select (bit 0): Static Value (Low)
- Config Assignment:**

	HIGH	LOW	M		HIGH	LOW	M	
Config 0	H	L	L	default	Config 9	L	L	L
Config 1	H	L	M	default	Config 10	L	L	M
Config 2	H	L	H	default	Config 11	L	L	H
Config 3	H	M	L	default	Config 12	L	M	L
Config 4	H	M	M	default	Config 13	L	M	M
Config 5	H	M	H	default	Config 14	L	M	H
Config 6	H	H	L	default	Config 15	L	H	L
Config 7	H	H	M	default	Config 16	L	H	M
Config 8	H	H	H	default	Config 17	L	H	H

Legend: L = low / M = mid / H = high

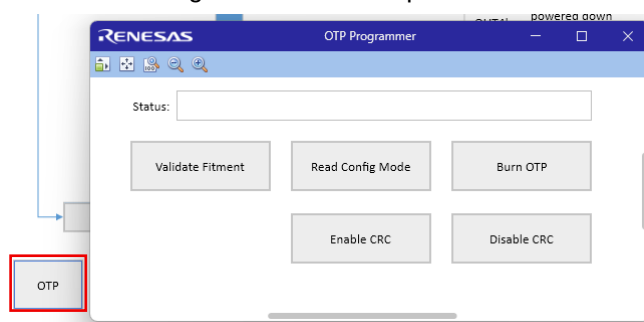
14.4 EEPROM

1. Go to the main block diagram and push the EEPROM button.
2. Push the 3 dots to pick a location to export bin or hex file.
3. Make sure you are connected to VC8.
4. Pick the EEPROM address to Erase/Program/Verify.



14.5 OTP

1. From the main diagram, push the OTP button.
2. When your configs are complete, push the Validate Fitment button to see if all configs will fit into OTP space.
3. Blank VC8 parts can also have the config burned to OTP space with 'Burn OTP'.



15. Revision History

Revision	Date	Description
1.00	Jul 23, 2026	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.