

# Linux Interface Specification Device Driver SD/MMC

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,  
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and  
RZ/Five

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### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/Five Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description  Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of SD/MMC Linux interface Specification	Linux interface Specification – SD/MMC	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

#### 4. List of Abbreviations and Acronyms

Abbreviation	Full Form
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
eMMC	Embedded multi-media card
I/O	Input/Output
MMC	Multi-media card
SD	Secure digital
SDIO	Secure digital Input/Output
VCC	Voltage common collector
VCCQ	Output stage logic power voltage

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# 1. Overview

## 1.1 Overview

This manual explains the driver module (this module) that controls the SD card/MMC interfaces on RZ/G Series, RZ/V Series and RZ/Five Series. Detailed explanation is skipped because the interface of this module is based on Linux.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group and RZ/Five.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S.

## 1.2 Function

This module transmits/receives data to/from the SD card/MMC interfaces on RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group and RZ/G3S Group.

The following table lists the functions of this module.



**Table 1-1 Driver Function<sup>1</sup>**

function	support status
SD Memory Card	SD, SDHC, SDXC <sup>2</sup> support
SDIO Card	Support
eMMC	Support
Transfer mode	(1) SD/SDIO: 1bit, 4bit (2) eMMC: 1bit, 4bit, 8bit
Bus speed mode	(1) SD/SDIO - Support: Default Speed(DS), High Speed(HS), and UHS-I (SDR104 / SDR50 / SDR25 / SDR12 / DDR50) (2) eMMC - Support: Backward-compatible, high-speed, HS200 support
DMA function	Internal DMAC support
Card power control	Support <sup>3</sup>
Card Detection(CD)	Support <sup>3</sup>
Card Detection(DAT3)	Not support
Write Protection	Not support
SPI mode	Not support
SD Mechanical Write Protect Switch	Support <sup>3</sup>
SD CPRM Security	Not support
SDIO CMD52 During Data Transfer(C52PUB)	Not support
SDIO Data Transfer Abort(IOABT)	Not support
SDIO Read Wait(RWREQ)	Not support
SDIO Wake Up	Not support
SDIO Suspend/Resume	Not support
eMMC Boot operation	Support
eSD Boot operation	Support (except RZ/Five)

---

<sup>1</sup> Aggressively clock gating to substitute in RuntimePM.

<sup>2</sup> SDXC memory cards that are formatted with the exFAT cannot be mounted because BSP standard file system does not support the exFAT.

<sup>3</sup> This function corresponds to the GPIO customization interface in the device-dependent. Please refer to 4.1 for details.

### 1.3 Connected Port

This module supports SD/MMC ports on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/V2N Evaluation Board Kit, RZ/V2H Evaluation Board Kit, RZ/G3E SMARC Evaluation Board Kit and RZ/G3S Evaluation Board Kit.

**Table 1-2 Connected ports on (RZ/G2L, RZ/G2LC, RZ/G2UL and RZ/V2L) Evaluation Board Kit**

channel	connected to	support status	Remark
SDHI0 (MMC0)	High Speed Connector (CN7)	Yes	-
SDHI1	SD Card Connector (CN8)	Yes	-

**Table 1-3 Connected ports on RZ/V2N Evaluation Board Kit**

Channel	Connected to	Support status	Remark
SDHI0 (MMC0)	eMMC card or uSD Card Slot (uSD0)	Yes	Both eMMC and uSD
SDHI1	uSD Card Slot (uSD1)	Yes	
SDHI2	-	No	No interface support

**Table 1-4 Connected ports on RZ/V2H Evaluation Board Kit**

Channel	Connected to	Support status	Remark
SDHI0 (MMC0)	eMMC card or uSD Card Slot (uSD0)	Yes	Both eMMC and uSD
SDHI1	uSD Card Slot (uSD1)	Yes	
SDHI2	-	No	No interface support

**Table 1-5 Connected ports on RZ/G3E SMARC Evaluation Board Kit**

Channel	Connected to	Support status	Remark
SDHI0 (MMC0)	eMMC card or uSD Card Slot (uSD0)	Yes	Both eMMC and uSD
SDHI1	uSD Card Slot (uSD1)	Yes	
SDHI2	uSD Card Slot (uSD2)	Yes	

**Table 1-6 Connected port on RZ/G3S Smarc Evaluation Board Kit**

Channel	Connected to	Support status	Remark
SDHI0 (MMC0)	eMMC card or uSD Card Slot (uSD0)	Yes	Both MMC and uSD
SDHI1	uSD Card Slot (uSD1)	Yes	Only uSD
SDHI2	uSD Card Slot (uSD2)	Yes	Only uSD

## 1.4 Reference

### 1.4.1 Standard

The following table shows the standard that this module corresponds.

**Table 1-7 Standard**

Reference No.	Issue	Title	Edition	Date
-	SD Card Association	SD Specifications Part 1 Physical Layer Simplified Specification	Version 4.10	Jan. 22, 2013
-	SD Card Association	SD Specifications Part E1 SDIO Simplified Specification	3.00	Feb. 25, 2011
JESD84-B51	JEDEC STANDARD Multi-Media Card Association	Embedded Multi-Media Card (e•MMC) Electrical Standard (5.1)	5.1	Feb. 2015

### 1.4.2 Related Documents

There is no document related to this module.

## 1.5 Restrictions

None.

## 1.6 Notice

None.

## 2. Terminology

The following table shows the terminology related to this module.

**Table 2-1 Terminology**

Terms	Explanation
MMC	Multi-Media Card This media corresponds to the standard of the removable disk which was established in 1998 by Sun Disk and Siemens jointly.
eMMC	Embedded Multi-Media Card
SD	Secure Digital This media corresponds to the standard of the removable disk which was established in 1999 by Panasonic, Sun Disk and Toshiba jointly.
SDIO	Secure Digital Input/Output This media corresponds to I/O interface standard of SD card which uses the specifications of the physical shape and the electrical feature. It can use a SD card socket. There is a card with wireless LAN or a digital camera function.
DMA	Direct Memory Access
DMAC	DMA Controller
SDHI	SD card host interface H/W module
SPI	Serial Peripheral Interface
CPRM	Content Protection for Recordable Media
GPIO	General-purpose I/O

## 3. Operating Environment

### 3.1 Hardware Environment

The following table shows the hardware needed to use this module.

**Table 3-1 Hardware specification**

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

### 3.2 Module Configuration

The following figure shows the configuration of this module.

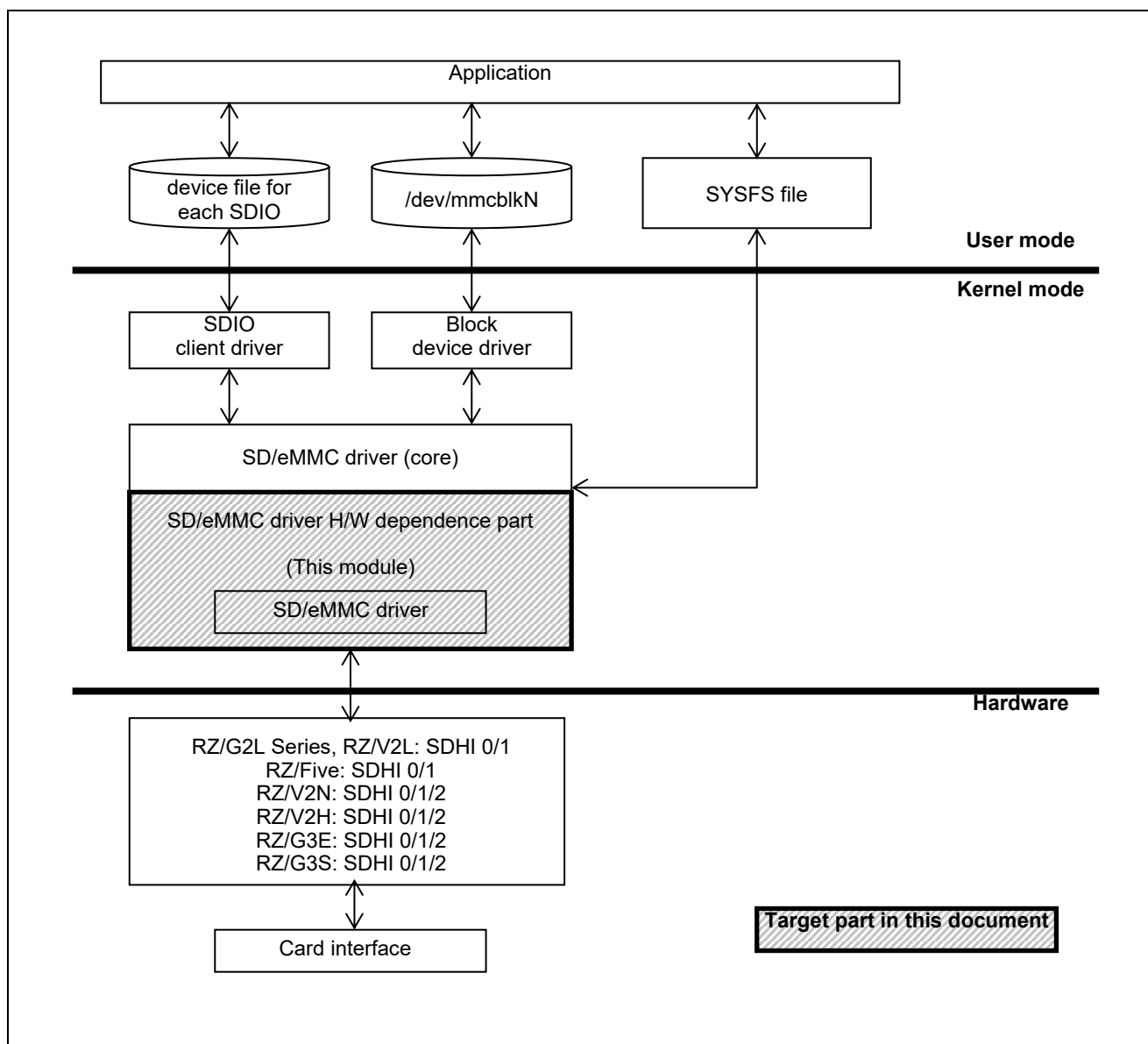


Figure 3-1 Module Configuration

### 3.3 State Transition Diagram

There is no state transition diagram for this module.

## 4.External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

Device node of this module is described below.

**Table 4-1 SDHI Device Node**

Channel	Device node	Major number	Minor number
SDHIx	/dev/mmcblkN <sup>4</sup>	179	0~96

In addition, the device node of SDIO might be different according to SDIO card to use.

ex) SDIO UART card to use

/dev/ttySDIO0

---

<sup>4</sup> The numerical value might be different according to the system. (ex, /dev/mmcblk0)

## 4.1 GPIO Customization Interface

This module uses the interface that can be controlled via "Card Power Control", "Card Detection", "Mechanical Write Protect Switch", and "Voltage Switch" by GPIOs. The GPIO interface can be used when you register GPIO to device tree file in the device-dependent part.

RZ/V2N, RZ/V2H and RZ/G3E do not support Pin Voltage Switching function from Pin control so create a device tree property to check the support of this function. If Pin Voltage Switching function support is unavailable, ignore the pinctrl setting and just change the voltage of Vccq.

The following table shows the GPIO interface and properties of this module.

**Table 4-2 GPIO Customization Interface**

Function	Interface	Property
Card Power Control	mmc_regulator_set_ocr	vmmc-supply
Card Detection	mmc_gpio_get_cd	cd-gpios
Mechanical Write Protect Switch	mmc_gpio_get_ro	wp-gpios
Voltage Switch	regulator_set_voltage	vqmmc-supply

### 4.1.1 Setting of Pins

#### 4.1.1.1 Data and Control Pins

Depending on SoC, data and control pins of SDHI can be multiplexed or dedicated pins

- Figure below is device tree bindings for multiplexed pins definition:

```
* SW_SDIO_M2E:
*      0 - Smarc SDIO signal is connected to uSD1
*      1 - Smarc SDIO signal is connected to M.2 Key E connector

#if (!SW_SDIO_M2E)
    sdhi1_pins: sd1 {
        sd1_mux {
            pinmux = <RZV2H_PORT_PINMUX(1, 4, 8)>; /* QSD1_CD */
        };

        sd1_data {
            pinmux = <RZV2H_PORT_PINMUX(G, 2, 1)>, /* QSD1_DAT0 */
                    <RZV2H_PORT_PINMUX(G, 3, 1)>, /* QSD1_DAT1 */
                    <RZV2H_PORT_PINMUX(G, 4, 1)>, /* QSD1_DAT2 */
                    <RZV2H_PORT_PINMUX(G, 5, 1)>; /* QSD1_DAT3 */
        };
    };
#endif
```



```

        sd1_ctrl {
            pinmux = <RZV2H_PORT_PINMUX(G, 0, 1)>, /* QSD1_CLK */
                  <RZV2H_PORT_PINMUX(G, 1, 1)>; /* QSD1_CMD */
        };
    };
#endif

```

**Figure 4–1 RZ/G3E SDHI channel 1 multiplexed pins with SDIO\_M2E**

- Figure below is device tree bindings for dedicated pins definition:

```

sdhi0_pins: sd0emmc {
    sd0-emmc-ctrl {
        pins = "SD0_CLK", "SD0_CMD";
        renesas,output-impedance = <3>;
    };

    sd0-iops {
        pins = "QSD0_IOVS";
        renesas,output-impedance = <3>;
    };

    sd0-emmc-data {
        pins = "QSD0_DAT0", "QSD0_DAT1", "QSD0_DAT2", "QSD0_DAT3",
              "QSD0_DAT4", "QSD0_DAT5", "QSD0_DAT6", "QSD0_DAT7";
        renesas,output-impedance = <3>;
    };

    sd0-emmc-rst {
        pins = "SD0_RSTN";
        renesas,output-impedance = <3>;
    };
};

```

**Figure 4–2 RZ/G3E eMMC dedicated pins**

With

"SD0\_RSTN", "SD0\_CLK", "SD0\_CMD", "QSD0\_IOVS", "QSD0\_DAT0", "QSD0\_DAT1", "QSD0\_DAT2", "QSD0\_DAT3",  
"QSD0\_DAT4", "QSD0\_DAT5", "QSD0\_DAT6", "QSD0\_DAT7"

from file: *drivers/pinctrl/renesas/pinctrl-rzg2l.c*

```
static struct rzg2l_dedicated_configs rzg3e_dedicated_pins[] = {
.....

    { "SD0_CLK", RZG2L_SINGLE_PIN_PACK(0x9, 0, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR)) },
    { "SD0_CMD", RZG2L_SINGLE_PIN_PACK(0x9, 1, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "SD0_RSTN", RZG2L_SINGLE_PIN_PACK(0x9, 2, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR)) },
    { "QSD0_PWEN", RZG2L_SINGLE_PIN_PACK(0x9, 3, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR)) },
    { "QSD0_IOVS", RZG2L_SINGLE_PIN_PACK(0x9, 4, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR)) },
    { "QSD0_DAT0", RZG2L_SINGLE_PIN_PACK(0xa, 0, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT1", RZG2L_SINGLE_PIN_PACK(0xa, 1, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT2", RZG2L_SINGLE_PIN_PACK(0xa, 2, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT3", RZG2L_SINGLE_PIN_PACK(0xa, 3, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT4", RZG2L_SINGLE_PIN_PACK(0xa, 4, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT5", RZG2L_SINGLE_PIN_PACK(0xa, 5, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT6", RZG2L_SINGLE_PIN_PACK(0xa, 6, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
    { "QSD0_DAT7", RZG2L_SINGLE_PIN_PACK(0xa, 7, (PIN_CFG_IOLH_RZV2H | PIN_CFG_SR |
                                                PIN_CFG_IEN | PIN_CFG_PUPD)) },
};
```

According to hardware documents, data and control pin of SD0/1 (RZ/G3S SMARC) is not muxed and can be see in device tree as below

```
&pinctrl {  
    sdhi0_emmc_pins: sd0-emmc {  
        pins = "SD0_DATA0", "SD0_DATA1", "SD0_DATA2", "SD0_DATA3",  
               "SD0_DATA4", "SD0_DATA5", "SD0_DATA6", "SD0_DATA7",  
               "SD0_CLK", "SD0_CMD", "SD0_RST#";  
        power-source = <1800>;  
    };  
}
```

**Figure 4-3 Example setting eMMC pins of SDHI0 on RZ/G3S SMARC**

```
&pinctrl {  
    sdhi0_pins: sd0 {  
        data {  
            pins = "SD0_DATA0", "SD0_DATA1", "SD0_DATA2", "SD0_DATA3";  
            power-source = <3300>;  
        };  
        ctrl {  
            pins = "SD0_CLK", "SD0_CMD";  
            power-source = <3300>;  
        };  
        cd {  
            pinmux = <RZG2L_PORT_PINMUX(0, 0, 1)>; /* SD0_CD */  
        };  
    };  
    sdhi0_uhs_pins: sd0-uhs {  
        data {  
            pins = "SD0_DATA0", "SD0_DATA1", "SD0_DATA2", "SD0_DATA3";  
            power-source = <1800>;  
        };  
        ctrl {  
            pins = "SD0_CLK", "SD0_CMD";  
            power-source = <1800>;  
        };  
        cd {  
            pinmux = <RZG2L_PORT_PINMUX(0, 0, 1)>; /* SD0_CD */  
        };  
    };  
};
```

**Figure 4-4 Example setting for SD pins of SDHI0 on RZ/G3S SMARC**

```

&pinctrl {
    sdhi2_pins: sd2 {
        data {
            pins = "P11_2", "P11_3", "P12_0", "P12_1";

            input-enable;
        };

        ctrl {
            pins = "P11_1";

            input-enable;
        };

        mux {
            pinmux = <RZG2L_PORT_PINMUX(11, 0, 8)>, /* SD2_CLK */
                    <RZG2L_PORT_PINMUX(11, 1, 8)>, /* SD2_CMD */
                    <RZG2L_PORT_PINMUX(11, 2, 8)>, /* SD2_DATA0 */
                    <RZG2L_PORT_PINMUX(11, 3, 8)>, /* SD2_DATA1 */
                    <RZG2L_PORT_PINMUX(12, 0, 8)>, /* SD2_DATA2 */
                    <RZG2L_PORT_PINMUX(12, 1, 8)>, /* SD2_DATA3 */
                    <RZG2L_PORT_PINMUX(14, 1, 7)>; /* SD2_CD# */
        };
    };
};

```

**Figure 4-5 Example setting for muxed SD pins of SDHI2 on RZ/G3S SMARC**

**Note:** While data and control pins of SDHI0/1 are fixed and used for SDHI, these pins of SDHI2 are muxed with other modules.

#### 4.1.2 Card Power Control

The Card Power Control GPIO is driven by the fixed voltage regulator driver and enables *mmc\_regulator\_set\_ocr* control API. Binding of the driver and GPIO pin must be specified in board-specific device tree.

The following paragraph shows an example of device tree binding of this GPIO pin.

```
/ {
    vmmc_sdhi1: regulator-vcc-sdhi1 {
        compatible = "regulator-fixed";

        regulator-name = "SDHI1 Vmmc";
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
        gpios = <&pinctrl RZG2L_GPIO(39, 2) GPIO_ACTIVE_HIGH>;
        enable-active-high;
    };
    ...
};
&sdhi1 {
    ...
    vmmc-supply = <&vmmc_sdhi1>;
    ...
};
```

Figure 4–6 Configuration Examples for Card Power Control

#### 4.1.3 Card Detection

The Card Detection enables *mmc\_gpio\_get\_cd* control API. Binding of the driver and GPIO pin must be specified in board-specific device tree.

The following paragraph shows an example of device tree binding of this GPIO pins

```
sdhi1_pins: sd1 {
    ...
    sd1_mux_uhs {
        pinmux = <RZG2L_PORT_PINMUX(19, 0, 1)>; /* SD1_CD */
    };
    ....
};
```

Figure 4–7 Configuration Examples for Card Detection

#### 4.1.4 Mechanical Write Protect Switch

The Mechanical Write Protect Switch enables *mmc\_gpio\_get\_ro* control API. Biding for this GPIO must be specified in board-specific device tree.

The following paragraph shows an example of device tree binding of this GPIO pin.

```
&sdhi1 {  
    ...  
    ..  
    wp-gpios = <&pinctrl RZG2L_GPIO(0, 3) GPIO_ACTIVE_HIGH>;  
    ...  
    ...  
}
```

**Figure 4–8 Configuration Examples for Write Protection**

Note: Input LOW logic to this GPIO pin will enable Write Protection, and input HIGH logic will disable it (default HIGH). However, this change will not apply to the card already inserted, until it is removed and inserted again.

#### 4.1.5 Voltage Switch

The Voltage Switch GPIO of SDHI is driven by the regulator GPIO driver and enables *regulator\_set\_voltage* control API. Binding of the driver and GPIO pin must be specified in board-specific device tree.

The following paragraph shows an example of device tree binding of this GPIO pin.

```
/ {
    vccq_sdhi1: regulator-vccq-sdhi1 {
        compatible = "regulator-gpio";

        regulator-name = "SDHI1 VccQ";
        regulator-min-microvolt = <1800000>;
        regulator-max-microvolt = <3300000>;

        gpios = < &pinctrl RZG2L_GPIO(39, 1) GPIO_ACTIVE_HIGH>;
        gpios-states = <1>;
        states = <3300000 1 1800000 0>;
    };
    ...
};
...
&sdhi1 {
    pinctrl-0 = <&sdhi1_pins>;
    pinctrl-1 = <&sdhi1_pins_uhs>;
    pinctrl-names = "default", "state_uhs";

    vmmc-supply = <&reg_3p3v>;
    vqmmc-supply = <&vccq_sdhi1>;
    ...
};
```

**Figure 4–9 Configuration Examples for Voltage Switch (SDHI)**

**Note:** On RZ/G3S SMARC, SDHI2 only use 3.3v

The Voltage Switch GPIO of eMMC is driven by fixed voltage regulator driver. Binding of the driver and GPIO pin must be specified in board-specific device tree.

The following paragraph shows an example of device tree binding of this GPIO pin.



```

/{
    reg_1p8v: regulator0 {
        compatible = "regulator-fixed";
        regulator-name = "fixed-1.8V";
        regulator-min-microvolt = <1800000>;
        regulator-max-microvolt = <1800000>;
        regulator-boot-on;
        regulator-always-on;
    };

    reg_3p3v: regulator1 {
        compatible = "regulator-fixed";
        regulator-name = "fixed-3.3V";
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
        regulator-boot-on;
        regulator-always-on;
    };
    ...
};

&sdhi0 {
    pinctrl-0 = <&sdhi0_emmc_pins>;
    pinctrl-1 = <&sdhi0_emmc_pins>;
    pinctrl-names = "default", "state_uhs";

    vmmc-supply = <&reg_3p3v>;
    vqmmc-supply = <&reg_1p8v>;
    bus-width = <8>;
    mmc-hs200-1_8v;
    non-removable;
    fixed-emmc-driver-type = <1>;
    status = "okay";
};

```

**Figure 4–10 Configuration Examples for Voltage Switch (eMMC)**

**Notes:** When a 1.8V fixation amplitude SDIO card (and so on) is used, please set *vqmmc-supply* property as 1.8V amplitude for SDHI node in device tree. When this configuration is set, a 3.3V amplitude card will not be able to detect.

## 4.2 Error Codes

This module returns the error that is detected by SDHI in the following error code from H/W dependence part of SD driver to core part of SD driver.

**Table 4-3 Error Codes**

Detection error	Error code	Description
ERR6	-ETIMEDOUT	Response timeout error
ERR3	-EBUSY -EINVAL -ENOMEM	Data timeout (except response timeout) error
ERR2	-EINTR	END error
ERR1	-EILSEQ	CRC error

## 4.3 Transfer Mode Setting (DMA/PIO)

To change transfer mode of PIO and DMA, make the following setting with kernel configuration.

```
Device Drivers --->
  <*> MMC/SD/SDIO card support --->
    --- MMC/SD/SDIO card support
      <*> Renesas SDHI SD/SDIO controller support
        < > DMA for SDHI SD/SDIO controllers using SYS-DMAC
        -* - DMA for SDHI SD/SDIO controllers using on-chip bus mastering
        [ ] Renesas SDHI PIO transfer mode setting
```

**Figure 4-15 Kernel configuration**

“Renesas SDHI PIO transfer mode setting” select Yes or No according to the following.

- When switching the transfer mode from DMA to PIO, say Y here.
- When switching the transfer mode from PIO to DMA, say N here.

## 4.4 DIP-Switch and Macro Setting

On the RZ/G2L and RZ/V2L board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `EMMC` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/rzg2l-smarc-som.dtsi`)

- In eMMC case: define `EMMC` as 1
- In uSD case: define `EMMC` as 0

On the RZ/G2LC board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `SW_SD0_DEV_SEL` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/r9a07g044c2-smarc.dts`)

- In eMMC case: define `SW_SD0_DEV_SEL` as 1
- In uSD case: define `SW_SD0_DEV_SEL` as 0

On the RZ/G2UL and RZ/Five board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `SW_SD0_DEV_SEL` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/r9a07g043u11-smarc.dts`)

- In eMMC case: define `SW_SD0_DEV_SEL` as 1
- In uSD case: define `SW_SD0_DEV_SEL` as 0

**Note:** To enable uSD card connected on SDHI0 channel on RZ/G2L series, RZV2L and RZ/Five board SW1[2] should be at position ON

On the RZ/V2N board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `eMMC_SD_SEL` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/r9a09g056n44-evk.dts`)

- In eMMC case (connect eMMC sub-board to CN15): define `eMMC_SD_SEL` as 1
- In uSD case (connect micro-SD sub-board to CN15): define `eMMC_SD_SEL` as 0

On the RZ/V2H board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `CN15_eMMC_uSD` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk-ver2.dts`)

- In eMMC case (connect eMMC sub-board to CN15): define `CN15_eMMC_uSD` as 0
- In uSD case (connect micro-SD sub-board to CN15): define `CN15_eMMC_uSD` as 1

On the RZ/G3E board, eMMC or uSD device can be selected to connect on sdhi0 channel interface depending on `SW_SD0_DEV_SEL` macro setting in board devicetree file

(`arch/arm64/boot/dts/renesas/r9a09g047e57-smarc.dts`)

- In eMMC case: define `SW_SD0_DEV_SEL` as 0
- In uSD case: define `SW_SD0_DEV_SEL` as 1

**Note:** To enable uSD card connected on SDHI0 channel on RZ/G3E board SW4[1] should be at position ON

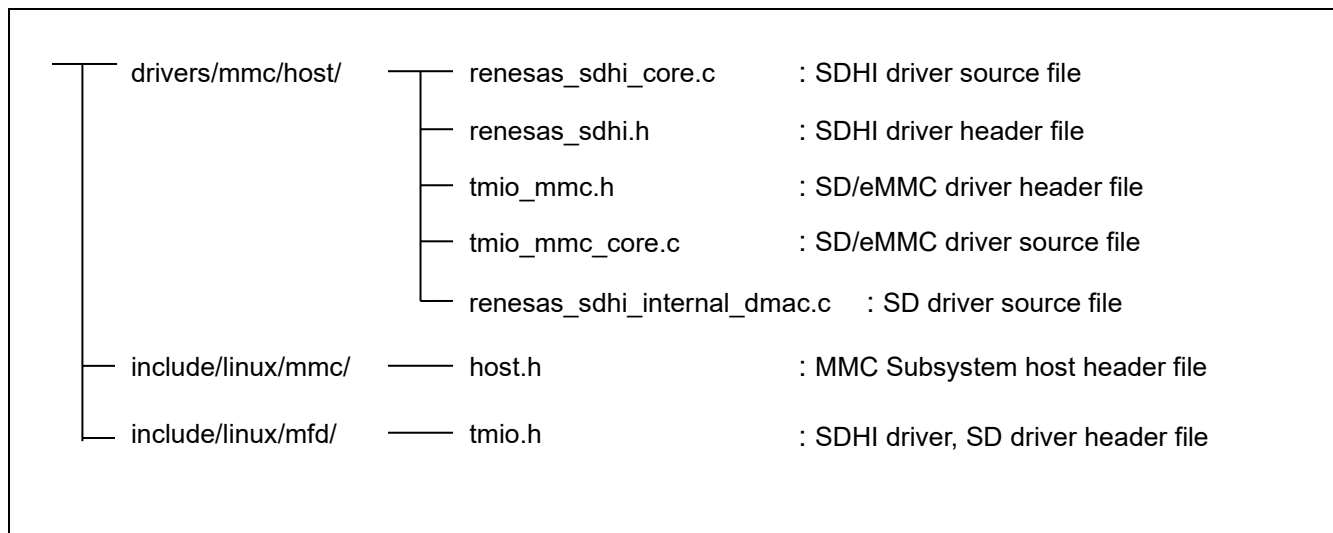
On the RZ/G3S board

- To select eMMC usage for SDHI0:  
Set macro `SW_CONFIG2` (in `arch/arm64/boot/dts/renesas/rzg3s-smarc-switches.h`) to `SW_OFF` and turn off `SW_CONFIG[2]` (on RZ/G3S SOM board) to enable eMMC.
- To select uSD usage for SDHI0:  
Set macro `SW_CONFIG2` to `SW_ON` and turn on `SW_CONFIG[2]` to enable SD0 slot on SOM.
- To use SD2 slot on RZ/G3S SMARC SOM:  
Set `SW_CONFIG3` (in `arch/arm64/boot/dts/renesas/rzg3s-smarc-switches.h`) to `SW_OFF` and turn on `SW_CONFIG[3]` (on SOM).

## 5. Integration

## 5.1 Directory Configuration

The directory configuration is described below.



### Figure 5–1 Directory Configuration

## 5.2 Integration Procedure

To enable the function of this module, make the following setting with kernel configuration.

```
Device Drivers  --->
<*> MMC/SD/SDIO card support  --->
--- MMC/SD/SDIO card support
<*>   Renesas SDHI SD/SDIO controller support
< >   DMA for SDHI SD/SDIO controllers using SYS-DMAC
-* -   DMA for SDHI SD/SDIO controllers using on-chip bus mastering
```

### Figure 5-2 Kernel configuration

### 5.3 Option Setting

### 5.3.1 Module Parameters

There are no module parameters.

### 5.3.2 Kernel Parameters

There are no kernel parameters.

REVISION HISTORY	Linux Interface Specification Device Driver SD/MMC User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 2021	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2LC, RZ/G2UL device
1.3	Mar. 31, 2022	—	Update information of new VLP.
1.4	May. 31, 2022	—	No modification, keep version to keep consistent with other documents
1.5	Jun. 24, 2022	—	Update information of RZ/Five.
1.6	Sep. 16, 2022	—	Update information
1.7	Dec. 15, 2022	—	Update information
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents
1.9	Mar. 31, 2025	2, 7, 9, 10	Update eSD Boot operation, node for Figure 3-1, mmc-supply regulator node, change to use pinmux for CD function.
1.10	May 30, 2025	1, 2, 13	<ul style="list-style-type: none"> <li>- Add MPU information support for both kernel versions v5.10 and v6.1.</li> <li>- Correct typo transfer mode in Table 1-1</li> <li>- Update PIO mode only support for v5.10</li> </ul>
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Renesas Electronics Corporation