

# Linux Interface Specification Device Driver Gigabit Ethernet

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,  
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and  
RZ/Five

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## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/Five Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description  Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of Gigabit Ethernet Linux interface Specification	Linux interface Specification - Gigabit Ethernet	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

#### 4. List of Abbreviations and Acronyms

Abbreviation	Full Form
GbEther	Gigabit Ethernet

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# 1. Overview

## 1.1 Overview

This manual explains the driver module (this module) that controls the Gigabit Ethernet controller in Linux Solution for the RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/Five.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group and RZ/Five.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group, RZ/V2N, RZ/V2H and RZ/G3E.

## 1.2 Function

This module supports the following functions by controlling Gigabit Ethernet (hardware) on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five.

- Transmission and reception of Ethernet frame.
- 1000 Mbps, 100 Mbps and 10Mbps transfer.
- Full-duplex mode.
- A MAC Address is set to a random value by default. It needs to be maintained to satisfy users' environments.
- TOE checksum offload for IPv4 Header, IPv4 TCP/UDP/ICMP, IPv6 TCP/UDP/ICMP.

## 1.3 Ethernet PHY devices

Supported Ethernet PHY device of this module is as follows:

**Table 1-1 Supported Ethernet PHY Devices for RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five Evaluation Board Kit**

Vendor	Product	Interface	Note
Micrel	KSZ9131RNXC	RGMII	Support Clause 28 of IEEE 802.3 Auto-Negotiation

**Table 1-2 Supported Ethernet PHY Devices for RZ/V2N, RZ/V2H and RZ/G3E Evaluation Board Kit**

Vendor	Product	Interface	Note
Micrel	KSZ9131RNXI	RGMII	Support Clause 28 of IEEE 802.3 Auto-Negotiation



## 1.4 Connected Port

**Table 1-3 Connector for RZ/G2L, RZ/V2L and RZ/Five Evaluation Board Kit**

Channel	Connector Name
Ethernet 0	CN9
Ethernet 1	CN8

**Table 1-4 Connector for RZ/V2N and RZ/V2H Evaluation Board Kit**

Channel	Connector Name
Ethernet 0	CN5
Ethernet 1	CN6

**Table 1-5 Connector for RZ/G3E and RZ/G3S SMARC Evaluation Board Kit**

Channel	Connector Name
Ethernet 0	ETHERNET1-0
Ethernet 1	

## 1.5 Reference

### 1.5.1 Standard

There are no reference documents on standards.

### 1.5.2 Related documents

The following table shows the document related to this module.

**Table 1-6 Related document**

Number	Issue	Title	Edition	Date
-	-	-	-	-

## 1.6 Restrictions

There is no restriction in this module.

## 2. Terminology

The following table shows the terminology related to this module.

**Table 2-1 Terminology**

Terms	Explanation
GbEther	Gigabit Ethernet

## 3. Operating Environment

### 3.1 Hardware Environment

The following table lists the hardware needed to use this module.

**Table 3-1 Hardware specification**

<b>Name</b>	<b>Product number</b>
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

### 3.2 Module Configuration

The following figure shows the configuration of this module.

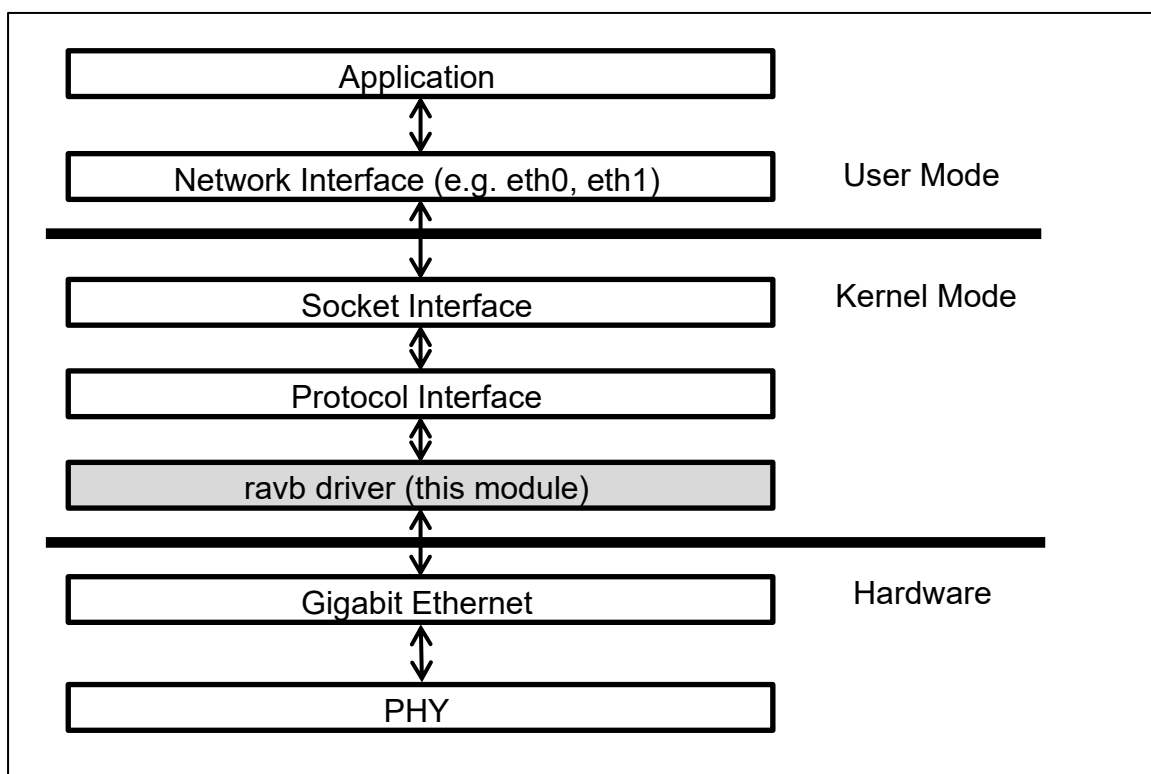


Figure 3-1 GbEther Module Configuration (RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five)

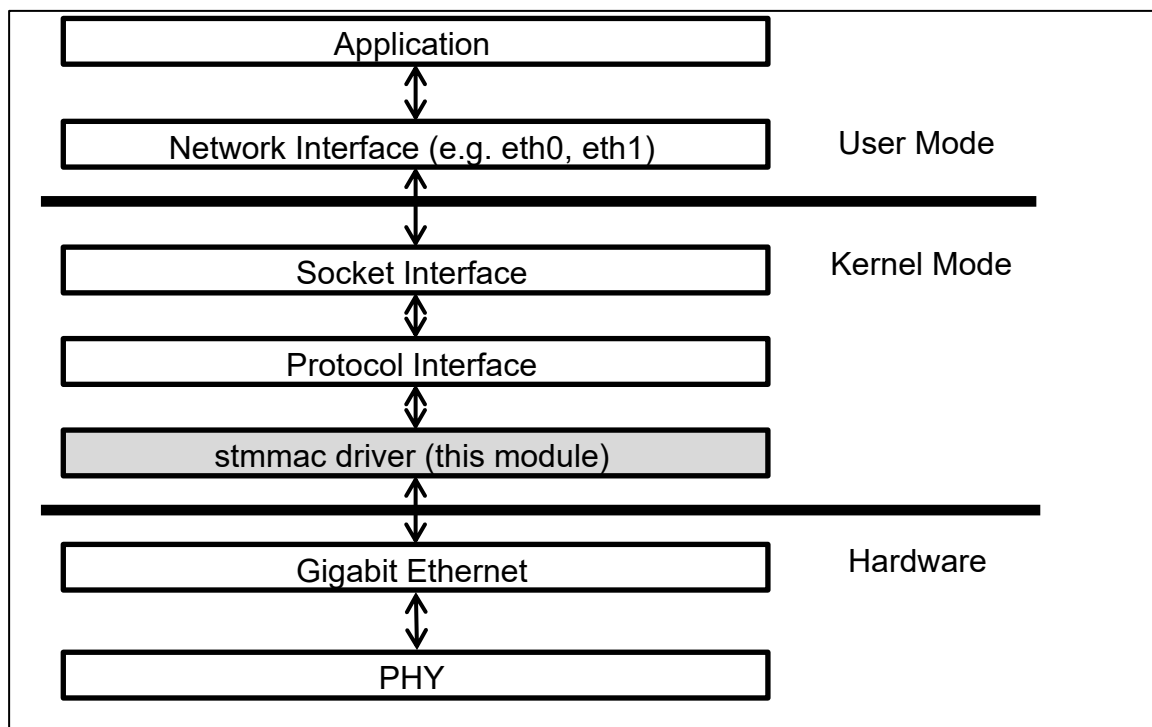


Figure 3-2 GbEther Module Configuration (RZ/V2N, RZ/V2H and RZ/G3E)

### **3.3 State Transition Diagram**

There is no state transition diagram for this module.

## 4. External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

This module is associated with the following Network Interfaces by default.

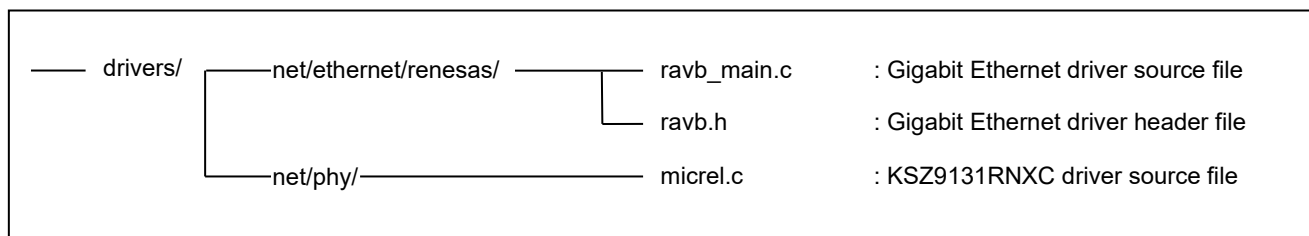
**Table 4-1 Network Interfaces**

<b>Name</b>	<b>Description</b>
eth0	Use eth0 by default configuration on v5.10.
eth1	Use eth1 by default configuration on v5.10.
end0	Use eth0 by default configuration on v6.1.
end1	Use eth1 by default configuration on v6.1.

## 5. Integration

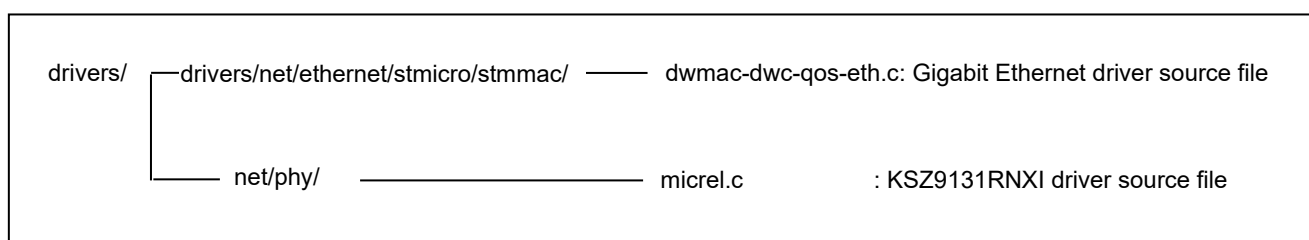
### 5.1 Directory Configuration

The directory configuration for RZ/G2L, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five is shown

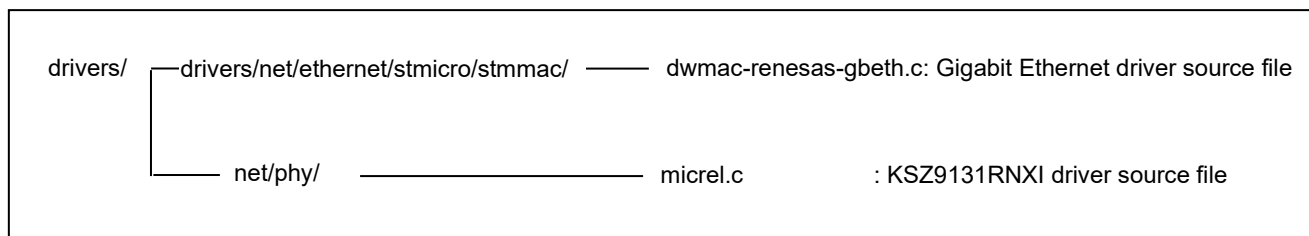


below.

**Figure 5-1 Directory Configuration (RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five)**



**Figure 5-2 Directory Configuration (RZ/G3E)**



**Figure 5-3 Directory Configuration (RZ/V2H and RZ/V2N)**

## 5.2 Integration Procedure

### 5.2.1 Kernel Configuration

To enable the function of this module, make the following setting with Kernel Configuration.

```
[*] Networking support --->
    Networking options --->
        [*] TCP/IP networking
        [*] IP: kernel level autoconfiguration
        [*] IP: DHCP support
        [*] IP: BOOTP support
    Device Drivers --->
        [*] Network device support --->
            [*] Ethernet driver support --->
                [*] Renesas devices
                <*> Renesas Ethernet AVB support
            -* PHY Device support and infrastructure --->
                <*> Micrel PHYs
```

**Figure 5–4 Kernel configuration (RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five)**

```
[*] Networking support --->
    Networking options --->
        [*] TCP/IP networking
        [*] IP: kernel level autoconfiguration
        [*] IP: DHCP support
        [*] IP: BOOTP support
    Device Drivers --->
        [*] Network device support --->
            [*] Ethernet driver support --->
                [*] STMicroelectronics devices --->
                    [*] STMicroelectronics Multi-Gigabit Ethernet driver --->
                        [*] STMMAC Platform bus support --->
                            <*> Support for snps,dwc-qos-ethernet.txt DT binding.
            -* PHY Device support and infrastructure --->
                <*> Micrel PHYs
```

**Figure 5–5 Kernel configuration (RZ/G3E)**

```
[*] Networking support --->
    Networking options --->
        [*] TCP/IP networking
        [*] IP: kernel level autoconfiguration
        [*] IP: DHCP support
        [*] IP: BOOTP support
    Device Drivers --->
        [*] Network device support --->
            [*] Ethernet driver support --->
                [*] STMicroelectronics devices --->
                    [*] STMicroelectronics Multi-Gigabit Ethernet driver --->
                        [*] STMMAC Platform bus support --->
                            <*> Renesas RZ/V2H(P) GBETH support.
            -* PHY Device support and infrastructure --->
                <*> Micrel PHYs
```

**Figure 5–6 Kernel configuration (RZ/V2H and RZ/V2N)**



## 5.3 Option Setting

### 5.3.1 Module Parameters

There are no module parameters.

### 5.3.2 Kernel Parameters

There are no kernel parameters.

### 5.3.3 Device tree definition:

Below figure lists the necessary properties to support GbEther:

- **r9a07g044.dtsi for RZ/G2L and RZ/G2LC, r9a07g043.dtsi for RZ/G2UL, and r9a07g054.dtsi for RZ/V2L:**

In arch/arm64/boot/dts/renesas/r9a07g044.dtsi:

```
eth0: ethernet@11c20000 {
    compatible = "renesas,r9a07g044-gbeth",
                "renesas,rzg2l-gbeth";
    reg = <0 0x11c20000 0 0x10000>;
    interrupts = <GIC_SPI 84 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 85 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 86 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A07G044_ETH0_CLK_AXI>,
            <&cpg CPG_MOD R9A07G044_ETH0_CLK_CHI>,
            <&cpg CPG_CORE R9A07G044_CLK_HP>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A07G044_ETH0_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5–7 Device node for GbEther channel 0 (RZ/G2L and RZ/G2LC)**

In arch/arm64/boot/dts/renesas/r9a07g044.dtsi:

```
eth1: ethernet@11c30000 {
    compatible = "renesas,r9a07g044-gbeth",
                "renesas,rzg2l-gbeth";

    reg = <0 0x11c30000 0 0x10000>;
    interrupts = <GIC_SPI 87 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 88 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 89 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A07G044_ETH1_CLK_AXI>,
            <&cpg CPG_MOD R9A07G044_ETH1_CLK_CHI>,
            <&cpg CPG_CORE R9A07G044_CLK_HP>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A07G044_ETH1_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5–8 Device node for GbEther channel 1 (RZ/G2L and RZ/G2LC)**

Note: All of the information in above device tree is used for RZ/G2L, RZ/G2LC, RZ/G2UL, and RZ/V2L except :

compatible: "renesas,r9a07g044-gbeth" is used for RZ/G2L and RZ/G2LC, "renesas,r9a07g043-gbeth" for RZ/G2UL, and "renesas,r9a07g054-gbeth" is used for RZ/V2L.

clocks: "R9A07G044\_ETH\*\_CLK\_\*" is used for RZ/G2L and RZ/G2LC, "R9A07G043\_ETH\*\_CLK\_\*" for RZ/G2UL, and "R9A07G054\_ETH\*\_CLK\_\*" is used for RZ/V2L.

resets: "R9A07G044\_ETH\*\_RST\_HW\_N" is used for RZ/G2L and RZ/G2LC, "R9A07G043\_ETH\*\_RST\_HW\_N" for RZ/G2UL, and "R9A07G054\_ETH\*\_RST\_HW\_N" for RZ/V2L.

- **r9a07g043f.dtsi for RZ/Five:**

```

In arch/riscv/boot/dts/renesas/r9a07g043f.dtsi:
#include <arm64/renesas/r9a07g043.dtsi>

In arch/arm64/boot/dts/renesas/r9a07g043.dtsi:

eth0: ethernet@11c20000 {
    compatible = "renesas,r9a07g043-gbeth",
                "renesas,rzg2l-gbeth";
    reg = <0 0x11c20000 0 0x10000>;
    interrupts = <SOC_PERIPHERAL_IRQ(84) IRQ_TYPE_LEVEL_HIGH>,
                <SOC_PERIPHERAL_IRQ(85) IRQ_TYPE_LEVEL_HIGH>,
                <SOC_PERIPHERAL_IRQ(86) IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A07G043_ETH0_CLK_AXI>,
            <&cpg CPG_MOD R9A07G043_ETH0_CLK_CHI>,
            <&cpg CPG_CORE R9A07G043_CLK_HP>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A07G043_ETH0_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};

```

**Figure 5–9 Device node for GbEther channel 0 (RZ/Five and RZ/G2UL)**

In arch/arm64/boot/dts/renesas/r9a07g043.dtsi:

```
eth1: ethernet@11c30000 {
    compatible = "renesas,r9a07g043-gbeth",
                "renesas,rzg2l-gbeth";
    reg = <0 0x11c30000 0 0x10000>;
    interrupts = <SOC_PERIPHERAL_IRQ(87) IRQ_TYPE_LEVEL_HIGH>,
                <SOC_PERIPHERAL_IRQ(88) IRQ_TYPE_LEVEL_HIGH>,
                <SOC_PERIPHERAL_IRQ(89) IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A07G043_ETH1_CLK_AXI>,
            <&cpg CPG_MOD R9A07G043_ETH1_CLK_CHI>,
            <&cpg CPG_CORE R9A07G043_CLK_HP>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A07G043F_ETH1_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5–10 Device node for GbEther channel 1 (RZ/Five and RZ/G2UL)**

- **r9a08g045.dtsi for RZ/G3S:**

In arch/arm64/boot/dts/renesas/r9a08g045.dtsi:

```
eth0: ethernet@11c30000 {
    compatible = "renesas,r9a08g045-gbeth", "renesas,rzg2l-gbeth";
    reg = <0 0x11c30000 0 0x10000>;
    interrupts = <GIC_SPI 68 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 69 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 70 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A08G045_ETH0_CLK_AXI>,
            <&cpg CPG_MOD R9A08G045_ETH0_CLK_CHI>,
            <&cpg CPG_MOD R9A08G045_ETH0_REFCLK>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A08G045_ETH0_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5–11 Device node for GbEther channel 0 (RZ/G3S)**

In arch/arm64/boot/dts/renesas/r9a08g045.dtsi:

```
eth1: ethernet@11c40000 {
    compatible = "renesas,r9a08g045-gbeth", "renesas,rzg2l-gbeth";
    reg = <0 0x11c40000 0 0x10000>;
    interrupts = <GIC_SPI 71 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 72 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 73 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "mux", "fil", "arp_ns";
    phy-mode = "rgmii";
    clocks = <&cpg CPG_MOD R9A08G045_ETH1_CLK_AXI>,
            <&cpg CPG_MOD R9A08G045_ETH1_CLK_CHI>,
            <&cpg CPG_MOD R9A08G045_ETH1_REFCLK>;
    clock-names = "axi", "chi", "refclk";
    resets = <&cpg R9A08G045_ETH1_RST_HW_N>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5–12 Device node for GbEther channel 1 (RZ/G3S)**

- **r9a09g056.dtsi for RZ/V2N:**

In arch/arm64/boot/dts/renesas/r9a09g056.dtsi:

```
eth0: ethernet@15c30000 {
    compatible = "renesas,r9a09g056-gbeth", "renesas,rzv2h-gbeth",
        "snps,dwmac-5.20";
    reg = <0 0x15c30000 0 0x10000>;
    interrupts = <GIC_SPI 765 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 767 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 766 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 772 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 773 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 774 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 775 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 768 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 769 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 770 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 771 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi",
        "rx-queue-0", "rx-queue-1", "rx-queue-2",
        "rx-queue-3", "tx-queue-0", "tx-queue-1",
        "tx-queue-2", "tx-queue-3";
    clocks = <&cpg CPG_MOD 0xbd>, <&cpg CPG_MOD 0xbc>,
        <&cpg CPG_CORE R9A09G056_GBETH_0_CLK_PTP_REF_I>,
        <&cpg CPG_MOD 0xb8>, <&cpg CPG_MOD 0xb9>,
        <&cpg CPG_MOD 0xba>, <&cpg CPG_MOD 0xbb>;
    clock-names = "stmmaceth", "pclk", "ptp_ref",
        "tx", "rx", "tx-180", "rx-180";
    resets = <&cpg 0xb0>;
    power-domains = <&cpg>;
    renesas,eth-syscon = <&sys 0>;
    snps,multicast-filter-bins = <256>;
    snps,perfect-filter-entries = <128>;
    rx-fifo-depth = <8192>;
    tx-fifo-depth = <8192>;
    snps,fixed-burst;
    snps,no-pbl-x8;
    snps,force_thresh_dma_mode;
    snps,en-tx-lpi-clockgating;
    snps,axi-config = <&stmmac_axi_setup>;
    snps,mtl-rx-config = <&mtl_rx_setup0>;
    snps,mtl-tx-config = <&mtl_tx_setup0>;
    snps,txpbl = <32>;
    snps,rxpbl = <32>;
    status = "disabled";

    mdio0: mdio {
        compatible = "snps,dwmac-mdio";
        #address-cells = <1>;
        #size-cells = <0>;
    };

    mtl_rx_setup0: rx-queues-config {
        snps,rx-queues-to-use = <4>;
        snps,rx-sched-sp;

        queue0 {
            snps,dcb-algorithm;
            snps,priority = <0x1>;
            snps,map-to-dma-channel = <0>;
        };

        queue1 {
            snps,dcb-algorithm;
            snps,priority = <0x2>;
        };
    };
};
```

```

        snps,map-to-dma-channel = <1>;
    };

    queue2 {
        snps,dcb-algorithm;
        snps,priority = <0x4>;
        snps,map-to-dma-channel = <2>;
    };

    queue3 {
        snps,dcb-algorithm;
        snps,priority = <0x8>;
        snps,map-to-dma-channel = <3>;
    };
};

mtl_tx_setup0: tx-queues-config {
    snps,tx-queues-to-use = <4>;
    snps,tx-sched-wrr;

    queue0 {
        snps,weight = <0x10>;
        snps,dcb-algorithm;
        snps,priority = <0x1>;
    };

    queue1 {
        snps,weight = <0x12>;
        snps,dcb-algorithm;
        snps,priority = <0x2>;
    };

    queue2 {
        snps,weight = <0x14>;
        snps,dcb-algorithm;
        snps,priority = <0x4>;
    };

    queue3 {
        snps,weight = <0x18>;
        snps,dcb-algorithm;
        snps,priority = <0x8>;
    };
};
};

```

Figure 5–13 Device node for GbEther channel 0 (RZ/V2N)



In arch/arm64/boot/dts/renesas/r9a09g056.dtsi:

```
eth1: ethernet@15c40000 {
    compatible = "renesas,r9a09g056-gbeth", "renesas,rzv2h-gbeth",
        "snps,dwmac-5.20";
    reg = <0 0x15c40000 0 0x10000>;
    interrupts = <GIC_SPI 780 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 782 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 781 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 787 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 788 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 789 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 790 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 783 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 784 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 785 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 786 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi",
        "rx-queue-0", "rx-queue-1", "rx-queue-2",
        "rx-queue-3", "tx-queue-0", "tx-queue-1",
        "tx-queue-2", "tx-queue-3";
    clocks = <&cpg CPG_MOD 0xc3>, <&cpg CPG_MOD 0xc2>,
        <&cpg CPG_CORE R9A09G056_GBETH_1_CLK_PTP_REF_I>,
        <&cpg CPG_MOD 0xbe>, <&cpg CPG_MOD 0xbf>,
        <&cpg CPG_MOD 0xc0>, <&cpg CPG_MOD 0xc1>;
    clock-names = "stmmaceth", "pclk", "ptp_ref",
        "tx", "rx", "tx-180", "rx-180";
    resets = <&cpg 0xb1>;
    power-domains = <&cpg>;
    renesas,eth-syscon = <&sys 1>;
    snps,multicast-filter-bins = <256>;
    snps,perfect-filter-entries = <128>;
    rx-fifo-depth = <8192>;
    tx-fifo-depth = <8192>;
    snps,fixed-burst;
    snps,no-pbl-x8;
    snps,force_thresh_dma_mode;
    snps,en-tx-lpi-clockgating;
    snps,axi-config = <&stmmac_axi_setup>;
    snps,mtl-rx-config = <&mtl_rx_setup1>;
    snps,mtl-tx-config = <&mtl_tx_setup1>;
    snps,txpbl = <32>;
    snps,rxpbl = <32>;
    status = "disabled";

    mdio1: mdio {
        compatible = "snps,dwmac-mdio";
        #address-cells = <1>;
        #size-cells = <0>;
    };

    mtl_rx_setup1: rx-queues-config {
        snps,rx-queues-to-use = <4>;
        snps,rx-sched-sp;

        queue0 {
            snps,dcb-algorithm;
            snps,priority = <0x1>;
            snps,map-to-dma-channel = <0>;
        };

        queue1 {
            snps,dcb-algorithm;
            snps,priority = <0x2>;
            snps,map-to-dma-channel = <1>;
        };
    };
};
```

```

        queue2 {
            snps,dcb-algorithm;
            snps,priority = <0x4>;
            snps,map-to-dma-channel = <2>;
        };

        queue3 {
            snps,dcb-algorithm;
            snps,priority = <0x8>;
            snps,map-to-dma-channel = <3>;
        };
};

mtl_tx_setup1: tx-queues-config {
    snps,tx-queues-to-use = <4>;
    snps,tx-sched-wrr;

    queue0 {
        snps,weight = <0x10>;
        snps,dcb-algorithm;
        snps,priority = <0x1>;
    };

    queue1 {
        snps,weight = <0x12>;
        snps,dcb-algorithm;
        snps,priority = <0x2>;
    };

    queue2 {
        snps,weight = <0x14>;
        snps,dcb-algorithm;
        snps,priority = <0x4>;
    };

    queue3 {
        snps,weight = <0x18>;
        snps,dcb-algorithm;
        snps,priority = <0x8>;
    };
};
};

```

Figure 5–14 Device node for GbEther channel 1 (RZ/V2N)

**Note:** All of the information in above device tree is used for RZ/V2N SoC device tree only.

- **r9a09g057.dtsi for RZ/V2H:**

```
eth0: ethernet@15c30000 {
    compatible = "renesas,r9a09g057-gbeth", "renesas,rzv2h-gbeth",
        "snps,dwmac-5.20";
    reg = <0 0x15c30000 0 0x10000>;
    interrupts = <GIC_SPI 765 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 767 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 766 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 772 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 773 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 774 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 775 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 768 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 769 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 770 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 771 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi",
        "rx-queue-0", "rx-queue-1", "rx-queue-2",
        "rx-queue-3", "tx-queue-0", "tx-queue-1",
        "tx-queue-2", "tx-queue-3";
    clocks = <&cpg CPG_MOD 0xbd>, <&cpg CPG_MOD 0xbc>,
        <&cpg CPG_CORE R9A09G057_GBETH_0_CLK_PTP_REF_I>,
        <&cpg CPG_MOD 0xb8>, <&cpg CPG_MOD 0xb9>,
        <&cpg CPG_MOD 0xba>, <&cpg CPG_MOD 0xbb>;
    clock-names = "stmmaceth", "pclk", "ptp_ref",
        "tx", "rx", "tx-180", "rx-180";
    resets = <&cpg 0xb0>;
    power-domains = <&cpg>;
    renesas,eth-syscon = <&sys 0>;
    snps,multicast-filter-bins = <256>;
    snps,perfect-filter-entries = <128>;
    rx-fifo-depth = <8192>;
    tx-fifo-depth = <8192>;
    snps,fixed-burst;
    snps,no-pbl-x8;
    snps,force_thresh_dma_mode;
    snps,axi-config = <&stmmac_axi_setup>;
    snps,mtl-rx-config = <&mtl_rx_setup0>;
    snps,mtl-tx-config = <&mtl_tx_setup0>;
    snps,txpbl = <32>;
    snps,rxpbl = <32>;
    status = "disabled";

    mdio0: mdio {
        compatible = "snps,dwmac-mdio";
        #address-cells = <1>;
        #size-cells = <0>;
    };

    mtl_rx_setup0: rx-queues-config {
        snps,rx-queues-to-use = <4>;
        snps,rx-sched-sp;

        queue0 {
            snps,dcb-algorithm;
            snps,priority = <0x1>;
            snps,map-to-dma-channel = <0>;
        };

        queue1 {
            snps,dcb-algorithm;
            snps,priority = <0x2>;
            snps,map-to-dma-channel = <1>;
        };

        queue2 {
```

```

        snps,dcb-algorithm;
        snps,priority = <0x4>;
        snps,map-to-dma-channel = <2>;
    };

    queue3 {
        snps,dcb-algorithm;
        snps,priority = <0x8>;
        snps,map-to-dma-channel = <3>;
    };
};

mtl_tx_setup0: tx-queues-config {
    snps,tx-queues-to-use = <4>;
    snps,tx-sched-wrr;

    queue0 {
        snps,weight = <0x10>;
        snps,dcb-algorithm;
        snps,priority = <0x1>;
    };

    queue1 {
        snps,weight = <0x12>;
        snps,dcb-algorithm;
        snps,priority = <0x2>;
    };

    queue2 {
        snps,weight = <0x14>;
        snps,dcb-algorithm;
        snps,priority = <0x4>;
    };

    queue3 {
        snps,weight = <0x18>;
        snps,dcb-algorithm;
        snps,priority = <0x8>;
    };
};
};

```

**Figure 5–15 Device node for GbEther channel 0 (RZ/V2H)**

```

eth1: ethernet@15c40000 {
    compatible = "renesas,r9a09g057-gbeth", "renesas,rzv2h-gbeth",
        "snps,dwmac-5.20";
    reg = <0 0x15c40000 0 0x10000>;
    interrupts = <GIC_SPI 780 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 782 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 781 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 787 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 788 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 789 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 790 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 783 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 784 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 785 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 786 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi",
        "rx-queue-0", "rx-queue-1", "rx-queue-2",
        "rx-queue-3", "tx-queue-0", "tx-queue-1",
        "tx-queue-2", "tx-queue-3";
    clocks = <&cpg CPG_MOD 0xc3>, <&cpg CPG_MOD 0xc2>,
        <&cpg CPG_CORE R9A09G057_GBETH_1_CLK_PTP_REF_I>,
        <&cpg CPG_MOD 0xbe>, <&cpg CPG_MOD 0xbf>,
        <&cpg CPG_MOD 0xc0>, <&cpg CPG_MOD 0xc1>;
    clock-names = "stmmaceth", "pclk", "ptp_ref";
}

```

```

        "tx", "rx", "tx-180", "rx-180";
resets = <&cpg 0xb1>;
power-domains = <&cpg>;
renesas,eth-syscon = <&sys 1>;
snps,multicast-filter-bins = <256>;
snps,perfect-filter-entries = <128>;
rx-fifo-depth = <8192>;
tx-fifo-depth = <8192>;
snps,fixed-burst;
snps,no-pbl-x8;
snps,force_thresh_dma_mode;
snps,axi-config = <&stmmac_axi_setup>;
snps,mtl-rx-config = <&mtl_rx_setup1>;
snps,mtl-tx-config = <&mtl_tx_setup1>;
snps,txpbl = <32>;
snps,rxpbl = <32>;
status = "disabled";

mdio1: mdio {
    compatible = "snps,dwmac-mdio";
    #address-cells = <1>;
    #size-cells = <0>;
};

mtl_rx_setup1: rx-queues-config {
    snps,rx-queues-to-use = <4>;
    snps,rx-sched-sp;

    queue0 {
        snps,dcb-algorithm;
        snps,priority = <0x1>;
        snps,map-to-dma-channel = <0>;
    };

    queue1 {
        snps,dcb-algorithm;
        snps,priority = <0x2>;
        snps,map-to-dma-channel = <1>;
    };

    queue2 {
        snps,dcb-algorithm;
        snps,priority = <0x4>;
        snps,map-to-dma-channel = <2>;
    };

    queue3 {
        snps,dcb-algorithm;
        snps,priority = <0x8>;
        snps,map-to-dma-channel = <3>;
    };
};

mtl_tx_setup1: tx-queues-config {
    snps,tx-queues-to-use = <4>;
    snps,tx-sched-wrr;

    queue0 {
        snps,weight = <0x10>;
        snps,dcb-algorithm;
        snps,priority = <0x1>;
    };

    queue1 {
        snps,weight = <0x12>;
        snps,dcb-algorithm;
        snps,priority = <0x2>;
    };
};

```

```
};  
  
queue2 {  
    snps,weight = <0x14>;  
    snps,dcb-algorithm;  
    snps,priority = <0x4>;  
};  
  
queue3 {  
    snps,weight = <0x18>;  
    snps,dcb-algorithm;  
    snps,priority = <0x8>;  
};  
};
```

**Figure 5–16 Device node for GbEther channel 1 (RZ/V2H)**

- **r9a09g047.dtsi for RZ/G3E:**

In arch/arm64/boot/dts/renesas/r9a09g047.dtsi:

```
eth0: ethernet@15C30000 {
    compatible = "renesas,rzv2h-eqos",
                 "snps,dwc-qos-ethernet-4.10";
    reg = <0 0x15C30000 0 0x10000>;
    interrupts = <GIC_SPI 765 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 767 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 766 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi";
    clocks = <&cpg CPG_MOD 189>,
             <&cpg CPG_MOD 188>,
             <&cpg CPG_MOD 184>,
             <&cpg CPG_MOD 186>,
             <&cpg CPG_MOD 185>,
             <&cpg CPG_MOD 187>,
             <&ptp_clock>;
    clock-names = "master_bus", "slave_bus", "tx",
                  "tx_180", "rx", "rx_180", "ptp_ref";
    resets = <&cpg 176>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
    snps,write-requests = <15>;
    snps,read-requests = <15>;
    snps,burst-map = <0x7>;
};
```

**Figure 5–17 Device node for GbEther channel 0 (RZ/G3E)**

In arch/arm64/boot/dts/renesas/r9a09g047.dtsi:

```
eth1: ethernet@15C40000 {
    compatible = "renesas,rzv2h-eqos",
                 "snps,dwc-qos-ethernet-4.10";

    reg = <0 0x15C40000 0 0x10000>;
    interrupts = <GIC_SPI 780 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 782 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 781 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "macirq", "eth_wake_irq", "eth_lpi";
    clocks = <&cpg CPG_MOD 195>,
             <&cpg CPG_MOD 194>,
             <&cpg CPG_MOD 190>,
             <&cpg CPG_MOD 192>,
             <&cpg CPG_MOD 191>,
             <&cpg CPG_MOD 193>,
             <&ptp_clock>;
    clock-names = "master_bus", "slave_bus", "tx",
                  "tx_180", "rx", "rx_180", "ptp_ref";
    resets = <&cpg 177>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
    snps,write-requests = <15>;
    snps,read-requests = <15>;
    snps,burst-map = <0x7>;
};
```

**Figure 5–18 Device node for GbEther channel 1 (RZ/G3E)**

**Note:** All of the information in above device tree is used for RZ/G3E SoC device tree only.



- **rzg2l-smarc-som.dtsi** for RZ/G2L and RZ/V2L, **rzg2lc-smarc-som.dtsi** for RZ/G2LC, **rzg2ul-smarc.dtsi** for RZ/G2UL and RZ/Five:

In arch/arm64/boot/dts/renesas/rzg2l-smarc-som.dtsi:

```
&eth0 {
    pinctrl-0 = <&eth0_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy0>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy0: ethernet-phy@7 {
        compatible = "ethernet-phy-id0022.1640",
                    "ethernet-phy-ieee802.3-c22";

        reg = <7>;
        interrupt-parent = <&irqc>;
        interrupts = <RZG2L_IRQ2 IRQ_TYPE_LEVEL_LOW>;
        rxc-skew-psec = <2400>;
        txc-skew-psec = <2400>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–19 Device node for enabling GbEther channel 0 (RZ/G2L and RZ/V2L)**

In arch/arm64/boot/dts/renesas/rzg2l-smarc-som.dtsi:

```
&eth1 {
    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy1: ethernet-phy@7 {
        compatible = "ethernet-phy-id0022.1640",
            "ethernet-phy-ieee802.3-c22";

        reg = <7>;
        interrupt-parent = <&irqc>;
        interrupts = <RZG2L_IRQ3 IRQ_TYPE_LEVEL_LOW>;
        rxc-skew-psec = <2400>;
        txc-skew-psec = <2400>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–20 Device node for enabling GbEther channel 1 (RZ/G2L and RZ/V2L)**

In arch/arm64/boot/dts/renesas/rzg2lc-smarc-som.dtsi:

```
&eth0 {
    pinctrl-0 = <&eth0_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy0>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy0: ethernet-phy@7 {
        compatible = "ethernet-phy-id0022.1640",
            "ethernet-phy-ieee802.3-c22";
        reg = <7>;
        interrupt-parent = <&irqc>;
        interrupts = <RZG2L_IRQ0 IRQ_TYPE_LEVEL_LOW>;
        rxc-skew-psec = <2400>;
        txc-skew-psec = <2400>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–21 Device node for enabling GbEther channel 0 (RZ/G2LC)**

- **rzfive-smarc-som.dtsi for RZ/Five:**

In arch/riscv/boot/dts/renesas/rzfive-smarc-som.dtsi:

```
#include <arm64/renesas/rzg2ul-smarc-som.dtsi>
```

In arch/arm64/boot/dts/renesas/rzg2ul-smarc-som.dtsi:

```
#if (!SW_ET0_EN_N)
```

```
&eth0 {
```

```
    pinctrl-0 = <&eth0_pins>;
```

```
    pinctrl-names = "default";
```

```
    phy-handle = <&phy0>;
```

```
    phy-mode = "rgmii-id";
```

```
    status = "okay";
```

```
    phy0: ethernet-phy@7 {
```

```
        compatible = "ethernet-phy-id0022.1640",
```

```
                "ethernet-phy-ieee802.3-c22";
```

```
        reg = <7>;
```

```
        interrupt-parent = <&irqc>;
```

```
        interrupts = <RZG2L_IRQ2 IRQ_TYPE_LEVEL_LOW>;
```

```
        rxc-skew-psec = <2400>;
```

```
        txc-skew-psec = <2400>;
```

```
        rxdv-skew-psec = <0>;
```

```
        txen-skew-psec = <0>;
```

```
        rxd0-skew-psec = <0>;
```

```
        rxd1-skew-psec = <0>;
```

```
        rxd2-skew-psec = <0>;
```

```
        rxd3-skew-psec = <0>;
```

```
        txd0-skew-psec = <0>;
```

```
        txd1-skew-psec = <0>;
```

```
        txd2-skew-psec = <0>;
```

```
        txd3-skew-psec = <0>;
```

```
    };
```

```
};
```

```
#endif
```

**Figure 5–22 Device node for enabling GbEther channel 0 (RZ/Five and RZ/G2UL)**

In arch/arm64/boot/dts/renesas/rzg2ul-smarc-som.dtsi:

```
&eth1 {
    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy1: ethernet-phy@7 {
        compatible = "ethernet-phy-id0022.1640",
            "ethernet-phy-ieee802.3-c22";
        reg = <7>;
        interrupt-parent = <&irqc>;
        interrupts = <RZG2L_IRQ7 IRQ_TYPE_LEVEL_LOW>;
        rxc-skew-psec = <2400>;
        txc-skew-psec = <2400>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–23 Device node for enabling GbEther channel 1 (RZ/Five and RZ/G2UL)**

- **rzg3s-smarc-som.dtsi for RZ/G3S:**

In arch/arm64/boot/dts/renesas/rzg3s-smarc-som.dtsi

```
&eth0 {
    pinctrl-0 = <&eth0_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy0>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy0: ethernet-phy@7 {
        reg = <7>;
        interrupt-parent = <&pinctrl>;
        interrupts = <RZG2L_GPIO(12, 0) IRQ_TYPE_EDGE_FALLING>;
        rxc-skew-psec = <0>;
        txc-skew-psec = <0>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–24 Device node for enabling GbEther channel 0 (RZ/G3S)**

In arch/arm64/boot/dts/renesas/rzg3s-smarc-som.dtsi

```
&eth1 {
    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";
    status = "okay";

    phy1: ethernet-phy@7 {
        reg = <7>;
        interrupt-parent = <&pinctrl>;
        interrupts = <RZG2L_GPIO(12, 1) IRQ_TYPE_EDGE_FALLING>;
        rxc-skew-psec = <0>;
        txc-skew-psec = <0>;
        rxdv-skew-psec = <0>;
        txen-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–25 Device node for enabling GbEther channel 1 (RZ/G3S)**

- **r9a09g056n48-rzv2n-evk.dts for RZ/V2N:**

In arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts

```
&eth0 {
    pinctrl-0 = <&eth0_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy0>;
    phy-mode = "rgmii-id";
    status = "okay";
};

&mdio0 {
    phy0: ethernet-phy@0 {
        compatible = "ethernet-phy-id0022.1640", "ethernet-phy-ieee802.3-c22";
        reg = <0>;
        rxc-skew-psec = <0>;
        txc-skew-psec = <0>;
        rxdv-skew-psec = <0>;
        txdv-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–26 Device node for enabling GbEther channel 0 (RZ/V2N)**



```
In arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts

&eth1 {
    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";
    status = "okay";
};

&mdio1 {
    phy1: ethernet-phy@1 {
        compatible = "ethernet-phy-id0022.1640", "ethernet-phy-ieee802.3-c22";
        reg = <0>;
        rxc-skew-psec = <0>;
        txc-skew-psec = <0>;
        rxdv-skew-psec = <0>;
        txdv-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–27 Device node for enabling GbEther channel 1 (RZ/V2N)**

- **rzv2h-evk-common.dtsi for RZ/V2H**

In arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi

```
&eth0 {  
    pinctrl-0 = <&eth0_pins>;  
    pinctrl-names = "default";  
    phy-handle = <&phy0>;  
    phy-mode = "rgmii-id";  
    status = "okay";  
};  
  
&mdio0 {  
    phy0: ethernet-phy@0 {  
        compatible = "ethernet-phy-id0022.1640", "ethernet-phy-ieee802.3-c22";  
        reg = <0>;  
        rxc-skew-psec = <0>;  
        txc-skew-psec = <0>;  
        rxdv-skew-psec = <0>;  
        txdv-skew-psec = <0>;  
        rxd0-skew-psec = <0>;  
        rxd1-skew-psec = <0>;  
        rxd2-skew-psec = <0>;  
        rxd3-skew-psec = <0>;  
        txd0-skew-psec = <0>;  
        txd1-skew-psec = <0>;  
        txd2-skew-psec = <0>;  
        txd3-skew-psec = <0>;  
    };  
};
```

**Figure 5–28 Device node for enabling GbEther channel 0 (RZ/V2H)**

In arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi

```
&eth1 {
    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";
    status = "okay";
};

&mdio1 {
    phy1: ethernet-phy@1 {
        compatible = "ethernet-phy-id0022.1640", "ethernet-phy-ieee802.3-c22";
        reg = <0>;
        rxc-skew-psec = <0>;
        txc-skew-psec = <0>;
        rxdv-skew-psec = <0>;
        txdv-skew-psec = <0>;
        rxd0-skew-psec = <0>;
        rxd1-skew-psec = <0>;
        rxd2-skew-psec = <0>;
        rxd3-skew-psec = <0>;
        txd0-skew-psec = <0>;
        txd1-skew-psec = <0>;
        txd2-skew-psec = <0>;
        txd3-skew-psec = <0>;
    };
};
```

**Figure 5–29 Device node for enabling GbEther channel 1 (RZ/V2H)**

- **rzg3e-smarc-som.dtsi for RZ/G3E:**

In arch/arm64/boot/dts/renesas/ rzg3e-smarc-som.dtsi

```
&eth0 {
    phy-handle = <&phy0>;
    phy-mode = "rgmii-id";

    pinctrl-0 = <&eth0_pins>;
    pinctrl-names = "default";
    status = "okay";

    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: ethernet-phy@7 {
            compatible = "ethernet-phy-id0022.1640",
                        "ethernet-phy-ieee802.3-c22";

            reg = <7>;
            rxc-skew-psec = <1400>;
            txc-skew-psec = <1400>;
            rxdv-skew-psec = <0>;
            txdv-skew-psec = <0>;
            rxd0-skew-psec = <0>;
            rxd1-skew-psec = <0>;
            rxd2-skew-psec = <0>;
            rxd3-skew-psec = <0>;
            txd0-skew-psec = <0>;
            txd1-skew-psec = <0>;
            txd2-skew-psec = <0>;
            txd3-skew-psec = <0>;

            interrupt-parent = <&icu>;
            interrupts = <RZG2L_IRQ2 IRQ_TYPE_LEVEL_LOW>;
        };
    };
};
```

**Figure 5–30 Device node for enabling GbEther channel 0 (RZ/G3E)**

In arch/arm64/boot/dts/renesas/ rzg3e-smarc-som.dtsi

```
eth1 {
    phy-handle = <&phy1>;
    phy-mode = "rgmii-id";

    pinctrl-0 = <&eth1_pins>;
    pinctrl-names = "default";
    status = "okay";

    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy1: ethernet-phy@7 {
            compatible = "ethernet-phy-id0022.1640",
                        "ethernet-phy-ieee802.3-c22";

            reg = <7>;
            rxc-skew-psec = <1400>;
            txc-skew-psec = <1400>;
            rxdv-skew-psec = <0>;
            txdv-skew-psec = <0>;
            rxd0-skew-psec = <0>;
            rxd1-skew-psec = <0>;
            rxd2-skew-psec = <0>;
            rxd3-skew-psec = <0>;
            txd0-skew-psec = <0>;
            txd1-skew-psec = <0>;
            txd2-skew-psec = <0>;
            txd3-skew-psec = <0>;

            interrupt-parent = <&icu>;
            interrupts = <RZG2L_IRQ15 IRQ_TYPE_LEVEL_LOW>;
        };
    };
};
```

**Figure 5–31 Device node for enabling GbEther channel 1 (RZ/G3E)**

#### 5.3.4 DIP-Switch setting

To enable ETH0 on RZ/G2UL, RZ/Five:

- Set SW\_ET0\_EN\_N (in arch/arm64/boot/dts/renesas/r9a07g043u11-smarc.dts) to 0.
- Set SW1-3 (on SMARC module) to ON.

To enable ETH0 and ETH1 on RZ/G3S:

- Set SW\_CONFIG3 (in arch/arm64/boot/dts/renesas/ [rzg3s-smarc-switches.h](#)) to SW\_ON.to disable DATA2/3 pins of SD2 and enable P12\_0, P12\_1 for Ethernet GPIO interrupt pins.
- Set switch 3 of SW\_CONFIG (on SMARC module) to OFF.

### 5.3.5 Enable/Disable checksum offload

ethx (x: 0, 1, 2, ...)

To enable on tx path: ethtool -K ethx tx on

To enable on rx path: ethtool -K ethx rx on

To disable on tx path: ethtool -K ethx tx off

To disable on rx path: ethtool -K ethx rx off

Revision History	Linux Interface Specification Device Driver Gigabit Ethernet User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 2021	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	8,9	Update information device tree
1.4	May. 31, 2022	—	No modification, keep version to keep consistent with other documents
1.5	June. 24, 2022	—	Add RZ/Five Device
1.6	Sep. 15, 2022	8-15	Update device node to remain consistent with Linux kernel 5.10
1.7	Dec. 15, 2022	—	No modification, keep version to keep consistent with other documents
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents
1.9	Mar. 31, 2024	1, 16	Add support TOE checksum offload
1.10	Mar. 31, 2025	8-16	Correct device tree node for RZ/Five due to it now using same folder with RZ/G2UL
1.11	May. 30, 2025	1, 6	<ul style="list-style-type: none"> <li>- Add MPU information support for both kernel versions v5.10 and v6.1</li> <li>- Update Network Interfaces name.</li> </ul>
1.12	Jun. 30, 2025	—	Add RZ/V2N information
1.13	Jul. 22, 2025	—	Add RZ/G3E information
1.14	Nov. 28, 2025	1, 4	Add information of RZ/G2UL, RZ/V2L and RZ/G3S support for kernel v6.1 Update hardware specification table
1.15	Dec. 19, 2025	—	Add RZ/V2H information
1.16	Mar. 27, 2026	8-9, 16-20	Update directory configuration of RZ/V2N Update information device tree of RZ/V2N



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RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,  
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and RZ/Five



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