

Linux Interface Specification Device Driver RSPI

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group
and RZ/Five Group

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/Five Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
User's manual for Software	Description of RSPI Linux interface Specification	Linux interface Specification Device Driver RSPI	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
RSPI	Renesas Serial Peripheral Interface

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1. Overview

1.1 Overview

This manual explains the driver module that controls the RSPI on RZ/G2L Group, RZ/V2L Group, RZ/V2H Group, RZ/V2N Group, RZ/G3E Group, RZ/G3S Group and RZ/Five Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group and RZ/Five Group.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/V2H Group, RZ/V2N Group, RZ/G3S Group and RZ/G3E Group.

1.2 Function

This module transmits/receives data to/from a device connected to the SPI interface on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2H, RZ/V2N, RZ/G3E, RZ/G3S and RZ/Five and provides the following functions:

- SPI transfer functions
- Data format: 8, 16, 32 bits data word length.
- Bit rate adjustment
 - RZ/G2L series, RZ/V2L, RZ/Five from 500 Kbps to 16,67 Mbps
 - RZ/G3S from 500 Kbps to 25 Mbps
 - RZ/V2H, RZ/V2N and RZ/G3E from 500 Kbps to 50 Mbps
- Buffer configuration
- SSL control function
 - RZ/G2L Group, RZ/V2L, RZ/G3S and RZ/Five: One SSL signal for each channel.
 - RZ/G3E, RZ/V2H and RZ/V2N: Four SSL pins (SSLn0 to SSLn3) each channel.
- Control in master transfer
- Control in slave transfer
- Interrupt sources
- Loop back mode

Connected Device: This module connects the following device on RZ/G2L group, RZ/V2L, RZ/Five, RZ/G3S, RZ/V2N, RZ/V2H and RZ/G3E

Table 1-1 Connected device (RZ/G2L group, RZ/V2L and RZ/Five)

Channel	Connected device	Support Status	Remark
RSPI0	-	No	-
RSPI1	Low speed connector PMOD0	Yes	Female headers (CLK, SSL, TX, RX)
RSPI2	-	No	-

Table 1-2 Connected device RZ/V2N and RZ/V2H

Channel	Connected device	Support Status	Remark
RSPI0	-	No	-
RSPI1	-	No	-
RSPI2	PMOD Type2/2A (SPI) Connector	Yes	Male pins (CLK, SSL, TX, RX)

Table 1-3 Connected device RZ/G3E and RZ/G3S

Channel	Connected device	Support Status	Remark
RSPI0	PMOD0_2A (SPI) Connector	Yes	Male pins (CLK, SSL, TX, RX)
RSPI1	-	No	-
RSPI2	-	No	-

1.3 Reference

1.3.1 Standards

The following table shows the standard that this module corresponds.

Table 1-4 Standard (RZ/G2L group, RZ/V2L, RZ/Five, RZ/G3S, RZ/V2N, RZ/V2H and RZ/G3E)

Reference Number	Issue	Title	Edition	Date
-	-	-	-	-

1.3.2 Related Documents

The following table shows the document related to this module.

Table 1-5 Related documents

Number	Issue	Title	Edition	Date
-	-	-	-	-

1.4 Restrictions

The MPU supports slave mode but RZ/G3E SMARC Evaluation Board Kit and RZ/G3S SMARC Evaluation Board Kit does not support due to Hardware limitation.

1.5 Notice

There is no notice in this module.

2. Terminology

The following table shows the terminology related to this module.

Table 2-1 Terminology

Terms	Explanation
RSPI	Renesas Serial Peripheral Interface
MOSI	Master Out Slave In
MISO	Master In Slave Out
SSL	Slave Select

3. Operating Environment

3.1 Hardware Environment

The following table lists the hardware needed to use this module.

Table 3-1 Hardware specification

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

3.2 Module Configuration

The following figure shows the configuration of this module.

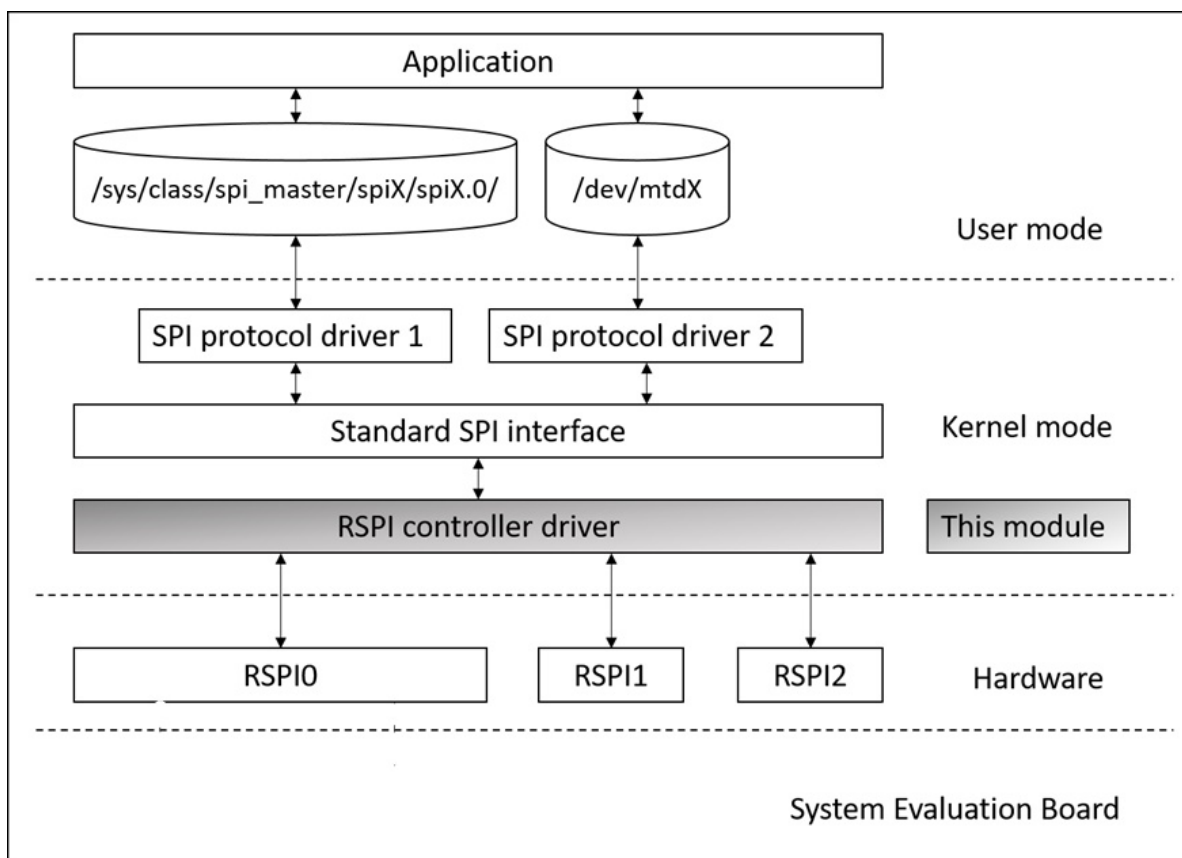


Figure 3-1 RSPI Driver Module configuration (RZ/G2L group, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five)

3.3 State Transition Diagram

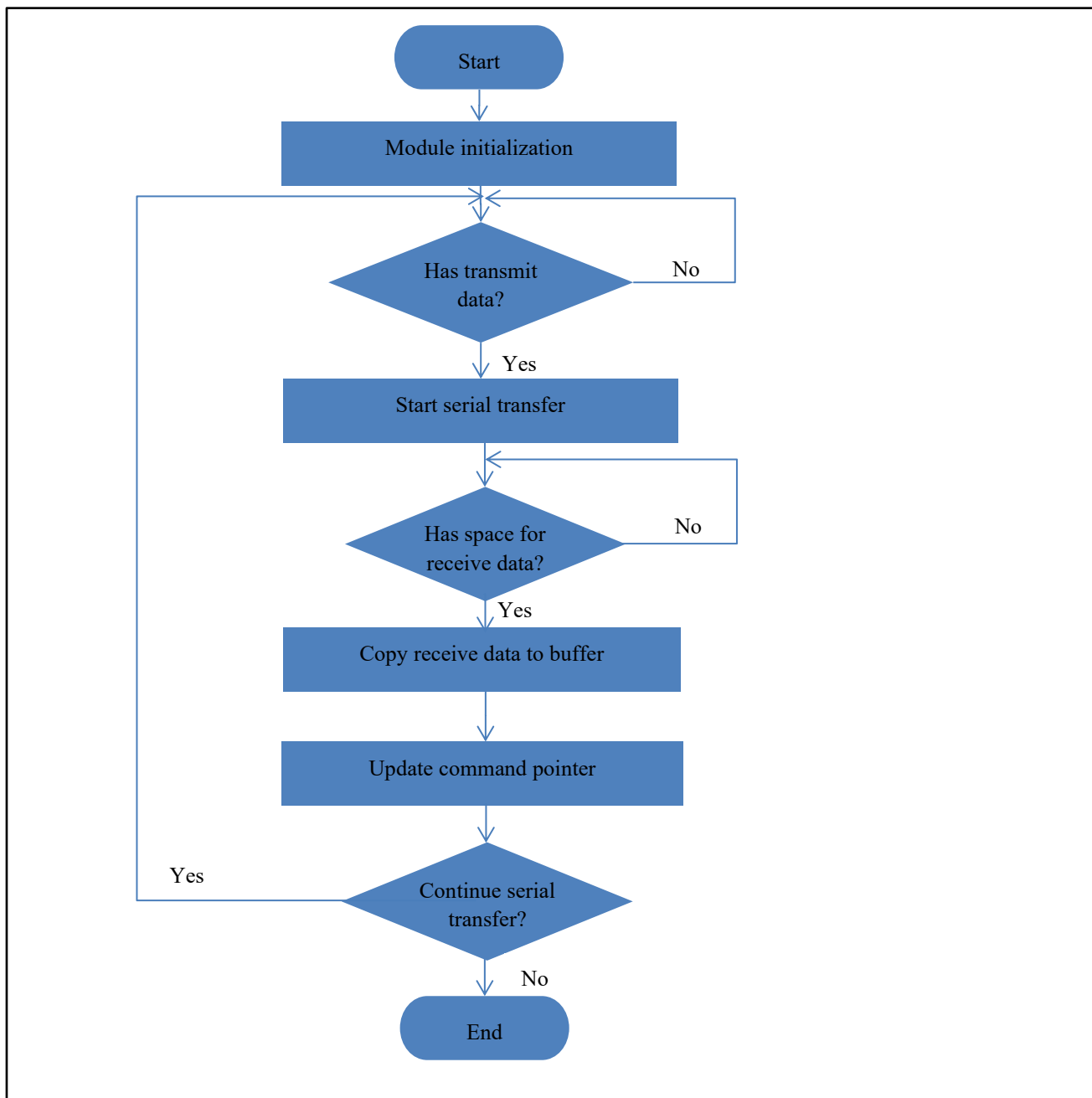


Figure 3-2 RSPI state transition diagram

4. External Interface

4.1 Sysfs Interface

Table 4-1 RSPI device node (RZ/G2L group, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five)

RSPI	Device Node
RSPI0	/sys/class/spi_master/spi0/spi0.0
RSPI1	/sys/class/spi_master/spi1/spi1.0
RSPI2	/sys/class/spi_master/spi2/spi2.0

4.2 External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

5. Integration

5.1 Directory Configuration

The directory configuration is shown below

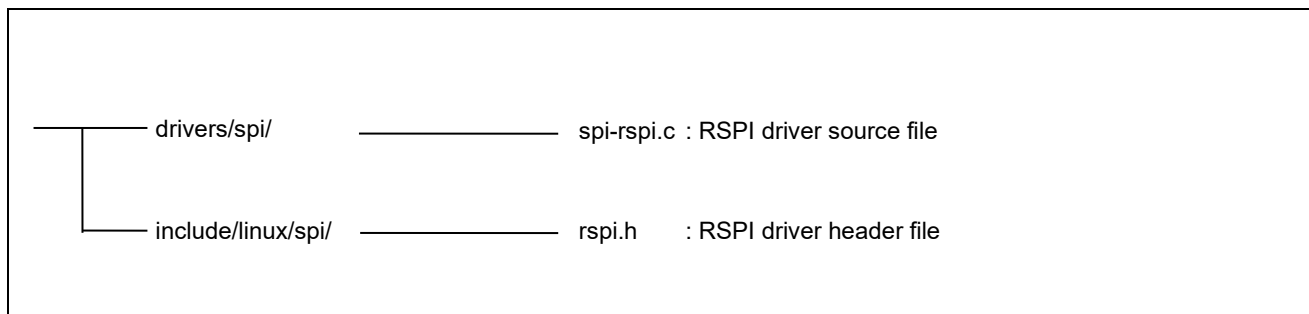


Figure 5-1 Directory configuration (RZ/G2L group, RZ/V2L, RZ/G3S and RZ/Five)

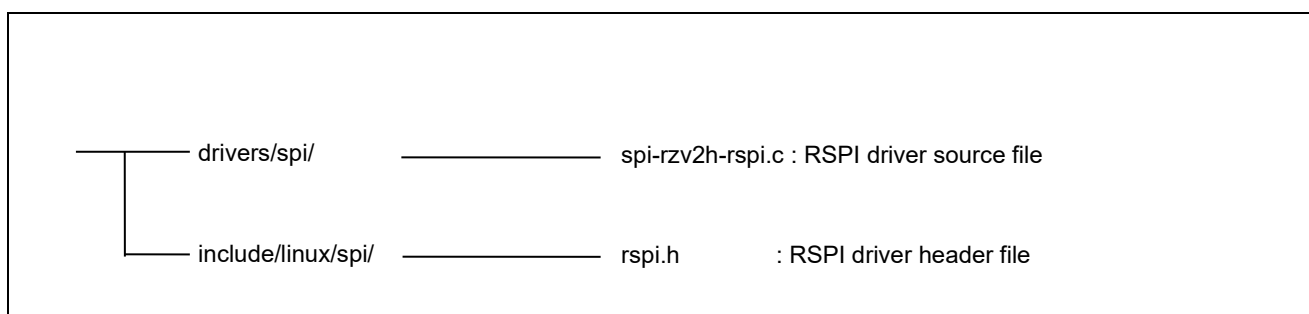


Figure 5-2 Directory configuration (RZ/V2H, RZ/V2N and RZ/G3E)

5.2 Integration Procedure

- Add required device tree settings including RSPI channels to be used, pins definition, and SPI sub-node device's setting
- Add user space interface support
- Add required kernel configurations of the module

5.2.1 Device tree setting

The target files by board are as following:

- rz-smarc-common.dtsi (RZ/G2L, RZ/G2LC and RZ/V2L)
- rzg2ul-smarc.dtsi (RZ/G2UL)
- rzfive-smarc.dtsi (RZ/Five)
- r9a09g056n48-rzv2n-evk.dts (RZ/V2N)
- rzv2h-evk-common.dtsi, r9a09g057h44-rzv2h-evk.dts
and r9a09g057h44-rzv2h-evk-ver2.dts (RZ/V2H)
- rzg3e-smarc.dtsi (RZ/G3E)
- rzg3s-smarc.dtsi (RZ/G3S)

(1) Add rspi1 pin function to rzg2l-smarc-pinfunction.dtsi (for RZ/G2L) and rzg2lc-smarc-pinfunction.dtsi for RZG2LC, rzfive-smarc.dtsi for RZ/Five

```
&pinctrl {
    ....
    spi1_pins: spi1 {
        pinmux = <RZG2L_PORT_PINMUX(44, 0, 1)>,
                <RZG2L_PORT_PINMUX(44, 1, 1)>,
                <RZG2L_PORT_PINMUX(44, 2, 1)>,
                <RZG2L_PORT_PINMUX(44, 3, 1)>;
    };
    ....
}
```

Figure 5-3 Pin function setting (RZ/G2L, RZ/G2LC and RZ/V2L)

```
&pinctrl {
    ....
    #if (SW_ET0_EN_N)
        spi1_pins: rspi1 {
            pinmux = <RZG2L_PORT_PINMUX(4, 0, 2)>, /* CK */
                    <RZG2L_PORT_PINMUX(4, 1, 2)>, /* MOSI */
                    <RZG2L_PORT_PINMUX(4, 2, 2)>, /* MISO */
                    <RZG2L_PORT_PINMUX(4, 3, 1)>; /* SSL */
        };
    #endif
}
```

Figure 5-4 Pin function setting (RZ/G2UL and RZ/Five)

Add rspi2 pin function to r9a09g056n48-rzv2n-evk.dts (for RZ/V2N)

```
&pinctrl {
    ....
    rspi2_pins: rspi2 {
        pinmux = <RZV2N_PORT_PINMUX(B, 3, 5)>, /* MISO */
                <RZV2N_PORT_PINMUX(B, 4, 5)>, /* MOSI */
                <RZV2N_PORT_PINMUX(A, 7, 5)>, /* SSL */
                <RZV2N_PORT_PINMUX(B, 5, 5)>; /* RSPCK */
    };
    ....
}
```

Figure 5-5 Pin function setting RZ/V2N

Add rspi2 pin function to rzv2h-evk-common.dtsi (for RZ/V2H)

```
&pinctrl {
    ....
    rspi2_pins: spi2 {
        pinmux = <RZV2H_PORT_PINMUX(B, 3, 5)>, /* MISO */
                <RZV2H_PORT_PINMUX(B, 4, 5)>, /* MOSI */
                <RZV2H_PORT_PINMUX(A, 7, 5)>, /* SSL */
                <RZV2H_PORT_PINMUX(B, 5, 5)>; /* RSPCK */
    };
    ....
}
```

Figure 5-6 Pin function setting RZ/V2H

Add rspi0 pin function to rzg3e-smarc.dtsi (for RZ/G3E)

```
&pinctrl {
    ....
    spi0_pins: spi0 {
        pinmux = <RZV2H_PORT_PINMUX(M, 4, 2)>, /* MISOA */
                <RZV2H_PORT_PINMUX(M, 5, 2)>, /* MOSIA */
                <RZV2H_PORT_PINMUX(M, 7, 2)>, /* SSLA0 */
                <RZV2H_PORT_PINMUX(M, 6, 2)>; /* RSPCKA */
    };
    ....
}
```

Figure 5-7 Pin function setting RZ/G3E

Add rspi0 pin function to rzg3s-smarc.dtsi (for RZ/G3S)

```
&pinctrl {
    ....
    spi0_pins: spi0 {
        pinmux = <RZG2L_PORT_PINMUX(15, 0, 1)>, /* CK */
                <RZG2L_PORT_PINMUX(15, 1, 1)>, /* MOSI */
                <RZG2L_PORT_PINMUX(15, 2, 1)>, /* MISO */
                <RZG2L_PORT_PINMUX(15, 3, 1)>; /* SSL */
    };
    ....
}
```

Figure 5-8 Pin function setting RZ/G3S

(2) Enable status property

Setting on board RZ/G2UL and RZ/Five SW1-3 = "OFF" and Set "SW_ET0_EN_N = 1" in device-tree

```
&spi1 {
    pinctrl-0 = <&spi1_pins>;
    pinctrl-names = "default";

    status = "okay";
};
```

Figure 5-9 Enable node setting in rz-smarc-common.dtsi for RZ/G2L group, RZ/V2L, RZ/Five

Setting on board RZ/V2N "RSPI2_RSCI9_SEL = 0" in device-tree

```
&rspi2 {
    pinctrl-0 = <&rspi2_pins>;
    pinctrl-names = "default";

    status = "okay";
};
```

Figure 5-10 Enable node setting RZ/V2N

```
&spi0 {
    pinctrl-0 = <&spi0_pins>;
    pinctrl-names = "default";

    status = "okay";
};
```

Figure 5-11 Enable node setting RZ/G3E and RZ/G3S

Setting on board RZ/V2H "RSPI2_RSCI9_SEL = 0" in device-tree

```
&rspi2 {
    pinctrl-0 = <&rspi2_pins>;
    pinctrl-names = "default";

    status = "okay";
};
```

Figure 5-12 Enable node setting RZ/V2H

5.2.2 Master and slave mode devicetree setting

Use the slave device name of the connection destination as the compatible value. The following form is ideal.
Maker name, slave device name.

The editing contents sample for master mode:

```
/* Add a subnode. */
slavedev@0 {
    compatible = "maker,slavedev";
    reg = <0>;
    spi-max-frequency = <25000000>;
    spi-cpha;
    spi-cpol;
};
```

Figure 5-13 The setting for master mode in spi enable node (RZ/G2L group, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five)

The editing contents sample for slave mode:

```
spi-slave;
slave {
    compatible = "maker,slavedev";
    spi-cpha;
    spi-cpol;
};
```

Figure 5-14 The setting for slave mode in spi enable node (RZ/G2L, RZ/G2LC, RZ/V2L, RZ/V2N, RZ/V2H and RZ/Five)

5.2.3 Master and slave mode device Interface

Add the compatible value of the subnode to the next file.
"Maker name, slave device name"; file : drivers/spi/spidev.c

```
static const struct spi_device_id spidev_spi_ids[] = {
    ...
    { .name = "slavedev" },      <-- Add this line
    {},
};
static const struct of_device_id spidev_dt_ids[] = {
    ...
    { .compatible = "maker,slavedev", .data = &spidev_of_check },    <-- Add this line.
    {},
};
```

Figure 5-15 Add slavedev compatible (RZ/G2L group, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five)

5.2.4 Kernel Configuration

To enable the function of this module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  [*] SPI support --->
    [*] Renesas RSPI/QSPI controller
```

Figure 5-16 Kernel configuration (RZ/G2L group, RZ/V2L, RZ/G3S and RZ/Five)

```
Device Drivers --->
  [*] SPI support --->
    [*] Renesas RZ/V2H RSPI controller
```

Figure 5-17 Kernel configuration RZ/V2H, RZ/V2N and RZ/G3E

Add the configuration to enable slave mode:

arch/arm64/configs/defconfig:

```
CONFIG_SPI_SLAVE=y
```

Note:

DIP-SWITCH SETTING:

Set up dip switch to enable RSPI1:

- RZ/G2LC: Define SW_RSPI_CAN (in rzg2lc-smarc.dtsi) is 0 and sw1-4 (on module board) is ON.
- RZ/G2UL: Define SW_ET0_EN_N (in rzg2ul-smarc.dtsi) is 1 and sw1-3 (on module board) is OFF.
- RZ/Five: Define SW_ET0_EN_N (in rzfive-smarc.dtsi) is 1 and sw1-3 (on module board) is OFF.

SEL_FUNCTION SETTING:

- RZ/V2N: Define RSPI2_RSCI9_SEL (in r9a09g056n48-rzv2n-evk.dts) is 0.
- RZ/V2H: Define RSPI2_RSCI9_SEL (in r9a09g057h44-rzv2h-evk.dts, or r9a09g056h44-rzv2h-evk-ver2.dts) is 0.

Please be aware of 5V/3.3V voltage switching.

Enable RSPI's DMA for RZ/G2{L, LC, UL} and RZ/V2L:

```
&spi1 {
.....
+       dmas = <&dmac 0x2e99>, <&dmac 0x2e9a>;
+       dma-names = "tx", "rx";
.....
};
```

Please use the configure as below to enable DMA if RSPI0, RSPI2 are used.

RSPI0:

Define in devicetree:

```
dmas = <&dmac 0x2e95>, <&dmac 0x2e96>;
dma-names = "tx", "rx";
```

RSPI2:

Define in devicetree:

```
dmas = <&dmac 0x2e9d>, <&dmac 0x2e9e>;
dma-names = "tx", "rx";
```

Enable RSPI's DMA for RZ/G3E, RZ/V2N and RZ/V2H:

```
&spi0 {
.....
+       dmas = <&dmac1 0x7F448D>, <&dmac1 0x7F448C>;
+       dma-names = "tx", "rx";
.....
};
```

Please use the configure as below to enable DMA if RSPI1, RSPI2 are used. (RZ/G3E, RZ/V2N and RZ/V2H)

RSPI1:

Define in devicetree:

```
dmas = <&dmac1 0x7F448F>, <&dmac1 0x7F448E>;
dma-names = "tx", "rx";
```

RSPI2:

Define in devicetree:

```
dmas = <&dmac1 0x7F4491>, <&dmac1 0x7F4490>;
dma-names = "tx", "rx";
```

Enable RSPI's DMA for RZ/G3S:

```
&spi0 {  
.....  
+      dmas = <&dmac 0x2ed9>, <&dmac 0x2eda>;  
+      dma-names = "tx", "rx";  
.....  
};
```

Please use the configure as below to enable DMA if RSPI1, RSPI2 are used.(RZ/G3S)

RSPI1:

Define in devicetree:

```
      dmas = <&dmac1 0x2edd>, <&dmac1 0x2ede>;  
      dma-names = "tx", "rx";
```

RSPI2:

Define in devicetree:

```
      dmas = <&dmac 0x2ee1>, <&dmac 0x2ee2>;  
      dma-names = "tx", "rx";
```


5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

5.3.2 Kernel Parameters

There are no kernel parameters.

Revision History	Linux Interface Specification Device Driver RSPI User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 2021	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents.
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	7	Update devicetree setting
1.4	May. 31, 2022	9	Add DMA definitions note.
1.5	June. 24, 2022	9	Add RZ/Five device Update: Modify DMA definitions note
1.6	Sep. 15, 2022	—	No modification
1.7	Dec. 15, 2022	—	No modification
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents.
1.9	Mar. 31, 2024	8	Update devicetree setting for slave device in master mode
1.10	May. 30, 2025	1	Add MPU information support for both kernel versions v5.10 and v6.1. Correct 1.2 Function
		8	Correct Figure 5-5
1.11	Jun. 30, 2025	—	Add RZ/V2N support information
1.12	Jul. 22, 2025	—	Add RZ/G3E support information
		10	Replace name 5.2.2 to Slave mode devicetree setting
		11	Replace name 5.2.3 to Slave mode device Interface
1.13	Nov. 28, 2025	1	Add information of RZ/G2UL,RZ/V2L and RZ/G3S support for kernel v6.1 Update 1.2 function for RZ/G2L series, RZ/V2L, RZ/Five, RZ/G3E and RZ/G3S
		15	Update enable RSPI's DMA for RZ/G3E and RZ/G3S
		—	
1.14	Dec. 19, 2025	—	Add RZ/V2H support information
		16	Update node DMA V2N
1.15	Mar. 27, 2026	1	Update RZ/G3S maximum transfer speed to 25MHz
		5	Update product name for RZ/V2N EVK boards
		—	Update RZ/V2N and RZ/V2H support information

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