

Linux Interface Specification Device Driver USB2.0 Host

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and
RZ/Five

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/G3E Group, RZ/G3S Group, RZ/V2H Group and RZ/V2N Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
User's manual for Software	Description of USB Linux interface Specification	Linux interface Specification Device Driver USB2.0 Host	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols
3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Description
BSP	Board Support Package
CPRM	Content Protection for Recordable Media
DMA	Direct Memory Access
DMAC	DMA Controller
EHCI	Enhanced Host Controller Interface
GPL	GNU General Public License
LGPL	GNU Lesser General Public License
MTD	Memory Technology Device
NCQ	Native Command Queuing
OHCI	Open Host Controller Interface
OSS	Open Source Software
USB	Universal Serial Bus
VLP	Verified Linux Package

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1. Overview

1.1 Overview

This manual explains the driver module (this module) that controls the USB 2.0 Host controller on RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2H and RZ/V2N Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L group, RZ/G3S and RZ/Five.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/G3E, RZ/G3S, RZ/V2H and RZ/V2N.

1.2 Function

This module controls the USB 2.0 Host controller on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2H and RZ/V2N transmits/receives data to/from the USB device.

The function of this module is based on OHCI, EHCI of standard Linux.

- USB memory device support
- USB keyboard device support
- USB mouse device support

1.3 Connected Port

This module supports RZ/G2L, RZ/V2L, RZ/Five, RZ/V2N, RZ/G3S, RZ/G3E and RZ/V2H evaluation kit as below tables.

Table 1-1 Connected Port (RZ/G2L, RZ/V2L and RZ/Five)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	CN11	Type Micro AB connector
1	USB2.0 Host	CN12	Type A connector

Table 1-2 Connected Port (RZ/V2N)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	CN2	Type Micro AB connector

Table 1-3 Connected Port (RZ/G3E and RZ/G3S)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	USB0_OTG	Type Micro AB connector
1	USB2.0 Host	USB1B-1A_HOST (Top)	Type A connector
2	USB2.0 Host	USB1B-1A_HOST (Bottom)	Type A connector

Table 1-4 Connected Port (RZ/V2H)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	USB0_OTG	Type Micro AB connector
1	USB2.0 Host	USB1B-1A_HOST	Type A connector

1.4 Reference

1.4.1 Standard

There is no document related to standard for this module.

1.4.2 Related Documents

There is no document related to this module.

1.5 Restrictions

There is no restriction in this module.

2. Terminology

The following table shows the terminology related to this module.

Table 2-1 Terminology

Terms	Explanation
USB	Universal Serial Bus
HCD	Host Controller Driver
OHCI	Open Host Controller Interface
EHCI	Enhanced Host Controller Interface
OTG	On-The-GO
ADP	Attach Detection Protocol
HNP	Host Negotiation Protocol
SRP	Session Request Protocol

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this module.

Table 3.1 Hardware Environment

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

3.2 Module Configuration

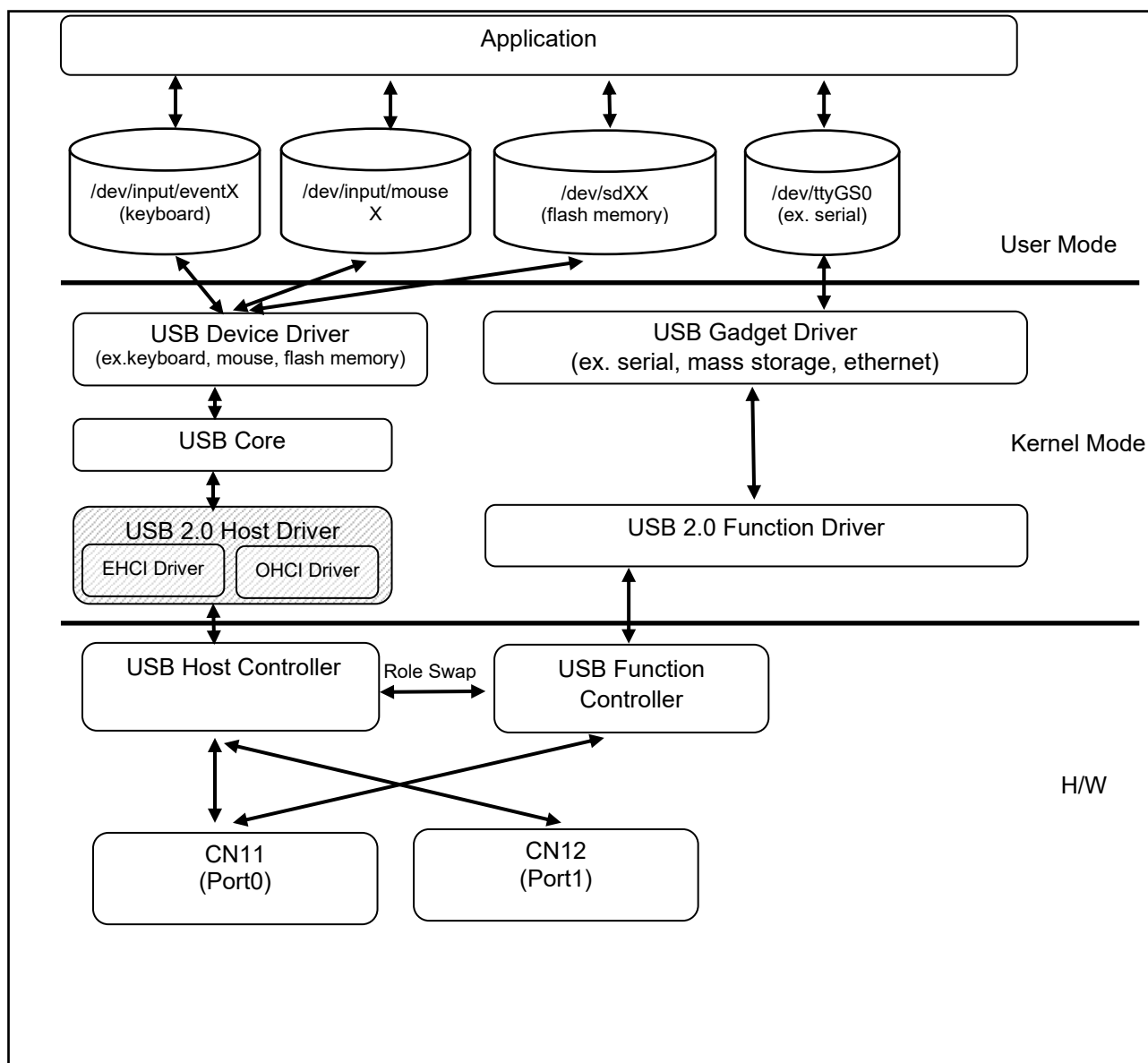


Figure 3-1 Modules Configuration (RZ/G2L Group, RZ/V2L Group, and RZ/Five)

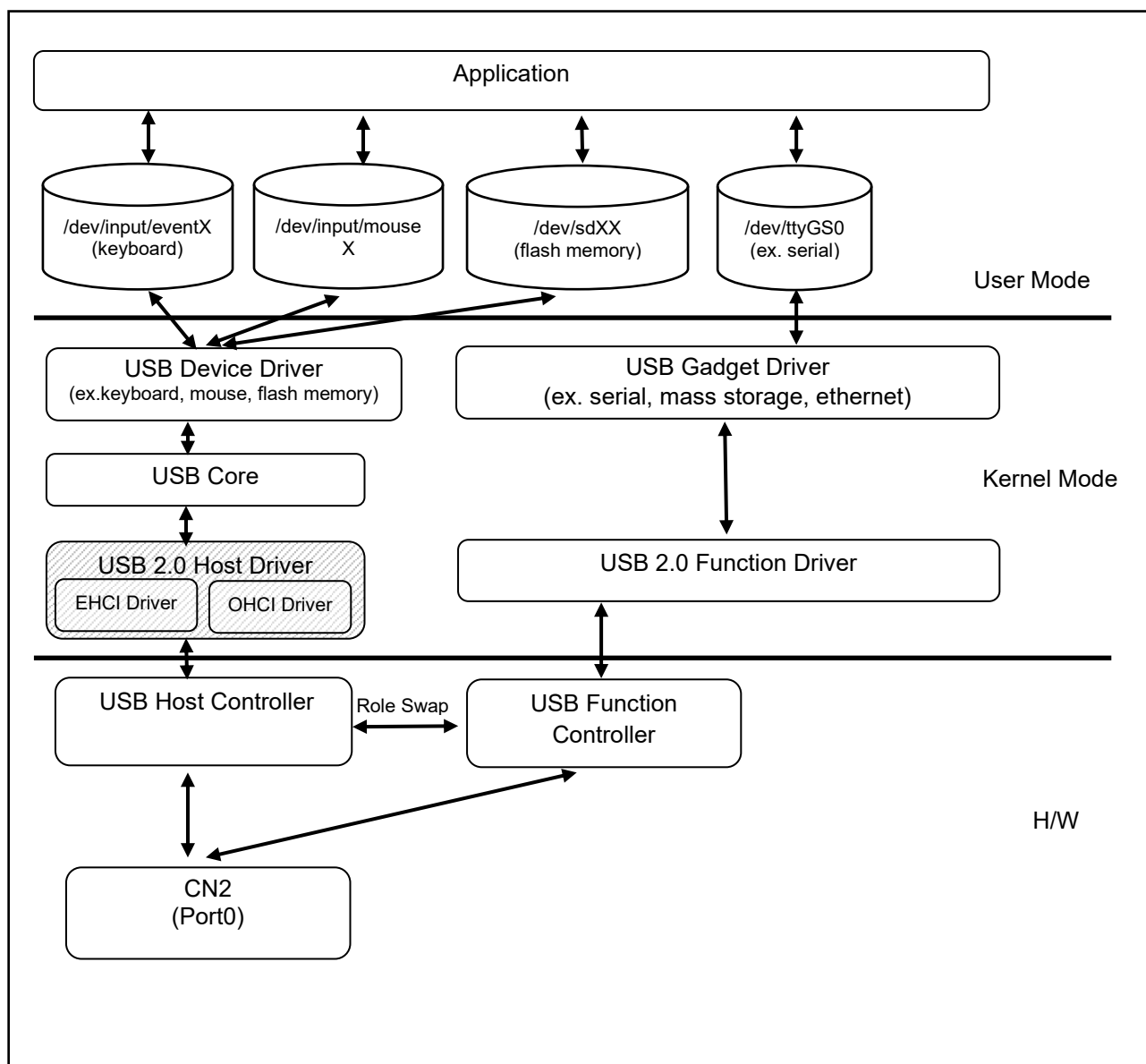


Figure 3-2 Modules Configuration (RZ/V2N)

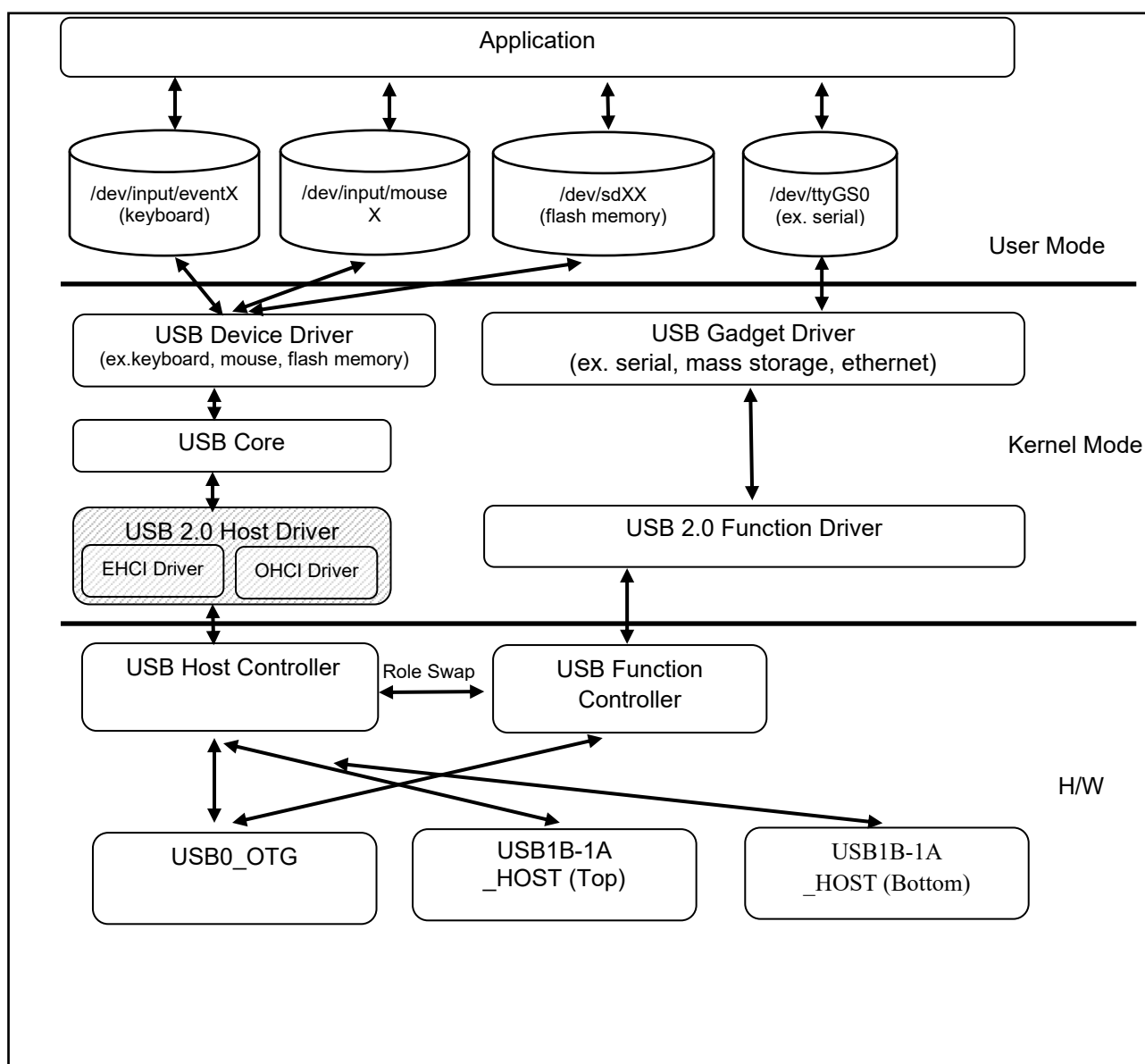


Figure 3-3 Modules Configuration (RZ/G3E and RZ/G3S)

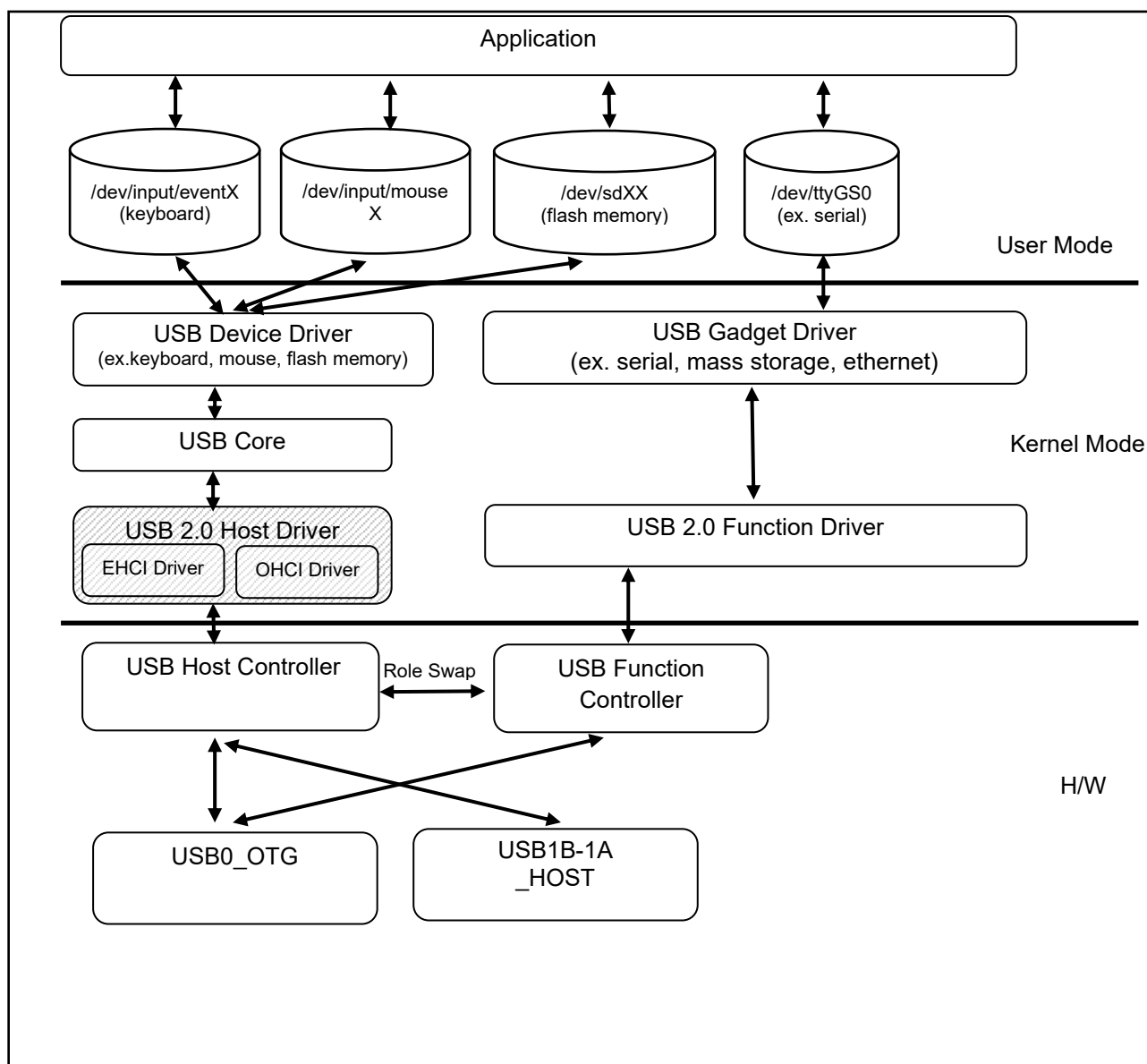


Figure 3-4 Modules Configuration (RZ/V2H)

3.3 State Transition Diagram

The following table shows the state transition of this module.

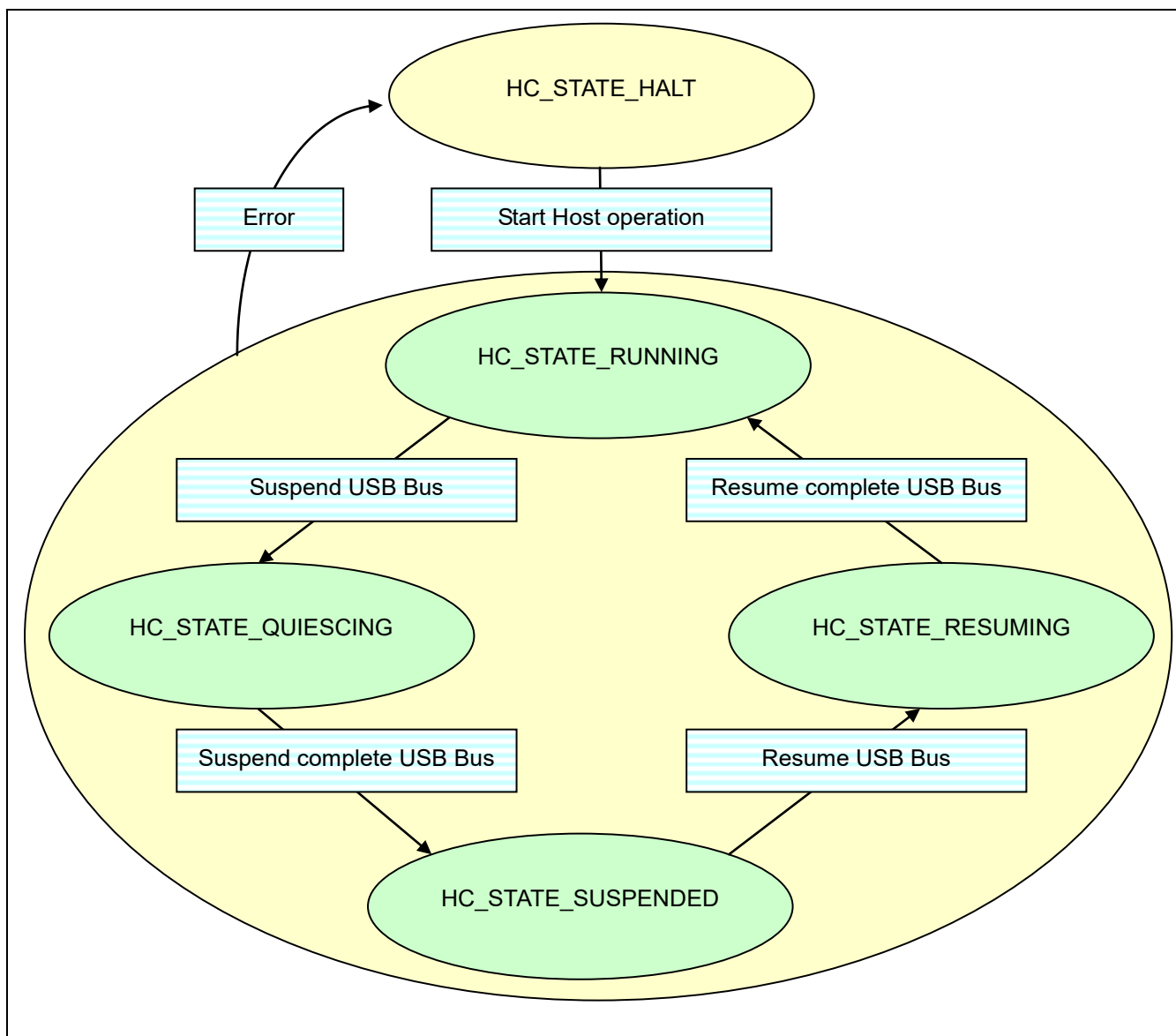


Figure 3-5 State Transition Diagram (RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2H and RZ/V2N)

4. External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

The device node of this module is shown below.

Table 4-1 Device Node (RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five)

Device	Channel	Device node	Major number	Minor number
Keyboard	0 – 1	/dev/input/eventX *	13	64 - 66
Mouse	0 – 1	/dev/input/mouseX1	13	32 - 33
USB memory	0 – 1	/dev/sdX1	8	0 - 1

Table 4-2 Device Node (RZ/V2N, RZ/G3E, RZ/V2H)

Device	Channel	Device node	Major number	Minor number
Keyboard	0	/dev/input/eventX *	13	64 - 66
Mouse	0	/dev/input/mouseX1	13	32 - 33
USB memory	0	/dev/sdX1	8	0 - 1

Note: * The numerical value may differ according to the system. (ex, /dev/input/event0)

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.

```

—drivers/phy/renesas/ — phy-rcar-gen3-usb2.c: R-Car Gen3 / RZ G2 USB phy driver for USB 2.0.
—drivers/reset/ — reset-rzg2l-usbphy-ctrl.c: USBPHY control driver source file
—drivers/host/ — ehci-platform.c: ehci driver source file
—drivers/host/ — ohci-platform.c: ohci driver source file
—drivers/regulator/ — renesas-usb-vbus-regulator.c: USB vbus output regulator driver source file

```

Figure 5-1 Directory Configuration (RZ/G2L Group, RZ/V2L Group, RZ/Five and RZ/G3S)

```

—drivers/phy/renesas/ — phy-rcar-gen3-usb2.c: R-Car Gen3 / RZ G2 USB phy driver for USB 2.0
                        and OTG VBUS control output regulator.
—drivers/reset/ — reset-rzv2h-usbphy-ctrl.c: USBPHY control driver source file
—drivers/host/ — ehci-platform.c: ehci driver source file
—drivers/host/ — ohci-platform.c: ohci driver source file
—drivers/mux/ — rzv2h-usb-vbenctl.c: VBUSEN control driver source file

```

Figure 5-2 Directory Configuration (RZ/G3E, RZ/V2H and RZ/V2N)

5.1.1 Device tree definition

Below figure lists the necessary properties to support USB 2.0 host in RZ/G2L, RZ/G2LC, RZ/G2UL and RZ/V2L Evaluation Board Kit.

```

phyrst: usbphy-ctrl@11c40000 {
    compatible = "renesas,r9a07g043-usbphy-ctrl",
                "renesas,rzg2l-usbphy-ctrl";
    reg = <0 0x11c40000 0 0x10000>;
    clocks = <&cpg CPG_MOD R9A07G043_USB_PCLK>;
    resets = <&cpg R9A07G043_USB_PRESETN>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    status = "disabled";

    usb0_vbus_otg: regulator-vbus {
        regulator-name = "vbus";
    };
};
ohci0: usb@11c50000 {
    compatible = "generic-ohci";
    reg = <0 0x11c50000 0 0x100>;
    interrupts = <SOC_PERIPHERAL_IRQ(91) IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G043_USB_PCLK>,
            <&cpg CPG_MOD R9A07G043_USB_U2H0_HCLK>;
    resets = <&phyrst 0>,

```

```

        <&cpg R9A07G043_USB_U2H0_HRESETN>;
        phys = <&usb2_phy0 1>;
        phy-names = "usb";
        power-domains = <&cpg>;
        status = "disabled";
};

ehci0: usb@11c50100 {
    compatible = "generic-ehci";
    reg = <0 0x11c50100 0 0x100>;
    interrupts = <SOC_PERIPHERAL_IRQ(92) IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G043_USB_PCLK>,
            <&cpg CPG_MOD R9A07G043_USB_U2H0_HCLK>;
    resets = <&phyrst 0>,
            <&cpg R9A07G043_USB_U2H0_HRESETN>;
    phys = <&usb2_phy0 2>;
    phy-names = "usb";
    companion = <&ohci0>;
    power-domains = <&cpg>;
    status = "disabled";
};

ohci1: usb@11c70000 {
    compatible = "generic-ohci";
    reg = <0 0x11c70000 0 0x100>;
    interrupts = <SOC_PERIPHERAL_IRQ(96) IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G043_USB_PCLK>,
            <&cpg CPG_MOD R9A07G043_USB_U2H1_HCLK>;
    resets = <&phyrst 1>,
            <&cpg R9A07G043_USB_U2H1_HRESETN>;
    phys = <&usb2_phy1 1>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

ehci1: usb@11c70100 {
    compatible = "generic-ehci";
    reg = <0 0x11c70100 0 0x100>;
    interrupts = <SOC_PERIPHERAL_IRQ(97) IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G043_USB_PCLK>,
            <&cpg CPG_MOD R9A07G043_USB_U2H1_HCLK>;
    resets = <&phyrst 1>,
            <&cpg R9A07G043_USB_U2H1_HRESETN>;
    phys = <&usb2_phy1 2>;
    phy-names = "usb";
    companion = <&ohci1>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 5-3: Enable USB2.0 host device nodes (r9a07g044.dtsi for G2L and G2LC, r9a07g043.dtsi for G2UL, r9a07g054.dtsi for V2L and r9a07g043.dtsi for RZ/Five)

Note: All the information in above device tree is used for RZ/G2L, RZ/G2LC, RZ/G2UL and RZ/V2L except: **clocks and resets:** R9A07G044_ for RZ/G2L, RZ/G2LC, R9A07G043_ for RZ/G2UL and R9A07G054_ for RZ/V2L, R9A07G043F_ for RZ/Five

Interrupts:

Nodes	RZ/G2{L, LC, UL} and RZ/V2L	RZ/Five
ohci0	<SOC_PERIPHERAL_IRQ(91) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(123) IRQ_TYPE_LEVEL_HIGH>
ohci1	<SOC_PERIPHERAL_IRQ(96) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(128) IRQ_TYPE_LEVEL_HIGH>
ehci0	<SOC_PERIPHERAL_IRQ(92) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(124) IRQ_TYPE_LEVEL_HIGH>
ehci1	<SOC_PERIPHERAL_IRQ(97) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(129) IRQ_TYPE_LEVEL_HIGH>

Below figure lists the necessary properties to support USB 2.0 host in RZ/V2N Evaluation Board Kit.

```

usb20phyrst: usb20phy-reset@15830000 {
    compatible = "renesas,r9a09g056-usb2phy-reset",
                "renesas,r9a09g057-usb2phy-reset";
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <0>;
    #mux-state-cells = <1>;
    status = "disabled";
};

usb2_phy0: usb-phy@15800200 {
    compatible = "renesas,usb2-phy-r9a09g056", "renesas,usb2-phy-
r9a09g057";

    reg = <0 0x15800200 0 0x700>;
    interrupts = <GIC_SPI 745 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>,
            <&cpg CPG_CORE R9A09G056_USB2_0_CLK_CORE0>;
    clock-names = "fck", "usb_x1";
    resets = <&usb20phyrst>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    mux-states = <&usb20phyrst 1>;
    status = "disabled";

    usb2_phy0_vbus_otg: vbus-regulator {
        regulator-name = "USB2PHY0-VBUS-OTG";
        status = "disabled";
    };
};

ohci0: usb@15800000 {
    compatible = "generic-ohci";
    reg = <0 0x15800000 0 0x100>;
    interrupts = <GIC_SPI 742 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb6>;
    resets = <&usb20phyrst>, <&cpg 0xac>;
    phys = <&usb2_phy0 1>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

```

```

    };

    ehci0: usb@15800100 {
        compatible = "generic-ehci";
        reg = <0 0x15800100 0 0x100>;
        interrupts = <GIC_SPI 743 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb6>;
        resets = <&usb20phyrst>, <&cpg 0xac>;
        phys = <&usb2_phy0 2>;
        phy-names = "usb";
        companion = <&ohci0>;
        power-domains = <&cpg>;
        status = "disabled";
    };

```

Figure 5-4: Enable USB2.0 host device nodes (r9a09g056.dtsi for RZ/V2N)

Note: All the information in above device tree is used for RZ/V2N

Below figure lists the necessary properties to support USB 2.0 host in RZ/G3E Evaluation Board Kit.

```

usb20phyrst: usb20phy-ctrl@15830000 {
    compatible = "renesas,r9a09g047-usbphy-ctrl",
        "renesas,rzv2h-usbphy-ctrl";
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    status = "disabled";
};

usb21phyrst: usb21phy-ctrl@15840000 {
    compatible = "renesas,r9a09g047-usbphy-ctrl",
        "renesas,rzv2h-usbphy-ctrl";
    reg = <0 0x15840000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb7>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    status = "disabled";
};

ohci0: usb@15800000 {
    compatible = "generic-ohci";
    reg = <0 0x15800000 0 0x100>;
    interrupts = <GIC_SPI 742 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>;
    resets = <&cpg 0xac>,
        <&usb20phyrst 0>;
    phys = <&usb2_phy0 1>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

ohci1: usb@15810000 {
    compatible = "generic-ohci";
    reg = <0 0x15810000 0 0x100>;
    interrupts = <GIC_SPI 747 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb4>;

```

```

        resets = <&cpg 0xad>,
                <&usb21phyrst 1>;
        phys = <&usb2_phy1 1>;
        phy-names = "usb";
        power-domains = <&cpg>;
        status = "disabled";
    };
    ehci0: usb@15800100 {
        compatible = "generic-ehci";
        reg = <0 0x15800100 0 0x100>;
        interrupts = <GIC_SPI 743 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb3>;
        resets = <&cpg 0xac>,
                <&usb20phyrst 0>;
        phys = <&usb2_phy0 2>;
        phy-names = "usb";
        companion = <&ohci0>;
        power-domains = <&cpg>;
        status = "disabled";
    };
    ehci1: usb@15810100 {
        compatible = "generic-ehci";
        reg = <0 0x15810100 0 0x100>;
        interrupts = <GIC_SPI 748 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb4>;
        resets = <&cpg 0xad>,
                <&usb21phyrst 1>;
        phys = <&usb2_phy1 2>;
        phy-names = "usb";
        companion = <&ohci1>;
        power-domains = <&cpg>;
        status = "disabled";
    };
};

```

Figure 5-5: Enable USB2.0 host device nodes (r9a09g047.dtsi for RZ/G3E)

Note: All the information in above device tree is used for RZ/G3E

Below figure lists the necessary properties to support USB 2.0 host in RZ/V2H Evaluation Board Kit.

```

usb20phyrst: usb20phy-ctrl@15830000 {
    compatible = "renesas,r9a09g057-usb2phy-reset",
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <0>;
    status = "disabled";
};
usb21phyrst: usb21phy-reset@15840000 {
    compatible = "renesas,r9a09g057-usb2phy-reset";
    reg = <0 0x15840000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <0>;
    status = "disabled";
};
ohci0: usb@15800000 {

```

```

        compatible = "generic-ohci";
        reg = <0 0x15800000 0 0x100>;
        interrupts = <GIC_SPI 742 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb6>;
        resets = <&usb20phyrst>, <&cpg 0xac>;
        phys = <&usb2_phy0 1>;
        phy-names = "usb";
        power-domains = <&cpg>;
        status = "disabled";
    };
    ohci1: usb@15810000 {
        compatible = "generic-ohci";
        reg = <0 0x15810000 0 0x100>;
        interrupts = <GIC_SPI 747 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb4>, <&cpg CPG_MOD 0xb7>;
        resets = <&usb21phyrst>, <&cpg 0xad>;
        phys = <&usb2_phy1 1>;
        phy-names = "usb";
        power-domains = <&cpg>;
        status = "disabled";
    };
    ehci0: usb@15800100 {
        compatible = "generic-ehci";
        reg = <0 0x15800100 0 0x100>;
        interrupts = <GIC_SPI 743 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb6>;
        resets = <&usb20phyrst>, <&cpg 0xac>;
        phys = <&usb2_phy0 2>;
        phy-names = "usb";
        companion = <&ohci0>;
        power-domains = <&cpg>;
        status = "disabled";
    };
    ehci1: usb@15810100 {
        compatible = "generic-ehci";
        reg = <0 0x15810100 0 0x100>;
        interrupts = <GIC_SPI 748 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD 0xb4>, <&cpg CPG_MOD 0xb7>;
        resets = <&usb21phyrst>, <&cpg 0xad>;
        phys = <&usb2_phy1 2>;
        phy-names = "usb";
        companion = <&ohci1>;
        power-domains = <&cpg>;
        status = "disabled";
    };
};

```

Figure 5-6: Enable USB2.0 host device nodes (r9a09g057.dtsi for RZ/V2H)

Note: All the information in above device tree is used for RZ/V2H

Below figure lists the necessary properties to support USB 2.0 host in RZ/G3S Evaluation Board Kit.

```

phyrst: usbphy-ctrl@11e00000 {
    compatible = "renesas,r9a08g045-usbphy-ctrl";
    reg = <0 0x11e00000 0 0x10000>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>;
    resets = <&cpg R9A08G045_USB_PRESETN>;
};

```

```

        power-domains = <&cpg>;
        #reset-cells = <1>;
        renesas,sysc-pwrrdy = <&sysc 0xd70 0x1>; (*1)
        status = "disabled";

        usb0_vbus_otg: regulator-vbus {
            regulator-name = "vbus";
        };
};

ohci0: usb@11e10000 {
    compatible = "generic-ohci";
    reg = <0 0x11e10000 0 0x100>;
    interrupts = <GIC_SPI 75 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
            <&cpg CPG_MOD R9A08G045_USB_U2H0_HCLK>;
    resets = <&phyrst 0>,
            <&cpg R9A08G045_USB_U2H0_HRESETN>;
    phys = <&usb2_phy0 1>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

ohci1: usb@11e30000 {
    compatible = "generic-ohci";
    reg = <0 0x11e30000 0 0x100>;
    interrupts = <GIC_SPI 80 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
            <&cpg CPG_MOD R9A08G045_USB_U2H1_HCLK>;
    resets = <&phyrst 1>,
            <&cpg R9A08G045_USB_U2H1_HRESETN>;
    phys = <&usb2_phy1 1>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

ehci0: usb@11e10100 {
    compatible = "generic-ehci";
    reg = <0 0x11e10100 0 0x100>;
    interrupts = <GIC_SPI 76 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
            <&cpg CPG_MOD R9A08G045_USB_U2H0_HCLK>;
    resets = <&phyrst 0>,
            <&cpg R9A08G045_USB_U2H0_HRESETN>;
    phys = <&usb2_phy0 2>;
    phy-names = "usb";
    companion = <&ohci0>;
    power-domains = <&cpg>;
    status = "disabled";
};

ehci1: usb@11e30100 {
    compatible = "generic-ehci";
    reg = <0 0x11e30100 0 0x100>;
    interrupts = <GIC_SPI 81 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,

```



```
        <&cpg CPG_MOD R9A08G045_USB_U2H1_HCLK>;
        resets = <&phyrst 1>,
        <&cpg R9A08G045_USB_U2H1_HRESETN>;
        phys = <&usb2_phy1 2>;
        phy-names = "usb";
        companion = <&ohci1>;
        power-domains = <&cpg>;
        status = "disabled";
    };
```

Figure 5-7: Enable USB2.0 host device nodes (r9a08g045.dtsi for RZ/G3S)

Note: All the information in above device tree is used for RZ/G3S

(*)1: renesas,sysc-pwrrdy property (only for RZ/G3S) handle SYS_USB_PWRRDY register to control USB region power.

Enable USB 2.0 Host in RZ/G2L, RZ/G2LC, RZ/G2UL and RZ/V2L Evaluation Board Kit.

```
&phyrst {
    status = "okay";
};
&ohci0 {
    dr_mode = "otg";
    status = "okay";
};

&ohci1 {
    status = "okay";
};

&ehci0 {
    dr_mode = "otg";
    status = "okay";
};

&ehci1 {
    status = "okay";
};

&usb2_phy0 {
    vbus-supply = <&usb0_vbus_otg>;
    status = "okay";
};

&usb2_phy1 {
    status = "okay";
};
```

Figure 5-8: Enable USB 2.0 Host (rz-smarc-common.dtsi for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five)

Below figure enables the necessary properties to support USB 2.0 host in RZ/V2N Evaluation Board Kit.

```
&usb20phyrst {
    status = "okay";
};

&usb2_phy0_vbus_otg {
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb20_pins>;
    pinctrl-names = "default";

    vbus-supply = <&usb2_phy0_vbus_otg>;
    status = "okay";
};

&ohci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
    status = "okay";
};

&ehci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
    status = "okay";
};
```

Figure 5-9: Enable USB 2.0 Host (r9a09g056n48-rzv2n-evk.dts for RZ/V2N)

Below figure enables the necessary properties to support USB 2.0 host in RZ/G3E Evaluation Board Kit.

```
&usb20phyrst {
    status = "okay";
};

&usb21phyrst {
    status = "okay";
};

&ohci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
    status = "okay";
};

&ohci1 {
    memory-region = <&global_cma>;
    status = "okay";
};

&ehci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
};
```

```
        status = "okay";
};
&ehci1 {
    memory-region = <&global_cma>;
    status = "okay";
};
```

Figure 5-10: Enable USB 2.0 Host (rzg3e-smarc.dtsi for RZ/G3E)

Below figure enables the necessary properties to support USB 2.0 host in RZ/G3S SMARC Evaluation Board Kit.

```
&phyrst {
    status = "okay";
};
&ehci0 {
    dr_mode = "otg";
    status = "okay";
};

&ehci1 {
    status = "okay";
};
&ohci0 {
    dr_mode = "otg";
    status = "okay";
};
&ohci1 {
    status = "okay";
};
```

Figure 5-11: Enable USB 2.0 Host (rzg3s-smarc.dtsi for RZ/G3S)

Below figure enables the necessary properties to support USB 2.0 host in RZ/V2H Evaluation Board Kit.

```
&usb20phyrst {
    status = "okay";
};
&usb21phyrst {
    status = "okay";
};
&ohci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
    status = "okay";
};
&ohci1 {
    memory-region = <&global_cma>;
    status = "okay";
};
&ehci0 {
    memory-region = <&global_cma>;
    dr_mode = "otg";
};
```

```

        status = "okay";
    };
    &ehci1 {
        memory-region = <&global_cma>;
        status = "okay";
    };

```

Figure 5-12: Enable USB 2.0 Host (rzv2h-evk-common.dtsi for RZ/V2H)

5.2 Integration Procedure

5.2.1 Kernel Configuration

To enable the functions of this module, make the following setting with Kernel Configuration.

```

Device Drivers --->
  [*] USB support ---->
    <*> Support for Host-side USB
    ...
    *** USB Host Controller Drivers ***
    <*> EHCI HCD (USB 2.0) support
    [*] Root Hub Transaction Translators
    ...
    <*> Generic EHCI driver for a platform device
    ...
    <*> OHCI HCD (USB 1.1) support
    ...
    <*> Generic OHCI driver for a platform device
    ...
Device Drivers --->
  PHY Subsystem ---->
    <*> Renesas R-Car generation 3 USB 2.0 PHY driver

Device Drivers --->
  Regulator Subsystem ---->
    <*> Renesas RZ/G2L USB VBUS regulator driver

Device Drivers --->
  Multiplexer drivers --->
    <*> Renesas RZ/V2H USB VBENCTL VBUS_SEL mux driver

```

Figure 5-13: Kernel configuration for this module (RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2N and RZ/V2H)

The following shows an example of integration of standard USB class drivers.

```

Device Drivers --->
  [*] SCSI device support ---->
    *- SCSI device support
    ...
    [ ] legacy /proc/scsi/ support
    *** SCSI support type (disk, tape, CD-ROM) ***
    <*> SCSI disk support

Device Drivers --->
  [*] USB support ---->
    *** NOTE: USB_STORAGE depends on SCSI but BLK_DEV_SD may ***
    *** also be needed; see USB_STORAGE Help for more info ***
    <*> USB Mass Storage support

Device Drivers --->
  Input device support ---->
    <*> Event interface

Device Drivers --->
  HID support ---->
    <*> Generic HID driver
    USB HID support ---->
    <*> USB HID transport layer

```

Figure 5-14: Kernel configuration for standard USB class drivers (RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2N and RZ/V2H)

5.2.2 Integration of a USB gadget driver

The example of integration of a USB gadget driver is shown below.

Please perform the following setup, when you integrate Mass Storage Gadget.

Please enable (input "Y") the following item in "USB Gadget Support".

```

Device Drivers --->
  [*] USB support ---->
    <*> USB Gadget support ---->
      <M> USB Gadget precomposed configurations
      <M> Mass Storage

```

Figure 5-15 Kernel configuration for USB Mass Storage Gadget driver

5.2.3 USB Attached SCSI (UAS)

UAS is a protocol used to move data to and from USB storage devices such as HDDs, SSDs and thumb drives. It uses the standard SCSI command set to provide faster transfers compared to the older USB Mass Storage Bulk-Only Transport (BOT) drivers.

Currently, in Renesas RZ Linux, it is supported as a kernel module named `uas`.

If your USB storage device supports SCSI protocol, please insert this kernel module to detect and increase higher performance.

Below is example command to insert this kernel module in runtime:

```
$ modprobe uas.ko
```

5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

5.3.2 Kernel Parameters

There are no kernel parameters.

Revision History	Linux Interface Specification Device Driver USB2.0 Host User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 21	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	8, 9, 10	Updated: - Name and working directory of USBPHY - Devicetree definition.
1.4	Mar. 31, 2022	—	No modification, keep version to keep consistent with other documents
1.5	June. 24, 2022	8	Updated: - Delete PHYRST setting (phrst is driver, enable to use, no need to setting by manually) - Add RZ/Five device.
1.6	Sep. 15, 2022	—	No modification
1.7	Dec. 15, 2022	—	No modification
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents
1.9	Mar. 31, 2025	5, 9	Remove USB DMAC Update name of device tree files
1.10	May. 30, 2025	1	Add MPU information support for both kernel versions v5.10 and v6.1.
1.11	Jun. 30, 2025	—	Add RZ/V2N information
1.12	Jul. 22, 2025	1	Updated: - RZ/G3E overview, function and connected ports.
		4	Add RZ/G3E hardware specification
		6	Update Figure 3-2 Modules Configuration (RZ/V2N) - Remove USBDMAC component.
		7	Add RZ/G3E modules configuration
		8	Update RZ/G3E Group to State Transition Diagram
		9	Update RZ/G3E Device Node
		10	Add RZ/G3E directory configuration
		13-14	Add USB2.0 host device nodes for RZ/G3E
		15	Add the way to enable USB 2.0 Host for RZ/G3E
1.13	Nov. 28, 2025	17	Update RZ/G3E figure 5-6, figure 5-7
		10 - 11	- Add vbus regulator driver path (figure 5-1). - Add vbus subnode to phyrst node (figure 5-3).
		12	Update interrupts table.
		14	- Add vbus-supply to usb2_phy0 node (figure 5-6).
		16	- Add Renesas USB VBUS regulator kernel configuration (figure 5-9).
1.14	Dec. 19, 2025	—	Add RZ/G3S information
		—	Add RZ/V2H information
1.15	Mar. 27, 2026	12	Add new chapter “5.2.3 USB Attached SCSI (UAS)” to describe about UAS protocol new support.
		4	Add product number for RZ/V2N Version 2
		13, 14, 20, 22	Update information for RZ/V2N

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Group, RZ/G3S Group, RZ/V2H and RZ/Five



Renesas Electronics Corporation