

Linux Interface Specification Device Driver A/D Converter

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and
RZ/Five Group

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/G3S Group, RZ/V2H Group and RZ/G3E Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of Thermal Linux interface Specification	Linux interface Specification - ADC	This User's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Terms	Explanation
ADC	<u>A</u> nalog-to- <u>D</u> igital <u>C</u> onverter
INT []	Function that returns the integer portion of the value enclosed in []
V _{in}	Analog input voltage
ADC_AVREF	Voltage of power supply pin(ADC_AVDD18) for the analog unit
ADCR	Value of A/D conversion result registers (ADCR7 to ADCR0)

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1. Overview

1.1 Overview

This manual explains the driver module (this module) that controls the ADC Controller on RZ/G2L group (except RZ/G2LC), RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/Five Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group and RZ/Five Group.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and RZ/V2N Group.

1.2 Function

The following functionality is supported:

- Trigger mode:
 - Software trigger
- Resolution: 12 bits (RZ/G2L, RZ/G2UL, RZ/V2L, RZ/Five, RZ/V2H, RZ/G3E, RZ/G3S), 8 bits/12 bits (RZ/V2N)
- Number of channels:
 - RZ/G2L and RZ/V2L: 8 channels
 - RZ/G2UL and RZ/Five: 2 channels
 - RZ/G2LC: not supported.
 - RZ/V2N: 3 units, 8 channels per unit
 - RZ/V2H: 8 channels.
 - RZ/G3E: 8 channels.
 - RZ/G3S: 8 channels for ADC and 1 channel for TSU
- Operation mode:
 - Select mode: 1-buffer mode (RZ/G2L, RZ/G2UL, RZ/V2L, RZ/Five, RZ/G3E, RZ/G3S)
 - Single Scan Mode (RZ/V2H, RZ/V2N)

1.3 Reference

1.3.1 Standard

There is no reference document on standards.

1.3.2 Related documents

There is no document related to this kernel.

1.4 Restrictions

None.

2. Terminology

The following table shows the terminology related to this kernel.

Table 2-1 Terminology

Terms	Explanation
ADC	<u>A</u> nalog-to- <u>D</u> igital <u>C</u> onverter
INT[]	Function that returns the integer portion of the value enclosed in []
Vin	Analog input voltage
ADC_AVREF	Voltage of power supply pin(ADC_AVDD18) for the analog unit
ADCR	Value of A/D conversion result registers (ADCR7 to ADCR0)

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this kernel.

Table 3-1 Hardware environment

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE

3.2 Module Configuration

The following figures show the configuration of this module.

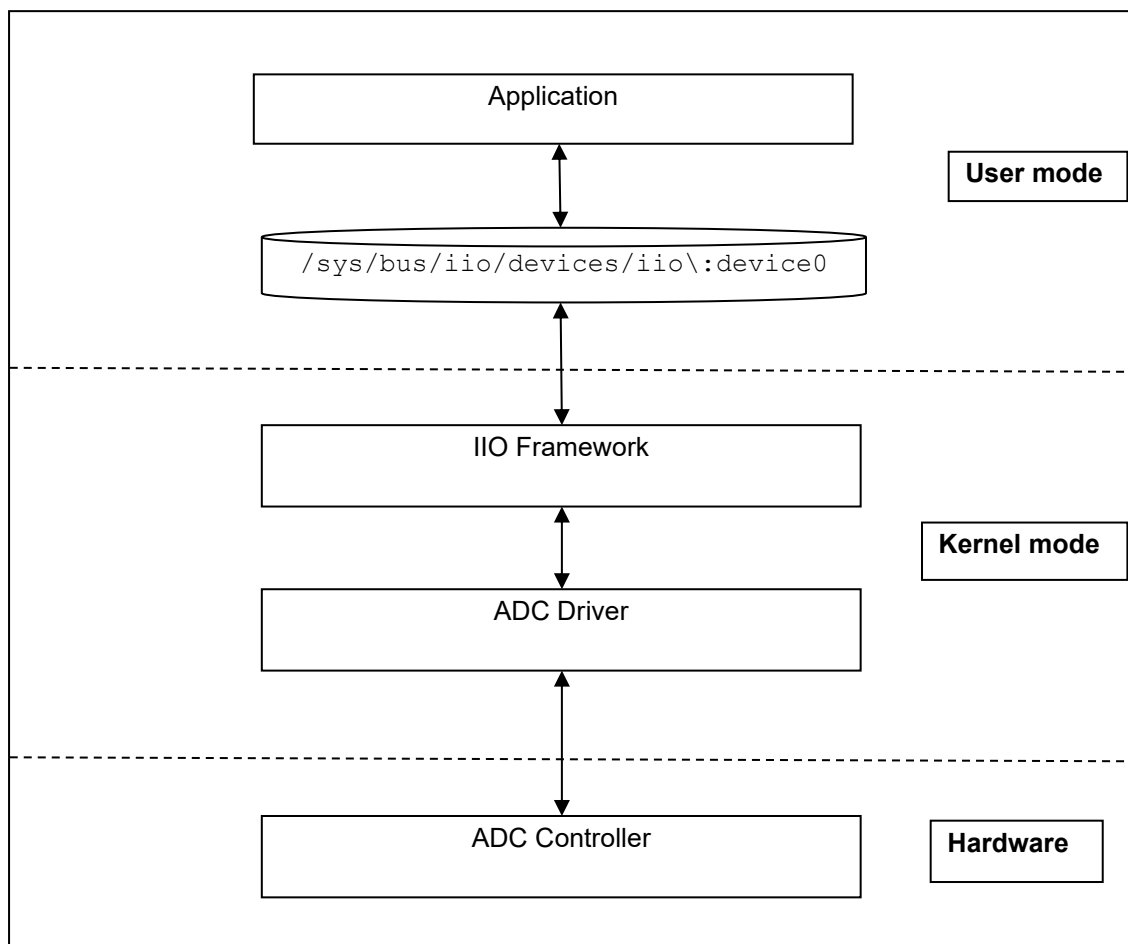


Figure 3-1 Module Configuration (RZ/G2L, RZ/G2UL, RZ/V2L, RZ/Five, RZ/V2H, RZ/G3E, RZ/G3S)

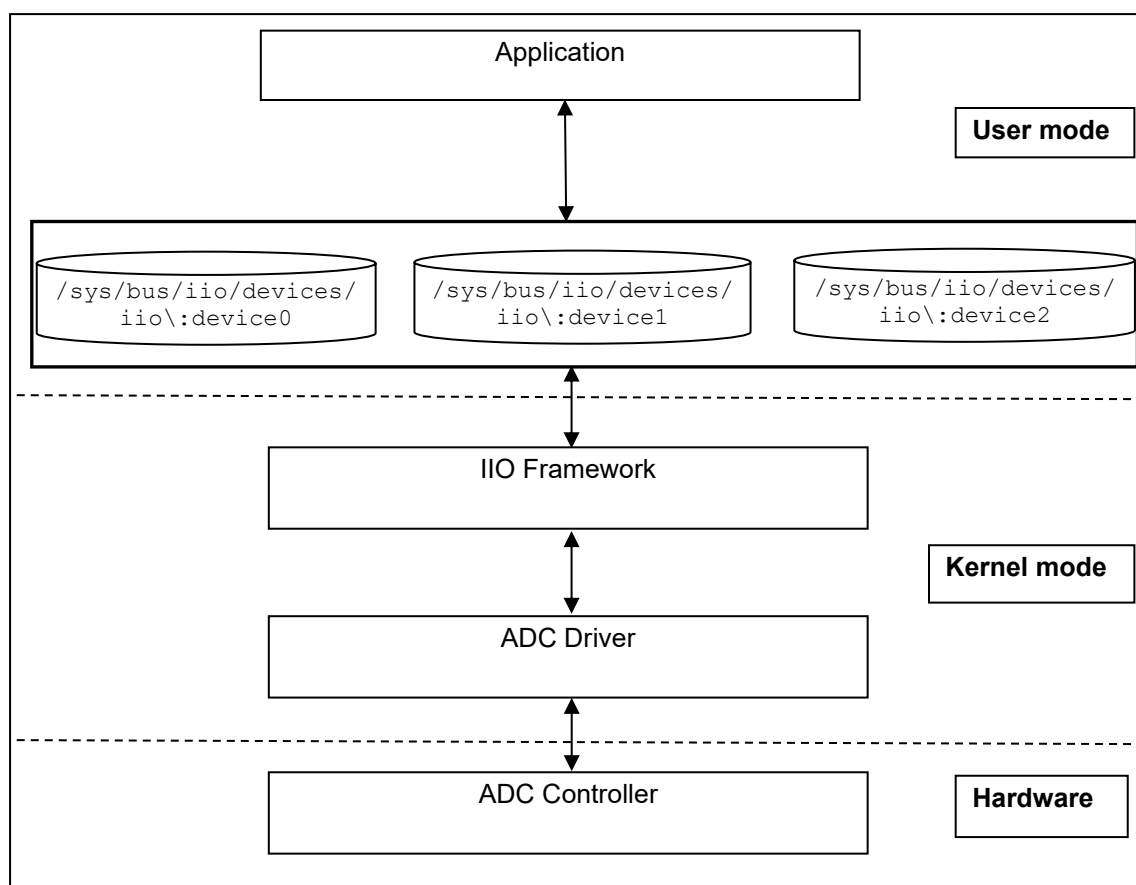


Figure 3-2 Module Configuration (RZ/V2N)

3.3 Operation

3.3.1 Type of A/D conversion Modes

Table 3-2 A/D Conversion Modes (RZ/G2L Group, RZ/V2L, RZ/G3E, RZ/G3S and RZ/Five)

Trigger Mode	Trigger Input Mode	Operating Mode	Conversion Count	Buffer Count	Operation
Software trigger	-	Select	Single	1 buffer	Selected 1 channel x 1-time conversion

Table 3-3 A/D Conversion Modes (RZ/V2H and RZ/V2N Group)

Trigger Mode	Operating Mode	Operation
Software trigger Internal trigger External trigger	Single scan mode	A/D conversion is performed only once on the analog inputs of arbitrarily selected channels.
	Continuous scan mode	A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels.
	Group scan mode	Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two.

Note 1. Currently, only the Single scan mode is supported in RZ/V2H and RZ/V2N's ADC device driver

3.3.2 Interrupt Functions

Table 3-4 and Table 3-5 list the interrupt sources that are used by this module on different RZ platforms.

On RZ/G2L Group, RZ/V2L, RZ/G3S Group and RZ/Five platforms, the INTS bit in the ADINT register is used to set the operation for outputting an interrupt request of the INTAD.

Table 3-4 List of Interrupt Sources (RZ/G2L Group, RZ/V2L, RZ/G3S and RZ/Five)

Interrupt Source	Condition for Generation	Enabling Interrupt	Confirming Interrupt Source	Method for Clearing Interrupt Source
		ADINT Register	ADSTS Register*1	ADSTS Register
A/D conversion end	When A/D conversion on the specified channel is completed	NTEN[7:0]*2	NTST[7:0]	Write 1 to the bits that were 1 when the register was read.
A/D conversion channel select error	<ul style="list-style-type: none"> When all of the CHSEL[7:0] bits in the ADM2 register were 0 at the start of A/D conversion*3 When multiple analog input channels are selected in select mode*3 	CSEEN	CSEST	Write 1 to the CSEST bit.

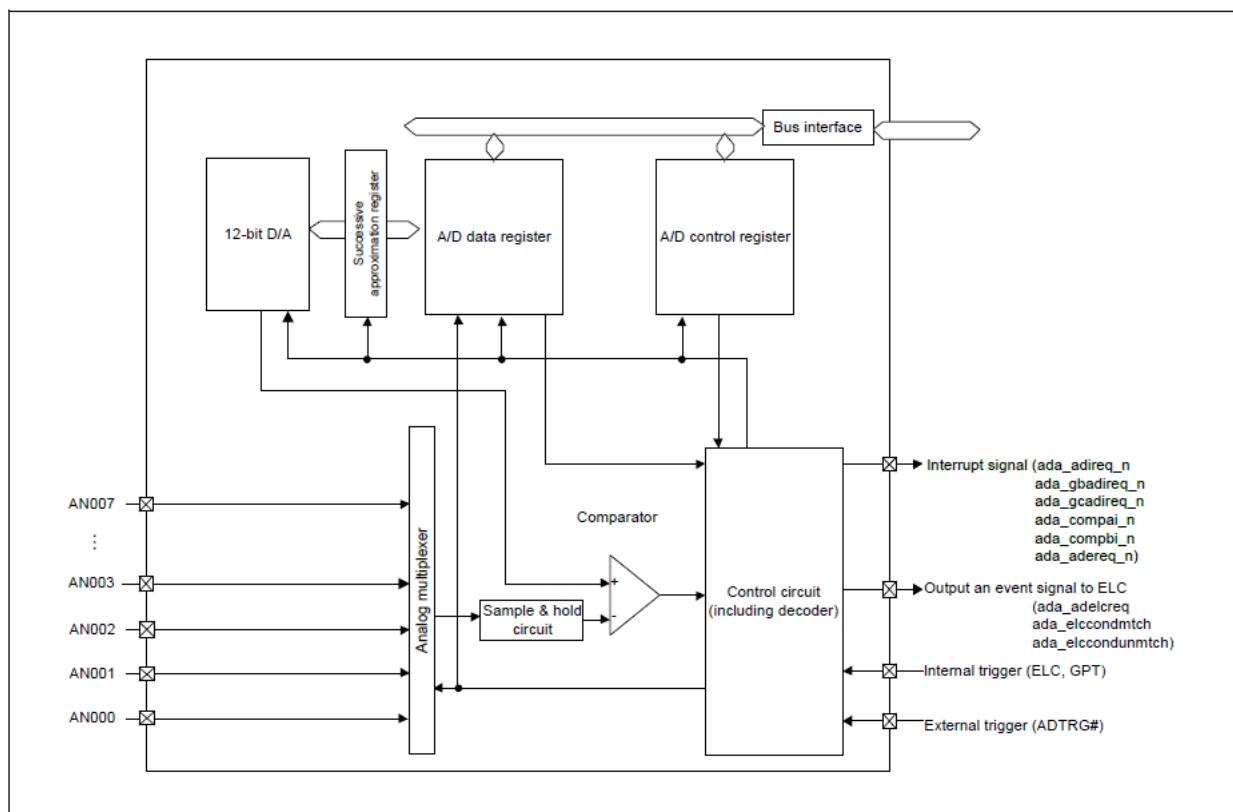
Note 1. If an interrupt source is generated regardless of the settings of the INTEN[7:0] and CSEEN bits in the ADINT register, the bit corresponding to the interrupt source is set to 1 in the ADSTS register.

Note 2. The A/D conversion end interrupt can be enabled or disabled individually for each channel.

Note 3. When an A/D conversion channel select error occurs, the ADCE bit in the ADM0 register becomes 0 and A/D conversion operation is stopped.

Table 3-5 List of Interrupt Sources (RZ/G3E, RZ/V2H and RZ/V2N)

Name	Interrupt Sources	CPU request	DMAC Activation	ELC Activation	EMC request
ada_adireq_n	A/D scan end interrupt, A/D scan end interrupt for Group A	Possible	Possible	Possible	Not possible
ada_gbadireq_n	A/D scan end interrupt for Group B	Possible	Possible	Possible	Not possible
ada_gcadireq_n	A/D scan end interrupt for Group C	Possible	Possible	Possible	Not possible
ada_compai_n	Window A compare match	Possible	Not possible	Not possible	Not possible
ada_compbi_n	Window B compare match	Possible	Not possible	Not possible	Not possible
ada_adelcreq	A/D scan end interrupt for ELC	Not possible	Not possible	Possible	Not possible
ada_elcondmtch	Compare match	Not possible	Possible	Possible	Not possible
ada_elcondunmtch	Compare mismatch	Not possible	Possible	Possible	Not possible
ada_adereq_n	A/D error interrupt request by overwrite check	Not possible	Not possible	Not possible	Possible

Figure 3-3 Block Diagram of 12-Bit A/D Converter Module Configuration (Unit0 to Unit2 for RZ/V2N, Unit0 only for RZ/V2H and RZ/G3E)

4. External Interface

The supported external interface of this module is explained.

4.1 Device Node

ADC channel	Device Node
ADC_CH0	/sys/bus/iio/devices/ iio : device0 /in_voltage0_raw
ADC_CH1	/sys/bus/iio/devices/ iio : device0 /in_voltage1_raw
ADC_CH2	/sys/bus/iio/devices/ iio : device0 /in_voltage2_raw
ADC_CH3	/sys/bus/iio/devices/ iio : device0 /in_voltage3_raw
ADC_CH4	/sys/bus/iio/devices/ iio : device0 /in_voltage4_raw
ADC_CH5	/sys/bus/iio/devices/ iio : device0 /in_voltage5_raw
ADC_CH6	/sys/bus/iio/devices/ iio : device0 /in_voltage6_raw
ADC_CH7	/sys/bus/iio/devices/ iio : device0 /in_voltage7_raw
ADC_CH8 (RZ/G3S only)	/sys/bus/iio/devices/ iio : device0 /in_temp8_raw

Note) RZ/G2L, RZ/V2L support 8 channels: ADC_CH0 to ADC_CH7.

RZ/G2UL and RZ/Five support 2 channels: ADC_CH0 and ADC_CH1.

RZ/G2LC does NOT support ADC.

RZ/V2N also supports **iio**:**device1**, and **iio**:**device2** which represent the ADC unit 1 and ADC unit 2 respectively.

RZ/V2H, RZ/G3E support 8 channels: ADC_CH0 to ADC_CH7.

RZ/G3S support 9 channels: ADC_CH0 to ADC_CH7 and ADC_CH8 dedicated for TSU.

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.

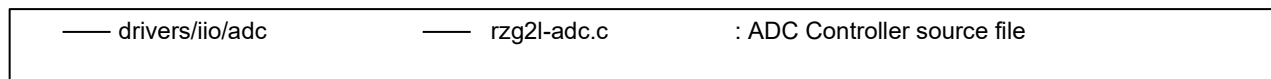


Figure 5-1 Directory configuration (RZ/G2L, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five)

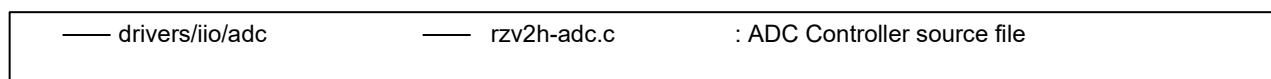


Figure 5-2 Directory configuration (RZ/V2H, RZ/G3E and RZ/V2N)

5.2 Integration Procedure

To enable the functions of this module, make the following setting in Kernel Configuration.

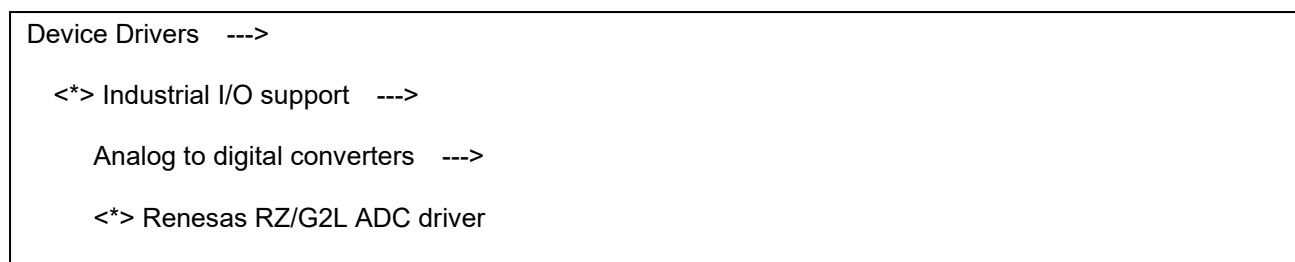


Figure 5-3 Kernel configuration (RZ/G2L Group, RZ/V2L, RZ/G3S Group and RZ/Five)

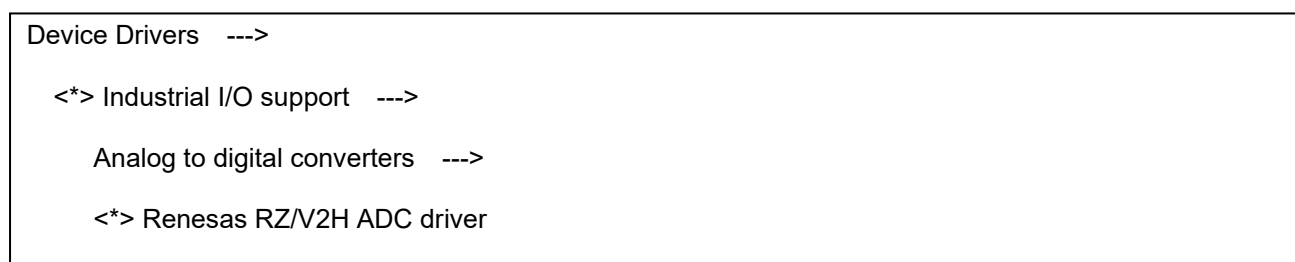


Figure 5-4 Kernel configuration (RZ/V2H, RZ/G3E and RZ/V2N)

5.3 Device Tree Setting

5.3.1 ADC node

Basic configuration information of ADC is defined in device tree SoC DTSI file (i.e. r9a07g044.dtsi for RZ/G2L, r9a09g056.dtsi for RZ/V2N, r9a09g057.dtsi for RZ/V2H, r9a09g047.dtsi for RZ/G3E, r9a08g045.dtsi for RZ/G3S). It is located in **arch/arm64/boot/dts/renesas** directory. Examples of device tree configuration for an ADC channel are described below:

```
adc: adc@10059000 {
    compatible = "renesas,r9a07g044-adc", "renesas,rzg2l-adc";
    reg = <0 0x10059000 0 0x400>;
    interrupts = <GIC_SPI 347 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A07G044_ADC_ADCLK>,
            <&cpg CPG_MOD R9A07G044_ADC_PCLK>;
    clock-names = "adclk", "pclk";
    resets = <&cpg R9A07G044_ADC_PRESETN>,
            <&cpg R9A07G044_ADC_ADRST_N>;
    reset-names = "presetn", "adrst-n";
    power-domains = <&cpg>;
    status = "disabled";
    #address-cells = <1>;
    #size-cells = <0>;
    channel@0 {
        reg = <0>;
    };
    channel@1 {
        reg = <1>;
    };
    channel@2 {
        reg = <2>;
    };
    channel@3 {
        reg = <3>;
    };
    channel@4 {
        reg = <4>;
    };
    channel@5 {
        reg = <5>;
    };
    channel@6 {
        reg = <6>;
    };
    channel@7 {
        reg = <7>;
    };
};
```

Figure 5-5 Device tree initial references information of ADC (RZ/G2L and RZ/V2L)

- Note) - All of the information in the above device tree is used for both RZ/G2L and RZ/V2L except :
- compatible: "renesas,adc-r9a07g044" is used for RZ/G2L, "renesas,adc-r9a07g054" is used for RZ/V2L, compatible: "renesas,adc-r9a07g043" is used for RZ/G2UL and RZ/Five.
 - clocks: R9A07G044_CLK_ADC is used for RZ/G2L, R9A07G054_CLK_ADC is used for RZ/V2L, and R9A07G043_CLK_ADC is used for RZ/G2UL and RZ/Five.
 - resets: R9A07G044_ADC_PRESETN, R9A07G044_ADC_ADRST_N are used for RZ/G2L, R9A07G054_ADC_PRESETN, R9A07G054_ADC_ADRST_N are used for RZ/V2L, and R9A07G043_ADC_PRESETN, R9A07G043_ADC_ADRST_N are used for RZ/G2UL and RZ/Five.

```

adc0: adc@11c00000 {
    compatible = "renesas,r9a09g057-adc", "renesas,rzv2h-adc";
    reg = <0 0x11C00000 0 0x400>;
    clocks = <&cpg CPG_MOD 0x108>,
            <&cpg CPG_MOD 0x107>;
    clock-names = "adclk", "pclk";
    resets = <&cpg 0xf6>;
    reset-names = "adrst-n";
    power-domains = <&cpg>;
    status = "disabled";
    #address-cells = <1>;
    #size-cells = <0>;
    channel@0 {
        reg = <0>;
    };
    channel@1 {
        reg = <1>;
    };
    channel@2 {
        reg = <2>;
    };
    channel@3 {
        reg = <3>;
    };
    channel@4 {
        reg = <4>;
    };
    channel@5 {
        reg = <5>;
    };
    channel@6 {
        reg = <6>;
    };
    channel@7 {
        reg = <7>;
    };
};

```

Figure 5-6 Device tree initial references information of ADC (RZ/V2N)

Note) - All of the information in the above device tree example is used for RZ/V2N

```

adc: adc@11c00000 {
    compatible = "renesas,r9a09g047-adc", "renesas,rzv2h-adc";
    reg = <0 0x11C00000 0 0x400>;
    clocks = <&cpg CPG_MOD 263>,
            <&cpg CPG_MOD 264>;
    clock-names = "pclk", "adclk";
    resets = <&cpg 246>;
    reset-names = "adrst-n";
    power-domains = <&cpg>;
    renesas,sysc-signal = <&sys 0x1600 0x1>;
    status = "disabled";

    #address-cells = <1>;
    #size-cells = <0>;

    channel@0 {
        reg = <0>;
    };
    channel@1 {
        reg = <1>;
    };
    channel@2 {
        reg = <2>;
    };
    channel@3 {
        reg = <3>;
    };
    channel@4 {
        reg = <4>;
    };
    channel@5 {
        reg = <5>;
    };
    channel@6 {
        reg = <6>;
    };
    channel@7 {
        reg = <7>;
    };
};

```

Figure 5-7 Device tree initial references information of ADC (RZ/G3E)

Note)- All of the information in the above device tree example is used for RZ/G3E.

```

adc: adc@10058000 {
    compatible = "renesas,r9a08g045-adc";
    reg = <0 0x10058000 0 0x1000>;
    interrupts = <GIC_SPI 312 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_ADC_ADCLK>,
            <&cpg CPG_MOD R9A08G045_ADC_PCLK>;
    clock-names = "adclk", "pclk";
    resets = <&cpg R9A08G045_ADC_PRESETN>,
            <&cpg R9A08G045_ADC_ADRST_N>;
    reset-names = "presetn", "adrst-n";
    power-domains = <&cpg>;

    #address-cells = <1>;
    #size-cells = <0>;
    #io-channel-cells = <1>;
    status = "disabled";

    channel@0 {
        reg = <0>;
    };

    channel@1 {
        reg = <1>;
    };

    channel@2 {
        reg = <2>;
    };

    channel@3 {
        reg = <3>;
    };

    channel@4 {
        reg = <4>;
    };

    channel@5 {
        reg = <5>;
    };

    channel@6 {
        reg = <6>;
    };

    channel@7 {
        reg = <7>;
    };

    channel@8 {
        reg = <8>;
    };
};

```

Figure 5-8 Device tree initial references information of ADC (RZ/G3S)

Note) - All of the information in the above device tree example is used for RZ/G3S

```
adc: adc@11c00000 {  
    compatible = "renesas,r9a09g057-adc", "renesas,rzv2h-adc";  
    reg = <0 0x11C00000 0 0x400>;  
    clocks = <&cpg CPG_MOD 0x107>,  
            <&cpg CPG_MOD 0x108>;  
    clock-names = "pclk", "adclk";  
    resets = <&cpg 0xf6>;  
    reset-names = "adrst-n";  
    power-domains = <&cpg>;  
    status = "disabled";  
  
    #address-cells = <1>;  
    #size-cells = <0>;  
  
    channel@0 {  
        reg = <0>;  
    };  
    channel@1 {  
        reg = <1>;  
    };  
    channel@2 {  
        reg = <2>;  
    };  
    channel@3 {  
        reg = <3>;  
    };  
    channel@4 {  
        reg = <4>;  
    };  
    channel@5 {  
        reg = <5>;  
    };  
    channel@6 {  
        reg = <6>;  
    };  
    channel@7 {  
        reg = <7>;  
    };  
};
```

Figure 5-9 Device tree initial references information of ADC (RZ/V2H)

5.4 Option Setting

5.4.1 Module Parameters

There are no module parameters.

5.4.2 Kernel Parameters

There are no kernel parameters.

Revision History	Linux Interface Specification Device Driver A/D Converter User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 2021	—	First Edition issued.
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents.
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L.
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device.
1.3	Mar. 31, 2022	12	Update information for device-tree.
1.4	May. 31, 2022	—	No modification, keep version to keep consistent with other documents.
1.5	June. 24, 2022	—	Add RZ/Five Device.
1.6	Sep. 15, 2022	—	Update information.
1.7	Dec. 15, 2022	—	No modification, change version to keep consistent with other documents.
1.8	Mar. 15, 2023	—	No modification, change version to keep consistent with other documents.
1.9	May. 30, 2025	1	- Add MPU information support for both kernel versions v5.10 and v6.1. - Correct current supported functionality of ADC.
		6	- Correct Table 3-2 A/D Conversion Modes.
		7	- Correct Table 3-3 List of Interrupt Functions.
		8	- Correct the number of channels supported in Note.
		9	- Correct Figure 5.2 Kernel configuration description.
		10	- Correct devicetree information description.
1.10	Jun. 30, 2025	—	Add RZ/V2N support information.
1.11	Jul. 22, 2025	—	Add RZ/G3E support information.
1.12	Nov. 28, 2025	1	Add information of RZ/G2UL and RZ/V2L support for kernel v6.1.
		—	Add RZ/G3S support information.
1.13	Dec. 19, 2025	—	Add RZ/V2H support information.
1.14	Mar. 27, 2026	4	Add RZ/V2N V2.0 product number.
		13	Update RZ/V2N device tree compatible string.

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