

Linux Interface Specification Device Driver Audio

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/Five,
RZ/V2N Group, RZ/V2H Group, RZ/G3S Group and
RZ/G3E Group

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group, RZ/V2H Group, RZ/G3S Group and RZ/G3E Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	This manual explains the Linux Audio device drivers in RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group, RZ/V2H Group, RZ/G3S Group and RZ/G3E Group Linux BSP.	Linux Interface Specification Device Driver Audio	This User's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Overview

This manual explains the Linux audio device drivers in the RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/V2N Group, RZ/V2H Group, RZ/G3S Group and RZ/G3E Group.

Note: Currently, RZ/G2L, RZ/V2L, RZ/G3S and RZ/Five are supported in two kernel versions v5.10 and v6.1. On RZ/V2N, RZ/V2H and RZ/G3E it's supported only kernel version v6.1. All the information is shown below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/G3S Group and RZ/Five.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3S Group and RZ/G3E.

1.2 Function

This module controls the PCM I/F that is provided by ALSA and transmits/receives the data to/from the Audio codecs on the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five platforms. This module also supports full duplex communication.

Note: On RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five, this feature is only supported from Linux Kernel version rz-5.10-cip41 and later, also rz-6.1-cip28 and later.

1.2.1 Connected Devices

In the RZ/G2L and RZ/V2L boards, there are two SSIs (among four available channels) connected to the peripheral devices which are described in (Table 1-1). In the RZ/G2LC Smarc board, one SSI channel connected to either WM8978 audio codec or ADV7535 HDMI transmitter (Table 1-2). In the RZ/G2UL Smarc board, one SSI channel connected to WM8978 codec (Table 1-3).

In the RZ/G3S board, there is only one SSI channel (among four available channels) connected to the peripheral device which is described in (Table 1-4). One SPDIF channel available on the SoC which is described in (Table 1-5).

In the RZ/V2N, RZ/V2H and RZ/G3E board, there are ten SSI channels available on the SoC, but only channels 3, 4 are connected to the DA7212 codec .and SSI channel 0 is connected to ADV7535 HDMI transmitter (Table 1-6). There are three SPDIF channels available on the SoC which are described in (Table 1-7). There are also 3 PDM channels available on the SOC which are described in (Table 1-8).

Table 1-1 SSI Connected device (RZ/G2L and RZ/V2L)

SSI channels	Peripheral device
SSI0 (playback and capture)	Edge connector (CN4) connected to Wolfson Microelectronics WM8978 audio codec
SSI1 (playback)	Edge connector (CN4) connected to ADV7535 HDMI audio/video transmitter
SSI2, SSI3	None

Table 1-2 SSI Connected device (RZ/G2LC Smarc)

SSI channels	Peripheral device
SSI0 (playback and capture)	Edge connector (CN4) connected to (a) or (b) depending on Dip Switch SW1-5 state: (a) Wolfson Microelectronics WM8978 audio codec (b) ADV7535 HDMI audio/video transmitter
SSI1, SSI2, SSI3	None

Table 1-3 SSI Connected device (RZ/G2UL Smarc, RZ/Five)

SSI channels	Peripheral device
SSI1 (playback and capture)	Edge connector (CN4) connected to Wolfson Microelectronics WM8978 audio codec (*). (*): Dip Switch SW1-3 must be set properly to enable SSI1 SW1-3: specified by SW_ET0_EN_N in device tree 0: ETHER0; 1: CAN0, CAN1, SSI1, RSPI1
SSI0, SSI2, SSI3	None

Table 1-4 SSI Connected device (RZ/G3S Smarc)

SSI channels	Peripheral device
SSI3 (playback and capture)	Codec DA7212
SSI0, SSI1, SSI2	None

Table 1-5 SPDIF connected device (RZ/G3S Smarc)

SSI channels	Peripheral device
SPDIF (playback and capture)	Dummy Codec

Table 1-6 SSI Connected device (RZ/V2N, RZ/V2H and RZ/G3E)

SSI channels	Peripheral device
SSI3 (output: playback)	Codec DA7212
SSI4 (input: capture)	Codec DA7212
SSI0 (output: playback)	ADV7535 HDMI audio/video transmitter
SSI1, SSI2, SSI5, SSI6, SSI7, SSI8, SSI9	None

Table 1-7 SPDIF Connected device (RZ/V2N, RZ/V2H and RZ/G3E)

SPDIF channels	Peripheral device
SPDIFn (playback and capture) *	Dummy codec (virtual device)

Note *: n = 0 to 2

Table 1-8 PDM Connected device (RZ/G3E)

PDM channels	Peripheral device
PDMn (capture) *	ICS-41350 (Dummy driver)

Note *: n = 0 to 2

1.2.2 Clock of connected devices

The following figure shows the clock of connected devices.

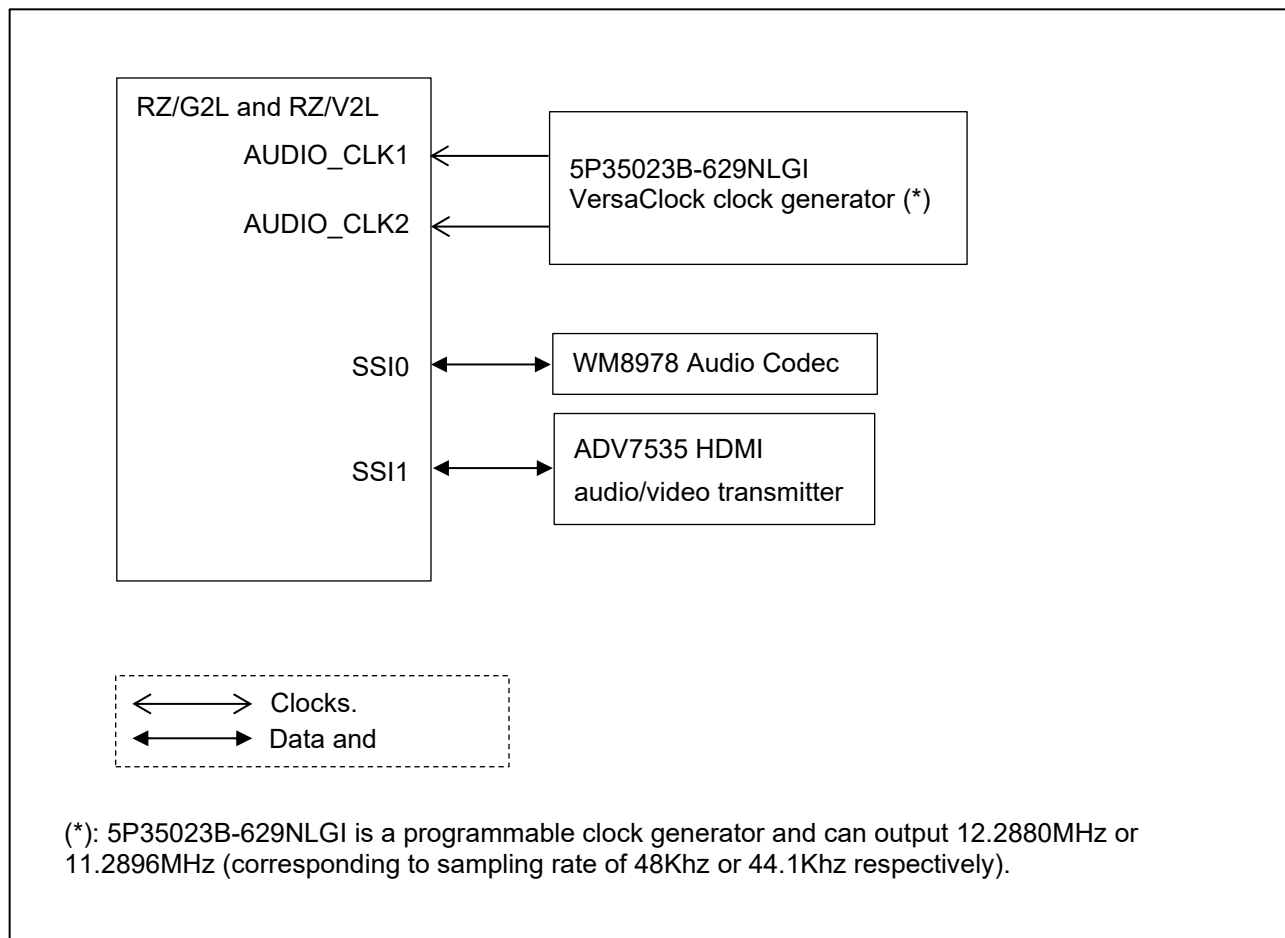
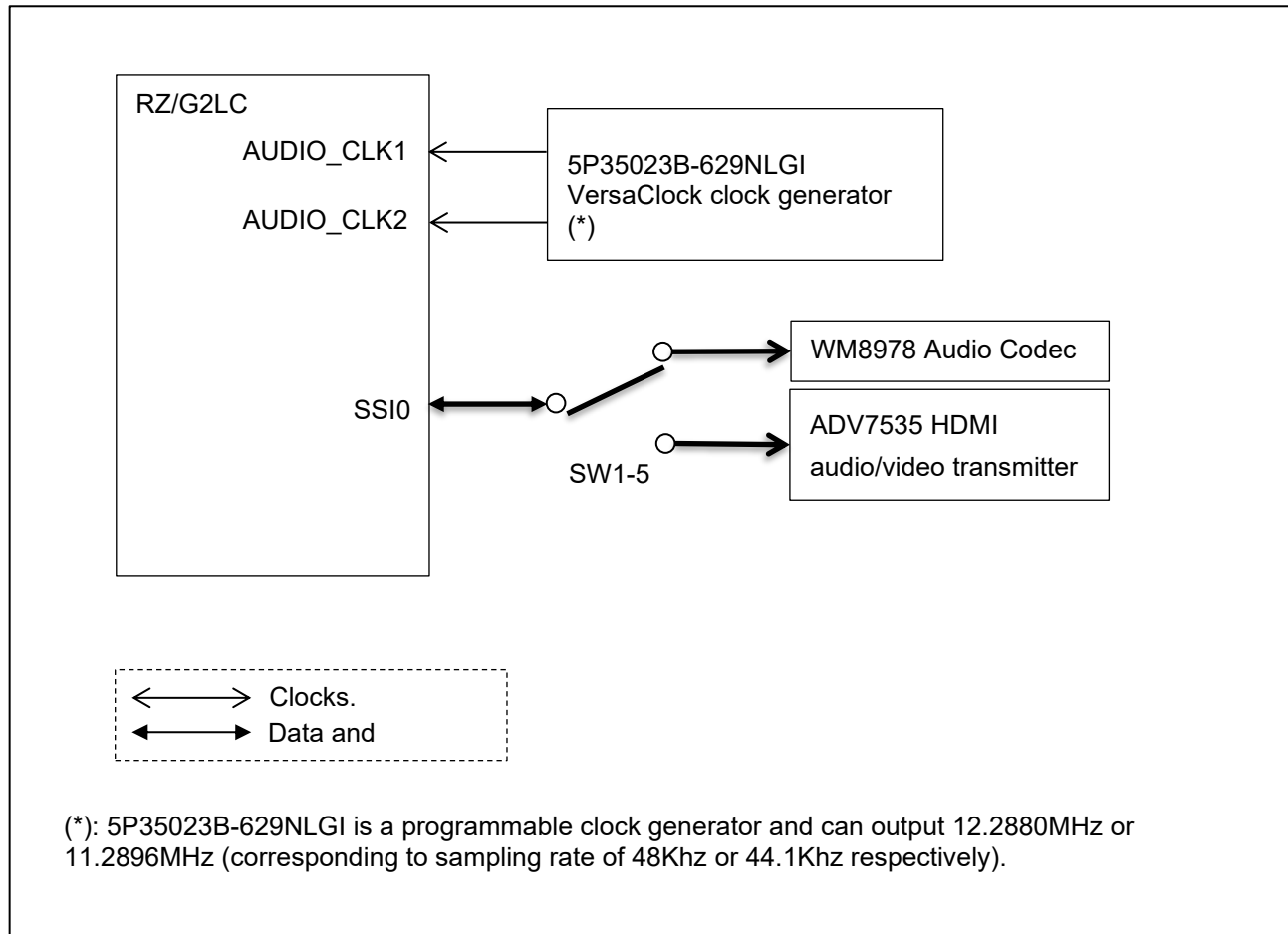
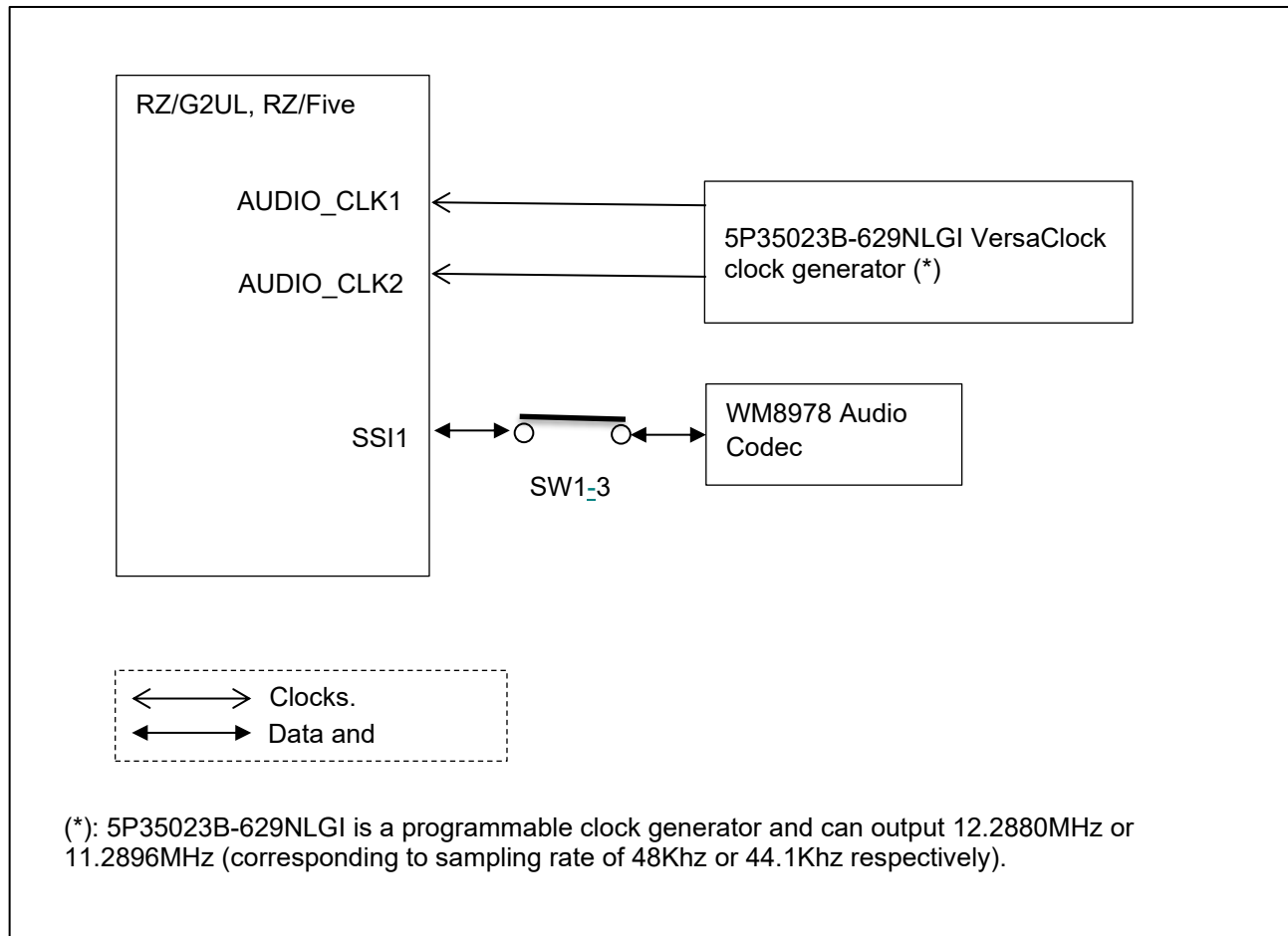
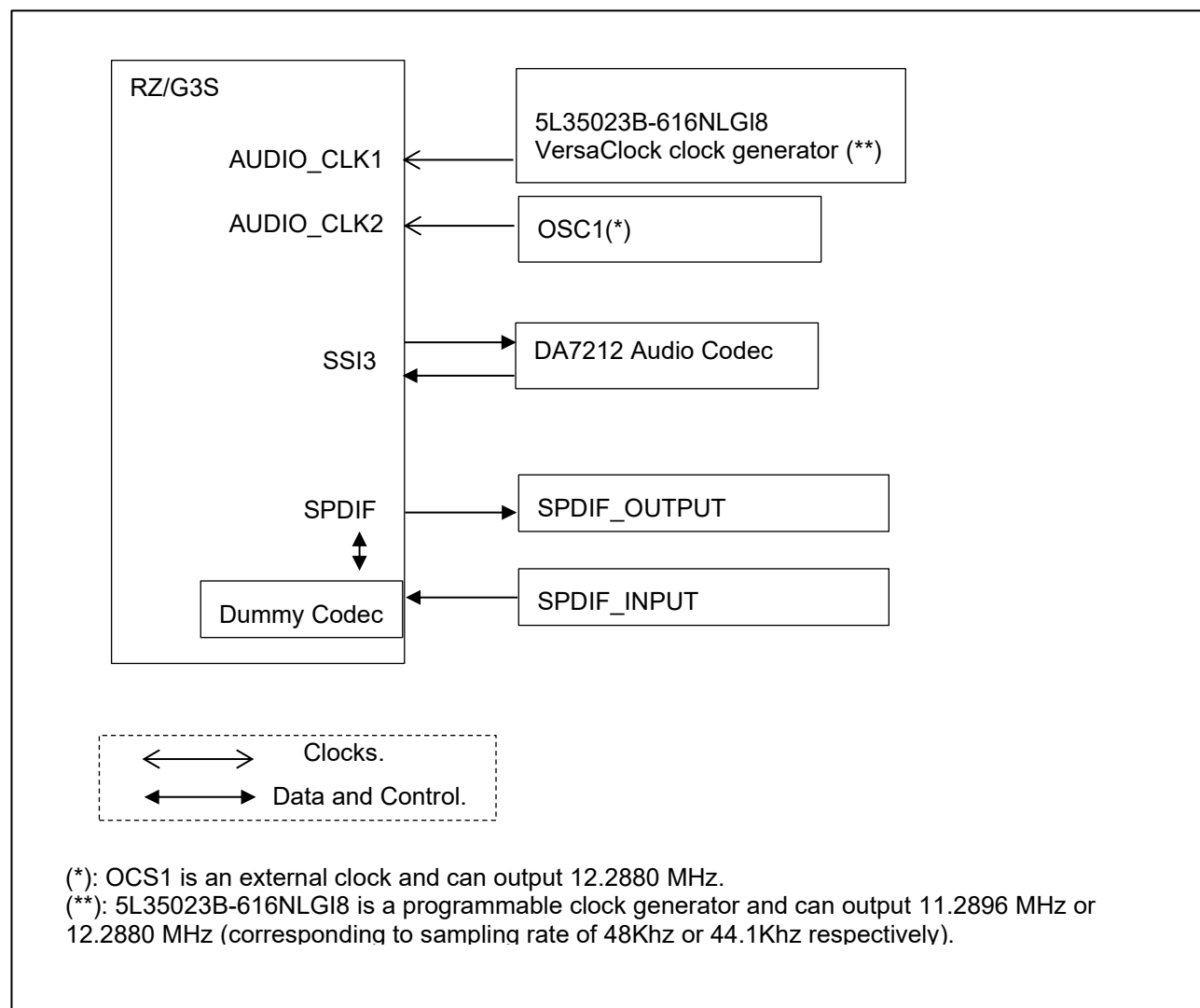
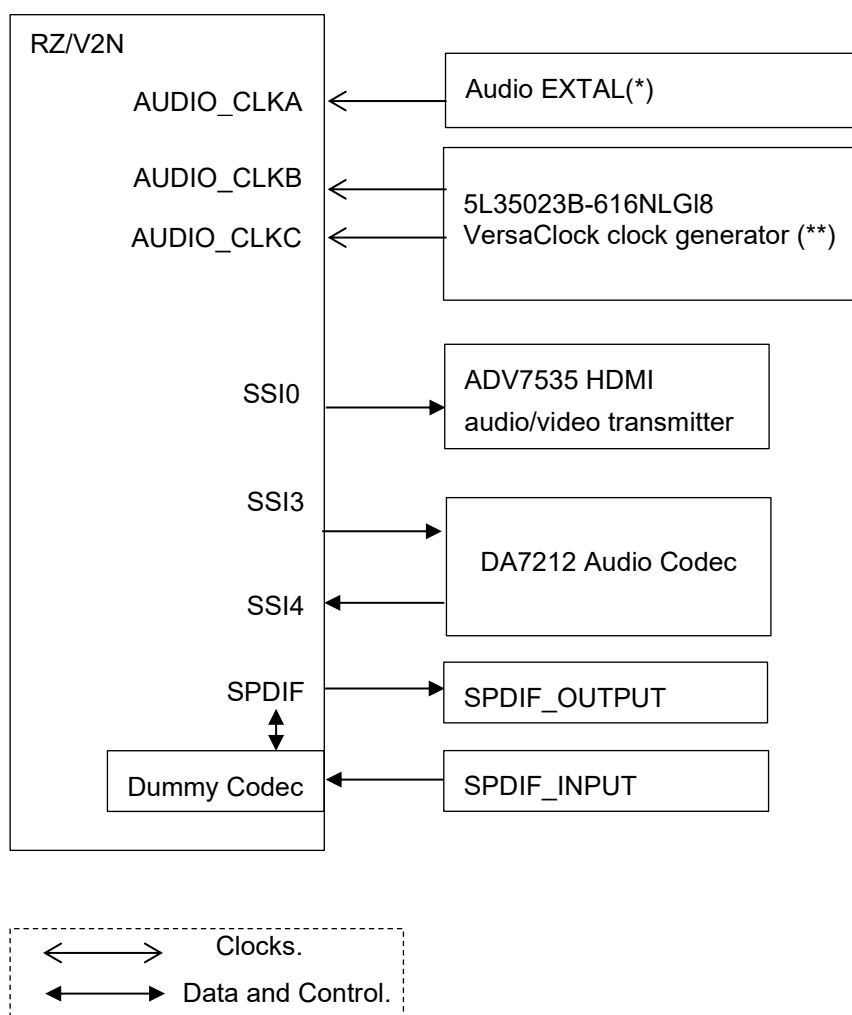


Figure 1-1 Clock of connected devices (RZ/G2L and RZ/V2L)

**Figure 1-2 Clock of connected devices (RZ/G2LC Smarc)**

**Figure 1-3 Clock of connected devices (RZ/G2UL Smarc and RZ/Five)**

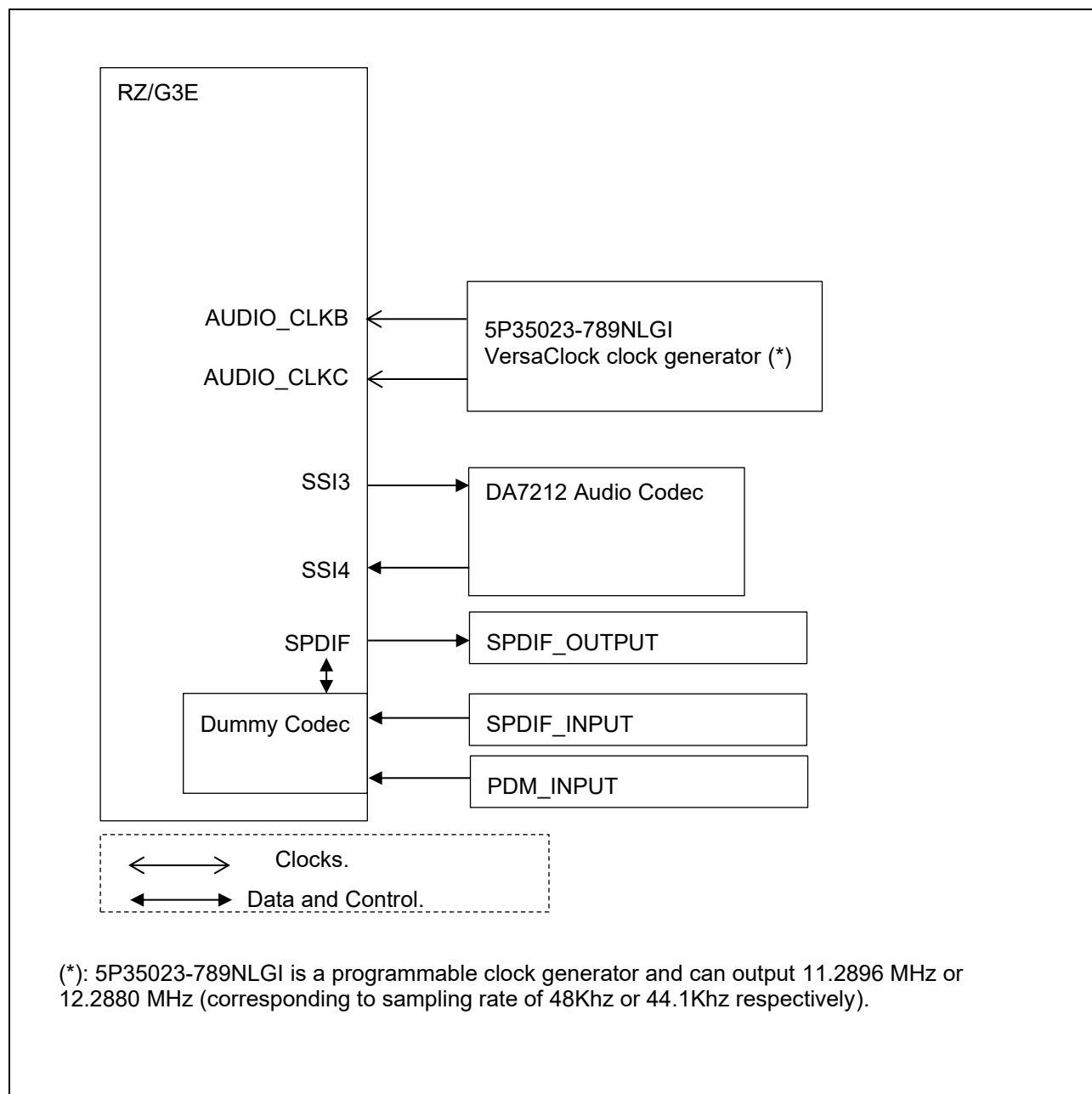
**Figure 1-4 Clock of connected devices (RZ/G3S)**



(*): Audio_EXTAL is an external clock and can output 22.5792 MHz.

(**): 5L35023B-616NLGI8 is a programmable clock generator and can output 22.5792 MHz or 24.5780 MHz (corresponding to sampling rate of 48Khz or 44.1Khz respectively).

Figure 1-5 Clock of connected devices (RZ/V2N and RZ/V2H)

**Figure 1-6 Clock of connected devices (RZ/G3E)**

1.2.3 PCM

Support for this module's PCM data depends on the codec support status. On the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five, 16-bit data is converted to 24-bit data by ALSA library and processed.

As an example of conversion by the ALSA library, the case of specifying the “plughw” option and S16_LE format is applicable. On the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five, the following command will convert 16-bit data to 24-bit data by the ALSA library.

```
# cat /dev/zero | aplay -D plughw:0,0 -d 30 -f S16_LE -r 44100 -c 2
```

In addition, supported PCM rates are limited by the clock range that can be supplied. On the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and RZ/Five platforms, data of 8000Hz to 48000Hz are resampled by ALSA library. Please refer to (Table 1-9) for more details.

Table 1-9 PCM function

Data format	S16_LE: Little Endian signed 16 bits (*1). S24_LE: Little Endian signed 24 bits. S32_LE: Little Endian signed 32 bits.
Sampling rate	8000Hz, 11025Hz, 12000Hz, 16000Hz, 22050Hz, 24000Hz, 44100Hz, 48000Hz, 88200Hz, 96000Hz, 192000Hz
Audio clock	128fs, 256fs, 384fs, 512fs
Serial data format	I ² S (2 channel)
Number of Channels	Monaural (*2) / Stereo 2ch

Notes)

*1: This module supports the 16-bit little endian signed data format, and depending on the target board, it can operate by converting it to 24-bit with the ALSA library.

*2: The monaural output format is converted to 2ch by ALSA library.

Table 1-10 PCM re-sampling rate by ALSA

Sampling rate	Device's Output	Device's Input
8000Hz	8000Hz	8000Hz
11025Hz	11025Hz	11025Hz
12000Hz	48000Hz	48000Hz
16000Hz	16000Hz	16000Hz
22050Hz	22050Hz	22050Hz
24000Hz	48000Hz	48000Hz
32000Hz	32000Hz	32000Hz
44100Hz	44100Hz	44100Hz
48000Hz	48000Hz	48000Hz

SPDIF is only supported on RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E platforms. This module supports 16-bit and 24-bit format. It also supports sampling frequencies of 32kHz, 44,1kHz and 48kHz with stereo mode only.

Table 1-11 PCM function for SPDIF

Data format	S16_LE: Little Endian signed 16 bits S24_LE: Little Endian signed 24 bits.
Sampling rate	32000Hz, 44100Hz, 48000Hz
Audio clock	256fs for RZ/V2N, 512fs for RZ/G3E and G3S
Number of Channels	Stereo 2ch

PDM is only supported on RZ/G3E platforms. This module supports 16-bit and 20-bit format. It also supports sampling frequencies of 8kHz,10kHz, 12kHz, 15kHz, 16kHz, 20kHz, 24kHz, 25kHz, 30kHz, 40kHz and 48kHz with mono mode only.

Table 1-12 PCM function for PDM

Data format	S16_LE: Little Endian signed 16 bits S20_LE: Little Endian signed 20 bits.
Sampling rate	8kHz,10kHz, 12kHz, 15kHz, 16kHz, 20kHz, 24kHz, 25kHz, 30kHz, 40kHz and 48kHz
Number of Channels	Mono 1ch

1.2.4 Audio Codec

On the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, and RZ/Five boards, this module supports the following function of Audio Codec LSI (WM8978). Please refer to Table 1-13 for more details. By default, Audio Codec LSI works in 'slave mode'.

Table 1-13 WM8978 specification

Data format	24bit, left justified (MSB first)	
Sampling rate	8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48KHz	
Channel	Output	LOUT1/ROUT1/LOUT2/ROUT2/OUT3/OUT4
	Input	L2/R2
Volume	DAC	
Playback source	Support: LOUT1/ROUT1	

On the RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E board, this module supports the following function of Audio Codec LSI (DA7212). Please refer to (Table 1-14) for more details. By default, Audio Codec LSI works in 'slave mode'.

Table 1-14 DA7212 specification

Data format	16, 20, 24, 32 bits wide I2S, Left Justified, Right Justified, DSP	
Sampling rate	8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2 and 96KHz	
Channel	Output	HP_L/HP_R/SP_P/SP_N
	Input	MIC1/MIC2
Volume	DAC	
Playback source	Support: HP_L/HP_R	

1.2.5 Routing

1.2.5.1 Routing on RZ/G2L Group , RZ/G3S Group and RZ/Five

On the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five boards, the audio routing supported by this module is as below. Refer to **section 4.3** for more details.

Table 1-15 Audio routing paths

Operation	Support route
Playback	Memory -> SSIn
Capture	SSIn -> Memory

Notes: SSIn: n=0 to 1

1.2.5.2 Routing on RZ/V2N Group, RZ/V2H Group and RZ/G3E Group

The audio routing on the RZ/V2N, RZ/V2H and RZ/G3E include sampling rate conversion, mixing ,channel transfer unit and ramp. It shows as below. Refer to **section 4.3** for more details.

Table 1-16 Audio Routing

Operation	Support route
Playback	Memory -> SSIn
	Memory -> SCU(SRCm) -> SSIn
	Memory -> SCU(SRCm -> DVCI) -> SSIn
	Memory -> SCU(SRCm -> CTUk -> MIXj -> DVCI) -> SSIn
	Memory -> SPDIFx -> Output pin
Capture	SSIn -> Memory
	SSIn -> SCU(SRCm) -> Memory
	SSIn -> SCU(SRCm -> DVCI) -> Memory
	Input pin -> SPDIFx -> Memory
	PDMy -> Memory

Notes: SSIn: n=0 to 9, SRCm: m=0 to 9, DVCI: l=0, 1, CTUk: k=0, 1, MIXj: j=0, 1, SPDIF: x=0, PDMy:y=0 to 2

Table 1-17 Audio Features

Module	Feature
Sampling rate conversion (SRC)	Support the sampling rate conversion function using the SRC
Mixing (MIX)	Mix two or four sources into one.
Channel transfer unit (CTU)	Provide the channel count conversion
Ramp	Aim to make gradual change to the specified volume at MIX and DVC.

1.2.6 Related Documents

The following tables show the document related to this module.

Table 1-18 Related documents for RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, and RZ/Five boards

Number	Issue	Title	Edition	Date
WM8978CGEFL/V	Wolfson Microelectronics plc	WM8978 Stereo CODEC with Speaker Driver	Revision 4.5	Sept.2011

Table 1-19 Related documents for RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E

Number	Issue	Title	Edition	Date
DA7212	Renesas Electronic Corporation	DA7212 Ultra Low Power Stereo Codec	Revision 3.5	Jan.2022

1.3 Restrictions

There is no reference document on standards.

1.4 Notice

The sampling rate uses the same setting in input/output. When playback/capture executes at the same time, a consistent sampling rate should be used.

2. Terminology

The following table shows the terminology related to this module.

Table 2-1 Terminology

Terms	Explanation
ADG	Audio clock generator
ALSA	Advanced Linux Sound Architecture The term on ALSA is provided by the ALSA site. http://www.alsa-project.org/
ASoC	ALSA for SoC
CTU	Channel transfer unit
DAI	Digital Audio Interfaces
DMAC	Direct Memory Access Controller
DVC	Digital volume and mute function
I2C	Inter-Integrated Circuit
MIX	Mixing unit
PCM	Pulse Code Modulation
SCU	Sampling rate converter unit SCU is RZ/G2 Group; includes SRC/CTU/MIX/DVC.
SRC	Sampling rate conversion
SSI	Serial sound interface
SSIU	Serial sound interface unit SSIU is RZ/G2 Group; provides the function of SSI (Serial sound interface).
SPDIF	Sony/Philips Digital Interface Format
TDM	Time Division Multiplexing
PDM	Pulse Density Modulation

3. Operating Environment

3.1 Hardware Environment

The following tables list the hardware devices needed to use this module.

Table 3-1 Hardware Environment

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

3.2 Module Configuration

The following figure shows the configuration of this module. DMA transfer is supported at both directions (capture and playback).

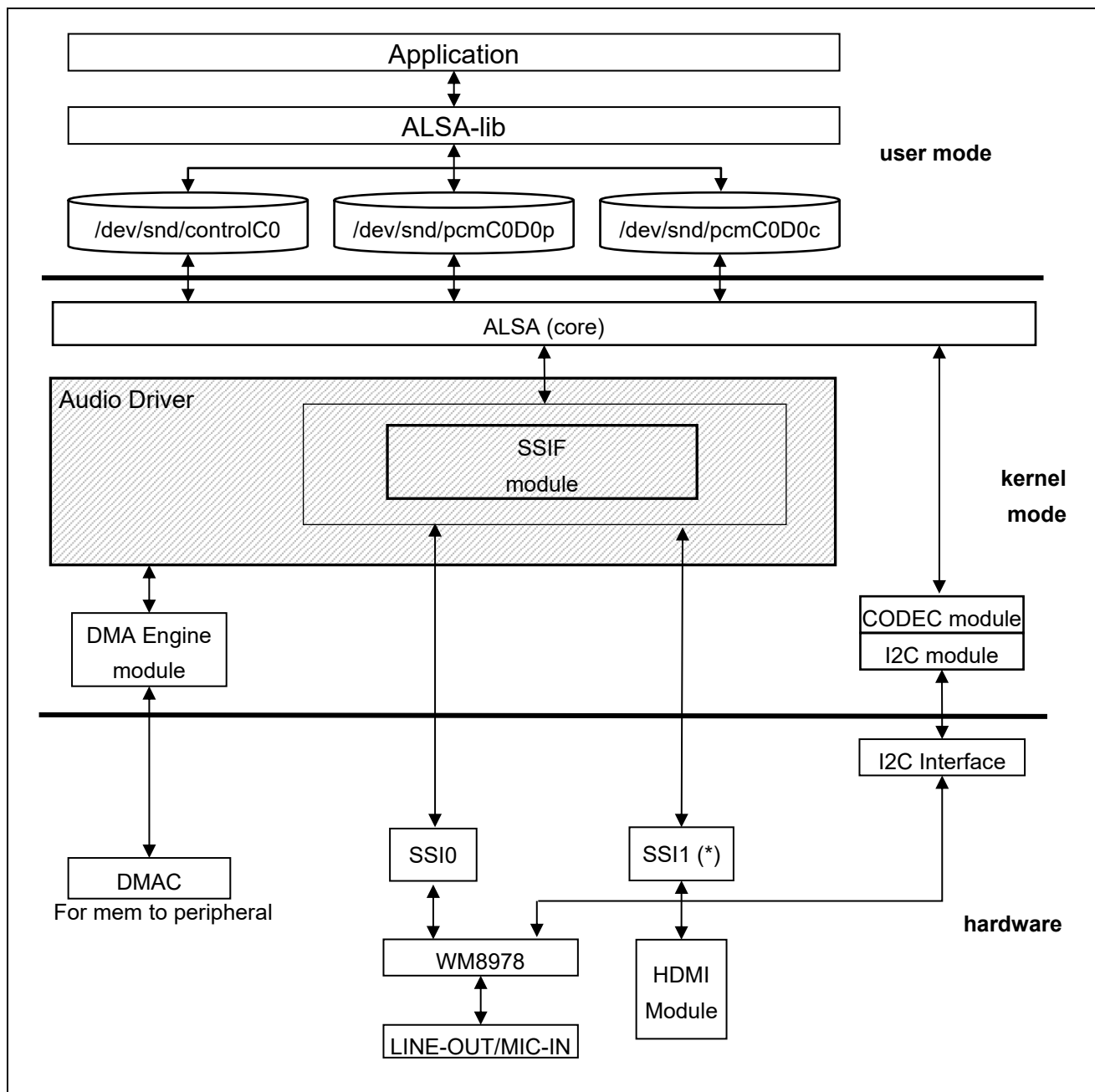


Figure 3-1 Audio Driver configuration (RZ/G2L, RZ/G2LC, and RZ/V2L)

*: SSIO1 connection is only available on RZ/G2L and RZ/V2L. In the RZ/G2LC, WM8978 and HDMI module are multiplexed, and both connected to SSIO0; SW1-5 selects which module is enabled.

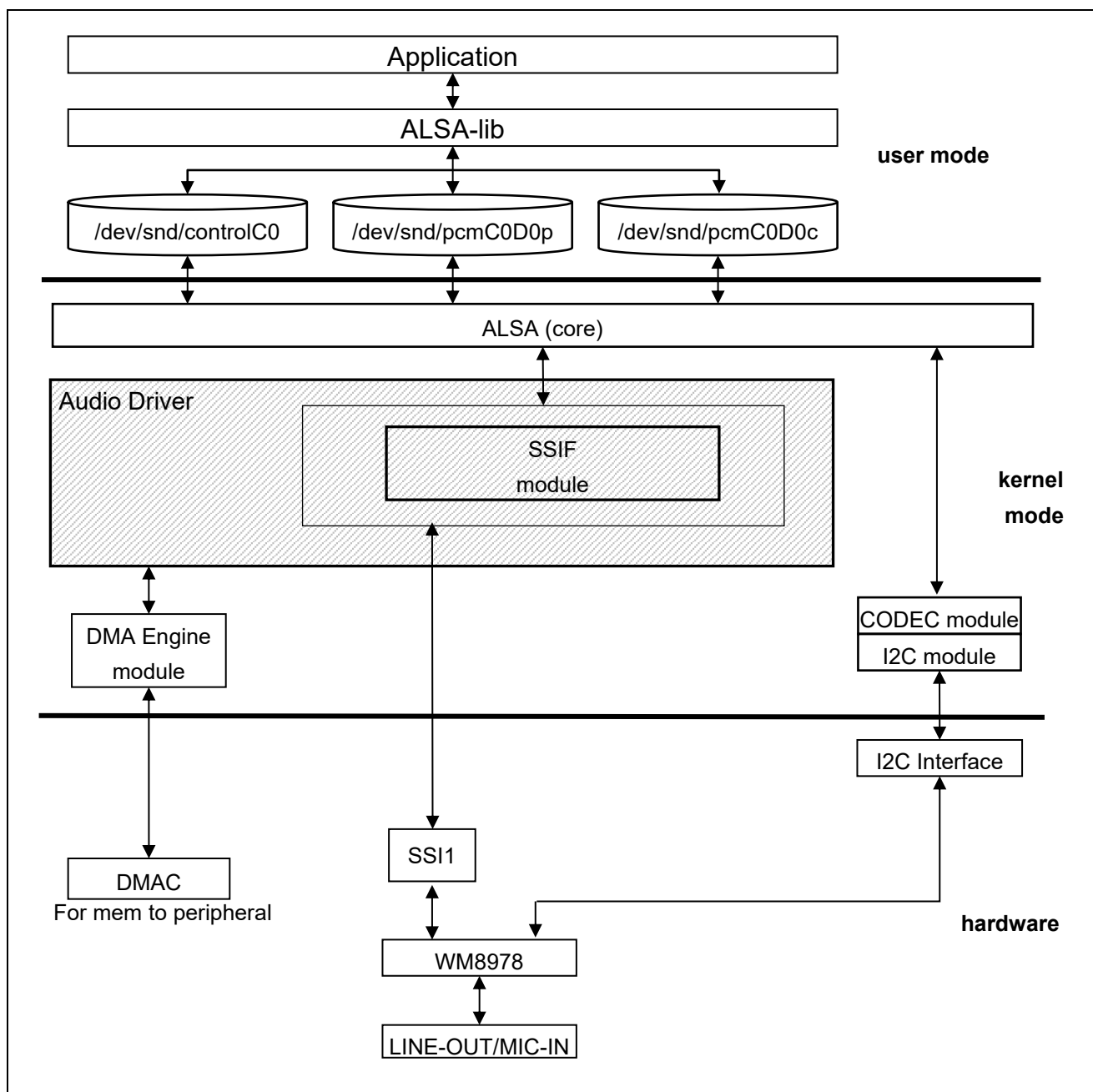


Figure 3-2 Audio Driver configuration (RZ/G2UL, and RZ/Five)

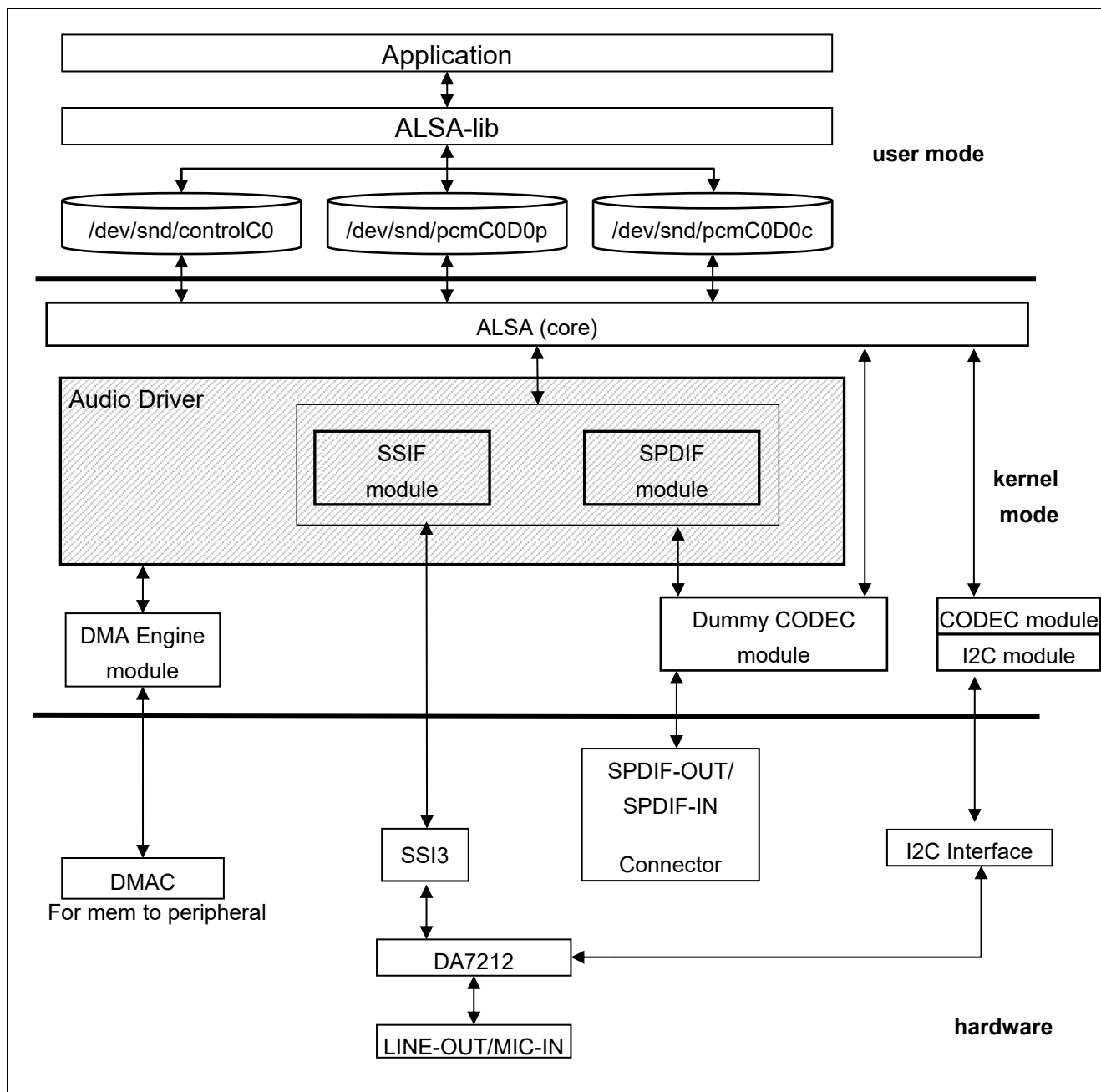


Figure 3-3 Audio Driver configuration for RZ/G3S

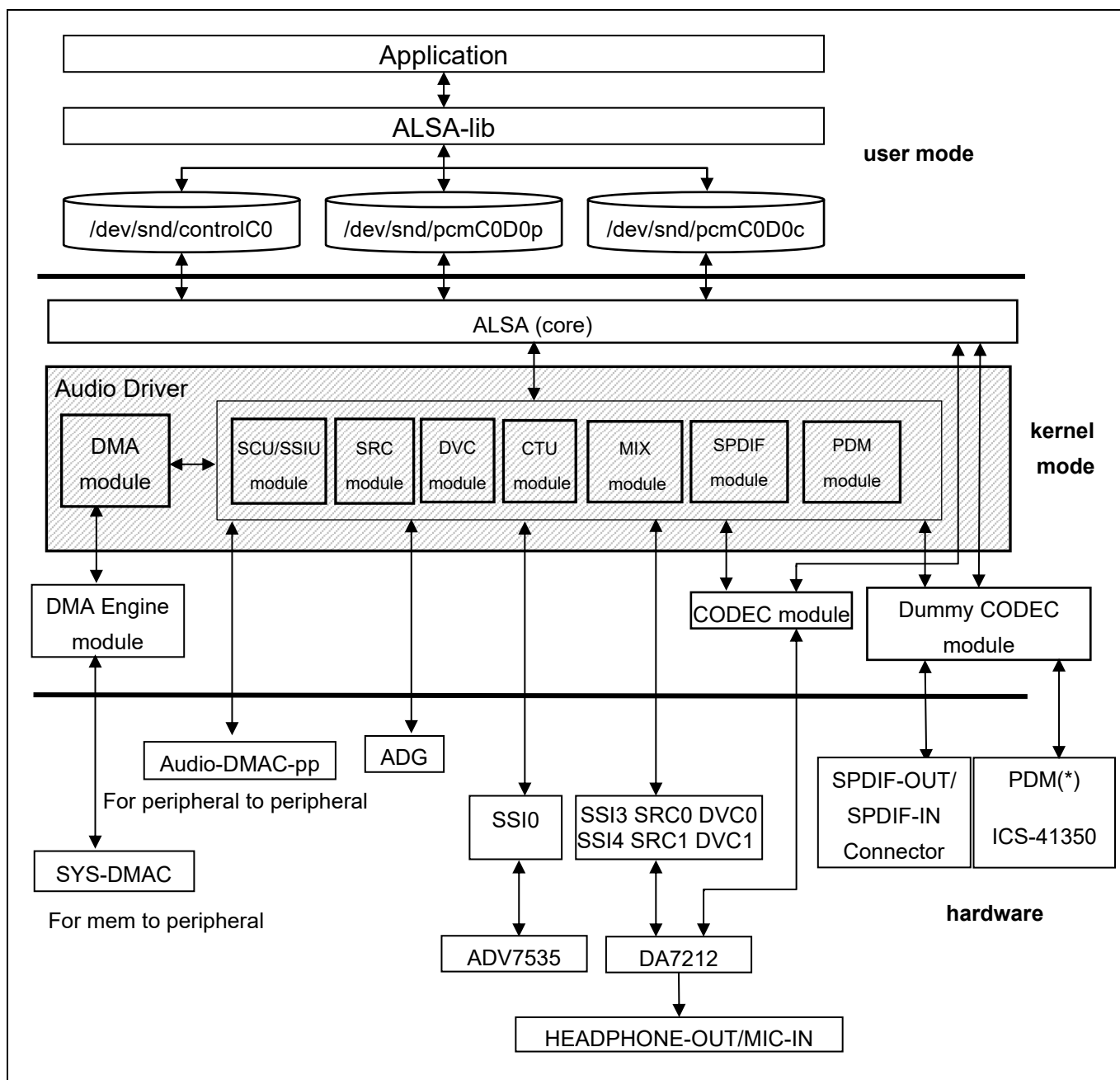


Figure 3-4 Audio Driver configuration (RZ/V2N, RZ/V2H and RZ/G3E)

(*) PDM only supported in RZ/G3E

3.3 State Transition Diagram

There is no state transition diagram for this module.

4. External Interface

This module is based on ALSA sound. This manual describes only a peculiar function.

4.1 Device

A device is expressed as follows by the ALSA interface.

Table 4-1 ALSA Device Interface

ALSA interface	Device node
Information Interface	/proc/asound
Control Interface	/dev/snd/controlCX
PCM Interface	/dev/snd/pcmCXDX
Timer Interface	/dev/snd/timer

String of device node format "X" indicates a numeric character.

4.2 Device Node

The following table shows the device nodes of this module. This case is BSP standard settings.

Table 4-2 Device node

Device node	Major number	Minor number
/dev/snd/controlC0	116	0
/dev/snd/controlC1	116	32
/dev/snd/pcmC0D0c	116	24
/dev/snd/pcmC0D0p	116	16
/dev/snd/pcmC1D0p	116	48
/dev/snd/timer	116	33

Notes: /dev/snd/controlC1, /dev/snd/pcmC1D0p are only available on RZ/G2L, RZ/V2L boards.

4.3 Setting route

This module provides the function of statically setting the audio routes for playback and capture paths.

Audio routes on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five can be defined in “**sound-dai**” (when using “simple-audio-card” method) or “**dais**” properties (when using “audio-graph-card” method) of the sound node in device tree.

On RZ/V2N, audio routes can be defined in “rcar_sound_dai” (when using “simple-audio-card”) or “ports” properties (when using “audio-graph-card” method) of “rcar_sound” node in device tree.

Please refer to **Table 4-3** for a list of device trees of the supported boards.

Table 4-3 Device tree files

Processor	LSI Version	Board	Board Revision	Memory Size	Device Tree	Included Files
RZ/G2L	-	RZ/G2L SMARC EVK	v01	2GB	r9a07g044l2-smarc.dts	r9a07g044l2.dtsi rzg2l-smarc.dtsi
RZ/G2LC	-	RZ/G2LC SMARC EVK	v01	2GB	r9a07g044c2-smarc.dts	r9a07g044c2.dtsi rzg2lc-smarc.dtsi
RZ/G2UL	-	RZ/G2UL SMARC EVK	v01	1GB	r9a07g043u11-smarc.dts	r9a07g043u11.dtsi rzg2ul-smarc.dtsi
RZ/V2L	-	RZ/V2L SMARC EVK	v01	2GB	r9a07g054l2-smarc.dts	r9a07g054l2.dtsi rzg2l-smarc.dtsi
RZ/Five		RZ/Five SMARC EVK	v01	1GB	r9a07g043f01-smarc.dts	r9a07g043f.dtsi rzfive-smarc.dtsi
RZ/V2N		RZ/V2N Evaluation Kit	v01	8GB	r9a09g056n48-v2n-evk.dts	r9a09g056.dtsi
RZ/V2H		RZ/V2H Evaluation Kit	v01	8GB	r9a09g057h44-rzv2h-evk.dts	r9a09g057.dtsi
RZ/G3E		RZ/G3E SMARC Evaluation Kit	v01	4GB	r9a09g047e57-smarc.dts	r9a09g047.dtsi
RZ/G3S		RZ/G3S SMARC Evaluation Kit	v01	4GB	r9a08g045s33-smarc.dts	r9a08g045.dtsi

4.3.1 Data transmission paths

This section describes Audio data route in different setting cases along with device tree example in each case.

4.3.1.1 Data transmission paths on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five

Data transmission paths in the Audio module of these boards are shown in (Figure 4-1)

Note: On RZ/G3S, SSI3 is used instead of SSI0/1.

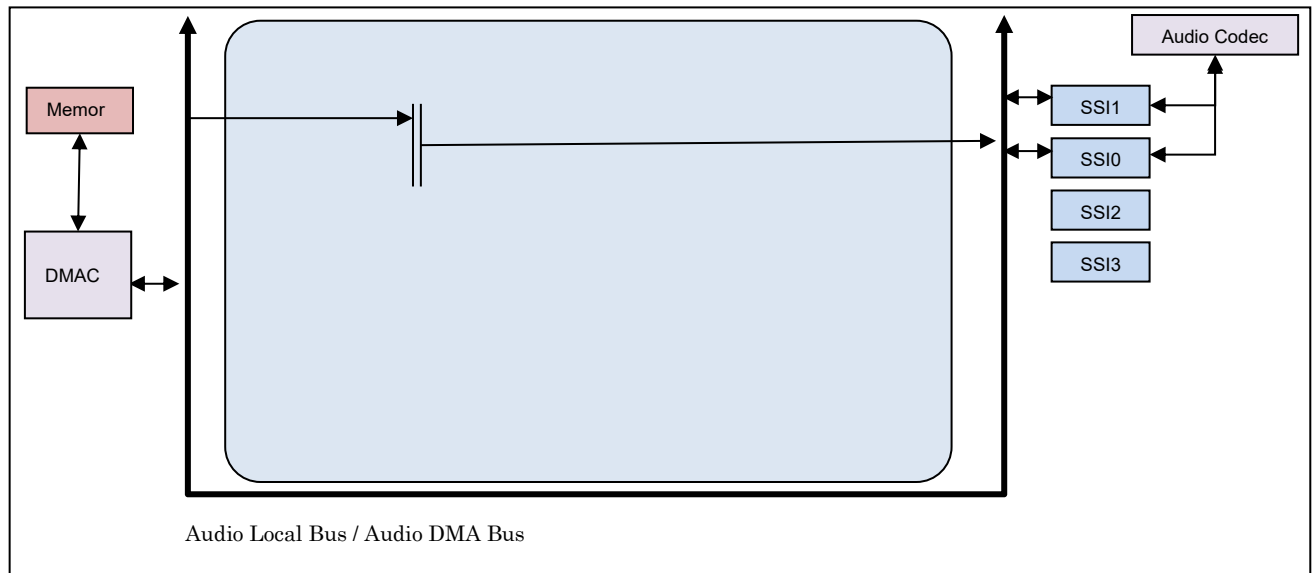


Figure 4-1 Data transmission paths (RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five)

4.3.1.2 Data transmission paths on RZ/V2N, RZ/V2H and RZ/G3E

On RZ/V2N, RZ/V2H and RZ/G3E, data transmission paths in the Audio module for SSI, SRC, CTU, MIX, DVC are shown in Figure 4-2.

The setting uses components as below:

&src0	&ctu00	&mix0	&dvc0	&ssi0
&src1	&ctu01	&mix1	&dvc1	&ssi1
&src2	&ctu02			&ssi2
&src3	&ctu03			&ssi3
&src4				&ssi4
&src5	&ctu10			&ssi5
&src6	&ctu11			&ssi6
&src7	&ctu12			&ssi7
&src8	&ctu13			&ssi8
&src9				&ssi9

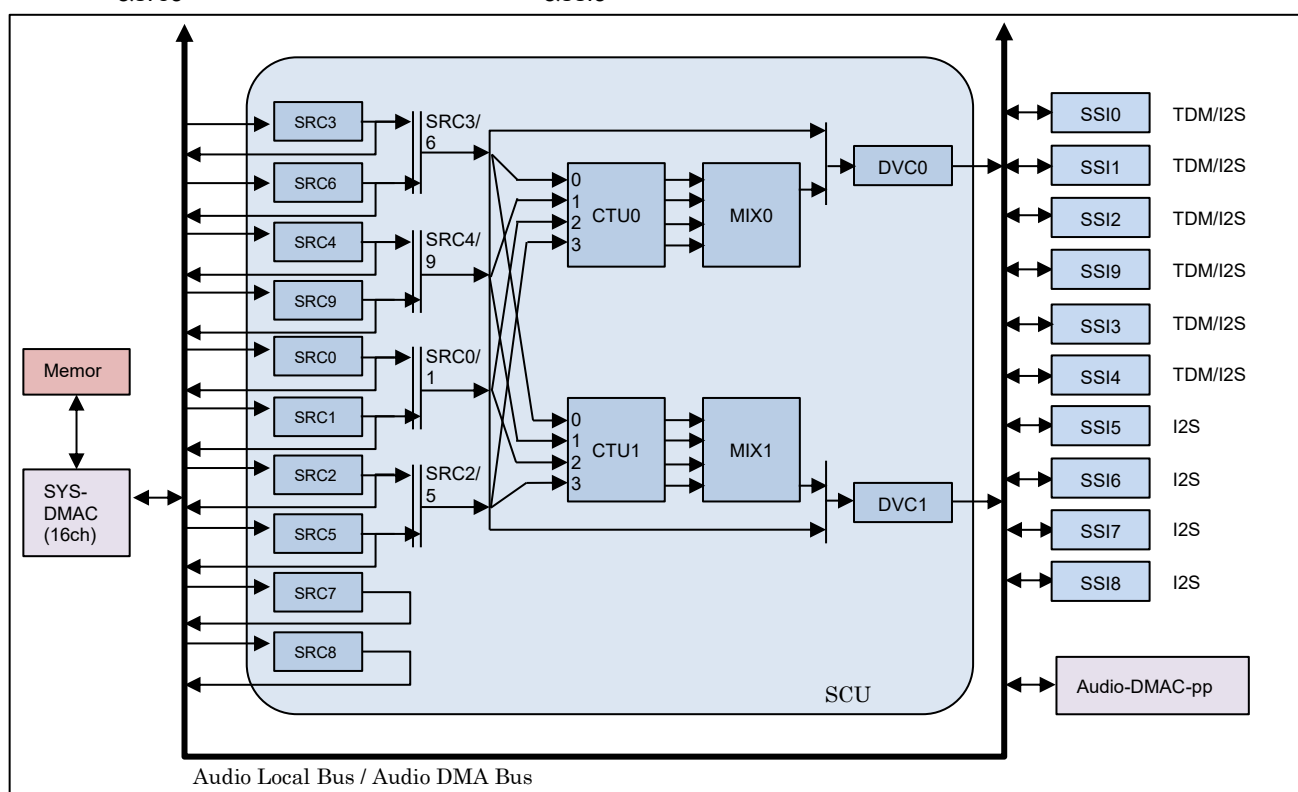


Figure 4-2 Data transmission paths (RZ/V2N, RZ/V2H and RZ/G3E)

4.3.2 Setting route for playback

4.3.2.1 On RZ/G2L, RZ/G2UL, RZ/G2LC, RZ/V2L, RZ/G3S and RZ/Five

(1) Setting case of “Memory -> SSI0 -> CODEC”

Route path shows the case of "Memory-> SSI0-> CODEC". On the RZ/G3S, the setting case is the same, but SSI3 is used instead of SSI0.

Transfer settings of audio are set to transfer data from the memory to the “SSI0” with or without using DMA at the driver.

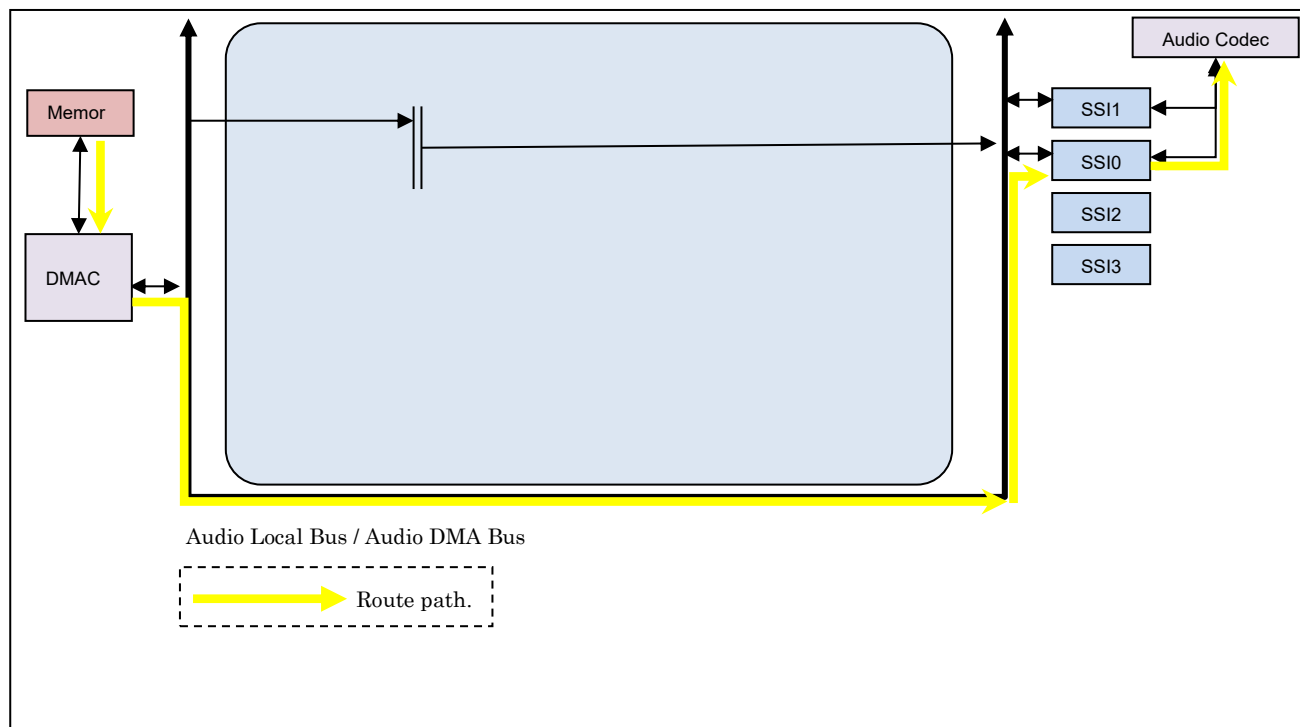


Figure 4-3 Memory-> SSI0->CODEC data path

This route case's description example is shown below.

```

snd_rzg2l: sound {
    compatible = "simple-audio-card";
    simple-audio-card,format = "i2s";
    simple-audio-card,bitclock-master = <&cpu_dai>;
    simple-audio-card,frame-master = <&cpu_dai>;
    simple-audio-card,mclk-fs = <256>;

    simple-audio-card,widgets = "Microphone", "Microphone Jack";
    simple-audio-card,routing =
        "L2", "Mic Bias",
        "R2", "Mic Bias",
        "Mic Bias", "Microphone Jack";

    cpu_dai: simple-audio-card,cpu {
        sound-dai = <&ssi0>;
    };

    codec_dai: simple-audio-card,codec {
        sound-dai = <&wm8978>;
        clocks = <&versa3 2>;
    };
};

x1: x1-clock {
    compatible = "fixed-clock";
    #clock-cells = <0>;
    clock-frequency = <24000000>;
};

&ssi0 {
    pinctrl-0 = <&ssi0_pins>;
    pinctrl-names = "default";

    dmas = <&dma0 0x9501>,
        <&dma0 0x9502>;
    dma-names = "tx", "rx";
    status = "okay";
};

&i2c3 {
    versa3: versa3@68 {
        compatible = "renesas,5p35023";
        reg = <0x68>;
        #clock-cells = <1>;
        clocks = <&x1>;
        renesas,settings = [
            80 00 11 19 4c 02 23 7f 83 19 08 a9 5f 25 24 bf
            00 14 7a e1 00 00 00 00 01 55 59 bb 3f 30 90 b6
            80 b0 45 c4 95];
        assigned-clocks = <&versa3 0>, <&versa3 1>,
            <&versa3 2>, <&versa3 3>,
            <&versa3 4>, <&versa3 5>;
        assigned-clock-rates = <24000000>, <11289600>,
            <11289600>, <12000000>,
            <25000000>, <12288000>;

    wm8978: codec@1a {
        compatible = "wlf,wm8978";
        #sound-dai-cells = <0>;
        reg = <0x1a>;
    };
};

```

Figure 4-4 Example of setting for Memory->SSI0->CODEC

```

&i2c0 {
    status = "okay";

    clock-frequency = <1000000>;

    da7212: codec@1a {
        compatible = "dlg,da7212";
        reg = <0x1a>;

        clocks = <&versa3 1>;
        clock-names = "mclk";

        #sound-dai-cells = <0>;

        dlg,micbias1-lvl = <2500>;
        dlg,micbias2-lvl = <2500>;
        dlg,dmic-data-sel = "lrise_rfall";
        dlg,dmic-samplephase = "between_clkedge";
        dlg,dmic-clkrate = <3000000>;

        VDDA-supply = <&reg_1p8v>;
        VDDSP-supply = <&reg_3p3v>;
        VDDMIC-supply = <&reg_3p3v>;
        VDDIO-supply = <&reg_1p8v>;
    };
};

&i2c1 {
    status = "okay";

    versa3: clock-generator@68 {
        compatible = "renesas,5l35023";
        reg = <0x68>;
        clocks = <&x3_clk>;
        #clock-cells = <1>;
        assigned-clocks = <&versa3 0>,
            <&versa3 1>,
            <&versa3 2>,
            <&versa3 3>,
            <&versa3 4>,
            <&versa3 5>;
        assigned-clock-rates = <24000000>,
            <12288000>,
            <11289600>,
            <25000000>,
            <100000000>,
            <100000000>;
        renesas,settings = [
            80 00 11 19 4c 42 dc 2f 06 7d 20 1a 5f 1e f2 27
            00 40 00 00 00 00 00 06 0c 19 02 3f f0 90 86
            a0 80 30 30 9c
        ];
    };
};

```

```

snd_rzg3s: sound {
    compatible = "simple-audio-card";
    simple-audio-card,name = "snd_rzg3s";

    ssi_link: simple-audio-card,dai-link@0 {
        format = "i2s";
        bitclock-master = <&cpu_dai0>;
        frame-master = <&cpu_dai0>;
        mclk-fs = <256>;

        cpu_dai0: cpu {
            sound-dai = <&ssi3>;
        };

        codec {
            sound-dai = <&da7212>;
            clocks = <&versa3 1>;
        };
    };
};

&ssi3 {
    clocks = <&cpg CPG_MOD R9A08G045_SSI3_PCLK2>,
            <&cpg CPG_MOD R9A08G045_SSI3_PCLK_SFR>,
            <&versa3 2>, <&audio_clk2>;
    pinctrl-names = "default";
    pinctrl-0 = <&ssi3_pins>, <&audio_clock_pins>;
    status = "okay";
};

```

Figure 4-5 Example of setting for Memory -> SSI3 -> CODEC on RZ/G3S

(2) Setting case of "Memory -> SPDIF -> CODEC" supported on RZ/G3S

Route path shows the case of "Memory-> SPDIF-> CODEC".

Transfer settings of audio are set to transfer data from the memory to the "SPDIF" with or without using DMA at the driver.

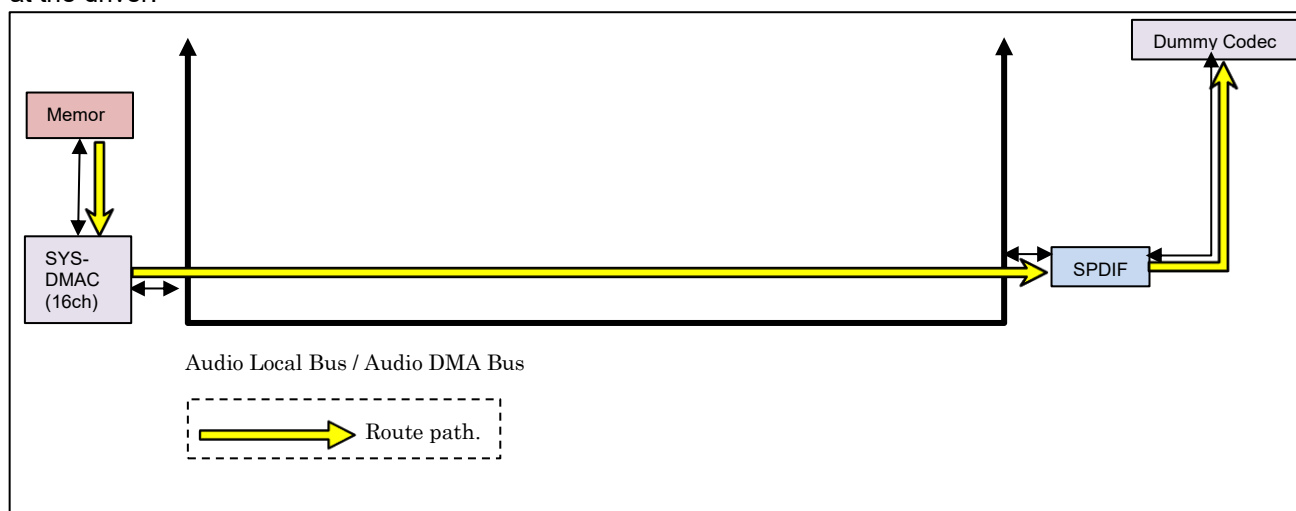


Figure 4-6 Memory -> SPDIF -> CODEC

This route case's description example is shown below:

```
snd_rzg3s: sound {
    compatible = "simple-audio-card";
    simple-audio-card,name = "snd_rzg3s";

    spdif_link: simple-audio-card,dai-link@1 {
        bitclock-master = <&cpu_dai1>;
        frame-master = <&cpu_dai1>;

        cpu_dai1: cpu {
            sound-dai = <&spdif>;
        };

        codec {
            sound-dai = <&dummy_codec>;
        };
    };
};

&spdif {
    pinctrl-0 = <&spdif_pins>;
    pinctrl-names = "default";
    status = "okay";
};
```

Figure 4-7 Example of setting for Memory -> SPDIF -> CODEC

4.3.2.2 On RZ/V2N, RZ/V2H and RZ/G3E

(1) Setting case of “Memory -> SSI3 -> CODEC”

Route path shows the case of "Memory-> SSI3-> CODEC".

Transfer settings of audio DMAC is set to transfer from the memory to the “SSIO3” at the driver. Audio DMAC-pp is no use in this case.

Please refer to “RZ/V2N Group User’s Manual: Hardware”, “RZ/V2H Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

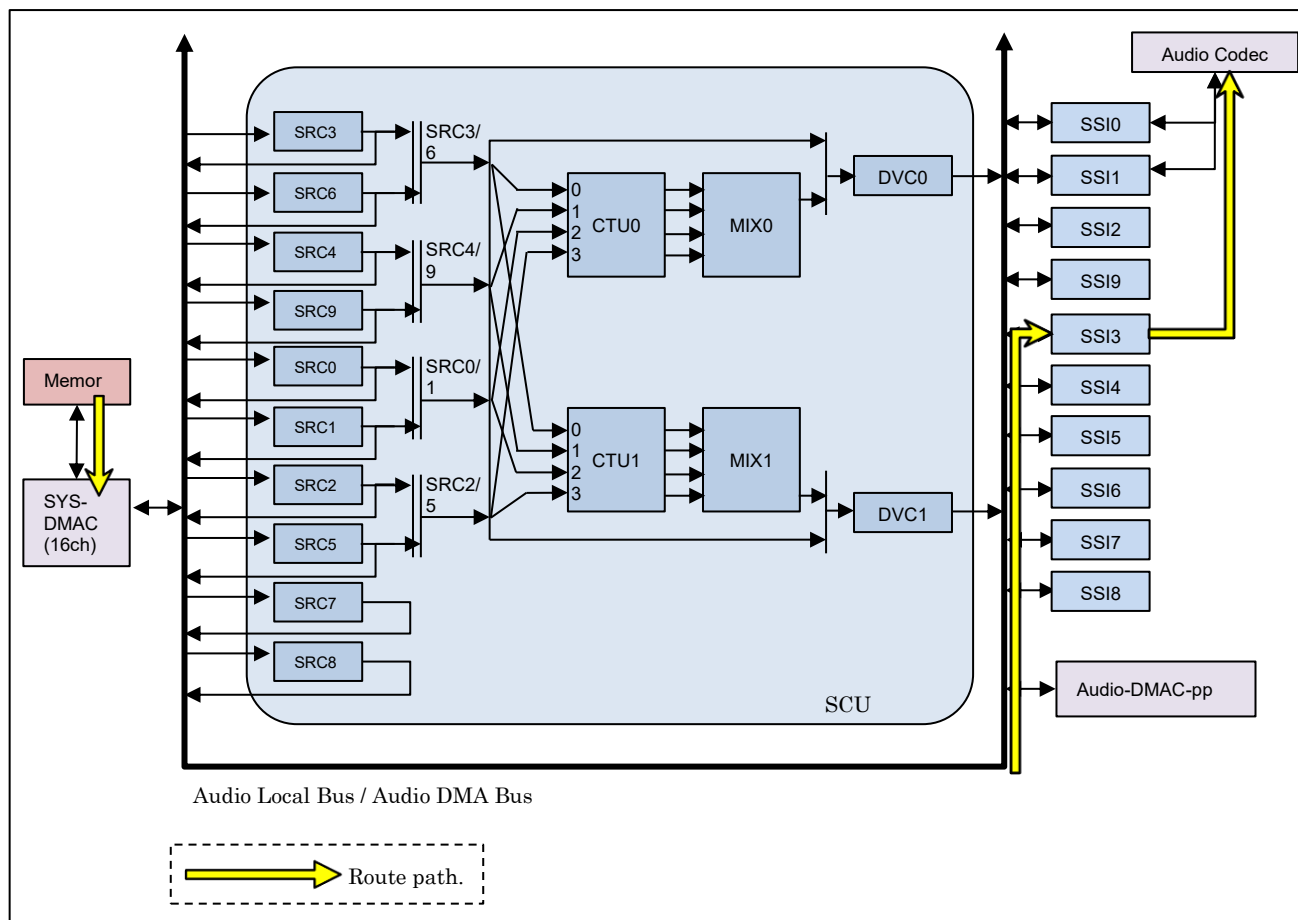


Figure 4-8 Memory->SSI3->CODEC data path (RZ/V2N, RZ/V2H and RZ/G3E)

The devicetree setting for this route case is described in

Figure 4-9

```
&i2c2 {
    da7212: codec@1a {
        port {
            da7212_endpoint: endpoint {
                remote-endpoint = <&rsnd_endpoint0>;
            };
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>;
            };
        };
    };
};
```

Figure 4-9 Example of setting for Memory -> SSI3 -> CODEC

(1) Setting case of “Memory -> SRC0 -> SSI3 -> CODEC”

Route path shows the case of "Memory-> SRC0 -> SSI3-> CODEC".

Transfer settings of audio DMAC is set to transfer from the memory to the “SCU_SRC10” at the driver. In addition, the transfer setting of audio DMAC-pp is set to transfer from “SCU_SRC00” to the “SSIO3” at the driver.

Please refer to “RZ/V2N Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

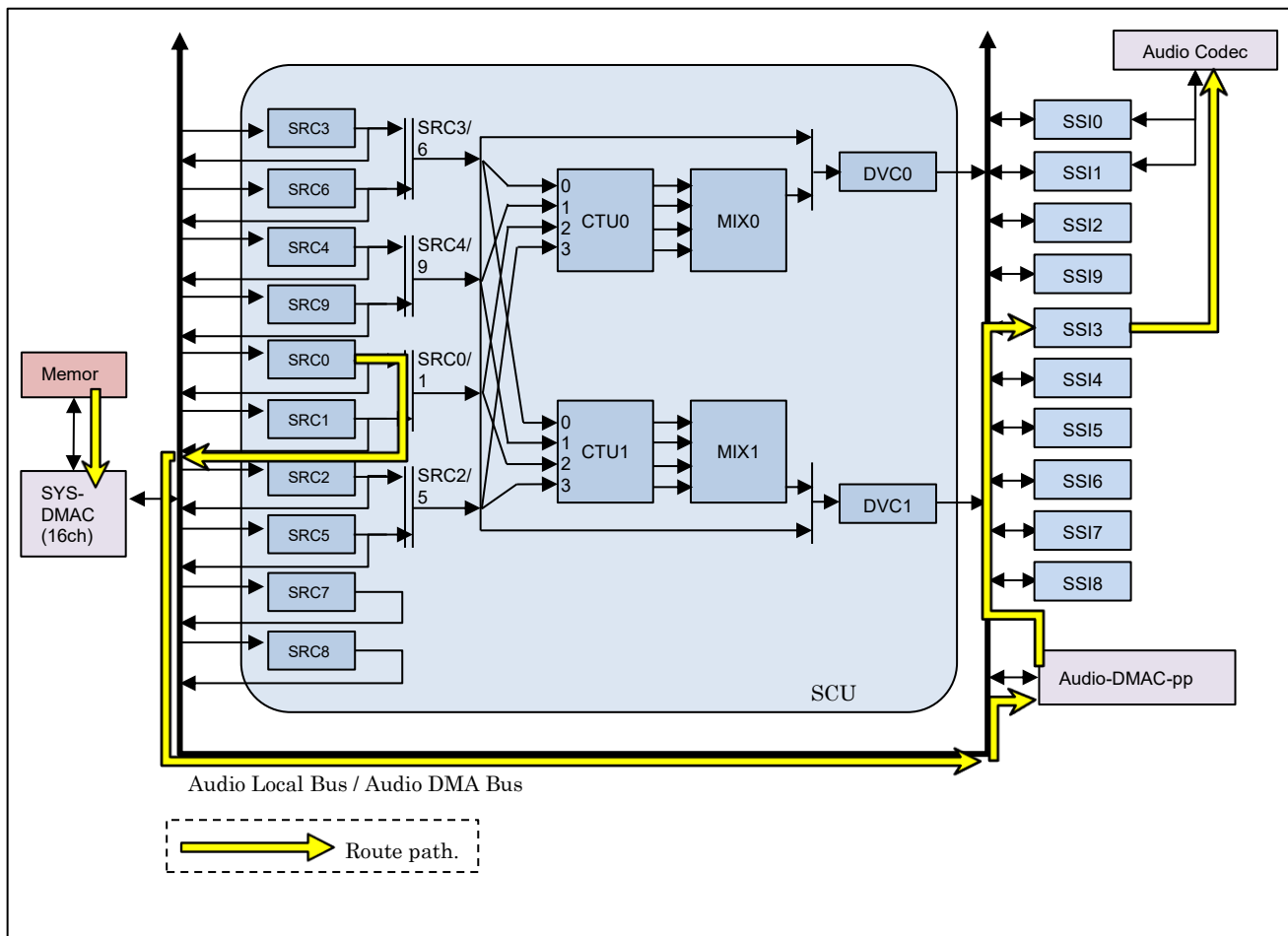


Figure 4-10 Memory->SRC0->SSI3->CODEC data path

This route case's description example is shown as below.

```

&i2c2 {
    da7212: codec@1a {
        port {
            da7212_endpoint: endpoint {
                remote-endpoint = <&rsnd_endpoint0>;
            };
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>, <&src0>;
            };
        };
    };
};

```

Figure 4-11 Example of setting for memory -> SRC0 ->SSI3 -> CODEC

(3) Setting case of “Memory -> SRC0 -> DVC0 -> SSI3 -> CODEC”

Route path shows the case of "Memory-> SRC0 -> DVC0 -> SSI3 -> CODEC".

Transfer settings of audio DMAC is set to transfer from the memory to the “SCU_SRCI0” at the driver. In addition, the transfer setting of audio DMAC-pp is set to transfer from “SCU_CMD0” to the “SSIO3” at the driver.

Please refer to “RZ/V2N Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

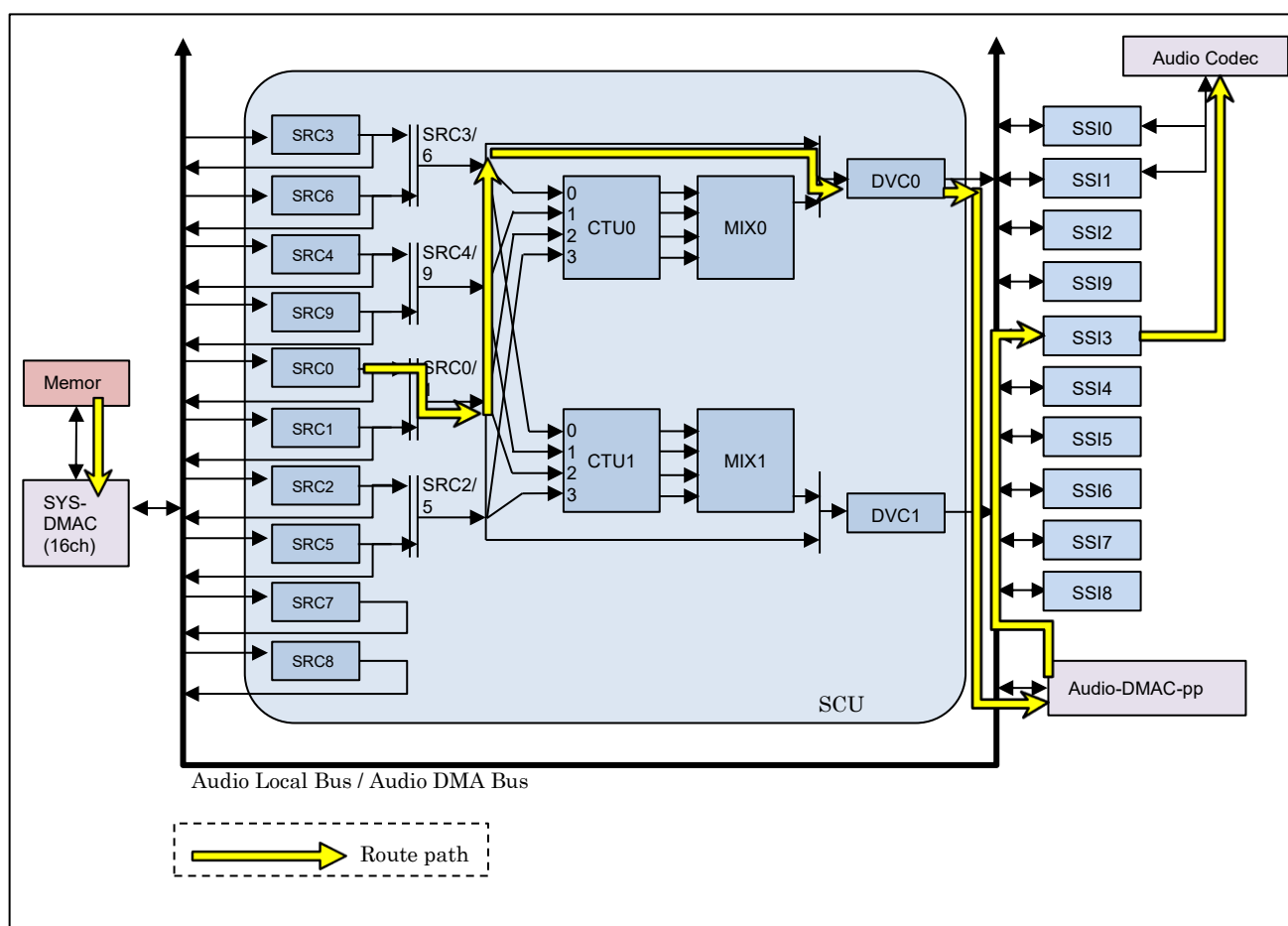


Figure 4-12 Memory->SRC0->DVC0->SSI3->CODEC data path

This route case's description example is shown as below.

```
&i2c2 {
    da7212: codec@1a {
        port {
            da7212_endpoint: endpoint {
                remote-endpoint = <&rsnd_endpoint0>;
            };
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>, <&src0>, <&dvc0>;
            };
        };
    };
};
```

Figure 4-13 Example of setting Memory->SRC0->DVC0->SSI3->CODEC

(4) Setting case of “Memory -> SRC1 -> CTU02 -> MIX0 -> DVC0 -> SSI3 -> CODEC” and “Memory -> SRC2 -> CTU03 -> MIX0 -> DVC0 -> SSI3 -> CODEC”

Route path shows the case of “Memory -> SRC1 -> CTU02 -> MIX0 -> DVC0 -> SSI3 -> CODEC” and “Memory -> SRC2 -> CTU03 -> MIX0 -> DVC0 -> SSI3 -> CODEC”. This route path setting is mixing the two audio.

Transfer settings of audio DMAC is set to transfer from the memory to the “SCU_SRC11” at the driver. In addition, the transfer setting of audio DMAC-pp is set to transfer from “SCU_CMD0” to the “SSIO3” at the driver.

Similarly, another transfer settings of audio DMAC is set to transfer from the memory to the “SCU_SRC12” at the driver.

Please refer to “RZ/V2N Group User’s Manual: Hardware”, “RZ/V2H Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

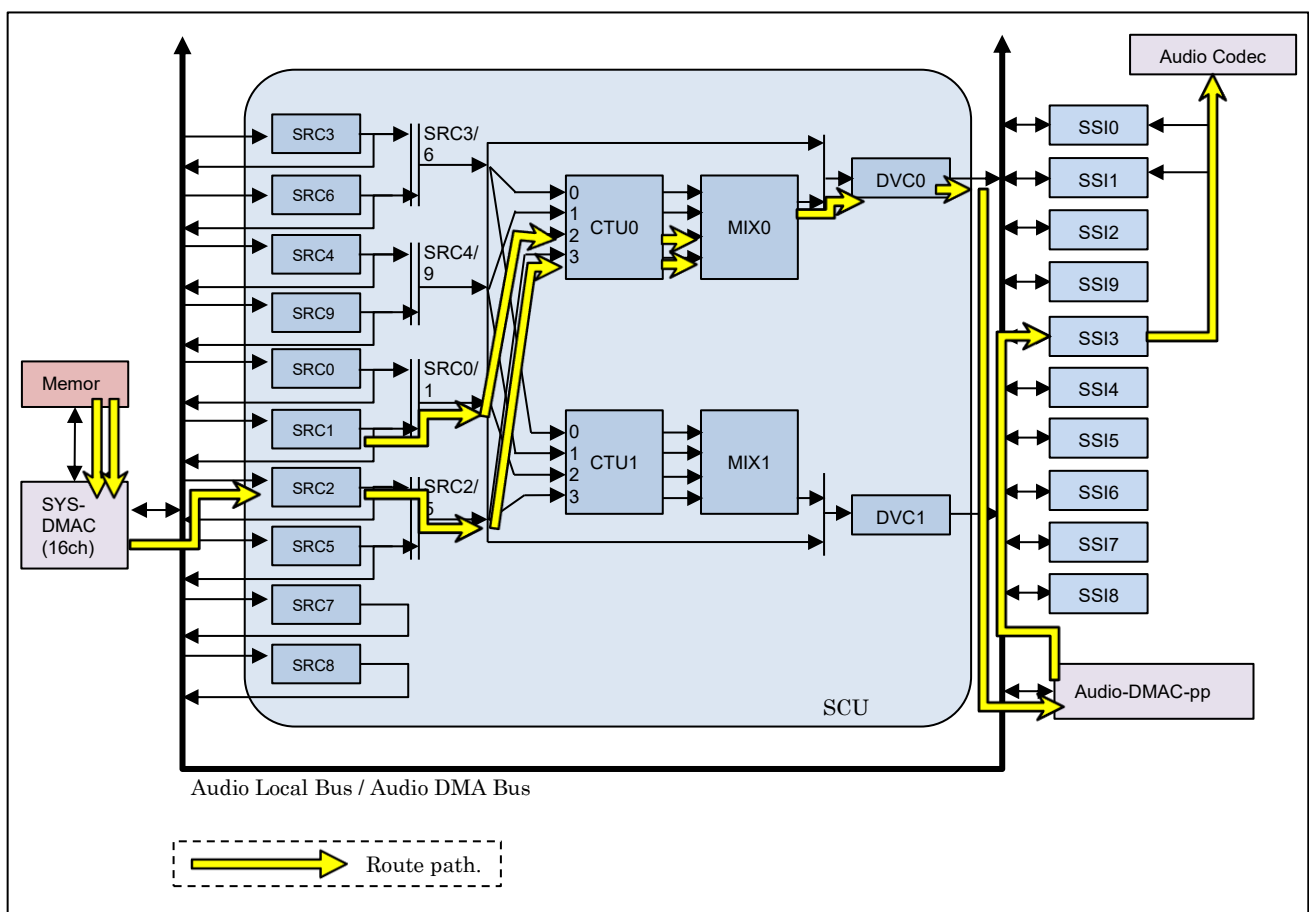


Figure 4-14 Memory->SRC1/2->CTU02/03->MIX0->DVC0->SSI3->CODEC data path

This route case's description example is shown as below.

```
&i2c2 {
    da7212: codec@1a {
        port {
            da7212_endpoint: endpoint {
                remote-endpoint = <&rsnd_endpoint0>;
            };
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&src1 &ctu02 &mix0 &dvc0 &ssi3>; // playback = <&src2 &ctu03 &mix0
                &dvc0 &ssi3>;
            };
        };
    };
};
```

Figure 4-15 Example of setting for Memory->SRC1/2->CTU02/03->MIX0->DVC0->SSI1->CODEC

```

&i2c3 {
    adv7535: hdmi@3d {
        compatible = "adi,adv7535";

        port@2 {
            reg = <2>;
            dsi_hdmi0_snd_in: endpoint {
                remote-endpoint = <&rsnd_endpoint1>;
            };
        };
    };

    sound_card: sound {
        compatible = "audio-graph-card";

        label = "rsnd_rzv2n";

        dais = <
            &rsnd_port0 /* HDMI */
        >;
    };

    &rcar_sound {
        pinctrl-0 = <&sound_pins>;
        pinctrl-names = "default";

        status = "okay";

        /* audio_clkout */
        #clock-cells = <0>;
        clock-frequency = <11289600>;

        /* Multi DAI */
        #sound-dai-cells = <1>;

        ports {
            #address-cells = <1>;
            #size-cells = <0>;

            rsnd_port0: port@0 {
                reg = <0>;
                rsnd_endpoint0: endpoint {
                    remote-endpoint = <&dsi_hdmi0_snd_in>;
                    dai-format = "i2s";
                    bitclock-master = <&rsnd_endpoint0>;
                    frame-master = <&rsnd_endpoint0>;

                    playback = <&ss0>;
                };
            };
        };
    };
};

```

Figure 4-16 Example of setting for Memory -> SSI0 -> HDMI_CODEC

(5) Setting case of “Memory -> SPDIF -> CODEC”

Route path shows the case of "Memory-> SPDIF-> CODEC".

Transfer settings of audio are set to transfer data from the memory to the “SPDIF” with or without using DMA at the driver.

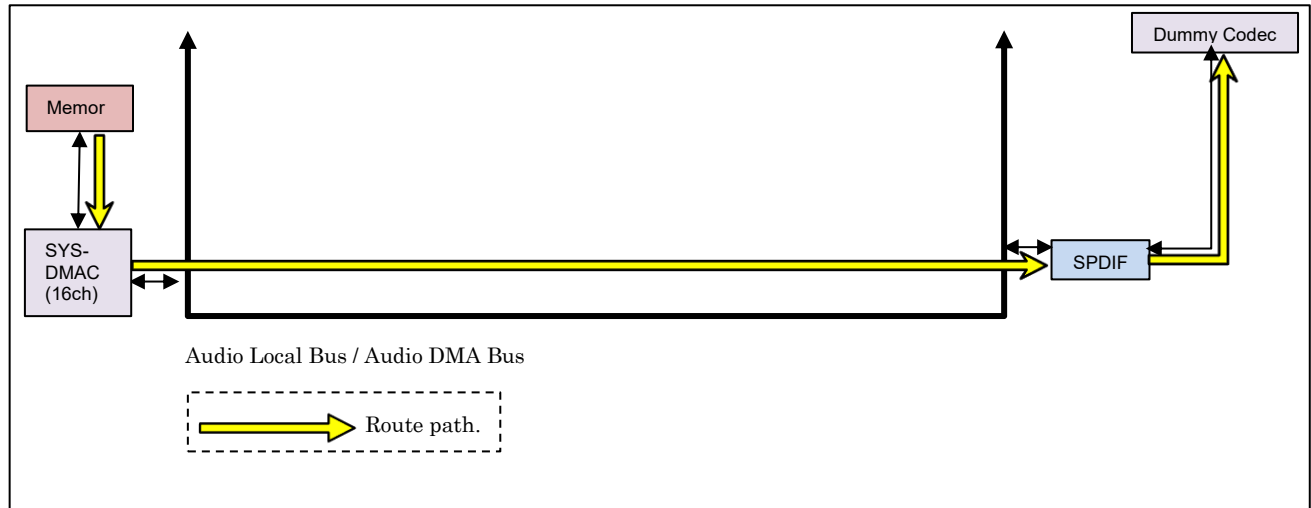


Figure 4-17 Memory -> SPDIF -> CODEC data path

This route case's description example is shown below:

```

codec_test0: codec_test0 {
    compatible = "linux,snd-soc-dummy";
    #sound-dai-cells = <0>;
    port {
        dummy_codec0: endpoint {
            remote-endpoint = <&spdif0_endpoint>;
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &spdif_port2
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        spdif_port0: port@0 {
            reg = <0>;
            spdif0_endpoint: endpoint {
                remote-endpoint = <&dummy_codec0>;

                bitclock-master = <&spdif0_endpoint>;
                frame-master = <&spdif0_endpoint>;

                playback = <&spdif0>;
            };
        };
    };
};

```

Figure 4-18 Example of setting for Memory -> SPDIF -> CODEC

4.3.3 Setting route for capture

4.3.3.1 On RZ/G2L, RZ/G2UL, RZ/G2LC, RZ/V2L, RZ/G3S and RZ/Five

(1) Setting case of “CODEC -> SSI0 -> Memory”

Route path shows the case of "CODEC-> SSI0-> Memory".

Transfer settings of audio are set to transfer data from the “SSI0” to the memory with or without using DMA at the driver.

On the RZ/G3S, the setting case is the same, but it is used SSI3 instead of both SSI0 and SSI1.

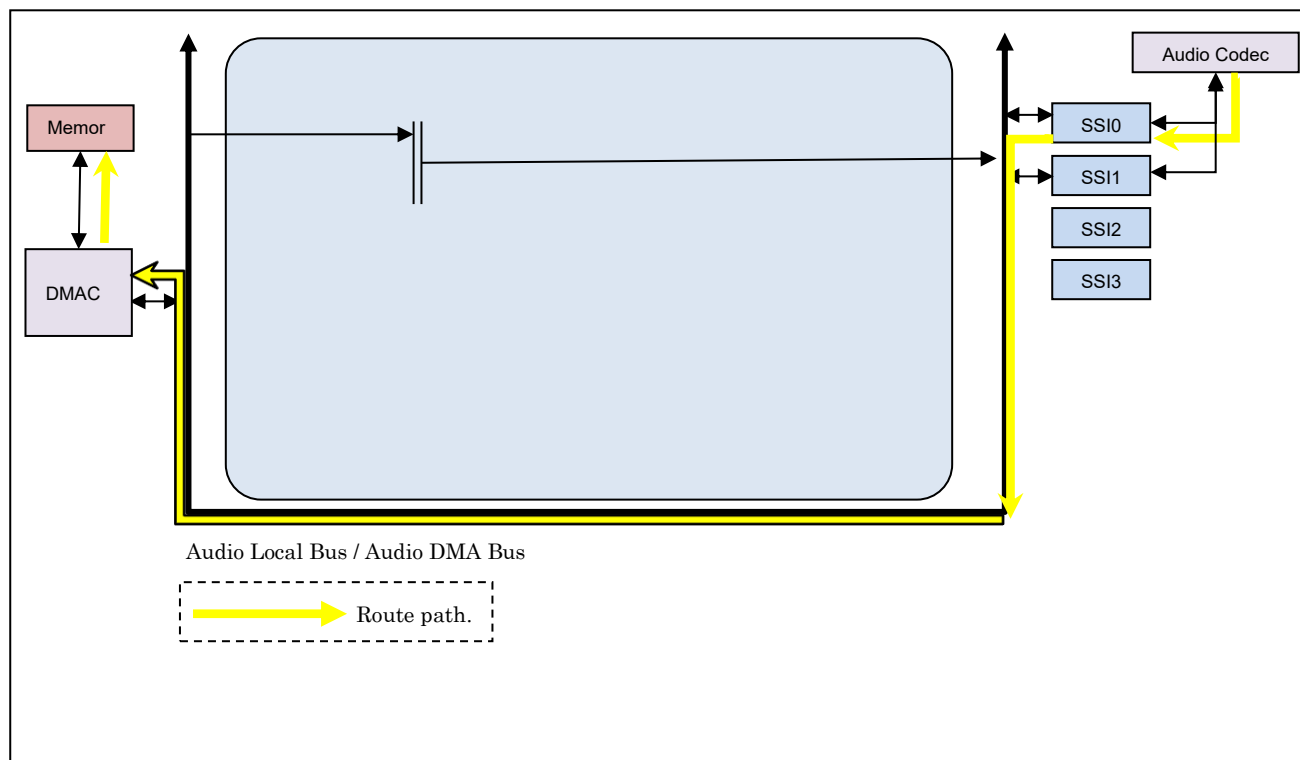


Figure 4-19 CODEC->SSI0->Memory data path

(2) Setting case of “Codec -> SPDIF -> Memory” supported on RZ/G3S

This feature supports RZ/G3S only. Transfer settings of audio are set to transfer data from the “SPDIF” to the memory with or without using DMA at the driver.

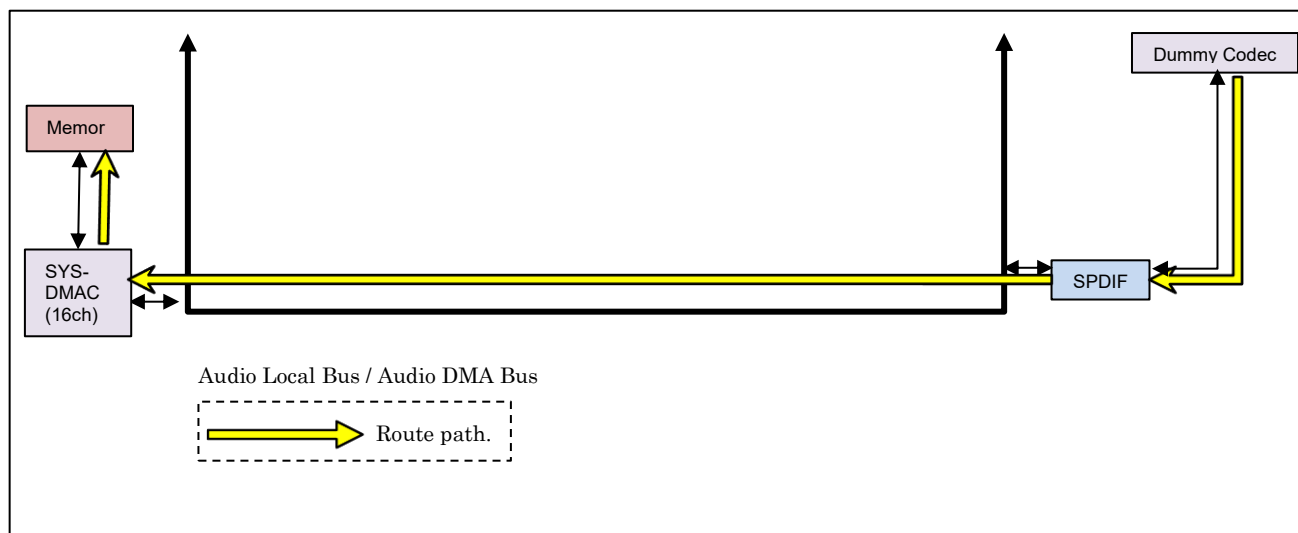


Figure 4-20 Codec->SPDIF->Memory data path on RZ/G3S

4.3.3.2 On RZ/V2N, RZ/V2H and RZ/G3E

(1) Setting case of “CODEC -> SSI4 -> Memory”

Route path shows the case of "CODEC-> SSI4-> Memory".

Transfer settings of audio DMAC is set to transfer from the “SSI4” to the memory at the driver. Audio DMAC-pp is no use in this case.

Please refer to “RZ/V2N Group User’s Manual: Hardware”, “RZ/V2H Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

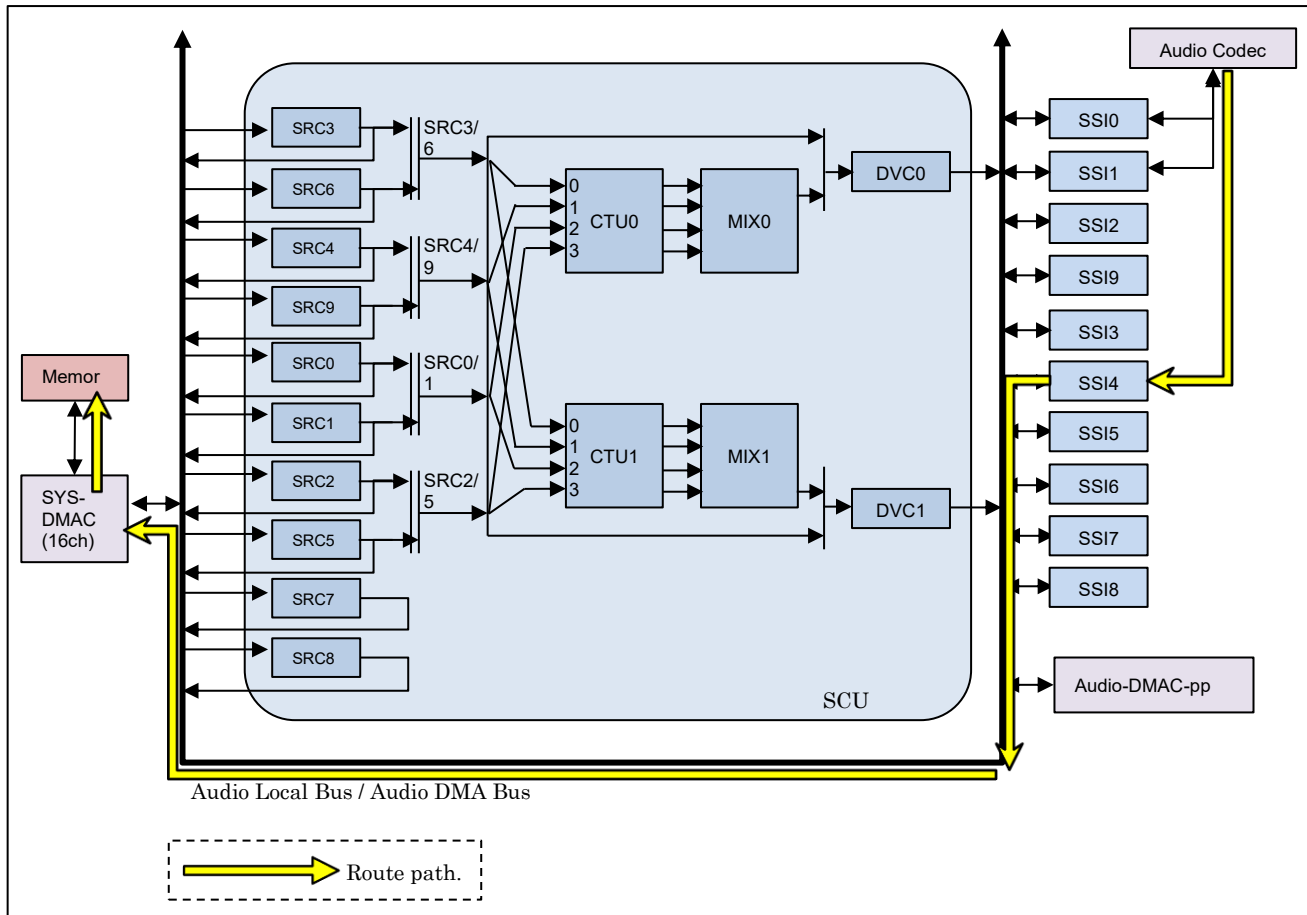


Figure 4-21 CODEC->SSI4 -> Memory data path

(2) Setting case of "CODEC -> SSI4 -> SRC0 -> Memory"

Route path shows the case of "CODEC -> SSI4 -> SRC0 -> Memory".

Transfer settings of audio DMAC is set to transfer from the "SCU_SRCI0" to the "memory" at the driver. In addition, the transfer setting of audio DMAC-pp is set to transfer from "SSI00" to the "SCU_SRCI0" at the driver.

Please refer to "RZ/V2N Group User's Manual: Hardware", "RZ/V2H Group User's Manual: Hardware" and "RZ/G3E Group User's Manual: Hardware" about SYS-DMAC/Audio-DMA-pp's source and destination definitions.

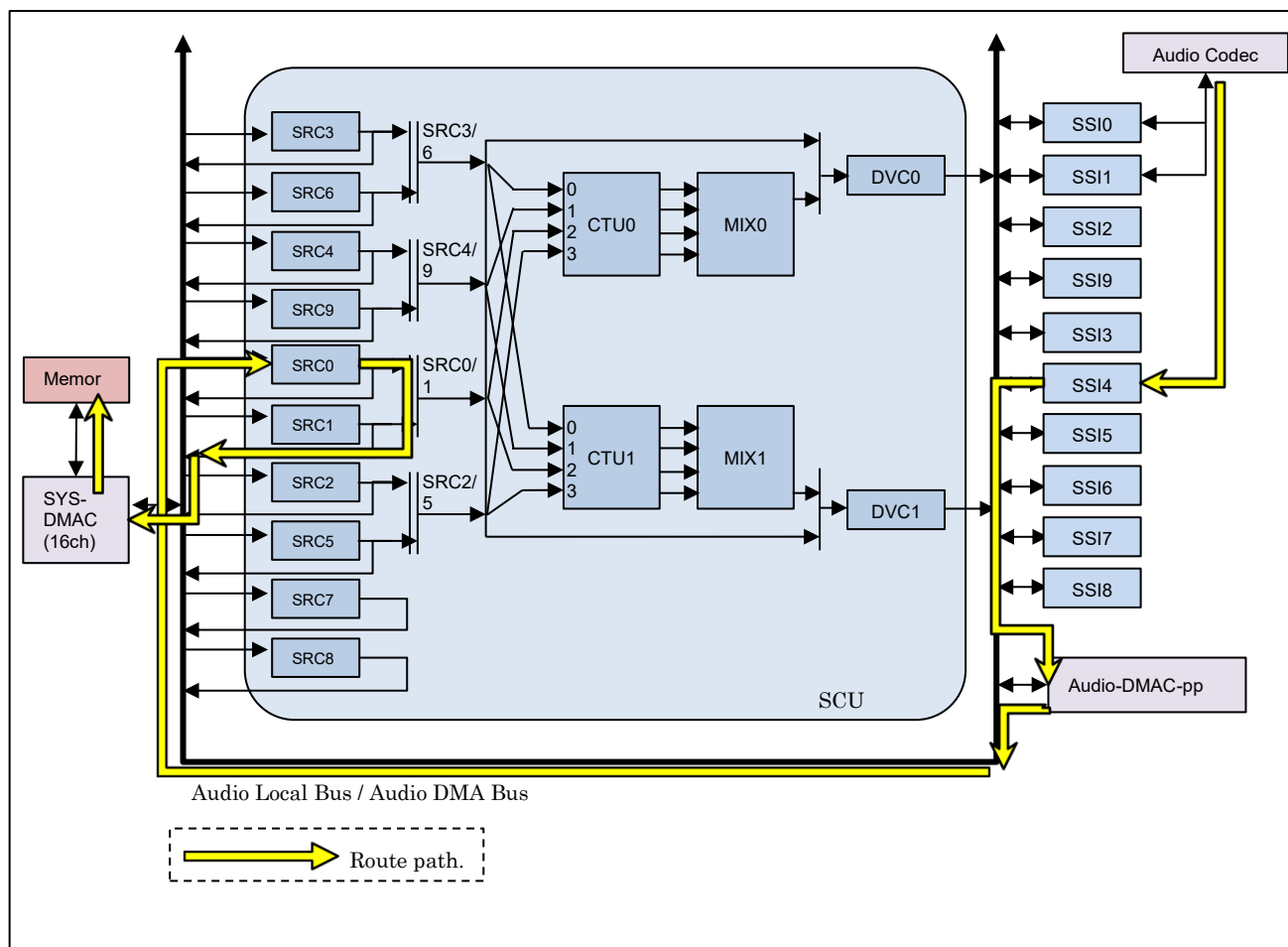


Figure 4-22 CODEC->SSI4->SRC0->Memory data path

(3) Setting case of “CODEC -> SSI4 -> SRC0 -> DVC0 -> Memory”

Route path shows the case of "CODEC -> SSI4 -> SRC0 -> DVC0 -> Memory".

Notes) When the DVC is enabled, the sampling rate conversions at the SRC input cannot be used by hardware constraints. Therefore, some features, such as "SRC In rate" of amixer control interface is disabled.

Transfer settings of audio DMAC is set to transfer from the “SCU_CMD0” to the Memory at the driver. In addition, the transfer setting of audio DMAC-pp is set to transfer from “SSIO0” to the “SCU_SRCI0” at the driver.

Please refer to “RZ/V2N Group User’s Manual: Hardware”, “RZ/V2H Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware” about SYS-DMAC/Audio-DMA-pp’s source and destination definitions.

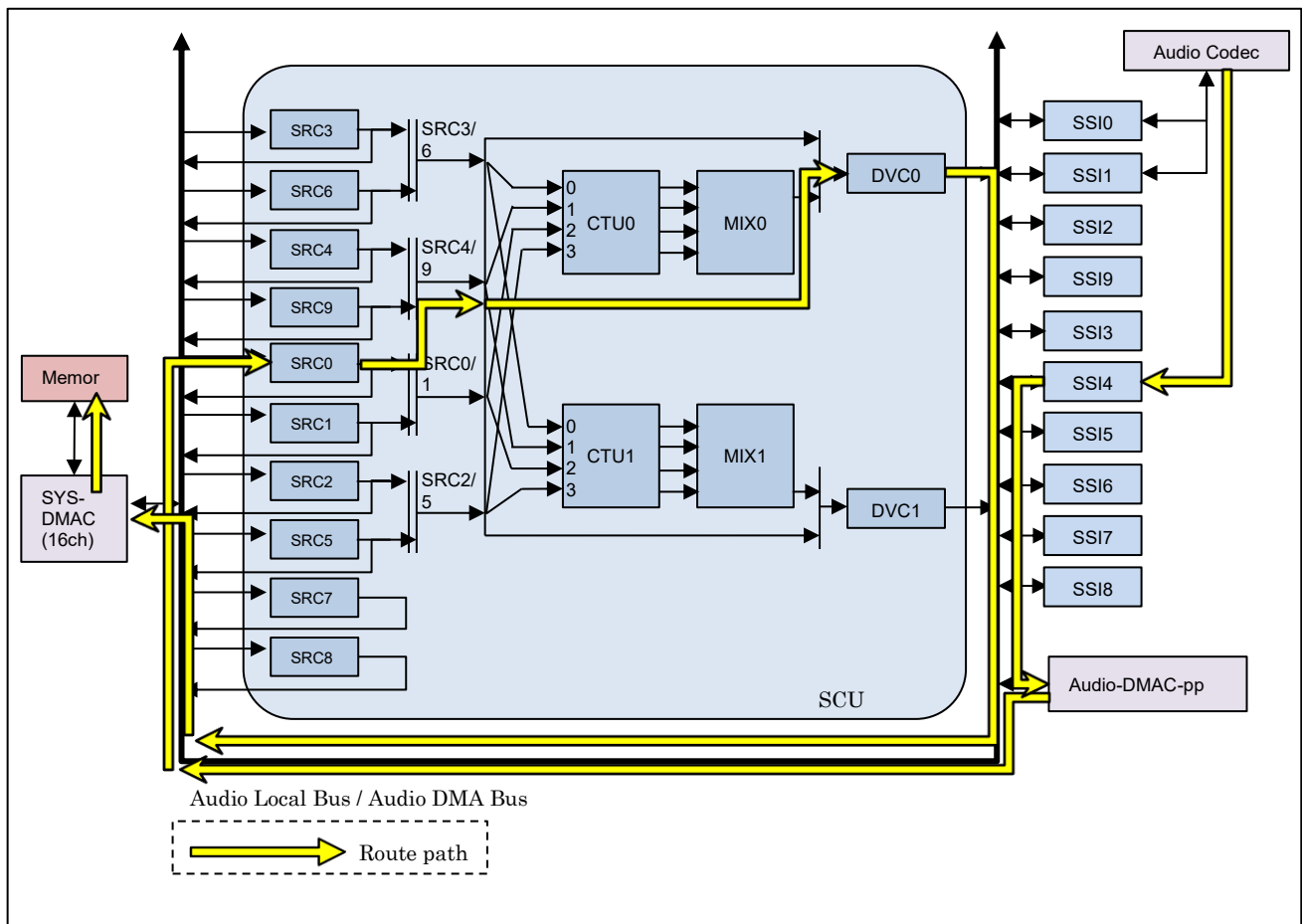


Figure 4-23 CODEC->SSI4->SRC0->DVC0->Memory data path

(4) Setting case of “CODEC -> SPDIF -> Memory”

Figure 4-23 demonstrates route path in case of "CODEC-> SPDIF-> Memory".

Transfer settings of audio are set to transfer data from the “SPDIF” to the memory with or without using DMA at the driver.

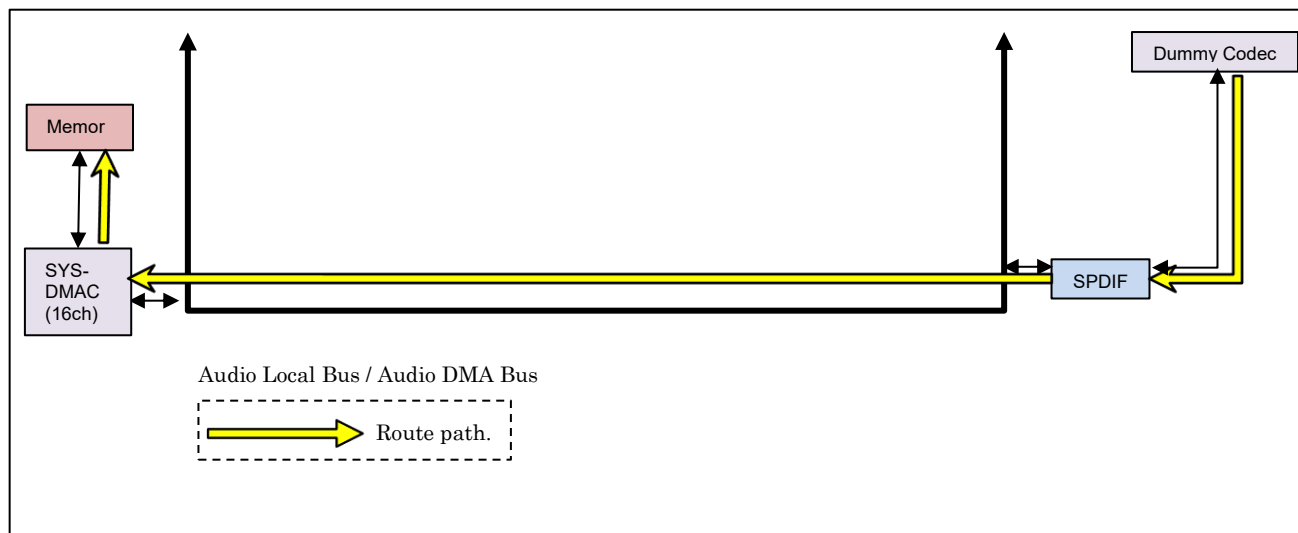


Figure 4-24 Codec->SPDIF->Memory data path

(5) Setting case of “CODEC -> PDM -> Memory”

This function is only available on RZ/G3E Group.

Route path shows the case of "CODEC-> PDM-> Memory".

Transfer settings of audio are set to transfer data from the “PDM” to the memory with or without using DMA at the driver.

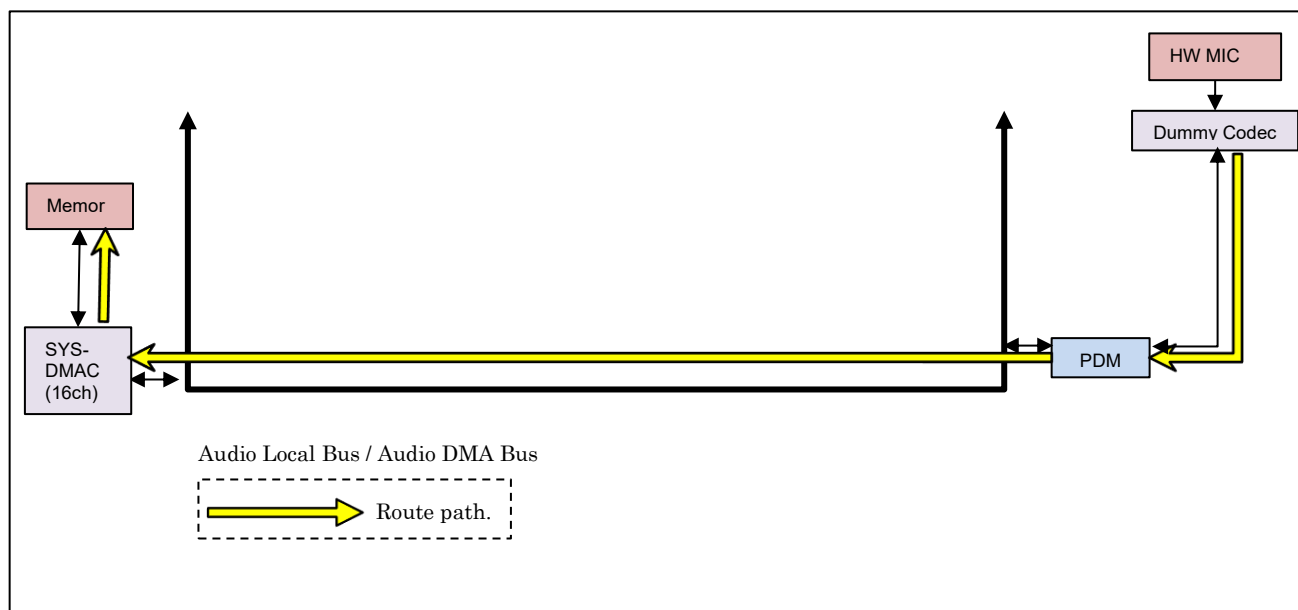


Figure 4-25 Codec->PDM->Memory data path

This route case's description example is shown below:

```
codec_test0: codec_test {
    compatible = "linux,snd-soc-dummy";
    #sound-dai-cells = <0>;
    port {
        dummy_codec: endpoint {
            remote-endpoint = <&pdm_endpoint>;
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rcar-sound";
    dais = <&rsnd_port0 /* DA7211 */
        &rsnd_port1 /* HDMI0 */
        &pdm_link>;
};

&pdm0 {
    pinctrl-0 = <&pdm0_pins>;
    pinctrl-names = "default";
    status = "okay";

    pdm_link: port {
        pdm_endpoint: endpoint {
            remote-endpoint = <&dummy_codec>;
        };
    };

    channel1 {
        status = "okay";
    };
};
```

Figure 4-26 Example of setting for Memory -> PDM -> CODEC

4.4 Sampling rate conversion

This function is only available on RZ/V2N, RZ/V2H and RZ/G3E Group.

This module supports the sampling rate conversion function using the SRC.

To use it, please enable `CONFIG_SND_SIMPLE_SCU_CARD` (if using ASoC Simple sound card) or `CONFIG_SND_AUDIO_GRAPH_SCU_CARD` (if using ASoC Audio Graph sound card) at kernel configuration (refer to section 5.2).

In addition, please set via 'device tree file', or the ALSA control interface. If both are set, the control interface is given priority.

4.4.1 Asynchronous Mode

To activate the sampling rate conversion, a description of the "simple-scu-audio-card" or "audio-graph-scu-card" needs to be provided in device tree file. The fixed sampling rate can be set by "*convert-rate*" property.

If "*simple-audio-card,convert-rate*" or "*audio-graph-card,convert-rate*" is not defined, the rate conversion doesn't work until the Mixer function enables it. It is possible to enable the rate conversion function with the following command. Rate conversions enabled by amixer will return with disabling upon completion of playback. Please enable again in necessary case.

```
# amixer cset name="SRC Out Rate Switch" on
```

Figure 4-27 Command example of enable the sampling rate conversion

And set the conversion rate example following command.

```
# <starting playback> &  
# amixer cset name="SRC Out Rate" 44100
```

Figure 4-28 Command example of set conversion rate

Figure 4-28 shows example of 44.1 kHz. This example shows that all input data will be converted to 44.1 kHz at playback. Input 44.1 kHz data will be converted to system specified Hz at capture.

(1) Device tree setting

```

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            convert-rate = <44100>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>;
            };
        };
    };
};

```

Figure 4-29 Description example of sampling rate setting

The clock format can be written in one of the following formats:

```
system-clock-frequency = <value>
```

Or

```
clocks = <&xxx>
```

Figure 4-30 Show example of using "clocks ="

```
sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
        &rsnd_port1 /* HDMI0 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>, <&src0>, <&dvc0>;
                capture = <&ssi4>, <&src1>, <&dvc1>;
            };
        };
    };
};
```

Figure 4-31 Description example of clock setting

4.4.2 Synchronous Mode

By using the ALSA control interface (amixer), we can convert the sampling rate by runtime. However, because audio codec IC (DA7212) maintains the sampling rate since the start, the sound will be fast/slow.

In the case of a route set up to use the DVC, SRC feature is disabled at the capture.

(1) Initial condition

Initial setting value is "0". In this case, the rate is converted to the same rate using the SRC. Settings can be confirmed by using the Mixer function. Its control names are "SRC Out Rate" and "SRC In Rate".

```
# amixer cget name='SRC Out Rate'
numid=67,iface=MIXER,name='SRC Out Rate'
; type=INTEGER,access=rw-----,values=1,min=0,max=192000,step=0
: values=0

# amixer cget name='SRC In Rate'
numid=69,iface=MIXER,name='SRC In Rate'
; type=INTEGER,access=rw-----,values=1,min=0,max=192000,step=0
: values=0
```

Figure 4-32 Commands to check current sampling rate

(2) Sampling rate setting

Mixer function can set sampling rate conversion. Control name is "SRC Out Rate" and "SRC In Rate". This function works only when changing settings during playback or recording. Rate conversions enabled by amixer will return with disabling upon completion of playback. Please enable again in necessary case. Available range is from 0 to 48000. When "0" is set, sampling rate converts to same rate. Figure 4-33 shows example of conversion to 44.1kHz.

```
# amixer cget name='SRC Out Rate'
numid=67,iface=MIXER,name='SRC Out Rate'
; type=INTEGER,access=rw-----,values=1,min=0,max=192000,step=0
: values=44100

# amixer cget name='SRC In Rate'
numid=69,iface=MIXER,name='SRC In Rate'
; type=INTEGER,access=rw-----,values=1,min=0,max=192000,step=0
: values=44100
```

Figure 4-33 Commands to fixed sampling rate

4.5 Rate Continuous

This function is only available on RZ/V2N, RZ/V2H and RZ/G3E. By this setting, ALSA can support all sampling rate. However, initial setting of this driver only supports specific sampling rate (refer to Table 1-9), because this feature is disabled.

If you would like to enable this rate continuous function, please modify source code of `sound/soc/sh/rcar/core.c`. The setting of "rates", "rate_min" and "rate_max" in `snd_soc_dai_driver` structure is required. Figure 4-34 demonstrates the modification.

In case of RZ/V2N, RZ/V2H and RZ/G3E please also make similar changes to CODEC source code of `sound/soc/codecs/da7213.c`.

And more, description of device tree

```
sound/soc/codecs/da7213.c

static struct snd_soc_dai_driver da7213_dai = {
    name = "da7213-hifi",
    .playback = {
        .channels_min = 1,
        .channels_max = 2,
        - .rates = SNDRV_PCM_RATE_8000_96000,
        + .rates = SNDRV_PCM_RATE_CONTINUOUS,
        + .rate_min = 8000,
        + .rate_max = 192000,
    },
};
```

sound/soc/sh/rcar/core.c

```

#include <linux/pm_runtime.h>
+//#include <sound/pcm.h>
#include "rsnd.h"

-#define RSND_RATES SNDRV_PCM_RATE_8000_192000
+##define RSND_RATES SNDRV_PCM_RATE_CONTINUOUS
#define RSND_FMTS (SNDRV_PCM_FMTBIT_S24_LE | SNDRV_PCM_FMTBIT_S16_LE)
====
static void __rsnd_dai_probe(struct rsnd_priv *priv, struct device_node *dai_np, int dai_i, int is_graph)
{
    snprintf(rdai->playback.name, RSND_DAI_NAME_SIZE, "DAI%d Playback", dai_i);
    drv->playback.rates = RSND_RATES;
+   drv->playback.rate_min = 32000;
+   drv->playback.rate_max = 48000;
    drv->playback.formats = RSND_FMTS;
    drv->playback.channels_min = 2;
    drv->playback.channels_max = 8;
    drv->playback.stream_name = rdai->playback.name;

    snprintf(rdai->capture.name, RSND_DAI_NAME_SIZE, "DAI%d Capture", dai_i);
    drv->capture.rates = RSND_RATES;
+   drv->capture.rate_min = 32000;
+   drv->capture.rate_max = 48000;
    drv->capture.formats = RSND_FMTS;
    drv->capture.channels_min = 2;
    drv->capture.channels_max = 8;
    drv->capture.stream_name = rdai->capture.name;

```

Figure 4-34 Setting of Rate Continuous

4.6 CTU Function

This function is only available on RZ/V2N, RZ/V2H and RZ/G3E group. Details at “RZ/V2N Group User’s Manual: Hardware”, “RZ/V2H Group User’s Manual: Hardware” and “RZ/G3E Group User’s Manual: Hardware”.

Those sections are:

- Sampling Rate Converter Unit (SCU)
 - Register Description
 - CTUn Scale Value e00 ~ e37 register
 - Operation
 - CMD Block
 - Functional Blocks in CMD

4.6.1 CTU module setting

(1) Device tree file setting

This is an example of all input data will be converted to 2ch as output data.

```
snd_rzv2n: sound {  
    ...  
  
    convert-channels = <2>;  
    ...  
};
```

Figure 4-35: Description example of CTU setting

(2) Example of using

The example of using CTU.

ex1) using matrix

output 0ch = (input 0ch x 0) + (input 1ch x 1)
output 1ch = (input 0ch x 1) + (input 1ch x 0)

\$ amixer set “CTU Reset” on
\$ amixer set “CTU Pass” 9,10
\$ amixer set “CTU SV0” 0,4194304
\$ amixer set “CTU SV1” 4194304,0

ex2) changing connection

\$ amixer set “CTU Reset” on
\$ amixer set “CTU Pass” 2,1

4.7 MIX Function

This function is only available on RZ/V2N, RZ/V2H and RZ/G3E Group. It supports the merges sounds path. Up to four sound interfaces can be set on one card device on the system, and these sounds are merged by MIX.

4.7.1 MIX module setting

(1) Device tree file setting

```
&i2c2 {
    da7212: codec@1a {
        port {
            da7212_endpoint: endpoint {
                remote-endpoint = <&rsnd_endpoint0>;
            };
        };
    };
};

sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&src1 &ctu02 &mix0 &dvc0 &ssi3>;
            };
        };
    };
};
```

Figure 4-36 Description example of MIX setting on RZ/V2N

(2) Example of using

The example of using MIX.

```
$ aplay -D plughw:0,0 xxxx.wav &  
$ aplay -D plughw:0,1 yyyy.wav
```

4.8 Amixer control interfaces

On RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L and RZ/Five, amixer controls including volume control, Aux Boost, etc. are provided by WM8978 audio codec driver. Please refer to WM8978 manuals for more details.

On RZ/V2N and RZ/G3E this module can adjust the volume and so on by Mixer function.

4.8.1 Control list

4.8.1.1 On RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L and RZ/Five

A list of available mixer controls in the system can be obtained by executing below ALSA commands:

```
$ amixer controls  
$ amixer scontrols
```

4.8.1.2 On RZ/V2N, RZ/V2H and RZ/G3E

The content of the supported control is shown below.

Table 4-4 External function (Standard) [1/2]

Control Name	Overview	Parameter [*] : initial value)		Remark
DVC In	Capture control DVC	(Left, Right) = (0, 0) [*]	0 - 8388607 (0 - 100 %)	
DVC In Mute	Capture mute	(Left, Right) = (0, 0) [*]	off, off	
		(Left, Right) = (0, 1)	off, on	
		(Left, Right) = (1, 0)	on, off	
		(Left, Right) = (1, 1)	on, on	
DVC In Ramp	Capture volume control	0 [*]	off	
		1	on	
DVC In Ramp Down Rate	Capture volume control	'128 dB/1 step' [*] (Other parameters refer to Table 4-9)	Item #0	
			Item #1 - #23	
DVC In Ramp Up Rate	Capture volume control	'128 dB/1 step' [*] (Other parameters refer to Table 4-9)	Item #0	
			Item #1 - #23	
DVC Out	Playback control DVC	(Left, Right) = (0, 0) [*]	0 - 8388607 (0 - 100 %)	
DVC Out Mute	Playback mute	(Left, Right) = (0, 0) [*]	off, off	
		(Left, Right) = (0, 1)	off, on	
		(Left, Right) = (1, 0)	on, off	
		(Left, Right) = (1, 1)	on, on	
DVC Out Ramp	Playback volume control	0 [*]	off	
		1	on	
DVC Out Ramp Down Rate	Playback volume control	128 dB/1 step [*] (Other parameters refer to Table 4-9)	Item #0	
			Item #1 - #23	
DVC Out Ramp Up Rate	Playback volume control	128 dB/1 step [*] (Other parameters refer to Table 4-9)	Item #0	
			Item #1 - #23	
Digital Playback Volume1	Playback volume control	255 [*]	0 - 255	
Digital Playback Volume2	Playback volume control	255 [*]	0 - 255	*1
Digital Playback Volume3	Playback volume control	255 [*]	0 - 255	*1
Digital Playback Volume4	Playback volume control	255 [*]	0 - 255	*1
Digital Playback Volume5	Playback volume control	255 [*]	0 - 255	*1
Digital Playback Volume6	Playback volume control	255 [*]	0 - 255	*1

Table 4-5 External function (Standard) [2/2]

Control Name	Overview	Parameter (["] : initial value)		Remark
SRC In Rate	Input Rate of Sampling Rate Conversion	0 ["]	0 - 192000	*1
SRC Out Rate	Output Rate of Sampling Rate Conversion	0 ["]	0 - 192000	*1

*1: If more than one SRC device is valid, specify each with index=0 to 4. ex) 'SRC Out Rate',index=2

Table 4-6 External function (CTU)

Control Name	Overview	Parameter (["] : initial value)		Remark
'CTU Pass'	Pass mode setting	0	0 - 12	*1
'CTU Reset'	reset the settings	off	off/on	*1
'CTU SV0'	Scale value 0 setting	0	0 - 16777215	*1
'CTU SV1'	Scale value 1 setting	0	0 - 16777215	*1
'CTU SV2'	Scale value 2 setting	0	0 - 16777215	*1
'CTU SV3'	Scale value 3 setting	0	0 - 16777215	*1

*1: If more than one CTU device is valid, specify each with index=0 to 4. ex) 'CTU Pass',index=2

Table 4-7 External function (MIX)

Control Name	Overview	Parameter (["] : initial value)		Remark
'MIX Playback Volume'	Playback Volume Control	1023	0 - 1023	*1
'MIX Ramp Down Rate'	Ramp down rate control	128 dB/1 step ["] (Other parameters refer to Error! Reference source not found.)	Item #0 Item #1 - #10	- -
'MIX Ramp Switch'	Enable and disable control.	off	off/on	-
'MIX Ramp Up Rate'	Ramp up rate control.	128 dB/1 step ["] (Other parameters refer to Error! Reference source not found.)	Item #0 Item #1 - #10	- -

*1: If more than one MIX device is valid, specify each with index=0 to 4. ex) 'MIX Playback Volume',index=2

4.8.2 DVC function

This module is only available on RZ/V2N, RZ/V2H and RZ/G3E. This function can adjust the volume by Mixer function (amixer command), it can be controlling names 'DVC Out', 'DVC In', 'DVC Out Playback Volume', 'DVC In Capture Volume'. The argument can be a percentage value or a positive integer value. See Table 4-8 for the relationship between value and decibel.

Table 4-8 DVC volume control value

DVC percentage	dB	DVC (positive integer)	ratio	DVC percentage	dB	DVC (positive integer)	ratio
0%	-infinity	0	0.00	51%	12.21	4278190	4.08
1%	-21.94	83887	0.08	52%	12.38	4362076	4.16
2%	-15.92	167773	0.16	53%	12.55	4445962	4.24
3%	-12.40	251659	0.24	54%	12.71	4529848	4.32
4%	-9.90	335545	0.32	55%	12.87	4613734	4.40
5%	-7.96	419431	0.40	56%	13.03	4697620	4.48
6%	-6.38	503317	0.48	57%	13.18	4781506	4.56
7%	-5.04	587203	0.56	58%	13.33	4865393	4.64
8%	-3.88	671089	0.64	59%	13.48	4949279	4.72
9%	-2.85	754975	0.72	60%	13.62	5033165	4.80
10%	-1.94	838861	0.80	61%	13.77	5117051	4.88
11%	-1.11	922747	0.88	62%	13.91	5200937	4.96
12%	-0.35	1006633	0.96	63%	14.05	5284823	5.04
13%	0.34	1090519	1.04	64%	14.19	5368709	5.12
14%	0.98	1174405	1.12	65%	14.32	5452595	5.20
15%	1.58	1258292	1.20	66%	14.45	5536481	5.28
16%	2.14	1342178	1.28	67%	14.58	5620367	5.36
17%	2.67	1426064	1.36	68%	14.71	5704253	5.44
18%	3.17	1509950	1.44	69%	14.84	5788139	5.52
19%	3.64	1593836	1.52	70%	14.96	5872025	5.60
20%	4.08	1677722	1.60	71%	15.09	5955911	5.68
21%	4.51	1761608	1.68	72%	15.21	6039798	5.76
22%	4.91	1845494	1.76	73%	15.33	6123684	5.84
23%	5.30	1929380	1.84	74%	15.45	6207570	5.92
24%	5.67	2013266	1.92	75%	15.56	6291456	6.00
25%	6.02	2097152	2.00	76%	15.68	6375342	6.08
26%	6.36	2181038	2.08	77%	15.79	6459228	6.16
27%	6.69	2264924	2.16	78%	15.90	6543114	6.24
28%	7.00	2348810	2.24	79%	16.01	6627000	6.32
29%	7.31	2432697	2.32	80%	16.12	6710886	6.40
30%	7.60	2516583	2.40	81%	16.23	6794772	6.48
31%	7.89	2600469	2.48	82%	16.34	6878658	6.56
32%	8.16	2684355	2.56	83%	16.44	6962544	6.64
33%	8.43	2768241	2.64	84%	16.55	7046430	6.72
34%	8.69	2852127	2.72	85%	16.65	7130316	6.80
35%	8.94	2936013	2.80	86%	16.75	7214203	6.88
36%	9.19	3019899	2.88	87%	16.85	7298089	6.96
37%	9.43	3103785	2.96	88%	16.95	7381975	7.04
38%	9.66	3187671	3.04	89%	17.05	7465861	7.12
39%	9.88	3271557	3.12	90%	17.15	7549747	7.20
40%	10.10	3355443	3.20	91%	17.24	7633633	7.28
41%	10.32	3439329	3.28	92%	17.34	7717519	7.36
42%	10.53	3523215	3.36	93%	17.43	7801405	7.44
43%	10.73	3607102	3.44	94%	17.52	7885291	7.52
44%	10.93	3690988	3.52	95%	17.62	7969177	7.60
45%	11.13	3774874	3.60	96%	17.71	8053063	7.68
46%	11.32	3858760	3.68	97%	17.80	8136949	7.76
47%	11.50	3942646	3.76	98%	17.89	8220835	7.84
48%	11.69	4026532	3.84	99%	17.97	8304721	7.92
49%	11.87	4110418	3.92	100%	18.06	8388607	8.00
50%	12.04	4194304	4.00	-	-	-	-

4.8.3 Ramp function

This module is only available on RZ/V2N, RZ/V2H and RZ/G3E. It supports the Ramp function of MIX and DVC. This function can be used when you define to use MIX module or DVC module for audio route setting. Control of the ramp function is controlled using the amixer control interface.

Table 4-9 Ramp parameters for DVC

Item number	Ramp parameters
0	'128 dB/1 step'
1	'64 dB/1 step'
2	'32 dB/1 step'
3	'16 dB/1 step'
4	'8 dB/1 step'
5	'4 dB/1 step'
6	'2 dB/1 step'
7	'1 dB/1 step'
8	'0.5 dB/1 step'
9	'0.25 dB/1 step'
10	'0.125 dB/1 step'
11	'0.125 dB/2 steps'
12	'0.125 dB/4 steps'
13	'0.125 dB/8 steps'
14	'0.125 dB/16 steps'
15	'0.125 dB/32 steps'
16	'0.125 dB/64 steps'
17	'0.125 dB/128 steps'
18	'0.125 dB/256 steps'
19	'0.125 dB/512 steps'
20	'0.125 dB/1024 steps'
21	'0.125 dB/2048 steps'
22	'0.125 dB/4096 steps'
23	'0.125 dB/8192 steps'

Table 4-10 Ramp parameters for MIX

Item number	Ramp parameters
0	'128 dB/1 step'
1	'64 dB/1 step'
2	'32 dB/1 step'
3	'16 dB/1 step'
4	'8 dB/1 step'
5	'4 dB/1 step'
6	'2 dB/1 step'
7	'1 dB/1 step'
8	'0.5 dB/1 step'
9	'0.25 dB/1 step'
10	'0.125 dB/1 step'

4.8.4 Example of Control setting

4.8.4.1 On RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L and RZ/Five

Example of Control setting is shown as below. Please change the volume to suitable value for the sound source level.

Ex.1) Playback in Memory->SSI->CODEC route

```
$ amixer cset name='Left Input Mixer L2 Switch' on
$ amixer cset name='Right Input Mixer R2 Switch' on
$ amixer cset name='Headphone Playback Volume' 100
$ amixer cset name='PCM Volume' 100%
$ amixer cset name='Input PGA Volume' 25
$ aplay -D hw:0,0 <wavefile>
```

Ex.2) Capture in Memory<- SSI<-CODEC route

```
$ arecord -D plughw:0,0 -t wav -d 5 -c 2 -r 44100 -f S16_LE <wavefile>
```

4.8.4.2 On RZ/G3S

Example of Control settings is shown below"

Ex. 1) Playback in Memory->SSI3->CODEC

```
$ amixer -q cset name='Aux Switch' on
$ amixer -q cset name='Mixin Left Aux Left Switch' on
$ amixer -q cset name='Mixin Right Aux Right Switch' on
$ amixer -q cset name='ADC Switch' on
$ amixer -q cset name='Mixout Right Mixin Right Switch' off
$ amixer -q cset name='Mixout Left Mixin Left Switch' off
$ amixer -q cset name='Headphone Volume' 100%
$ mixer -q cset name='Headphone Switch' on
$ amixer -q cset name='Mixout Left DAC Left Switch' on
$ amixer -q cset name='Mixout Right DAC Right Switch' on
$ amixer -q cset name='DAC Left Source MUX' 'DAI Input Left'
$ amixer -q cset name='DAC Right Source MUX' 'DAI Input Right'
$ amixer -q sset 'Mic 1 Amp Source MUX' 'MIC_P'
$ amixer -q sset 'Mic 2 Amp Source MUX' 'MIC_P'
$ amixer -q sset 'Mixin Left Mic 1' on
$ amixer -q sset 'Mixin Right Mic 2' on
$ amixer -q sset 'Mic 1' 100% on
$ amixer -q sset 'Mic 2' 100% on
$ amixer -q sset 'Lineout' 100% on
$ amixer -q set "Headphone" 100% on
$ aplay -D hw:0,0 <wavefile>
```

Ex.2) Capture in Memory<-SSI3<-CODEC

```
$ arecord -D hw:0,0 <wavefile>
```

4.8.4.3 On RZ/V2N, RZ/V2H and RZ/G3E

The example of Control setting in RZ/V2N evaluation boards, RZ/V2H evaluation board and RZ/G3E SMARC is shown below. Please change the volume to suitable value for the sound source level.

In this example, <wavfile> is for 24-bit data. When using 16-bit data, please do not use "hw" option, please use "plughw" option.

Ex.1) Playback in Memory->SCU(DVC)->SSI->CODEC route

```
$ amixer set "Digital Playback Volume1" 80%
$ amixer set "DVC Out" 12%
$ aplay -D hw:0,0 <wavfile>
Note) "-D" option can use over 32kHz.
```

Ex.2) Playback in Memory->SSI->CODEC route

```
$ amixer set "Digital Playback Volume1" 80%
$ amixer set "DVC Out" 12%
$ aplay -D hw:0,0 <wavfile>
```

Ex.3) Capture in Memory<-SCU(DVC)<-SSI<-CODEC route

```
$ amixer set "DVC In" 12%
$ arecord -D hw:0,0 -t wav -d 5 -c 2 -r 44100 -f S24_LE <wavfile>
```

Ex.4) Slow down the playback of 48000Hz

```
$ amixer cset name='DVC Out' 12%
$ aplay <48KHz-wavfile> &
$ amixer cset name='SRC Out Rate' 52800
The amount of data increases, so it becomes slower playback.
```

Ex.5) Ramp control case of playback

```
$ amixer set "DVC Out" 0%
$ amixer set "Digital Playback Volume1" 100%
$ amixer set "DVC Out Ramp Up Rate" "0.125 dB/64 steps"
$ amixer set "DVC Out Ramp Down Rate" "0.125 dB/512 steps"
$ amixer set "DVC Out Ramp" on
$ aplay <wavfile> &
$ amixer set "DVC Out" 75%
$ sleep 10
$ amixer set "DVC Out" 0%
```

4.9 Multi-channel Function

This feature is only available on RZ/V2N, RZ/V2H and RZ/G3E Group. It supports Multi-channel by Multi-SSI, or TDM-SSI.

Multi-SSI Function

This function supports 6ch case. The SSI of stereo x3 is available.

Device tree file setting

This example of SSI0/SSI1/SSI2 (= for 6ch).

```
&rcar_sound {  
    ...  
    rcar_sound,dai {  
        dai0 {  
            playback = <&ssi0 &ssi1 &ssi2 &src0 &dvc0>;  
        };  
    };  
};
```

Figure 4-37 Description example of Multi-channel setting

4.10 SPDIF interface

This function is only available on RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E Group. For default, SPDIF on RZ/G3S and RZ/G3E are not enabled.

4.10.1 Control list

A list of available controls in the system can be obtained by executing below ALSA commands:

```
$ aplay
$ arecord
```

A list of available options for controls in the system shows as below:

Table 4-11 Control option

Features	Support
Sampling frequencies	32kHz, 44.1kHz and 48kHz
Audio word size	16 bits and 24 bits
Number of channels	2 channels (stereo)

4.10.2 Example of Control setting

Example of Control setting is shown as below for capture mode and playback mode

Playback: \$ aplay -D hw:0,1 -f <word_size> -r <sampling_freq> -c 2 -t raw <wavefile>

Capture: \$ arecord -D plughw:0,1 -d <time> -c 2 -r <sampling_rate> -f <word_size> <wavefile>

Ex.1) Playback in Memory->SPDIF->Dummy CODEC route: playback file <wave> at 16 bits and sampling frequency 44.1kHz.

```
$ aplay -D hw:0,1 -f S16_LE -r 44100 -c 2 -t raw <wavefile>
```

Ex.2) Capture in Memory<- SPDIF<-Dummy CODEC route: record into file <wave> with at 16 bits and sampling frequency 44.1kHz.

```
$ arecord -D plughw:0,1 -d 5 -c 2 -r 44100 -f S16_LE <targetfile>
```

4.11 PDM

This function is only available on RZ/G3E Group.

4.11.1 Control list

A list of available controls in the system can be obtained by executing below ALSA commands:

```
$ arecord
```

A list of available options for controls in the system shows as below:

Table 4-12 Control option

Features	Support
Sampling frequencies	8kHz, 10kHz, 12kHz, 15kHz, 16kHz, 20kHz, 24kHz, 25kHz, 30kHz, 40kHz and 48kHz
Audio word size	16 bits and 20 bits
Number of channels	1 channel (mono)

4.11.2 Example of Control setting

Example of Control setting is shown as below for capture mode

Capture: `$ arecord -D plughw:0,2 -d <time> -c 1 -r <sampling_rate> -f <word_size> <wavefile>`

Ex) Capture in Memory<- PDM<-Dummy CODEC route: record into file <wave> with at 16 bits and sampling frequency 48kHz.

```
$ arecord -D plughw:0,2 -d 5 -c 1 -r 48000 -f S16_LE <targetfile>
```


4.12 Function Specification

4.12.1 ALSA API

The ALSA API support situation of this module is shown below.

Table 4-13 ALSA API support

API (the C library reference Modules)	Support	Remark
Input Interface	yes	-
Output Interface	yes	-
Error handling	yes	-
Configuration Interface	yes	-
Control Interface	yes	-
PCM Interface: Stream Information	yes	-
PCM Interface: Hardware Parameters	yes	-
PCM Interface: Software Parameters	yes	-
PCM Interface: Access Mask Functions	yes	-
PCM Interface: Format Mask Functions	yes	-
PCM Interface: Status Functions	yes	-
PCM Interface: Description Functions	yes	-
PCM Interface: Debug Functions	yes	-
PCM Interface: Helper Functions	yes	-
PCM Interface: Deprecated Functions	yes	-
Timer Interface	yes	-
Hardware Dependent Interface	-	-
Global defines and functions	-	-
PCM Interface: Sub format Mask Functions	-	-
PCM Interface: Hook Extension	-	-
PCM Interface: Scope Plugin Extension	-	-
PCM Interface: Simple setup functions	-	-
Instrument Interface	-	-
PCM Interface: Direct Access (MMAP) Functions	-	-
Raw Midi Interface	-	-
MIDI Sequencer	-	-
External PCM plugin SDK	-	-
External Control Plugin SDK	-	-

5.Integration

5.1 Source code Directory Structure

Figure 5-1 describes the directory structure of Audio drivers source code in RZ/G2L, RZ/G3S and RZ/V2L platform.

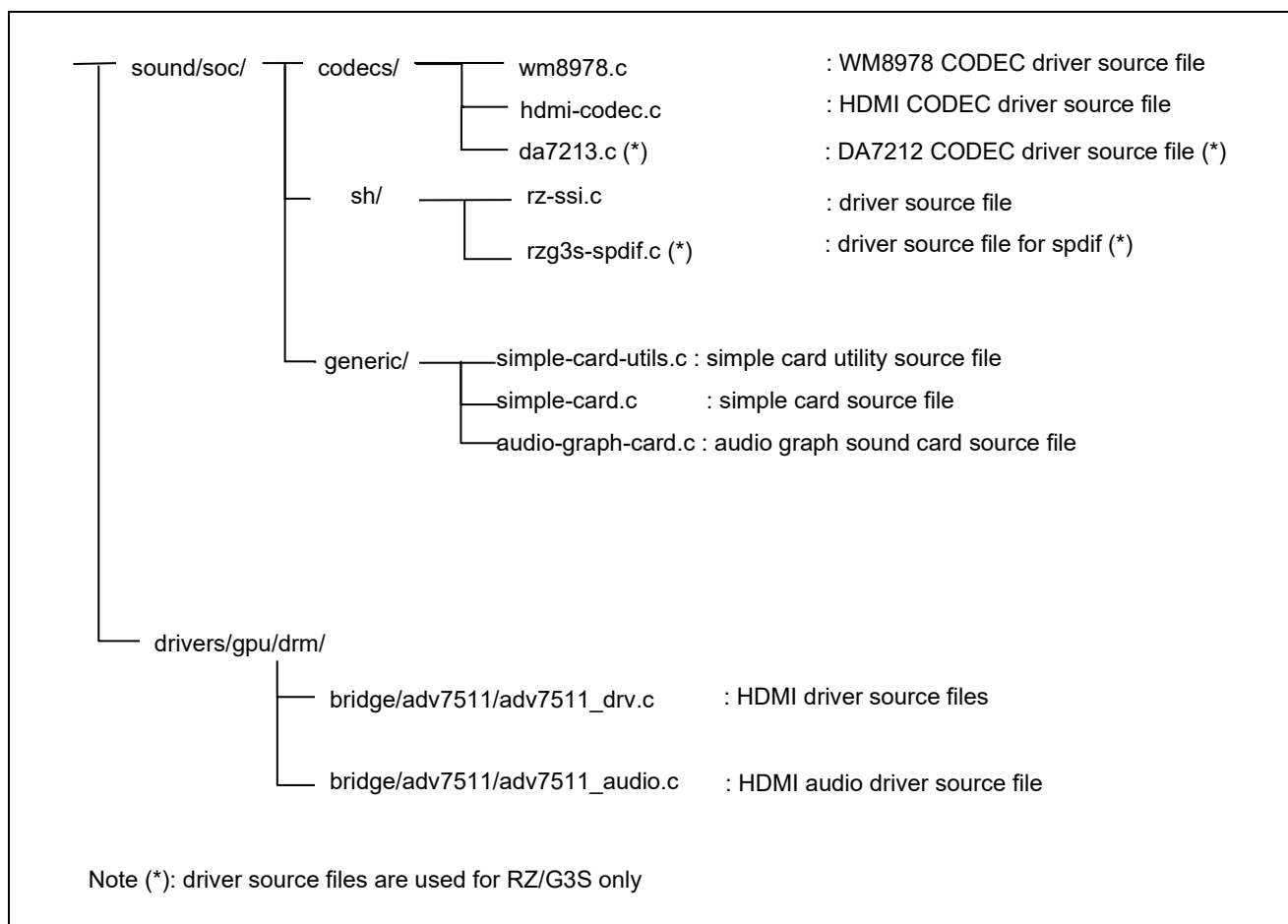


Figure 5-1 Directory configuration (RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five)

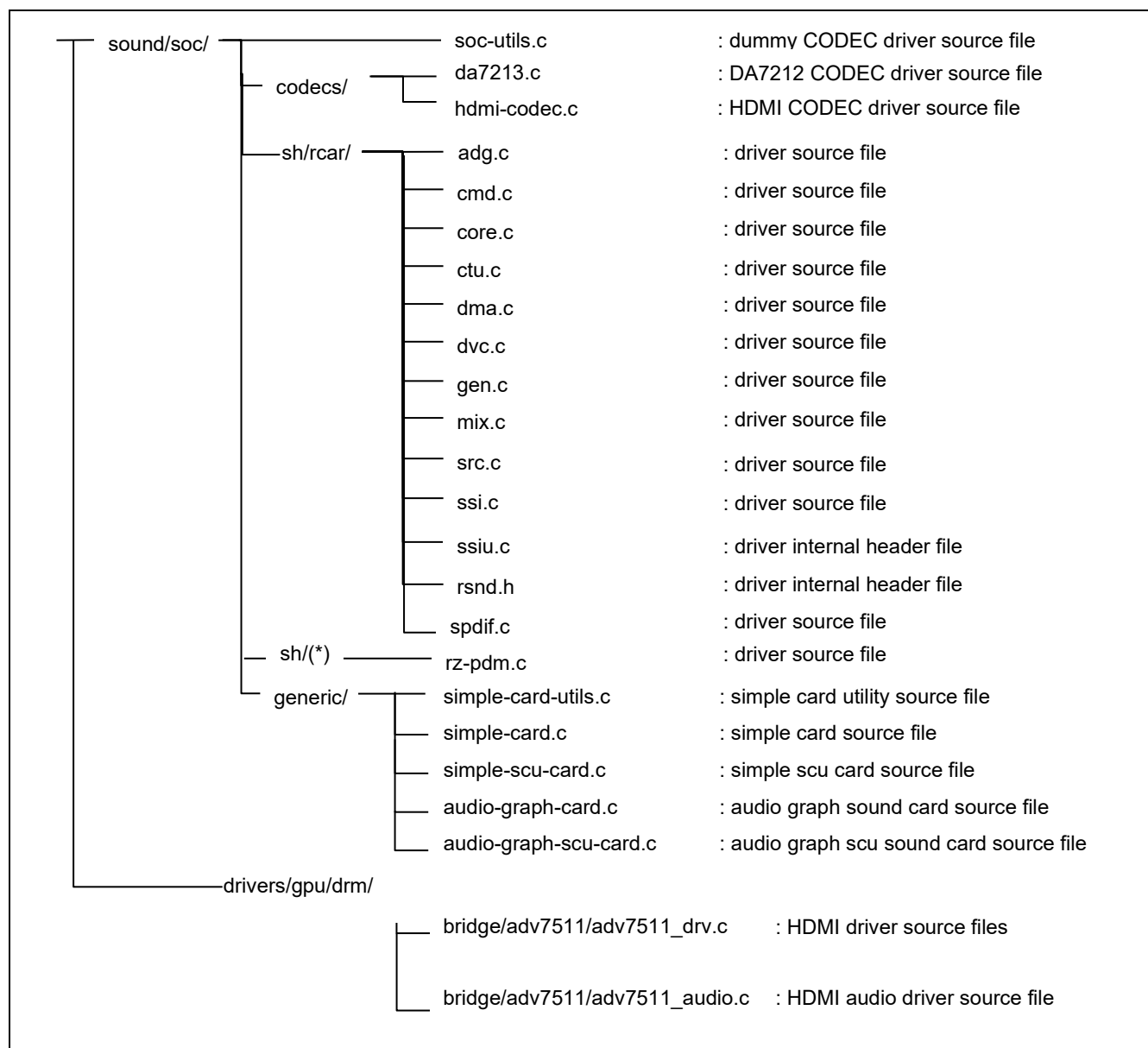


Figure 5-2 Directory configuration (RZ/V2N, RZ/V2H and RZ/G3E)

(*) Only support on RZ/G3E

5.2 Kernel configuration

5.2.1 On RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five

To enable the function of this module, make the following setting in Kernel menuconfig.

```
Device Drivers --->
  <*> Sound card support --->
    <*> Advanced Linux Sound Architecture --->
      ALSA for SoC audio support --->
        SoC Audio support for Renesas SoCs --->
          <*> RZ/G2L series SSIF-2 support
          <*> ASoC Simple sound card support
            < > ASoC Simple SCU sound card support
          <*> ASoC Audio Graph sound card support
            < > ASoC Audio Graph SCU sound card support

        CODEC drivers --->
          <*> Wolfson Microelectronics WM8978 code
          <*> Dialog DA7213 CODEC (*)
```

Figure 5-3 Kernel menuconfig for audio drivers

Figure 5-4 lists the required kernel config symbols to support audio (including HDMI audio)

```
CONFIG_SOUND=y
CONFIG_SND=y
CONFIG_SND_PCM=y
CONFIG_SND_PCM_TIMER=y
CONFIG_SND_SUPPORT_OLD_API=y
CONFIG_SND_PROC_FS=y
CONFIG_SND_VERBOSE_PROCFS=y
CONFIG_SND_DRIVERS=y
CONFIG_SND_SOC=y
CONFIG_SND_SOC_GENERIC_DMAENGINE_PCM=y
CONFIG_SND_SOC_RZ=y
CONFIG_SND_SOC_RZG3S_SPDIF=y(*)
CONFIG_SND_SOC_I2C_AND_SPI=y
CONFIG_SND_SOC_WM8978=y
CONFIG_SND_SIMPLE_CARD_UTILS=y
CONFIG_SND_SIMPLE_CARD=y
CONFIG_SND_AUDIO_GRAPH_CARD=y

# required for HDMI Audio
CONFIG_DRM_I2C_ADV7511=y
CONFIG_DRM_I2C_ADV7511_AUDIO=y
CONFIG_SND_SOC_HDMI_CODEC=y
# required for DMA support
CONFIG_DMA_ENGINE=y
CONFIG_DMA_VIRTUAL_CHANNELS=y
CONFIG_DMA_OF=y
CONFIG_RZ_DMACE=y
```

Figure 5-4 Kernel config symbols for audio drivers.

Note: (*) is used for RZ/G3S only.

5.2.2 On RZ/V2N, RZ/V2H and RZ/G3E

To enable the function of this module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  <*>Device Drivers --->
    <*> Sound card support --->
      <*> Advanced Linux Sound Architecture --->
        <*> ALSA for SoC audio support --->
          <*> SoC Audio support for Renesas SoCs --->
            <*> SND_SOC_RZV2H
            <*> Renesas RZ PDM support (*)
```

Figure 5-5 Kernel configuration for audio devices

Following setting with Kernel Configuration use to enable DA7212 Codec.

```
Device Drivers --->
  <*> Sound card support --->
    <*> Advanced Linux Sound Architecture --->
      <*> ALSA for SoC audio support --->
        <*> CODEC drivers --->
          <*> SND_SOC_DA7213
```

Figure 5-6 Kernel configuration for DA7212

```
CONFIG_SOUND=y
CONFIG_SND=y
CONFIG_SND_PCM=y
CONFIG_SND_PCM_TIMER=y
CONFIG_SND_SUPPORT_OLD_API=y
CONFIG_SND_PROC_FS=y
CONFIG_SND_VERBOSE_PROCFS=y
CONFIG_SND_DRIVERS=y
CONFIG_SND_SOC=y
CONFIG_SND_SOC_GENERIC_DMAENGINE_PCM=y
CONFIG_SND_SOC_RCAR=y
CONFIG_SND_SOC_DA7213=y
CONFIG_SND_SOC_I2C_AND_SPI=y
CONFIG_SND_SOC_WM8978=y
CONFIG_SND_SIMPLE_CARD_UTILS=y
CONFIG_SND_SIMPLE_CARD=y
CONFIG_SND_AUDIO_GRAPH_CARD=y
#required for PDM
CONFIG_SND_SOC_RZ_PDM=y (*)

# required for HDMI Audio
CONFIG_DRM_I2C_ADV7511=y
CONFIG_DRM_I2C_ADV7511_AUDIO=y
CONFIG_SND_SOC_HDMI_CODEC=y
# required for DMA support
CONFIG_DMA_ENGINE=y
CONFIG_DMA_VIRTUAL_CHANNELS=y
CONFIG_DMA_OF=y
```

Figure 5-7 Kernel config symbols for audio drivers

(*) PDM only support on RZ/G3E

5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

5.3.2 Kernel Parameters

There are no kernel parameters.

5.3.3 Device tree bindings

Table 5-1 lists the necessary binding properties to support audio in the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/G3S and RZ/Five platforms.

Table 5-1 Device tree properties

properties	description
compatible	"renesas,rz-ssi"
reg	Should contain the register physical address and length
interrupts	Should contain SSI interrupt int, dma rx and dma tx
interrupt-names	Peripheral interrupt names. "int", "tx", and "rx" are required
clocks	Must define clocks for SSIF module clock, and master clock for audio
clock-names	Must define names of clocks. "ssi" and at least one master clock, whether "audio_clk1" or "audio_clk2" are required.
resets	Should define reset handler ID for SSIF module
dmass	DMA transmit/receive channel IDs (optional)
dmas-names	DMA transmit/receive channel names (optional)
ports	Should define the audio codec endpoint. Required when using audio-graph-card. See Linux device tree bindings document of audio-graph-card for details.

Figure 5-8 Demonstrates an example of device tree setting which can be found in Documentation/devicetree/bindings/sound/ renesas,rz-ssi.yaml and device tree files listed in **Table 4-3**.

Table 5-2 lists the necessary binding properties to support audio in the RZ/V2N, RZ/V2H and RZ/G3E platforms.

properties	description
compatible	"renesas,rcar_sound-r9a09g056"/ "renesas,rcar_sound-r9a09g047"
reg	Should contain the register physical address. Required registers are: SCU/ADG/SSIU/SSI/Audio-DMAC-pp/SPDIF
rcar_sound,ssi	Should contain SSI features. The number of SSI sub node should be same as HW. sub node properties: - interrupts : Should contain SSI interrupt - shared-pin : If shared clock pin - dmas : Should contain Audio DMAC entry - dma-names : SSI case "rx" (=playback), "tx" (=capture). SSIU case "rxu" (=playback), "txu" (=capture). - status : SSI case "disabled" don't control module.
rcar_sound,ssiu	Should contain SSIU feature. The number of SSI sub node should be same as HW. sub node properties: - dmas : Should contain Audio DMAC entry - dma-names : "rx" (=playback), "tx" (=capture). - status : SSI case "disabled" don't control module.
rcar_sound,src	Should contain SRC feature. The number of SRC sub node should be same as HW. sub node properties: - interrupts : - dmas : Should contain Audio DMAC entry - dma-names : SSI case "rx" (=playback), "tx" (=capture). SSIU case "rxu" (=playback), "txu" (=capture). - status : SSI case "disabled" don't control module.
rcar_sound,ctu	Should contain CTU feature The number of CTU sub node should be same as HW.
rcar_sound,mix	Should contain MIX feature The number of MIX sub node should be same as HW.
rcar_sound,dvc	Should contain DVC feature The number of DVC sub node should be same as HW. sub node properties: - dmas : Should contain Audio DMAC entry - dma-names : "tx" (=playback/capture)
rcar_sound,spdif	Should contain SPDIF feature. The number of SPDIF sub node should be same as HW. sub node properties: - interrupts : Should contain SPDIF interrupt - dmas : Should contain Audio DMAC entry - dma-names : SPDIF case "rx" (=playback), "tx" (=capture). - status : SPDIF case "disabled" don't control module.
rcar_sound,dai	DAI contents The number of DAI sub node should be same as HW. sub node properties: - playback : list of playback modules - capture : list of capture modules For audio output/input route path refer to "4.3 Setting route".
#sound-dai-cells	It must be 0 if your system is using single DAI. It must be 1 if your system is using multi DAI.

Table 5-3 Device Tree properties for PDM on RZ/G3E Platform

properties	description
compatible	"renesas,rz-pdm"
reg	Should contain the register physical address and length
interrupts	Should contain PDM interrupt int err0~2, dat0~2, sdet
interrupt-names	Peripheral interrupt names. "int_pdm_err0~2", "int_pdm_dat0~2", and "int_pdm_sdet" are required
clocks	Must define clocks for PDM module clock.
clock-names	Must define names of clocks. "pdm_pclk", "pdm_pclk_sfr", "pdm_cclk" are required.
resets	Should define reset handler ID for PDM module
dmass	DMA receive channel IDs (optional)
dma-names	DMA receive channel names (optional)


```

In arch/arm64/boot/dts/renesas/r9a07g044.dtsi (RZ/G2L):
soc: soc {
    ssi0: ssi@10049c00 {
        compatible = "renesas,r9a07g044-ssi",
            "renesas,rz-ssi";
        reg = <0 0x10049c00 0 0x400>;
        interrupts = <GIC_SPI 326 IRQ_TYPE_LEVEL_HIGH>,
            <GIC_SPI 327 IRQ_TYPE_EDGE_RISING>,
            <GIC_SPI 328 IRQ_TYPE_EDGE_RISING>,
            <GIC_SPI 329 IRQ_TYPE_EDGE_RISING>;
        interrupt-names = "int_req", "dma_rx", "dma_tx", "dma_rt";
        clocks = <&cpg CPG_MOD R9A07G044_SSI0_PCLK2>,
            <&cpg CPG_MOD R9A07G044_SSI0_PCLK_SFR>,
            <&audio_clk1>, <&audio_clk2>;
        clock-names = "ssi", "ssi_sfr", "audio_clk1", "audio_clk2";
        resets = <&cpg R9A07G044_SSI0_RST_M2_REG>;
        dmas = <&dmac 0x2655>, <&dmac 0x2656>;
        dma-names = "tx", "rx";
        power-domains = <&cpg>;
        #sound-dai-cells = <0>;
        status = "disabled";
    };
};

In arch/arm64/boot/dts/renesas/rz-smarc-common.dtsi (RZ/G2L):
/{
    snd_rzg2l: sound {
        compatible = "simple-audio-card";
        simple-audio-card,format = "i2s";
        simple-audio-card,bitclock-master = <&cpu_dai>;
        simple-audio-card,frame-master = <&cpu_dai>;
        simple-audio-card,mclk-fs = <256>;

        simple-audio-card,widgets = "Microphone", "Microphone Jack";
        simple-audio-card,routing =
            "L2", "Mic Bias",
            "R2", "Mic Bias",
            "Mic Bias", "Microphone Jack";

        cpu_dai: simple-audio-card,cpu {
            sound-dai = <&ssi0>;
        };

        codec_dai: simple-audio-card,codec {
            sound-dai = <&wm8978>;
            clocks = <&versa3 2>;
        };
    };

    -----
};

&ssi0 {
    pinctrl-0 = <&ssi0_pins>;
    pinctrl-names = "default";

    status = "okay";
};

```

Figure 5-8 Example of Device tree settings for Audio on RZ/G2L, RZ/G2UL, RZ/G2LC, RZ/V2L and RZ/Five

In **arch/arm64/boot/dts/renesas/r9a08g045.dtsi (RZ/G3S)**:

```
soc: soc {
    ssi3: ssi@100a8c00 {
        compatible = "renesas,r9a08g045-ssi",
                     "renesas,rz-ssi";
        reg = <0 0x100a8c00 0 0x400>;
        interrupts = <GIC_SPI 249 IRQ_TYPE_LEVEL_HIGH>,
                     <GIC_SPI 250 IRQ_TYPE_EDGE_RISING>,
                     <GIC_SPI 251 IRQ_TYPE_EDGE_RISING>;
        interrupt-names = "int_req", "dma_rx", "dma_tx";
        clocks = <&cpg CPG_MOD R9A08G045_SSI3_PCLK2>,
                 <&cpg CPG_MOD R9A08G045_SSI3_PCLK_SFR>,
                 <&audio_clk1>, <&audio_clk2>;
        clock-names = "ssi", "ssi_sfr", "audio_clk1", "audio_clk2";
        resets = <&cpg R9A08G045_SSI3_RST_M2_REG>;
        dmas = <&dmac 0x2671>, <&dmac 0x2672>;
        dma-names = "tx", "rx";
        power-domains = <&cpg>;
        #sound-dai-cells = <0>;
        status = "disabled";
    };
    spdif: spdif@100a9000 {
        compatible = "renesas,r9a08g045-spdif",
                     "renesas,rz-spdif";
        reg = <0 0x100a9000 0 0x400>;
        interrupts = <GIC_SPI 387 IRQ_TYPE_LEVEL_HIGH>;
        interrupt-names = "intreq_spdif_n";
        clocks = <&cpg CPG_MOD R9A08G045_SPDIF_PCLK>,
                 <&audio_clk1>, <&audio_clk2>;
        clock-names = "spdif-tx-rx", "audio_clk1", "audio_clk2";
        resets = <&cpg R9A08G045_SPDIF_RST>;
        dmas = <&dmac 0x1e79>, <&dmac 0x1e7a>;
        dma-names = "tx", "rx";
        power-domains = <&cpg>;
        #sound-dai-cells = <0>;
        status = "disabled";
    };
};
```

```

In arch/arm64/boot/dts/renesas/rzg3s-smarc.dtsi (RZ/G3S):
snd_rzg3s: sound {
    compatible = "simple-audio-card";
    simple-audio-card,name = "snd_rzg3s";

    ssi_link: simple-audio-card,dai-link@0 {
        format = "i2s";
        bitclock-master = <&cpu_dai0>;
        frame-master = <&cpu_dai0>;
        mclk-fs = <256>;

        cpu_dai0: cpu {
            sound-dai = <&ssi3>;
        };

        codec {
            sound-dai = <&da7212>;
            clocks = <&versa3 1>;
        };
    };

    #if SPDIF_SEL
        spdif_link: simple-audio-card,dai-link@1 {
            bitclock-master = <&cpu_dai1>;
            frame-master = <&cpu_dai1>;

            cpu_dai1: cpu {
                sound-dai = <&spdif>;
            };

            codec {
                sound-dai = <&dummy_codec>;
            };
        };
    #endif
};

&ssi3 {
    clocks = <&cpg CPG_MOD R9A08G045_SSI3_PCLK2>,
            <&cpg CPG_MOD R9A08G045_SSI3_PCLK_SFR>,
            <&versa3 2>, <&audio_clk2>;
    pinctrl-names = "default";
    pinctrl-0 = <&ssi3_pins>, <&audio_clock_pins>;
    status = "okay";
};
#if SPDIF_SEL
&spdif {
    pinctrl-0 = <&spdif_pins>;
    pinctrl-names = "default";
    status = "okay";
};
#endif

```

Figure 5-9 Example of device tree settings for Audio on RZ/G3S.

Note: In case of using SPDIF, must set SPDIF_SEL as ON due to pins multiplexing with other modules.

By default, RZ/V2N evaluation boards, RZ/V2H evaluation board and RZ/G3E SMARC evaluation boards work in Master mode in which BCLK/LRCLK clocks are controlled by internal R-Car sound module. When working in Slave mode, the audio codec generates BCLK/LRCLK. In this case, **bitclock-master** and **frame-master** device-tree properties are required to set the audio codec as the master of BCLK/LRCLK.

```
In arch/arm64/dts/renesas/r9a09g056n48-rzv2n-evk.dts
sound_card: sound {
    compatible = "audio-graph-card";

    label = "rsnd_rzv2n";

    dais = <
        &rsnd_port0 /* DA7212 */
        &rsnd_port1 /* HDMI0 */
        &spdif_port0
        &spdif_port2
    >;
};

&rcar_sound {
    pinctrl-0 = <&sound_pins>;
    pinctrl-names = "default";

    status = "okay";

    /* audio_clkout */
    #clock-cells = <0>;
    clock-frequency = <11289600>;

    /* Multi DAI */
    #sound-dai-cells = <1>;

    ports {
        #address-cells = <1>;
        #size-cells = <0>;

        rsnd_port0: port@0 {
            reg = <0>;
            rsnd_endpoint0: endpoint {
                remote-endpoint = <&da7212_endpoint>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint0>;
                frame-master = <&rsnd_endpoint0>;
                mclk-fs = <256>;

                playback = <&ssi3>, <&src0>, <&dvc0>;
                capture = <&ssi4>, <&src1>, <&dvc1>;
            };
        };

        rsnd_port1: port@1 {
            reg = <1>;
            rsnd_endpoint1: endpoint {
                remote-endpoint = <&dsi_hdmi0_snd_in>;

                dai-format = "i2s";
                bitclock-master = <&rsnd_endpoint1>;
                frame-master = <&rsnd_endpoint1>;

                playback = <&ssi0>;
            };
        };

        spdif_port0: port@2 {
            reg = <2>;
```

```

        spdif0_endpoint: endpoint {
            remote-endpoint = <&dummy_codec0>;

            bitclock-master = <&spdif0_endpoint>;
            frame-master = <&spdif0_endpoint>;

            playback = <&spdif0>;
            capture = <&spdif0>;
        };
};

spdif_port2: port@3 {
    reg = <3>;
    spdif2_endpoint: endpoint {
        remote-endpoint = <&dummy_codec2>;

        bitclock-master = <&spdif2_endpoint>;
        frame-master = <&spdif2_endpoint>;

        playback = <&spdif2>;
        capture = <&spdif2>;
    };
};

};

&ssi4 {
    shared-pin;
};

```

Figure 5-10 Example of device tree settings for RZ/V2N boards when working in audio Slave mode.

In **arch/arm64/boot/dts/renesas/rzg3e-smarc-som.dtsi**

```

codec_test0: codec_test {
    compatible = "linux,snd-soc-dummy";
    #sound-dai-cells = <0>;

    port {
        dummy_codec: endpoint {
            remote-endpoint = <&pdm_endpoint>;
        };
    };

    sound_card: sound {
        compatible = "audio-graph-card";

        label = "rcar-sound";
        dais = <&rsnd_port0 /* DA7211 */
              &rsnd_port1 /* HDMI0 */
              &pdm_link
              >;
    };

    &rcar_sound {
        pinctrl-0 = <&sound_clk_pins &sound_pins>;
        pinctrl-names = "default";

        status = "okay";

        /* audio_clkout */
        #clock-cells = <0>;
        clock-frequency = <11289600>;

        /* Multi DAI */
        #sound-dai-cells = <1>;
    };
};

```

```

ports {
    #address-cells = <1>;
    #size-cells = <0>;
    rsnd_port0: port@0 {
        reg = <0>;
        rsnd_endpoint0: endpoint {
            remote-endpoint = <&da7212_endpoint>;

            dai-format = "i2s";
            bitclock-master = <&rsnd_endpoint0>;
            frame-master = <&rsnd_endpoint0>;

            playback = <&ssi3>;
            capture = <&ssi4>, <&src0>, <&dvc0>;
        };
    };

    rsnd_port1: port@1 {
        reg = <1>;
        rsnd_endpoint1: endpoint {
            remote-endpoint = <&adv7535_codec_ep>;

            dai-format = "i2s";
            bitclock-master = <&rsnd_endpoint1>;
            frame-master = <&rsnd_endpoint1>;

            playback = <&ssi0>;
        };
    };
};

&pdm0 {
    pinctrl-0 = <&pdm0_pins>;
    pinctrl-names = "default";
    status = "okay";

    pdm_link: port {
        pdm_endpoint: endpoint {
            remote-endpoint = <&dummy_codec>;
        };
    };

    channel1 {
        status = "okay";
    };
};

```

Figure 5-11 Example of device tree settings for RZ/G3E boards

Revision History	Linux Interface Specification Device Driver Audio User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Jun. 11, 2021	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, change version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2Ls
1.2	Feb. 15, 2022	—	Add RZ/G2LC, RZ/G2UL information
1.3	Mar. 31, 2022	—	No modification, change version to keep consistent with other documents
1.4	May. 31, 2022	—	No modification, change version to keep consistent with other documents
1.5	Jun. 24, 2022	—	Add RZ/Five information Update RZ/G2UL data diagram with SW1-3 connection
1.6	Sep. 15, 2022	—	No modification, change version to keep consistent with other documents
1.7	Dec. 15, 2022	—	No modification, change version to keep consistent with other documents
1.8	Mar. 15, 2023	—	No modification, change version to keep consistent with other documents
1.9	Mar. 31, 2024	5	Add more supported data format: S24_LE, S32_LE Add more supported sampling rate: 88200Hz, 96000Hz, 192000Hz
		—	Remove all SRC information due to no support.
1.10	Jun. 30, 2024	19	Add support Full duplex communication mode
1.11	Mar. 31, 2025	19	Remove support Full duplex communication mode due to a fixed limitation Update devicetree nodes for BSP-3.0.7
1.12	May. 30, 2025	1	Add MPU information support for both kernel versions v5.10 and v6.1
1.13	Jun. 30, 2025	—	Add RZ/V2N audio information support for kernel version v6.1
1.14	Jul. 22, 2025	—	Add RZ/G3E audio information support for kernel version v6.1
1.15	Nov. 28, 2025	—	Add information of RZ/G2UL, and RZ/V2L support for kernel v6.1 Add information of RZ/G3S support for both kernel v5.10 and v6.1
1.16	Dec. 19, 2025	—	Add information of RZ/V2H
1.17	Mar. 27, 2026	—	Add HDMI audio support and switch to use audio-graph-card in device tree for RZ/V2N

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