

Linux Interface Specification Device Driver USB2.0 Function

RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group and
RZ/Five

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/G3E Group, RZ/G3S Group, RZ/V2H Group and RZ/V2N Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
User's manual for Software	Description of USB Linux interface Specification	Linux interface Specification – USB 2.0 Function	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Description
BSP	Board Support Package
CPRM	Content Protection for Recordable Media
DMA	Direct Memory Access
DMAC	DMA Controller
EHCI	Enhanced Host Controller Interface
GPL	GNU General Public License
LGPL	GNU Lesser General Public License
MTD	Memory Technology Device
NCQ	Native Command Queuing
OHCI	Open Host Controller Interface
OSS	Open Source Software
USB	Universal Serial Bus
VLP	Verified Linux Package

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1. Overview

1.1 Overview

This manual explains the driver module (this module) that controls the USB 2.0 Function controller on RZ/G2L Group, RZ/V2L Group, RZ/G3E Group, RZ/G3S, RZ/V2H and RZ/V2N Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L group, RZ/G3S and RZ/Five.
- v6.1: RZ/G2L group, RZ/V2L group, RZ/G3E, RZ/G3S, RZ/V2H and RZ/V2N.

1.2 Function

This module controls USB 2.0 Function controller on RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S and transmission and reception of data are performed by USB2.0 standard between USB Host connected to the USB interface.

Port 0 is used as an OTG device in combination with the USB Host controller.

This module supports only role swaps, not using Host Negotiation Protocol (HNP) and no support for Session Request Protocol (SRP).

The following data transfer type is supported:

- Control transfer
- Isochronous transfer
- Bulk transfer
- Interrupt transfer

The number of end points assigned to each data transfer type is as follows.

type of transfer	The number of end point quota pipes
Control transfer	1
Interrupt transfer	4
Bulk transfer	3
Bulk or isochronous transfer	2

1.3 Connected Port

This module supports one USB ports in RZ/G2L, RZ/V2L, RZ/Five, RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E Evaluation Board.

Table 1-1 Connected Port (RZ/G2L, RZ/V2L and RZ/Five)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	CN11	Type micro AB connector

Table 1-2 Connected Port (RZ/V2N)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	CN2	Type micro AB connector

Table 1-2 Connected Port (RZ/G3E, RZ/G3S and RZ/V2H)

Port No.	Standard	Connector No.	Content
0	USB2.0 Host/Function	USB0_OTG	Type micro AB connector

1.4 Reference Document

1.4.1 Standard

Supported standard of this module is as follows.

Table 1-3 Standard (RZ/G2L, RZ/V2L, RZ/Five, RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S)

Reference No.	Issue	Title	Edition	Date
-	USB Implementers Forum, Inc	Universal Serial Bus Specification	Rev.2.0	Apr. 27, 2000

1.4.2 Related Document

There is no related document of this module.

1.5 Restrictions

There is no restriction in this module.

1.6 Notice

The notes of this module are shown below.

- The known problem in the standard gadget class driver for Linux is not supported.
- Only the standard Gadget interface for Linux is supported by this module.
- High Bandwidth of interrupt transfer is not supported.
- High Bandwidth of Isochronous transfer is not supported.

2. Terminology

The following table shows the terminology related to this module.

Table 2.1 Terminology

Terms	Explanation
USB	USB Universal Serial Bus
UDC	USB Device Controller
OTG	On-The-Go
EP	Endpoint

3. Operating Environment

3.1 Hardware Environment

The following table lists the hardware needed to use this module.

Table 3.1 Hardware Environment

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

3.2 Module Configuration

The following figure shows the configuration of this module.

Board	Port
RZ/G2L, RZ/V2L, RZ/Five	CN11
RZ/G3S	USB0_OTG
RZ/G3E	USB0_OTG
RZ/V2N	USB0_OTG
RZ/V2H	USB0_OTG

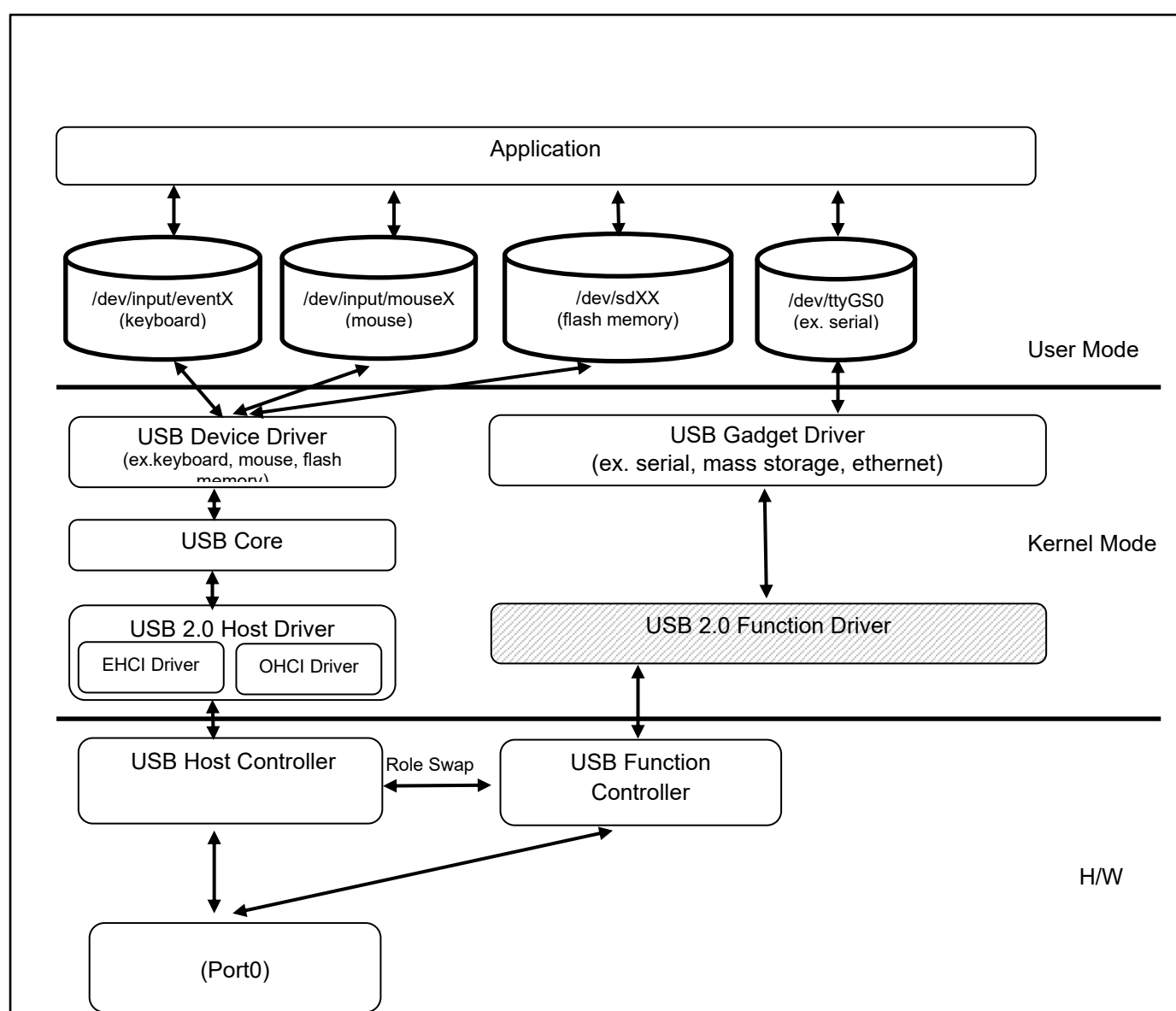


Figure 3-1 Module Configuration (RZ/G2L, RZ/V2L, RZ/Five, RZ/V2N, RZ/V2H, RZ/G3S and RZ/G3E)

3.3 State Transition Diagram

There is no state transition diagram for this module.

4. External Interface

The supported external interface of this module is explained.

Since it is based on USB standard, the definition described in "include/linux/usb/ch9.h" is omitted.

4.1 Global Variables and Constants

4.1.1 Global variables

There are no global variables for this module.

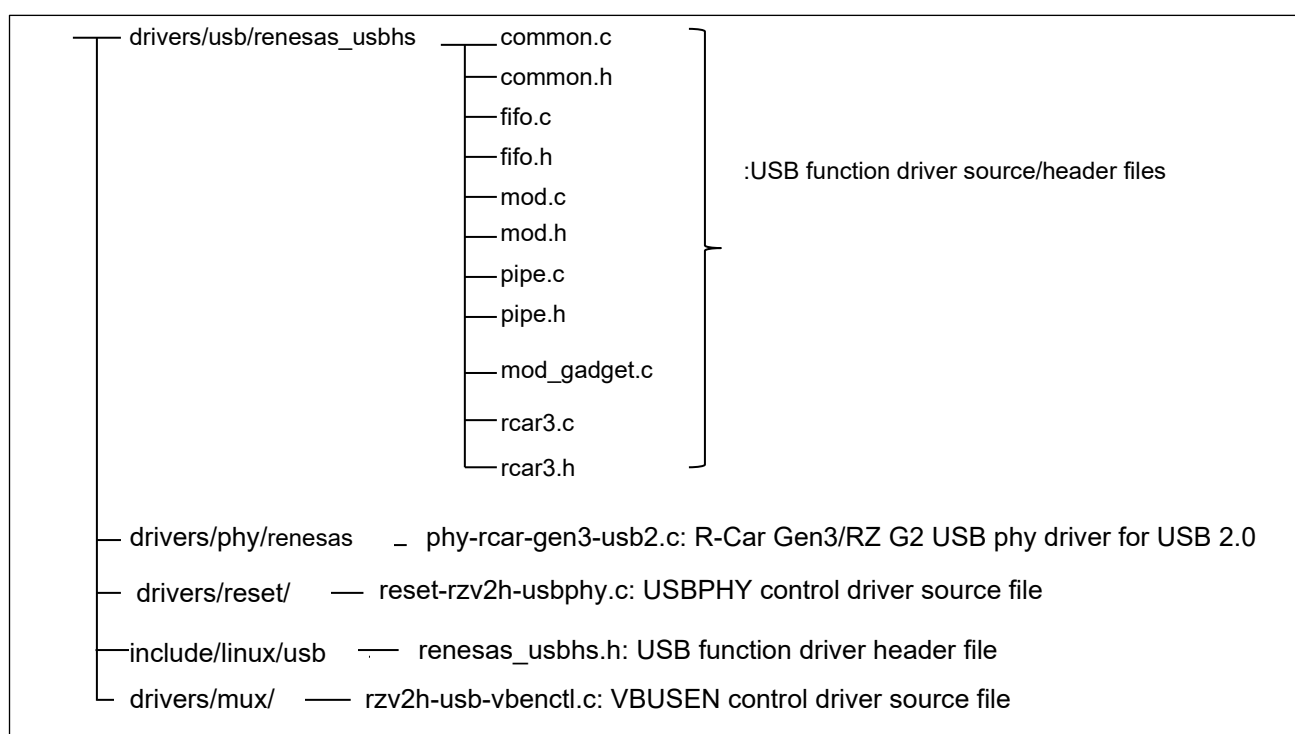
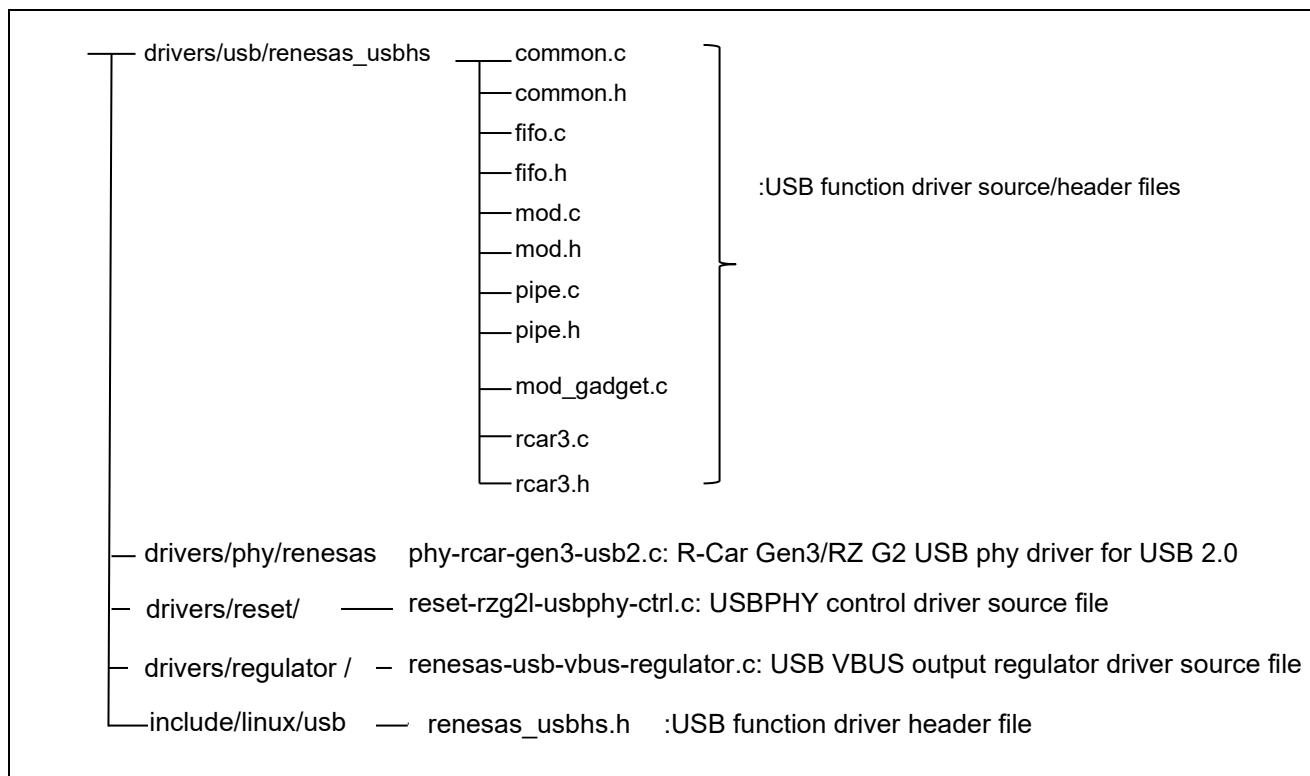
4.1.2 Global constants

There are no global constants for this module.

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.



5.1.1 Device tree definition

Below figure lists the necessary properties to support USB 2.0 function in RZ/G2L and RZ/V2L Evaluation Board Kit.

- **r9a07g044.dtsi for RZ/G2L, RZ/G2LC, r9a07g054.dtsi for RZ/V2L and r9a07g043.dtsi for RZ/G2UL, RZ/Five**

```

phyrst: usbphy-ctrl@11c40000 {
    compatible = "renesas,r9a07g044-usbphy-ctrl",
                "renesas,rzg2l-usbphy-ctrl";
    reg = <0 0x11c40000 0 0x10000>;
    clocks = <&cpg CPG_MOD R9A07G044_USB_PCLK>;
    resets = <&cpg R9A07G044_USB_PRESETN>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    status = "disabled";

    usb0_vbus_otg: regulator-vbus {
        regulator-name = "vbus";
    };
};

hsusb: usb@11c60000 {
    compatible = "renesas,usbhs-r9a07g044",
                "renesas,rza2-usbhs";
    reg = <0 0x11c60000 0 0x10000>;
    interrupts = <GIC_SPI 100 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 101 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 102 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 103 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G044_USB_PCLK>,
            <&cpg CPG_MOD R9A07G044_USB_U2P_EXR_CPUCLK>;
    resets = <&phyrst 0>,
            <&cpg R9A07G044_USB_U2P_EXL_SYSRST>;
    renesas,buswait = <7>;
    phys = <&usb2_phy0 3>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

usb2_phy0: usb-phy@11c50200 {
    compatible = "renesas,usb2-phy-r9a07g044",
                "renesas,rzg2l-usb2-phy";
    reg = <0 0x11c50200 0 0x700>;
    interrupts = <GIC_SPI 94 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G044_USB_PCLK>,
            <&cpg CPG_MOD R9A07G044_USB_U2H0_HCLK>;
    resets = <&phyrst 0>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};

```



```

usb2_phy1: usb-phy@11c70200 {
    compatible = "renesas,usb2-phy-r9a07g044",
                "renesas,rzg2l-usb2-phy";
    reg = <0 0x11c70200 0 0x700>;
    interrupts = <GIC_SPI 99 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A07G044_USB_PCLK>,
            <&cpg CPG_MOD R9A07G044_USB_U2H1_HCLK>;
    resets = <&phyrst 1>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 5-3: Enable USB2.0 function (hsusb), and USBPHY (phyrst , usb2_phy) device nodes

Note: All the information in above device tree is used for both RZ/G2L and RZ/V2L except:
 Clocks and resets: R9A07G044_ for RZ/G2L, RZ/G2LC, R9A07G043_ for RZG2UL, RZ/Five and
 R9A07G054_ for RZ/V2L.

Interrupt:

Nodes	RZ/G2L, RZ/G2LC, RZ/V2L
usb2_phy0	<GIC_SPI 94 IRQ_TYPE_LEVEL_HIGH>
usb2_phy1	<GIC_SPI 99 IRQ_TYPE_LEVEL_HIGH>
hsusb	<GIC_SPI 100 IRQ_TYPE_EDGE_RISING> <GIC_SPI 101 IRQ_TYPE_LEVEL_HIGH> <GIC_SPI 102 IRQ_TYPE_LEVEL_HIGH> <GIC_SPI 103 IRQ_TYPE_LEVEL_HIGH>

Nodes	RZ/G2UL	RZ/Five
usb2_phy0	<SOC_PERIPHERAL_IRQ(94) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(126) IRQ_TYPE_LEVEL_HIGH>
usb2_phy1	<SOC_PERIPHERAL_IRQ(99) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(131) IRQ_TYPE_LEVEL_HIGH>
hsusb	<SOC_PERIPHERAL_IRQ(100) IRQ_TYPE_EDGE_RISING> <SOC_PERIPHERAL_IRQ(101) IRQ_TYPE_LEVEL_HIGH> <SOC_PERIPHERAL_IRQ(102) IRQ_TYPE_LEVEL_HIGH> <SOC_PERIPHERAL_IRQ(103) IRQ_TYPE_LEVEL_HIGH>	<SOC_PERIPHERAL_IRQ(132) IRQ_TYPE_EDGE_RISING> <SOC_PERIPHERAL_IRQ(133) IRQ_TYPE_LEVEL_HIGH> <SOC_PERIPHERAL_IRQ(134) IRQ_TYPE_LEVEL_HIGH> <SOC_PERIPHERAL_IRQ(135) IRQ_TYPE_LEVEL_HIGH>

Below figure lists the necessary properties to support USB 2.0 function in RZ/V2N Evaluation Board Kit.

- **r9a09g056.dtsi for RZ/V2N**

```
usb20phyrst: usb20phy-reset@15830000 {
    compatible = "renesas,r9a09g056-usb2phy-reset",
        "renesas,r9a09g057-usb2phy-reset";
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <0>;
    #mux-state-cells = <1>;
    status = "disabled";
};

hsusb: usb@15820000 {
    compatible = "renesas,usbhs-r9a09g056",
        "renesas,rzg2l-usbhs";
    reg = <0 0x15820000 0 0x10000>;
    interrupts = <GIC_SPI 751 IRQ_TYPE_EDGE_RISING>,
        <GIC_SPI 752 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 753 IRQ_TYPE_LEVEL_HIGH>,
        <GIC_SPI 754 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb5>;
    resets = <&usb20phyrst>,
        <&cpg 0xae>;
    phys = <&usb2_phy0 3>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};

usb2_phy0: usb-phy@15800200 {
    compatible = "renesas,usb2-phy-r9a09g056", "renesas,usb2-phy-r9a09g057";
    reg = <0 0x15800200 0 0x700>;
    interrupts = <GIC_SPI 745 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>,
        <&cpg CPG_CORE R9A09G056_USB2_0_CLK_CORE0>;
    clock-names = "fck", "usb_x1";
    resets = <&usb20phyrst>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    mux-states = <&usb20phyrst 1>;
    status = "disabled";

    usb2_phy0_vbus_otg: vbus-regulator {
        regulator-name = "USB2PHY0-VBUS-OTG";
        status = "disabled";
    };
};
```

Figure 5-4: Enable USB2.0 function (hsusb), and USBPHY (phyrst , usb2_phy) device nodes RZ/V2N

Note: All the information in the above device tree is used for RZ/V2N.

Below figure lists the necessary properties to support USB 2.0 function in RZ/G3E Evaluation Board Kit.

- **r9a09g047.dtsi for RZ/G3E**

```
usb2_phy0: usb-phy@15800200 {
    compatible = "renesas,usb2-phy-r9a09g047",
                "renesas,rzv2h-usb2-phy";
    reg = <0 0x15800200 0 0x700>;
    interrupts = <GIC_SPI 745 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>;
    resets = <&usb20phyrst 0>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};
usb20phyrst: usb20phy-ctrl@15830000 {
    compatible = "renesas,r9a09g047-usbphy-ctrl",
                "renesas,rzv2h-usbphy-ctrl";
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    status = "disabled";
};
hsusb: usb@15820000 {
    compatible = "renesas,usbhs-r9a09g047",
                "renesas,rzg2l-usbhs";
    reg = <0 0x15820000 0 0x10000>;
    interrupts = <GIC_SPI 751 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 752 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 753 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 754 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb5>;
    resets = <&cpg 0xae>,
            <&usb20phyrst 0>;
    phys = <&usb2_phy0 3>;
    phy-names = "usb";
    power-domains = <&cpg>;
    status = "disabled";
};
```

Figure 5-5: Enable USB2.0 function (hsusb), and USBPHY (phyrst , usb2_phy) device nodes RZ/G3E

Note: All the information in the above device tree is used for RZ/G3E.

Below figure lists the necessary properties to support USB 2.0 function in RZ/G3S Evaluation Board Kit.

- **r9a08g045.dtsi for RZ/G3S**

```

phyrst: usbphy-ctrl@11e00000 {
    compatible = "renesas,r9a08g045-usbphy-ctrl";
    reg = <0 0x11e00000 0 0x10000>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>;
    resets = <&cpg R9A08G045_USB_PRESETN>;
    power-domains = <&cpg>;
    #reset-cells = <1>;
    renesas,sysc-pwrrdy = <&sysc 0xd70 0x1>; (*1)
    status = "disabled";

    usb0_vbus_otg: regulator-vbus {
        regulator-name = "vbus";
    };
};

usb2_phy0: usb-phy@11e10200 {
    compatible = "renesas,usb2-phy-r9a08g045";
    reg = <0 0x11e10200 0 0x700>;
    interrupts = <GIC_SPI 78 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
            <&cpg CPG_MOD R9A08G045_USB_U2H0_HCLK>;
    resets = <&phyrst 0>,
            <&cpg R9A08G045_USB_U2H0_HRESETN>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};

usb2_phy1: usb-phy@11e30200 {
    compatible = "renesas,usb2-phy-r9a08g045";
    reg = <0 0x11e30200 0 0x700>;
    interrupts = <GIC_SPI 83 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
            <&cpg CPG_MOD R9A08G045_USB_U2H1_HCLK>;
    resets = <&phyrst 1>,
            <&cpg R9A08G045_USB_U2H1_HRESETN>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};

hsusb: usb@11e20000 {
    compatible = "renesas,usbhs-r9a08g045",
                "renesas,rzg2l-usbhs";
    reg = <0 0x11e20000 0 0x10000>;
    interrupts = <GIC_SPI 85 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 86 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 87 IRQ_TYPE_LEVEL_HIGH>;

```

```

        <GIC_SPI 84 IRQ_TYPE_LEVEL_HIGH>;
        clocks = <&cpg CPG_MOD R9A08G045_USB_PCLK>,
        <&cpg CPG_MOD R9A08G045_USB_U2P_EXR_CPUCLK>;
        resets = <&phyrst 0>,
        <&cpg R9A08G045_USB_U2P_EXL_SYSRST>;
        renesas,buswait = <7>;
        phys = <&usb2_phy0 3>;
        phy-names = "usb";
        power-domains = <&cpg>;
        status = "disabled";
};

```

Figure 5-6: Enable USB2.0 function (hsusb), and USBPHY (phyrst , usb2_phy) device nodes RZ/G3S

Note: All the information in the above device tree is used for RZ/G3S.

(*)1: renesas,sysc-pwrrdy property (only for RZ/G3S) handle SYS_USB_PWRRDY register to control USB region power.

Below figure lists the necessary properties to support USB 2.0 function in RZ/V2H Evaluation Board Kit.

- **r9a09g057.dtsi for RZ/V2H**

```

usb20phyrst: usb20phy-reset@15830000 {
    compatible = "renesas,r9a09g057-usb2phy-reset";
    reg = <0 0x15830000 0 0x10000>;
    clocks = <&cpg CPG_MOD 0xb6>;
    resets = <&cpg 0xaf>;
    power-domains = <&cpg>;
    #reset-cells = <0>;
    status = "disabled";
};

usb2_phy0: usb-phy@15800200 {
    compatible = "renesas,usb2-phy-r9a09g057";
    reg = <0 0x15800200 0 0x700>;
    interrupts = <GIC_SPI 745 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&cpg CPG_MOD 0xb3>,
    <&cpg CPG_CORE R9A09G057_USB2_0_CLK_CORE0>;
    clock-names = "fck", "usb_x1";
    resets = <&usb20phyrst>;
    #phy-cells = <1>;
    power-domains = <&cpg>;
    status = "disabled";
};

hsusb: usb@15820000 {
    compatible = "renesas,usbhs-r9a09g057",
    "renesas,rzg2l-usbhs";
    reg = <0 0x15820000 0 0x10000>;
    interrupts = <GIC_SPI 751 IRQ_TYPE_EDGE_RISING>,
    <GIC_SPI 752 IRQ_TYPE_LEVEL_HIGH>,
    <GIC_SPI 753 IRQ_TYPE_LEVEL_HIGH>,

```

```

                                <GIC_SPI 754 IRQ_TYPE_LEVEL_HIGH>;
                                clocks = <&cpg CPG_MOD 0xb3>, <&cpg CPG_MOD 0xb5>;
                                resets = <&usb20phyrst>, cpg 0xae>;
                                phys = <&usb2_phy0 3>;
                                phy-names = "usb";
                                power-domains = <&cpg>;
                                status = "disabled";
};

```

Figure 5-7: Enable USB2.0 function (hsusb), and USBPHY (phyrst , usb2_phy) device nodes RZ/V2H

- **rz-smarc-common.dtsi for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL and RZ/Five**

```

&phyrst {
    status = "okay";
};

&hsusb {
    dr_mode = "otg";
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb0_pins>;
    pinctrl-names = "default";

    vbus-supply = <&usb0_vbus_otg>;
    status = "okay";
};

&usb2_phy1 {
    pinctrl-0 = <&usb1_pins>;
    pinctrl-names = "default";

    status = "okay";
};

```

Figure 5-8: Enable USB 2.0 function and USBPHY

r9a09g056n48-rzv2n-evk.dts for RZ/V2N.

```
&usb20phyrst {
    status = "okay";
};

&usb2_phy0_vbus_otg {
    status = "okay";
};

&hsusb {
    dr_mode = "otg";
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb20_pins>;
    pinctrl-names = "default";

    vbus-supply = <&usb2_phy0_vbus_otg>;
    status = "okay";
};
```

Figure 5-9: Enable USB 2.0 function and USBPHY for RZ/V2N**rzg3e-smarc.dtsi for RZ/G3E.**

```
&usb20phyrst {
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb20_pins>;
    pinctrl-names = "default";

    status = "okay";
};

&hsusb {
    dr_mode = "otg";
    status = "okay";
};
```

Figure 5-10: Enable USB 2.0 function and USBPHY for RZ/G3E

rzg3s-smarc.dtsi for RZ/G3S.

```

&phyrst {
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb0_pins>;
    pinctrl-names = "default";
    vbus-supply = <&usb0_vbus_otg>;
    status = "okay";
};

&usb2_phy1 {
    pinctrl-0 = <&usb1_pins>;
    pinctrl-names = "default";
    status = "okay";
};

&hsusb {
    dr_mode = "otg";
    status = "okay";
};

```

Figure 5-11: Enable USB 2.0 function and USBPHY for RZ/G3S

```

&usb20phyrst {
    status = "okay";
};

&usb2_phy0 {
    pinctrl-0 = <&usb20_pins>;
    pinctrl-names = "default";

    status = "okay";
};

&hsusb {
    dr_mode = "otg";
    status = "okay";
};

```

Figure 5-12: Enable USB 2.0 function and USBPHY for RZ/V2H

5.1.2 Integration of a USB Function control driver

To enable the function of this module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  [*] USB support --->
    <*> Renesas USBHS controller
    ...
    <*> USB Gadget Support --->
      <*> USB Peripheral Controller --->
        <M> Renesas USBHS controller

Device Drivers --->
  PHY Subsystem ---->
    <*> Renesas R-Car generation 3 USB 2.0 PHY driver

Device Drivers --->
  Regulator Subsystem ---->
    <*> Renesas RZ/G2L USB VBUS regulator driver
```

Figure 5-13: Kernel configuration for this module (RZ/G2L Group, RZ/V2L Group, RZ/Five, RZ/G3E, RZ/G3S, RZ/V2N and RZ/V2H)

5.2 Option Setting

5.2.1 Module Parameters

There are no module parameters.

5.2.2 Kernel Parameters

There are no kernel parameters.

6. USB 2.0 OTG Interface

6.1 Role Swap usage

1. The default value of role is Host. Run this command to switch mode from Host to Peripheral.

```
echo peripheral > /sys/devices/platform/soc/11c50200.usb-phy/role
```

2. Run this command to switch mode from Peripheral to Host.

```
echo host > /sys/devices/platform/soc/11c50200.usb-phy/role
```

Revision History	Linux Interface Specification Device Driver USB2.0 Function User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
0.50	Apr. 30, 21	—	First Edition issued
1.0	Jul. 15, 2021	—	No modification, keep version to keep consistent with other documents
1.1	Sep. 15, 2021	—	Merge RZ/G2L driver manual with RZ/V2L
1.2	Feb. 15, 2022	—	Add RZ/G2UL, RZ/G2LC device
1.3	Mar. 31, 2022	9, 10, 11	Update: - Name and working directory of USBPHY driver. - Devicetree definition
1.4	Mar. 31, 2022	—	No modification, keep version to keep consistent with other documents
1.5	June. 24, 2022	9	Update: - Remove: Configure USBPHY Control (usbphy is driver, enable to use, no need to setting by manually) - Add RZ/Five device
1.6	Sep. 15, 2022	—	No modification
1.7	Dec. 15, 2022	—	No modification
1.8	Mar. 15, 2023	—	No modification, keep version to keep consistent with other documents
1.9	Jun. 25, 2024	1	Update the number of end points assigned to each data transfer type table
1.10	Mar. 31, 2025	6, 9	Remove USB DMAC Update name of device tree files
1.11	May. 30, 2025	1	Add MPU information support for both kernel versions v5.10 and v6.1.
1.12	Jun. 30, 2025	—	Add RZ/V2N information
1.13	Jul. 22, 2025	1	Add RZ/G3E overview and function
		2	Add connected port for RZ/G3E
		4	Add RZ/G3E hardware specification
		5	Modify module configuration to support RZ/G3E Add port table for boards - Remove USBDMAC component. (RZ/V2N)
		8	Add directory configuration for RZ/G3E
		12-13-14	Add device tree nodes to enable USB2 function for RZ/G3E
1.14	Nov. 28, 2025	1	Add information of RZ/G2UL and RZ/V2L support for v6.1
		8	- Add USB Vbus regulator driver path (figure 5-1).
		9	- Add vbus regulator node to phyrst node figure 5-2.
		10	Update Interrupt table
		13	- Add vbus-supply to usb2_phy0 node (figure 5-4).
		14	- Add Renesas USB Vbus regulator kernel configuration (figure 5-6).
		—	Add RZ/G3S information
1.15	Dec. 19, 2025	—	Add RZ/V2H information
1.16	Mar. 27, 2026	4	Add product number for RZ/V2N Version 2
		8, 11, 16	Update information for RZ/V2N

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RZ/G2L Group, RZ/V2L Group, RZ/V2N Group,
RZ/V2H Group, RZ/G3E Group, RZ/G3S Group
and RZ/Five



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