

Linux Interface Specification Device Driver POE3

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/Five Group and
RZ/G3S Group

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (<http://www.renesas.com>).

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.1.10 Nov 28, 2025)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

• Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group and RZ/G3S Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of POE3 Linux interface Specification	Linux interface Specification – POE3	This user's manual
	Description of MTU3a Linux interface Specification	Linux interface Specification – MTU3a	
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
MTU3a	Multi-Function Timer Pulse Unit 3a
PWM	Pulse Width Modulation
POE3	Port Output Enable 3

Table of Contents

1. Overview.....	1
1.1 Overview	1
1.2 Function	1
1.3 Reference	1
1.3.1 Standard.....	1
1.3.2 Related documents	1
1.4 Restrictions	1
2. Terminology.....	2
3. Operating Environment.....	3
3.1 Hardware Environment	3
3.2 Module Configuration	4
3.3 Setting Procedure	4
4. External Interface.....	5
4.1 sysfs interface	5
4.2 Definitions	6
4.2.1 Device information in Device Tree	6
4.2.2 Input condition setting in Device Tree	8
4.2.3 Setting POE3 in Device Tree to control MTU3 outputs	9
5. Integration.....	11
5.1 Directory Configuration	11
5.2 Integration Procedure	11
5.3 Option Setting	11
5.3.1 Module Parameters	11
5.3.2 Kernel Parameters	11

1. Overview

1.1 Overview

This manual explains the driver module that controls the MTU3a module for RZ/G2L Group, RZ/V2L Group, RZ/Five Group and RZ/G3S Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/Five Group and RZ/G3S Group.
- v6.1: RZ/G2L Group, RZ/V2L Group and RZ/G3S Group.

1.2 Function

This driver module supports to place and release the high-impedance state for MTU3a pins in response of various conditions.

1.3 Reference

1.3.1 Standard

There is no reference document on standards.

1.3.2 Related documents

There is no document related to this kernel.

1.4 Restrictions

None.

2. Terminology

The following table shows the terminology related to this kernel.

Table 2-1 Terminology

Terms	Explanation
POE3	Port Output Enable 3
MTU3a	Multi-Function Timer Pulse Unit 3
PWM	Pulse width modulation
SPOER	Software port output enable register

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this kernel.

Table 3-1 Hardware environment

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE

3.2 Module Configuration

The following figure shows the configuration of this module.

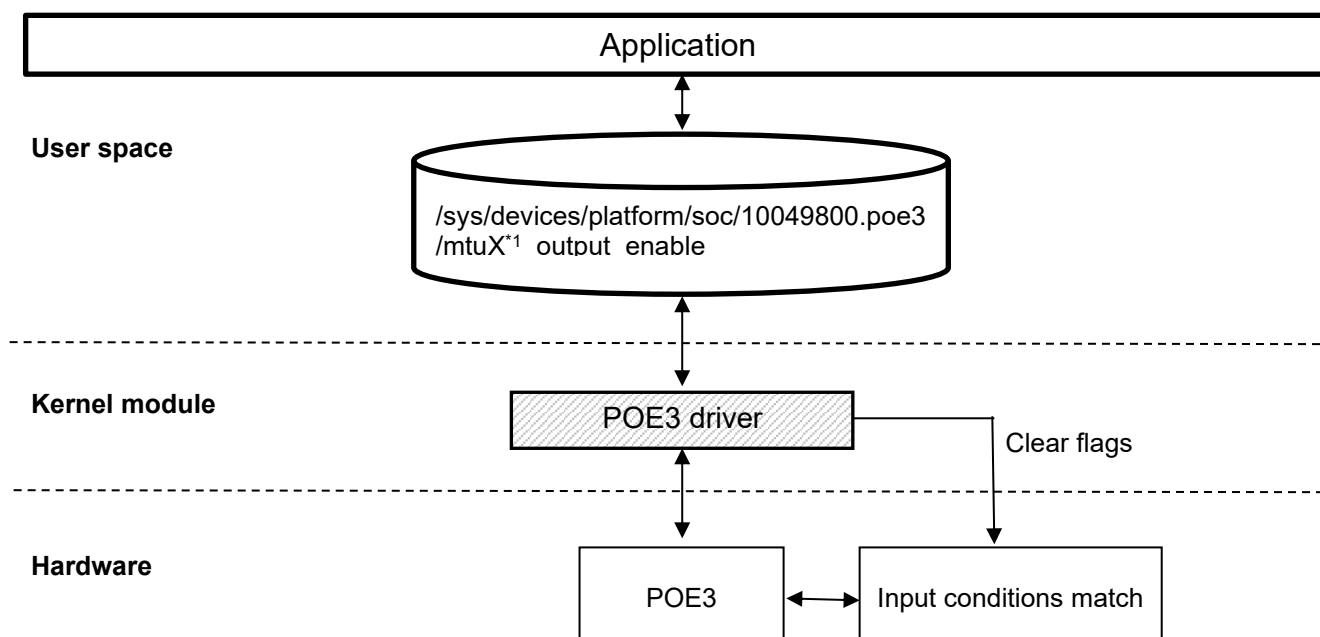


Figure 3-1 POE3 module configuration

Note 1: X could be 0, 34, or 67 depending on MTU3a channels' outputs which it's controlling.

3.3 Setting Procedure

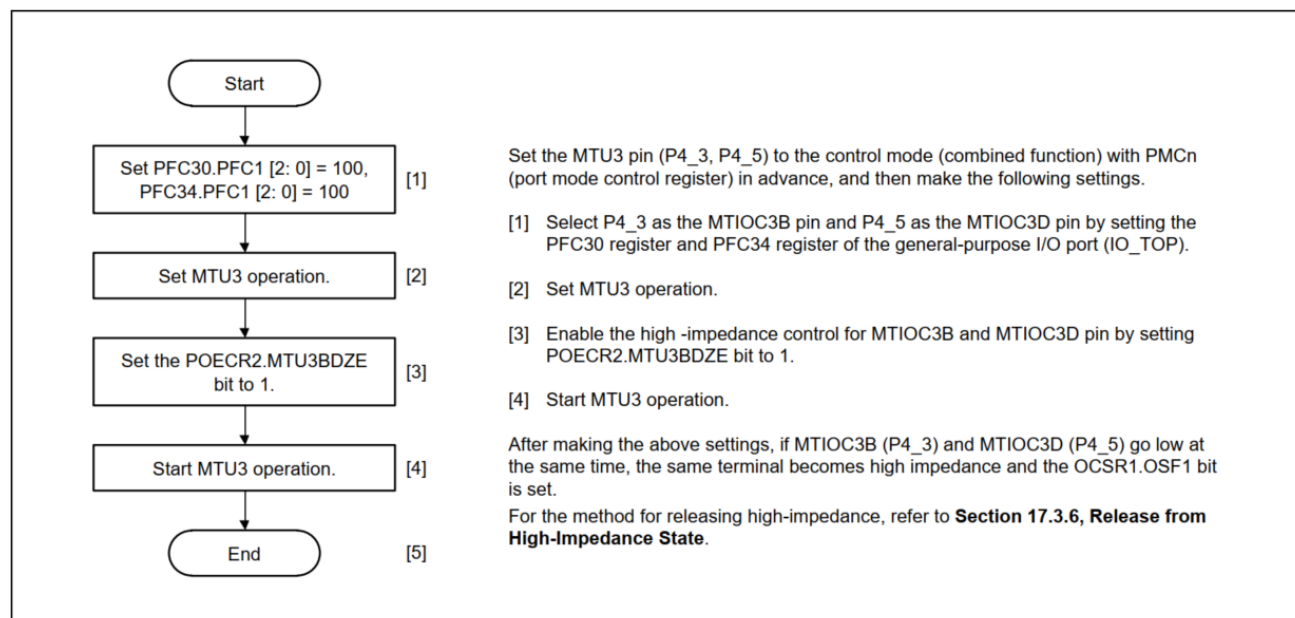


Figure 3-2 Procedure for Setting POE3

4. External Interface

This section explain about the functions this module supplies.

4.1 sysfs interface

POE3 supports to place MTU3 output pins in high-impedance state. To control work of POE3, we support sysfs device attributes of POE3 to disable or enable output of corresponding MTU3a pins. Details are described in below table.

Table 4.1-1 POE3 syfs and coressponding controlled MTU3 pins (RZ/G2L, RZ/G2LC, RZ/V2L and RZ/G3S)

MTU3a pins of channels	Device Node
MTU0	/sys/devices/platform/soc/10049800.poe3/mtu0_output_enable
MTU3 and MTU4	/sys/devices/platform/soc/10049800.poe3/mtu34_output_enable
MTU6 and MTU7	/sys/devices/platform/soc/10049800.poe3/mtu67_output_enable

To use above sysfs device attributes, user must do configuration in device tree, refer **4.2 Definitions** for more details.

POE3 will automatically place MTU3 pins in high-impedance state, if one of following conditions is matched.

- Modify SPOER register in kernel space by writing 0 to sysfs device attributes. For example. To place MTIOC3B and MTIOC3D of MTU3 channel in high-impedance state, let's type

```
#echo 0 > sys/devices/platform/soc/10049800.poe3/mtu34_output_enable
```
- Input conditions of assigned POE3 input pins happen. Those conditions could be falling edge or low-level sampling 16 times with clock rate $P0\phi/4$, $P0\phi/16$, $P0\phi/128$. To configure which pins are used as inputs of POE3 and setting conditions, refer **4.2 Definitions**
- Output levels of MTU3 complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.

To release MTU3 pins from high-impedance state and clear all relative triggered flags, let's type.

```
#echo 1 > sys/devices/platform/soc/10049800.poe3/mtu34_output_enable
```

4.2 Definitions

4.2.1 Device information in Device Tree

POE3 device properties are showed as below:

```
poe3: poe3@10049800 {
    compatible = "renesas,rz-poe3",
                 "renesas,r9a07g044-poe3";
    reg = <0 0x10049800 0 0x18>;
    interrupts = <GIC_SPI 214 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 215 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 216 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 217 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "oei1", "oei2", "oei3", "oei4";
    clocks = <&cpg CPG_MOD R9A07G044_POE3_CLKM_POE>;
    clock-names = "fck";
    resets = <&cpg R9A07G044_POE3_RST_M_REG>;
    power-domains = <&cpg>;
    status = "disabled";
};
```

Figure 4-1 Configuration example of POE3's required properties (RZ/G2L, RZ/G2LC and RZ/V2L)

Note: All of the information in above device tree is used for both RZ/G2L, RZ/G2LC and RZ/V2L except R9A07G044L_CLK_MTU is used for RZ/G2L, R9A07G044C_CLK_MTU is used for RZ/G2LC and R9A07G054L_CLK_MTU is used for RZ/V2L.

- compatible:
must be "renesas,poe3" or "renesas,rzg2l-mtu3".
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
interrupt specifier for POE3.
- interrupt-names:
mapped with interrupts and must be in the order with interrupts number.
- clocks, resets:
phandle + clock/reset specifier pairs.
- power-domains:
specify the power-domain for POE3.

```

poe3: poe3@10049800 {
    compatible = "renesas,rz-poe3",
                 "renesas,r9a08g045-poe3";
    reg = <0 0x10049800 0 0x18>;
    interrupts = <GIC_SPI 232 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 233 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 234 IRQ_TYPE_LEVEL_HIGH>,
                 <GIC_SPI 235 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "oei1", "oei2", "oei3", "oei4";
    clocks = <&cpg CPG_MOD R9A08G045_POE3_CLKM_POE>;
    clock-names = "fck";
    resets = <&cpg R9A08G045_POE3_RST_M_REG>;
    power-domains = <&cpg R9A08G045_PD_POE3>;
    status = "disabled";
};

```

Figure 4-2 Configuration example of POE3's required properties (RZ/G3S)

Note: All of the information in above device tree is used for RZ/G3S.

- **compatible:**
must be "renesas,rz-poe3" or "renesas, r9a08g045-poe3".
- **reg:**
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- **interrupts:**
interrupt specifier for POE3.
- **interrupt-names:**
mapped with interrupts and must be in the order with interrupts number.
- **clocks, resets:**
phandle + clock/reset specifier pairs.
- **power-domains:**
specify the power-domain for POE3.

4.2.2 Input condition setting in Device Tree

POE3 provides 4 pins which are POE0#, POE4#, POE8#, POE10#. Those pins are used to capture input signals to place MTU3 output pins in high-impedance state when conditions are matched.

The format of setting POE3 input pins with their condition are as below.

```
poe3_pins_mode = <pinA  conditionA>, <pinB  conditionB>, ...;
```

Where:

- pinA, pinB: are numbers which stand for their input pins. The values are 0, 4, 8, 10 corresponding to POE0#, POE4#, POE8#, POE10#.
- conditionA, conditionB: are numbers indicating conditions where interrupts will be triggered to place MTU3 pins in high-impedance state, if they're matched. Details are in below table.

Table 4-2 POE3 input conditions and their number in device tree setting(RZ/G2L, RZ/G2LC, RZ/V2L and RZ/G3S)

Condition number in device tree	Conditions
0	Falling edge happen.
1	Low level has been sampled continuously 16 times at P0φ/4 clock pulses.
2	Low level has been sampled continuously 16 times at P0φ/16 clock pulses.
3	Low level has been sampled continuously 16 times at P0φ/128 clock pulses.

To take fully effect, POE3 input pins configuration should be used along with pinctrl.

Here is an example to define POE0# whose condition is falling edge happening on this pin, POE4# whose condition is 16 times sampling low level continuously at P0φ/128 clock pulses, POE10# whose condition is 16 times sampling low level continuously at P0φ/4 clock pulses.

```
&pinctrl {
    poe3_pins: poe3 {
        pinmux = <RZG2L_PORT_PINMUX(12, 0, 3)>, /* POE0_N */
                <RZG2L_PORT_PINMUX(12, 1, 3)>, /* POE4_N */
                <RZG2L_PORT_PINMUX(13, 0, 3)>, /* POE8_N */
                <RZG2L_PORT_PINMUX(13, 1, 3)>; /* POE10_N */
    };
};
...
&poe3 {
    pinctrl-0 = <&poe3_pins>;
    pinctrl-names = "default";
    poe3_pins_mode = <0 0>, <4 3>, <10 1>;
};
```

Figure 4-3 Example of setting POE3's input pins

4.2.3 Setting POE3 in Device Tree to control MTU3 outputs

POE3 can control output pins for MTU0, MTU3 and MTU4 in pairs, MTU6 and MTU7 in pairs.

To add MTU3 outputs under control of POE3, user must add relative sub-node of the MTU3 channels to POE3 node in device tree. Those sub-nodes are **mtu3_ch0** for MTU0, **mtu3_ch34** for MTU3 and MTU4, **mtu3_ch67** for MTU6 and MTU7.

In each sub-node we have some properties.

- **mtu3_outputs**: is a required property to indicate which pins of the MTU3 channel are under control of POE3. The values may be from 0 to 4, details are described in **Table 4-3**.
- **addition_poe3_inputs**: is an optional property to add more input pins to make request when conditions on those pins are matched. The values are numbers of pins which user want to add, details are described in **Table 4-4**.

Table 4-3 POE3 sub-nodes and their mtu3_outputs value in device tree

Device tree Sub-node	mtu3_outputs value in device tree	MTU3 pins will be placed under control of POE3
mtu3_ch0	0	MTIOC0A
	1	MTIOC0B
	2	MTIOC0C
	3	MTIOC0D
mtu3_ch34	0	MTIOC3B and MTIOC3D
	1	MTIOC4A and MTIOC3C
	2	MTIOC4B and MTIOC4D
mtu3_ch67	0	MTIOC6B and MTIOC6D
	1	MTIOC7A and MTIOC7C
	2	MTIOC7B and MTIOC7D

Table 4-4 POE3 sub-nodes and addition_poe3_inputs in device tree

Device tree Sub-node	Default supported input pins	Additional pins and values addition_poe3_inputs of in devicetree
mtu3_ch0	POE8#	- 0 for POE0# - 4 for POE4# - 10 for POE10#
mtu3_ch34	POE0#	- 4 for POE4# - 8 for POE8# - 10 for POE10#
mtu3_ch67	POE4#	- 0 for POE0# - 8 for POE8# - 10 for POE10#

To take fully effect as expectation, sub-nodes properties, **poe3_pins_mode** and **pinctrl** should be used in combination.

Here is an example of combination definition of POE3 in device tree.

- MTU3 pins under POE3 control are: MTIOC0A, MTIOC0D, MTIOC3B and MTIOC3B, MTIOC7A and MTIOC7C, MTIOC7B and MTIOC7D.

- Input condition are: falling edge on POE0#, 16 times sampling low level continuously at P0φ/128 clock pulses on POE4#, 16 times sampling low level continuously at P0φ/16 clock pulses on POE8#, 16 times sampling low level continuously at P0φ/4 clock pulses on POE10#.
- Additional pins: MTU0 use POE4#, MTU3 and MTU4 use POE4# and POE10#, MTU6 and MTU7 don't use additional pins.

```

&pinctrl {
    poe3_pins: poe3 {
        groups = "poe_a";
        function = "poe";
    };
};
...
&poe3 {
    pinctrl-0 = <&poe3_pins>;
    pinctrl-names = "default";
    poe3_pins_mode = <0 0>, <4 3>, <8 2>, <10 1>;

    status = "okay";

    mtu3_ch0 {
        mtu3_outputs = <0 3>;
        addition_poe3_inputs = <4>;
    };

    mtu3_ch34 {
        mtu3_outputs = <0>;
        addition_poe3_inputs = <4 10>;
    };

    mtu3_ch67 {
        mtu3_outputs = <1 2>;
    };
};

```

Figure 4-4 Example of setting POE3 to control MTU3 pins

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.




```
—— drivers/clocksource/      —— renesas-poe3.c      : POE3 Driver source file
```

Figure 5-1 Directory configuration (RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five and RZ/G3S)

5.2 Integration Procedure

To enable the function of this module, make the following setting with Kernel Configuration.



```
Device Drivers  --->
  Clock Source drivers  --->
    [*] Renesas POE3 driver
```

Figure 5-2 Kernel configuration (RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five and RZ/G3S)

5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

5.3.2 Kernel Parameters

There are no kernel parameters.

Revision History	Linux Interface Specification Device Driver POE3 User's Manual: Software
------------------	---

Rev.	Date	Description	
		Page	Summary
1.2	Feb. 15, 2022	—	First Edition issued
1.3	Mar. 31, 2022	—	Update information of new VLP.
1.4	May. 31, 2022	—	No modification, change version to keep consistent with other documents
1.5	Jun. 24, 2022	—	Update information of RZ/Five.
1.6	Sep. 15, 2022	—	Update version of document.
1.7	Dec. 15, 2022	—	Update version of document.
1.8	Mar. 15, 2023	—	No modification, change version to keep consistent with other documents
1.9	May. 30, 2025	1	- Add MPU information support for both kernel versions v5.10 and v6.1.
1.10	Nov. 28, 2025	1	- Add information of RZ/G2UL and RZ/V2L support for kernel v6.1.
		—	- Add RZ/G3S information

Linux Interface Specification Device Driver POE3
User's Manual: Software

Publication Date: Rev. 1.10 Nov. 28, 2025

Published by: Renesas Electronics Corporation

RZ/G2L Group, RZ/V2L Group,
RZ/Five Group and RZ/G3S Group



Renesas Electronics Corporation