

Linux Interface Specification Device Driver xSPI

User's Manual: Software

RZ/V2N Group, RZ/V2H Group, RZ/G3E Group
and RZ/G3S Group

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU. A basic knowledge of electric circuits, logical circuits, and MPUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of Expanded SPI (xSPI) Linux interface Specification	Linux Interface Specification Device Driver xSPI	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
xSPI	Expanded Serial Peripheral Interface

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1. Overview

1.1 Overview

This manual explains the driver module (this module) that controls Expanded Serial Peripheral Interface (xSPI) on RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/V2N, RZ/G3E and RZ/G3S.
- v6.1: RZ/V2N, RZ/V2H and RZ/G3S.

1.2 Function

This module allows the connected memory devices to be accessed by reading the external address space or using Manual mode to transmit and receive data.

The following table lists the features of this module.

Table 1-1 Driver Features

Feature	Support status (RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S)
Master Mode	Support
Serial-Flash Memory Interface	- Clock frequency: 133MHz. - Support Protocol: 1/4 pin with SDR (1S-1S-1S and 1S-4S-4S)
Octa-Flash memory Interface	No support
External Address Space Read Mode	Support
Manual Mode	Support

1.3 Connected device

This module can connect serial flash and memory devices on RZV2N, RZ/V2H, RZ/G3E and RZ/G3S.

1.4 Reference

1.4.1 Standard

There is no document related to standard for this module.

1.4.2 Related documents

There is no document related to this module.

1.5 Restrictions

There is no restriction in this module.

1.6 Notice

On RZ/V2N Evaluation Board Kit, RZ/V2H Evaluation Board Kit, RZ/G3E Evaluation Board Kit and RZ/G3S Evaluation Board Kit, one serial flash memory device is connected and another serial flash memory device can connect in parallel to implement an 8-bit bus interface.

2. Terminology

The following table shows the terminology related to this kernel.

Table 2-1 Terminology

Terms	Explanation
xSPI	Expanded S erial P eripheral Interface.

3. Operating Environment

3.1 Hardware Environment

The following table lists the hardware needed to use this module.

Table 3-1 Hardware specification

Name	Product number
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE

3.2 Module Configuration

The following figure shows the RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S configuration of this module.

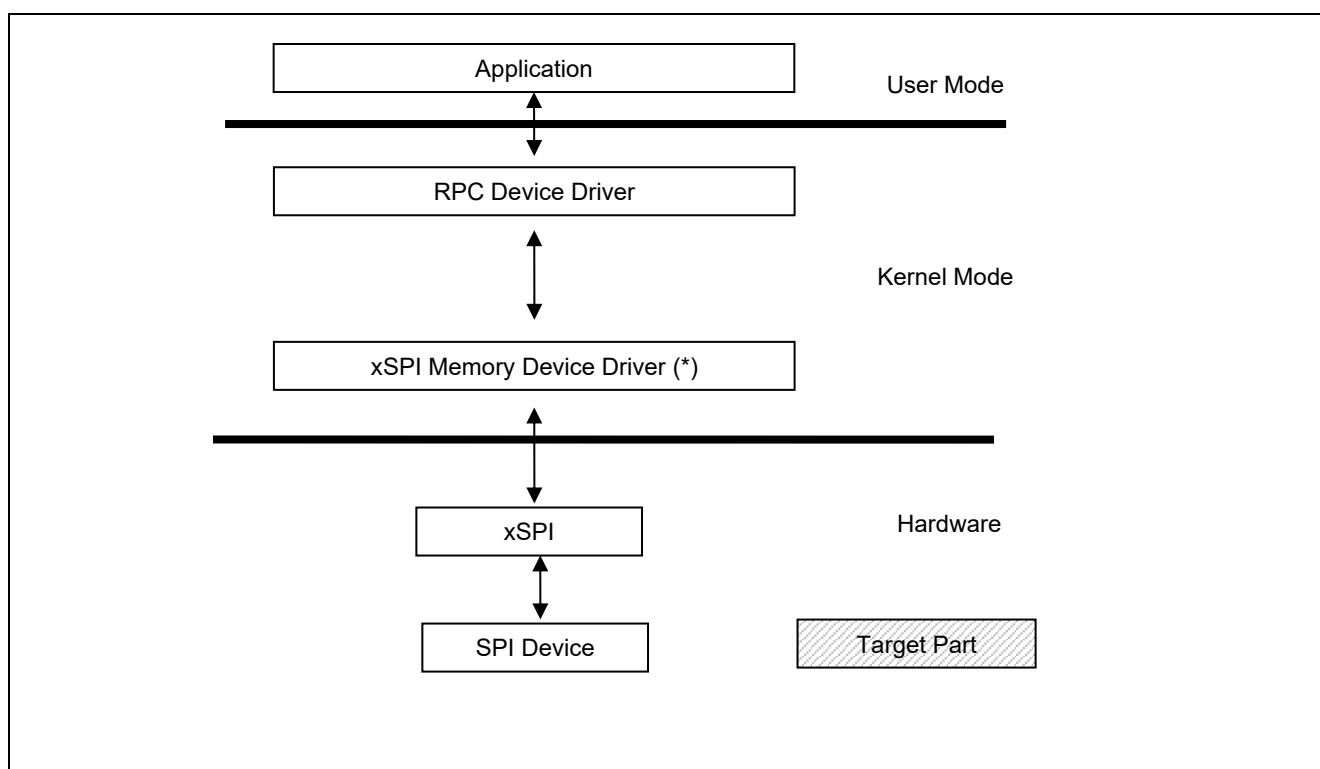


Figure 3-1 Module configuration

(*): This driver is supported only for RZ/V2N and RZ/G3S.

3.3 State Transition Diagram

The following figure shows the software flowchart of this module.

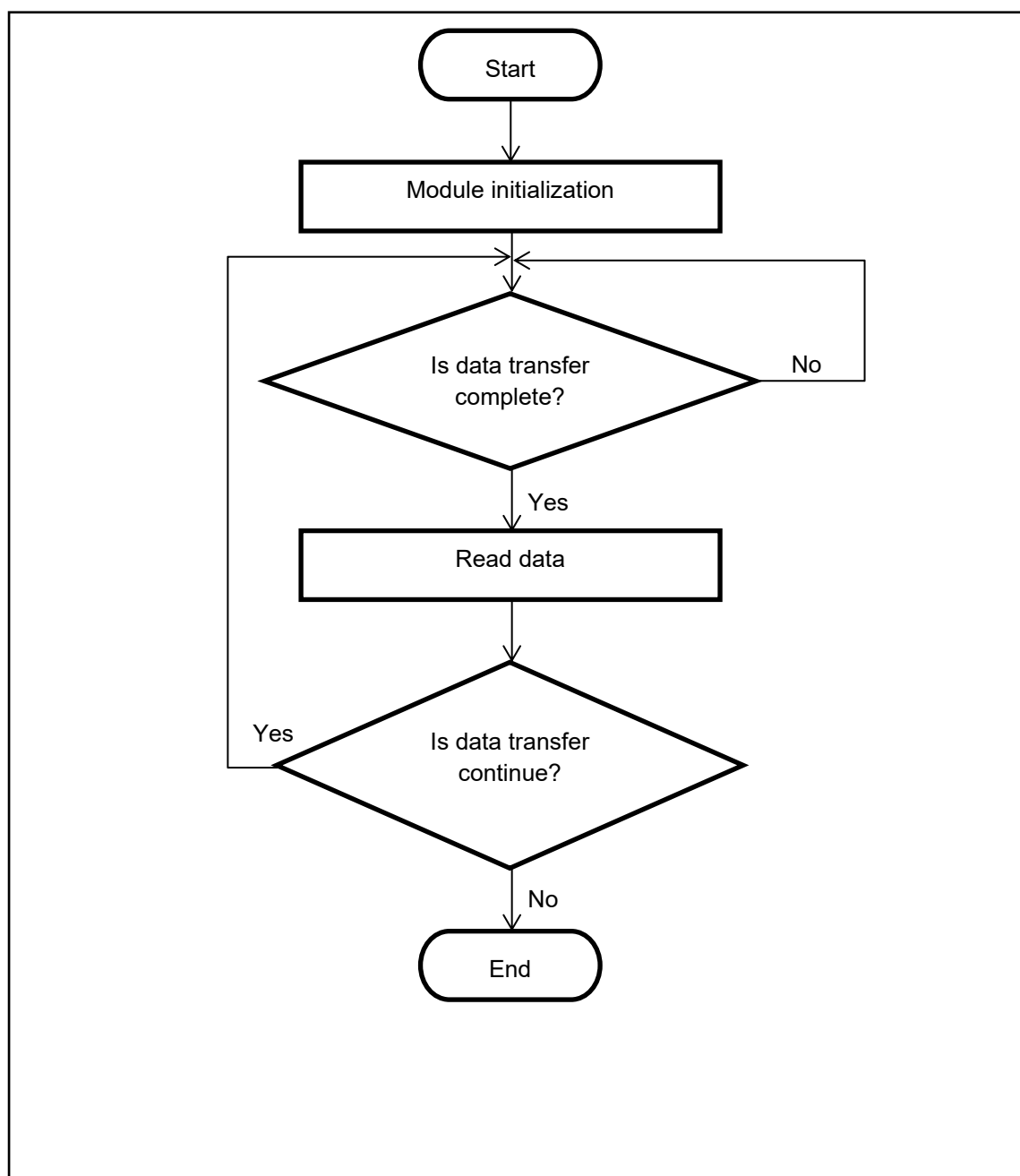


Figure 3–2 Module software flowchart

4. External Interface

4.1 Sysfs Interface

Table 4-1 Hardware specification

xSPI Interfaces	Notes
/sys/class/spi_master/spi1/spi1.0	-

4.2 External Function

Detailed explanation is skipped because the external interface of this module is based on Linux.

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.

_____ drivers/spi/	_____ drivers/spi/spi-rpc-if.c	: RPC driver source file
_____ drivers/memory/	_____ drivers/memory/renesas-xspi-if.c	: xSPI memory source

Figure 5–1 Directory Configuration RZ/V2N, RZ/G3S in kernel version v5.10

_____ drivers/spi/	_____ drivers/spi/spi-rpc-if.c	: RPC driver source file
_____ drivers/memory/	_____ drivers/memory/renesas-rpc-if.c	: xSPI memory source file

Figure 5–2 Directory Configuration RZ/V2N, RZ/V2H and RZ/G3S in kernel version v6.1

5.2 Integration Procedure

Add the setting of the channel to be used by modifying the settings in Device tree.

5.2.1 Device tree settings

The target file by board is as follows.

Directory: arch/arm64/boot/dts/renesas

- r9a09g056.dtsi for RZ/V2N.
- r9a09g056n48-evk.dts for RZ/V2N Evaluation Kit.
- r9a09g057.dtsi for RZ/V2H.
- rzv2h-evk-common.dtsi for RZ/V2H Evaluation Board Kit
- r9a09g047.dtsi for RZ/G3E.
- r9a09g047e57-smarc.dts for RZ/G3E SMARC Evaluation Board Kit
- r9a08g045.dtsi for RZ/G3S.
- rzg3s-smarc-som.dtsi for RZ/G3S SMARC SOM

5.2.1.1 Settings in SoC DTSI

Figure 5-3 and Figure 5-7 demonstrate devicetree setting of xSPI in SoC DTSI files of and RZ/V2N.

Figure 5-4 and Figure 5-8 demonstrate devicetree setting of xSPI in SoC DTSI files of and RZ/V2H.

Figure 5-5 and Figure 5-9 demonstrate devicetree setting of xSPI in SoC DTSI files of and RZ/G3E.

Figure 5-6 and Figure 5-10 demonstrate devicetree setting of xSPI in SoC DTSI files of and RZ/G3S.

```

xspi: spi@11030000 {
    compatible = "renesas,r9a09g056-xspi", "renesas,r9a09g047-xspi";
    reg = <0 0x11030000 0 0x10000>,
        <0 0x20000000 0 0x1000000>;
    reg-names = "regs", "dmap";
    interrupts = <GIC_SPI 228 IRQ_TYPE_EDGE_RISING>,
        <GIC_SPI 229 IRQ_TYPE_EDGE_RISING>;
    interrupt-names = "pulse", "err_pulse";
    clocks = <&cpg CPG_MOD 0x9f>,
        <&cpg CPG_MOD 0xa0>,
        <&cpg CPG_CORE R9A09G056_SPI_CLK_SPI>,
        <&cpg CPG_MOD 0xa1>;
    clock-names = "ahb", "axi", "spi", "spix2";
    resets = <&cpg 0xa3>, <&cpg 0xa4>;
    reset-names = "hresetn", "aresetn";
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};

```

Figure 5–3 xSPI Device tree setting in SoC DTSI (RZ/V2N)

```

xspi: spi@11030000 {
    compatible = "renesas,r9a09g057-xspi", "renesas,r9a09g047-xspi";
    reg = <0 0x11030000 0 0x10000>,
        <0 0x20000000 0 0x10000000>;
    reg-names = "regs", "dmap";
    interrupts = <GIC_SPI 228 IRQ_TYPE_EDGE_RISING>,
        <GIC_SPI 229 IRQ_TYPE_EDGE_RISING>;
    interrupt-names = "pulse", "err_pulse";
    clocks = <&cpg CPG_MOD 0x9f>,
        <&cpg CPG_MOD 0xa0>,
        <&cpg CPG_CORE R9A09G057_SPI_CLK_SPI>,
        <&cpg CPG_MOD 0xa1>;
    clock-names = "ahb", "axi", "spi", "spix2";
    resets = <&cpg 0xa3>, <&cpg 0xa4>;
    reset-names = "hresetn", "aresetn";
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};

```

Figure 5–4 xSPI Device tree setting in SoC DTSI (RZ/V2H)

```

xspi: spi@11030000 {
    compatible = "renesas,g3e-xspi-if";
    reg = <0 0x11030000 0 0x10000>,
        <0 0x20000000 0 0x1000000>;
    reg-names = "regs", "dmap";
    clocks = <&cpg CPG_MOD 161>,
        <&cpg CPG_MOD 159>,
        <&cpg CPG_MOD 160>,
        <&cpg CPG_MOD 162>;
    clock-names = "spi", "hclk", "aclk", "spix2";
    resets = <&cpg 163>,
        <&cpg 164>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};

```

Figure 5–5 xSPI Device tree setting in SoC DTSI (RZ/G3E)

```

xspi: spi@10060000 {
    compatible = "renesas,r9a08g045-xspi";
    reg = <0 0x10060000 0 0x10000>,
        <0 0x20000000 0 0x10000000>;
    reg-names = "regs", "dirmap";
    clocks = <&cpg CPG_MOD R9A08G045_SPI_CLK>,
        <&cpg CPG_MOD R9A08G045_SPI_HCLK>,
        <&cpg CPG_MOD R9A08G045_SPI_ACLK>,
        <&cpg CPG_MOD R9A08G045_SPI_CLKX2>;
    clock-names = "spi", "hclk", "aclk", "spix2";
    resets = <&cpg R9A08G045_SPI_HRESETN>,
        <&cpg R9A08G045_SPI_ARESETN>;
    power-domains = <&cpg>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};

```

Figure 5–6 xSPI Device tree setting in SoC DTSI (RZ/G3S)

5.2.1.2 Settings in board DTS

Following is device setting of xSPI in Board DTS file which is board-specific and extended for that in SoC:

```

&xspi {
    pinctrl-0 = <&xspi_pins>;
    pinctrl-names = "default";
    /*
     * MT25QU512ABB8E12 flash chip is capable of running at 166MHz
     * clock frequency. Set the clock frequency to the maximum 133MHz
     * supported by the RZ/V2N SoC.
     */
    assigned-clocks = <&cpg CPG_CORE R9A09G056_SPI_CLK_SPI>;
    assigned-clock-rates = <133333334>;
    status = "okay";

    flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0>;
        vcc-supply = <&reg_1p8v>;
        m25p,fast-read;
        spi-tx-bus-width = <4>;
        spi-rx-bus-width = <4>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x00060000>;
            };

            partition@60000 {
                label = "fip";
                reg = <0x00060000 0x1fa0000>;
            };

            partition@2000000 {
                label = "user";
                reg = <0x2000000 0x2000000>;
            };
        };
    };
};

```

Figure 5–7 xSPI setting in Board DTS RZ/V2N


```

&xspi {
    pinctrl-0 = <&xspi_pins>;
    pinctrl-names = "default";
    /*
     * MT25QU512ABB8E12 flash chip is capable of running at 166MHz
     * clock frequency. Set the clock frequency to the maximum 133MHz
     * supported by the RZ/V2H SoC.
     */
    assigned-clocks = <&cpg CPG_CORE R9A09G057_SPI_CLK_SPI>;
    assigned-clock-rates = <133333334>;
    status = "okay";

    flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0>;
        vcc-supply = <&reg_1p8v>;
        m25p,fast-read;
        spi-tx-bus-width = <4>;
        spi-rx-bus-width = <4>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x00060000>;
            };

            partition@60000 {
                label = "fip";
                reg = <0x00060000 0x1fa0000>;
            };

            partition@2000000 {
                label = "user";
                reg = <0x2000000 0x2000000>;
            };
        };
    };
};

```

Figure 5–8 xSPI setting in Board DTS RZ/V2H

```

&xspi {
    pinctrl-0 = <&xspi_pins>;

    pinctrl-names = "default";
    status = "okay";

    flash@0 {
        compatible = "atmel,at25ql128a", "jedec,spi-nor";
        reg = <0>;
        m25p,fast-read;
        spi-max-frequency = <50000000>;
        spi-tx-bus-width = <1>;
        spi-rx-bus-width = <1>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x00040000>;
                read-only;
            };

            partition@60000 {
                label = "fip";
                reg = <0x00060000 0x00FA0000>;
                read-only;
            };
        };
    };
};

```

Figure 5–9 xSPI setting in Board DTS RZ/G3E

```

&xspi {
    pinctrl-0 = <&xspi_pins>;
    pinctrl-names = "default";

    status = "okay";

    flash@0 {
        compatible = "atmel,at25ql128a", "jedec,spi-nor";
        reg = <0>;
        m25p,fast-read;
        spi-max-frequency = <50000000>;
        spi-tx-bus-width = <4>;
        spi-rx-bus-width = <4>;

        partitions {
            compatible = "fixed-partitions";
            #address-cells = <1>;
            #size-cells = <1>;

            partition@0 {
                label = "bl2";
                reg = <0x00000000 0x0001D200>;
                read-only;
            };
            partition@1D200 {
                label = "fip";
                reg = <0x0001D200 0x001C2E00>;
                read-only;
            };
            partition@1E0000 {
                label = "env";
                reg = <0x001E0000 0x00020000>;
                read-only;
            };
            partition@200000 {
                label = "test-area";
                reg = <0x00200000 0x00E00000>;
            };
        };
    };
};

```

Figure 5–10 xSPI setting in Board DTS RZ/G3S

Note: “spi-tx-bus-width” and “spi-rx-bus-width” properties determine xSPI protocol. Setting 1 to both the properties for using 1S-1S-1S protocol and setting 4 to both the properties for using 1S-4S-4S protocol.

5.2.2 Kernel configuration

To enable the function of this module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  [*] SPI support -->
    --- SPI support
        ...
    <*> Renesas RPC-IF SPI driver
  [*] Memory Controller drivers
    <*> Renesas xSPI driver
```

Figure 5–11 Kernel configuration for xSPI Driver RZ/V2N, RZ/G3S in kernel version v5.10

```
Device Drivers --->
  [*] SPI support -->
    --- SPI support
        ...
    <*> Renesas RPC-IF SPI driver
  [*] Memory Controller drivers
    <*> Renesas RPC-IF driver
```

Figure 5–12 Kernel configuration for xSPI Driver RZ/V2N, RZ/G3S in kernel version v6.1

```
Device Drivers --->
  [*] SPI support -->
    --- SPI support
        ...
    <*> Renesas RPC-IF SPI driver
```

Figure 5–13 Kernel configuration for xSPI Driver RZ/G3E and RZ/V2H

To use file system driver JFF2, make the following setting with Kernel Configuration.

```
File Systems --->
  <*> Miscellaneous filesystems -->
    <*> Journaling Flash File System v2 (JFFS2) support
    [*] JFFS2 write-buffering support
```

Figure 5–14 File system configuration for xSPI Driver RZ/V2N, RZ/V2H, RZ/G3E and RZ/G3S

5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

Revision History	Linux Interface Specification Device Driver xSPI User's Manual: Software
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Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2025	—	First Edition issued Add RZ/V2N support information
1.01	Jul. 22, 2025	—	Add RZ/G3E support information
1.02	Nov. 28, 2025	— 4	Add RZ/G3S support information Update hardware specification table
1.03	Dec. 19, 2025	—	Add RZ/V2H support information
1.04	Mar. 27, 2026	4	Update product name for RZ/V2N EVK boards
		8-9	Update RZ/V2N devicetree setting.

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