

Linux Interface Specification Device Driver GTM and CMTW

User's Manual: Software

RZ/G2L Group, RZ/V2L Group, RZ/G3S Group,
RZ/G3E Group, RZ/V2H Group, RZ/V2N Group
and RZ/Five Group

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MPU. It is intended for users designing application systems incorporating the MPU.. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary in order to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group and RZ/G3S Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	RZ/G2L Group User's Manual: Hardware	---
		RZ/V2L Group User's Manual: Hardware	---
		RZ/Five Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
		RZ/G3E Group User's Manual: Hardware	---
		RZ/G3S Group User's Manual: Hardware	---
User's manual for Software	Description of GTM and CMTW's Linux Interface Specification	Linux Interface Specification Device Driver GTM and CMTW	This user's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
GTM	General Timer
ELC	Event link controller
CMTW	Compare match timer W

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1. Overview

1.1 Overview

This manual explains the driver module that controls the GTM(OSTM) and CMTW Controller on RZ/G2L Group, RZ/V2L Group, RZ/V2N Group, RZ/V2H Group, RZ/G3E Group, RZ/Five Group and RZ/G3S Group.

Note: Currently, this device is supported in two kernel versions v5.10 and v6.1 with the information below:

- v5.10: RZ/G2L Group, RZ/V2L Group, RZ/Five Group, RZ/V2N Group and RZ/G3S Group.
- v6.1: RZ/G2L Group, RZ/V2L Group, RZ/G3E Group, RZ/V2H Group, RZ/V2N Group, RZ/Five Group and RZ/G3S Group.

Note: CMTW only support in kernel v6.1 on board RZ/V2N, RZ/V2H and RZ/G3E.

1.2 Function

GTM modules:

- 8 channels support (RZ/V2N, RZ/V2H, RZ/G3E, RZ/G3S), 3 channels support (RZ/G2L group, RZ/V2L, RZ/Five)
- 32-bit counter
- Two operating modes:
 - Internal timer mode
 - Free-running comparison mode

CMTW modules (only support RZ/V2N, RZ/V2H, RZ/G3E):

- 8 channels support
- 32-bit counter
- Generate interrupts each time a set period elapses

1.3 Reference

1.3.1 Standard

There is no reference document on standards.

1.3.2 Related documents

There is no document related to this kernel.

1.4 Restrictions

None.

2. Terminology

The following table shows the terminology related to this kernel.

Table 2-1 Terminology

Terms	Explanation
GTM	General timer
CMTW	Compare Match Timer W

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this kernel.

Table 3-1 Hardware specification

Name	Product number
RZ/G2L Evaluation Board Kit	RTK9744L23S01000BE
RZ/G2LC Evaluation Board Kit	RTK9744C22S01000BE
RZ/G2UL Evaluation Board Kit	RTK9743U11S01000BE
RZ/V2L Evaluation Board Kit	RTK9754L23S01000BE
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/G3S Evaluation Board Kit	RTK9845S33C01000BE
RZ/G3E Evaluation Board Kit	RTK9947E57S01000BE
RZ/Five Evaluation Board Kit	RTK9743F01S01000BE

3.2 Module Configuration

The following figure shows the configuration of module GTM.

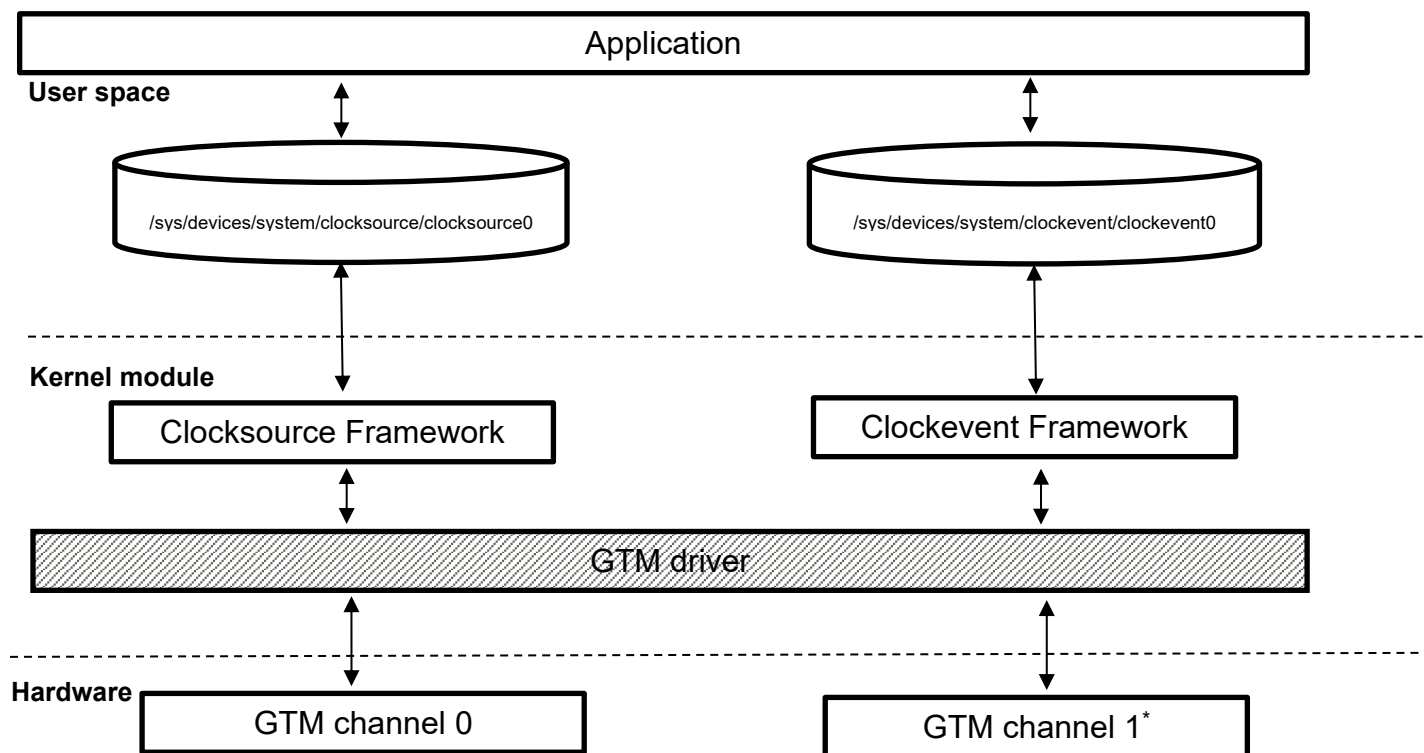


Figure 3-1 GTM Driver Module configuration

*: other channels maybe also selected as clock event

Note: GTM channel 0 is automatically selected for clocksource, schedule clock while other channels are chosen for clock events. However, cpuidle support for testing clock events has not been implemented.

The following figure shows the configuration of module CMTW

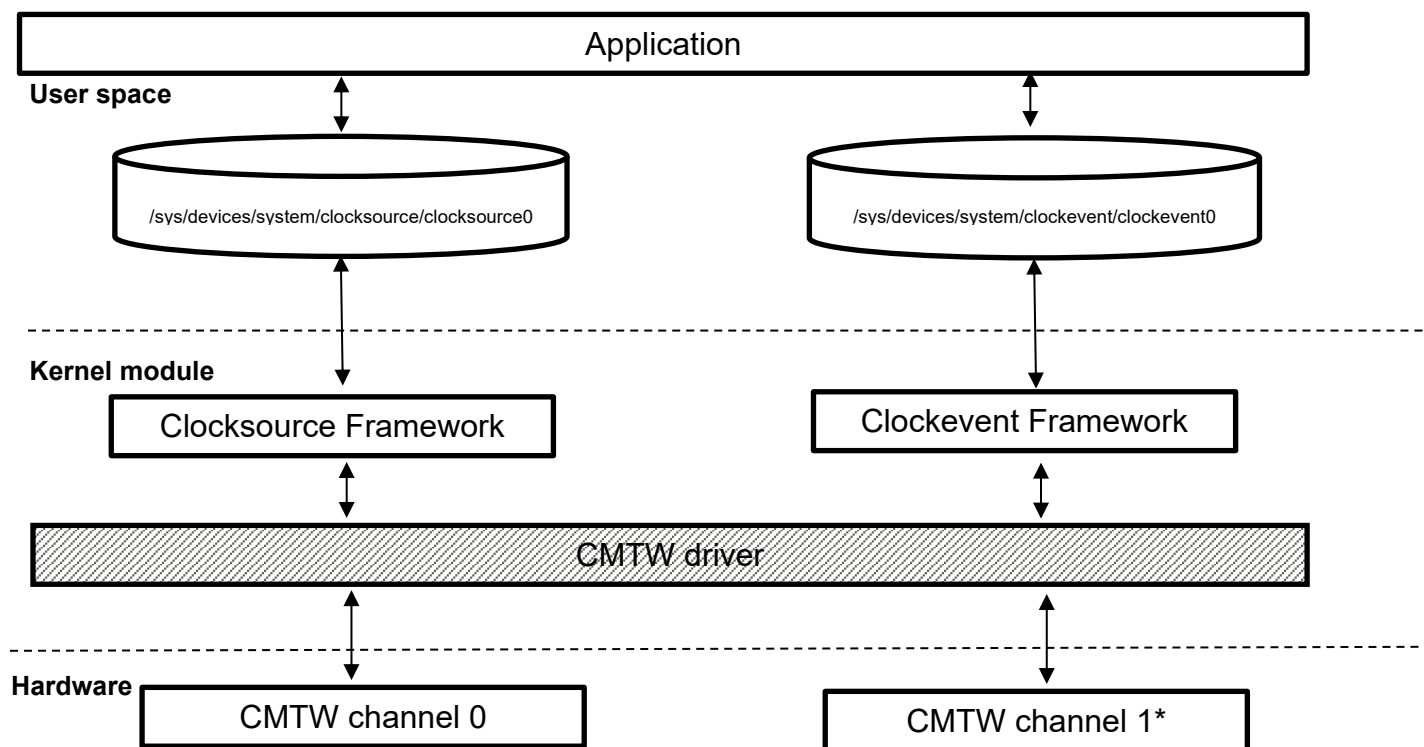


Figure 3-2 CMTW Driver Module configuration (RZ/G3E, RZ/V2H, RZ/V2N Group)

*: other channels maybe also selected as clock event

Note: CMTW channel 0 is automatically selected for clocksource, while other channels are chosen for clock events. However, cpuidle support for testing clock events has not been implemented.

4. External Interface

The supported external interface of this module is explained.

4.1 Device modes

GTM support up to:

- 3 timer channels from GTM channel 0 to channel 2 with RZ/G2L group, RZ/V2L, RZ/Five.
- 8 timer channels from GTM channel 0 to channel 7 with RZ/G3E, RZ/V2H, RZ/V2N and RZ/G3S.

User can configure them for clock source and clock event functionalities through device tree configuration and the sysfs interface.

Table 4-1 GTM device node

GTM channels	Device Node
GTM ch0	/sys/devices/system/clocksource/clocksource0

CMTW support up to 8 timer channels (4 channels × 2 units) with RZ/G3E, RZ/V2H, RZ/V2N. User can configure them for clock source and clock event functionalities through device tree configuration and the sysfs interface

Table 4-2 CMTW device node RZ/V2N, RZ/V2H and RZ/G3E

CMTW channels	Device Node
CMTW0 ch0	/sys/devices/system/clocksource/clocksource0
CMTW1 ch0	/sys/devices/system/clocksource/clocksource0

4.2 Linux interface

4.2.1 Clocksource and clockevent interface

This figure shows an example to use clocksource on userspace.

```
- To check available devices for clocksource function:
# cat /sys/devices/system/clocksource/clocksource0/available_clocksource
arch_sys_counter timer@11801000 11c01800.timer 13000c00.timer

- To set OSTM as clocksource:
# echo timer@11800000 > /sys/devices/system/clocksource/clocksource0/current_clocksource
[ 495.141173] clocksource: Switched to clocksource timer@11800000

- To Check current clocksource:
# cat /sys/devices/system/clocksource/clocksource0/current_clocksource
timer@11800000

- To set CMTW Ch0 as clocksource:
# echo 11c01800.timer > /sys/devices/system/clocksource/clocksource0/current_clocksource
[ 117.478914] clocksource: Switched to clocksource 11c01800.timer

- To Check current clocksource:
# cat /sys/devices/system/clocksource/clocksource0/current_clocksource
11c01800.timer

- To set CMTW Ch1 as clocksource:
# echo 13000c00.timer > /sys/devices/system/clocksource/clocksource0/current_clocksource
[ 128.514886] clocksource: Switched to clocksource 13000c00.timer

- To Check current clocksource:
# cat /sys/devices/system/clocksource/clocksource0/current_clocksource
13000c00.timer
```

Figure 4-1 Example of clocksource usage

4.3 Definitions

4.3.1 Device information in Device Tree

GTM device properties are shown as below of RZ/G2L group, RZ/V2L and RZ/Five

```

ostm0: timer@12801000 {
    compatible = "renesas,r9a07g044-ostm",
                "renesas,ostm";
    reg = <0x0 0x12801000 0x0 0x400>;
    interrupts = <GIC_SPI 46 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A07G044_OSTM0_PCLK>;
    resets = <&cpg R9A07G044_OSTM0_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};
ostm1: timer@12801400 {
    compatible = "renesas,r9a07g044-ostm",
                "renesas,ostm";
    reg = <0x0 0x12801400 0x0 0x400>;
    interrupts = <GIC_SPI 47 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A07G044_OSTM1_PCLK>;
    resets = <&cpg R9A07G044_OSTM1_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};
ostm2: timer@12801800 {
    compatible = "renesas,r9a07g044-ostm",
                "renesas,ostm";
    reg = <0x0 0x12801800 0x0 0x400>;
    interrupts = <GIC_SPI 48 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A07G044_OSTM2_PCLK>;
    resets = <&cpg R9A07G044_OSTM2_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 4-2 Configuration example of GTM's required properties (RZ/G2L group, RZ/V2L, RZ/Five)

Required properties:

- **compatible:**
must be "renesas,r9a07g044-ostm" for RZ/G2L, RZ/G2LC, RZ/V2L.
must be "renesas,r9a07g043-ostm" for RZ/G2UL, RZ/Five..
- **reg:**
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- **interrupts:**
must be " GIC_SPI 46 IRQ_TYPE_EDGE_RISING " for RZ/G2L, RZ/G2LC, RZ/V2L.
must be " SOC_PERIPHERAL_IRQ(46) IRQ_TYPE_EDGE_RISING " for RZ/G2UL, RZ/Five.
- **clocks, resets:**
must be " R9A07G044_OSTM0_PCLK" and "R9A07G044_OSTM0_PRESETZ" for RZ/G2L, RZ/G2LC, RZ/V2L.
must be " R9A07G043_OSTM0_PCLK" and "R9A07G043_OSTM0_PRESETZ" for RZ/G2UL, RZ/Five.
- **power-domains:**
specify the power-domain for GTM.

GTM device properties are shown as below of RZ/V2N, RZ/V2H and RZ/G3E.

```

ostm0: timer@11800000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x11800000 0x0 0x1000>;
    interrupts = <GIC_SPI 17 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x43>;
    resets = <&cpg 0x6d>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm1: timer@11801000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x11801000 0x0 0x1000>;
    interrupts = <GIC_SPI 18 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x44>;
    resets = <&cpg 0x6e>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm2: timer@14000000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x14000000 0x0 0x1000>;
    interrupts = <GIC_SPI 19 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x45>;
    resets = <&cpg 0x6f>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm3: timer@14001000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x14001000 0x0 0x1000>;
    interrupts = <GIC_SPI 20 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x46>;
    resets = <&cpg 0x70>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm4: timer@12c00000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x12c00000 0x0 0x1000>;
    interrupts = <GIC_SPI 21 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x47>;
    resets = <&cpg 0x71>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm5: timer@12c01000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x12c01000 0x0 0x1000>;
    interrupts = <GIC_SPI 22 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x48>;
    resets = <&cpg 0x72>;
    power-domains = <&cpg>;
    status = "disabled";
};

```



```

ostm6: timer@12c02000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x12c02000 0x0 0x1000>;
    interrupts = <GIC_SPI 23 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x49>;
    resets = <&cpg 0x73>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm7: timer@12c03000 {
    compatible = "renesas,r9a09g056-ostm", "renesas,ostm";
    reg = <0x0 0x12c03000 0x0 0x1000>;
    interrupts = <GIC_SPI 24 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x4a>;
    resets = <&cpg 0x74>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 4-3 Configuration example of GTM's required properties(RZ/V2N, RZ/V2H, RZ/G3E)

.Note: All of the information in above device tree is used for RZ/V2N, RZ/V2H and RZ/G3E except the compatible.

Required properties:

- compatible:
must be "renesas,r9a09g056-ostm" for RZ/V2N.
must be "renesas,r9a09g057-ostm" for RZ/V2H.
must be "renesas,r9a09g047-ostm" for RZ/G3E.
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
interrupt specifier for GTM.
- clocks, resets:
phandle and clock/reset specifier pairs for RZ/V2N, RZ/V2H and RZ/G3E.
- power-domains:
specify the power-domain for GTM.

GTM device properties are shown as below of RZ/G3S.

```

ostm0: timer@12801000 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";
    reg = <0x0 0x12801000 0x0 0x400>;
    interrupts = <GIC_SPI 44 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_OSTM0_PCLK>;
    resets = <&cpg R9A08G045_OSTM0_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm1: timer@12801400 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";
    reg = <0x0 0x12801400 0x0 0x400>;
    interrupts = <GIC_SPI 45 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_OSTM1_PCLK>;
    resets = <&cpg R9A08G045_OSTM1_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm2: timer@12801800 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";
    reg = <0x0 0x12801800 0x0 0x400>;
    interrupts = <GIC_SPI 46 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_OSTM2_PCLK>;
    resets = <&cpg R9A08G045_OSTM2_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm3: timer@12801c00 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";
    reg = <0x0 0x12801c00 0x0 0x400>;
    interrupts = <GIC_SPI 47 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_OSTM3_PCLK>;
    resets = <&cpg R9A08G045_OSTM3_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm4: timer@12802000 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";
    reg = <0x0 0x12802000 0x0 0x400>;
    interrupts = <GIC_SPI 48 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD R9A08G045_OSTM4_PCLK>;
    resets = <&cpg R9A08G045_OSTM4_PRESETZ>;
    power-domains = <&cpg>;
    status = "disabled";
};

ostm5: timer@12802400 {
    compatible = "renesas,r9a08g045-ostm",
        "renesas,ostm";

```

```

        reg = <0x0 0x12802400 0x0 0x400>;
        interrupts = <GIC_SPI 49 IRQ_TYPE_EDGE_RISING>;
        clocks = <&cpg CPG_MOD R9A08G045_OSTM5_PCLK>;
        resets = <&cpg R9A08G045_OSTM5_PRESETZ>;
        power-domains = <&cpg>;
    };

    ostm6: timer@12802800 {
        compatible = "renesas,r9a08g045-ostm",
            "renesas,ostm";
        reg = <0x0 0x12802800 0x0 0x400>;
        interrupts = <GIC_SPI 50 IRQ_TYPE_EDGE_RISING>;
        clocks = <&cpg CPG_MOD R9A08G045_OSTM6_PCLK>;
        resets = <&cpg R9A08G045_OSTM6_PRESETZ>;
        power-domains = <&cpg>;
        status = "disabled";
    };

    ostm7: timer@12802c00 {
        compatible = "renesas,r9a08g045-ostm",
            "renesas,ostm";
        reg = <0x0 0x12802c00 0x0 0x400>;
        interrupts = <GIC_SPI 51 IRQ_TYPE_EDGE_RISING>;
        clocks = <&cpg CPG_MOD R9A08G045_OSTM7_PCLK>;
        resets = <&cpg R9A08G045_OSTM7_PRESETZ>;
        power-domains = <&cpg>;
        status = "disabled";
    };

```

Figure 4-4 Configuration example of GTM's required properties (RZ/G3S)

Required properties:

- compatible:
must be "renesas,r9a08g045-ostm" for RZ/G3S.
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
must be "GIC_SPI 44 IRQ_TYPE_EDGE_RISING" for RZ/G3S.
- clocks, resets:
must be "R9A08G045_OSTM0_PCLK" and "R9A08G045_OSTM0_PRESETZ" for RZ/G3S.
- power-domains:
specify the power-domain for GTM.

CMTW device properties are shown as below of RZ/V2N and RZ/V2H.

```

cmtw0: timer@11C01800 {
    compatible = "renesas,rzv2n-cmtw";
    reg = <0 0x11C01800 0 0x1000>;
    interrupts = <GIC_SPI 455 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 456 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 457 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 458 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x3b>, <&cpg CPG_MOD 0x3c>,
            <&cpg CPG_MOD 0x3d>, <&cpg CPG_MOD 0x3e>;
    clock-names = "fck0", "fck1", "fck2", "fck3";
    resets = <&cpg 0x65>, <&cpg 0x66>,
            <&cpg 0x67>, <&cpg 0x68>;
    power-domains = <&cpg>;
    status = "disabled";
};

cmtw1: timer@13000C00 {
    compatible = "renesas,rzv2n-cmtw";
    reg = <0 0x13000C00 0 0x1000>;
    interrupts = <GIC_SPI 459 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 460 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 461 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 462 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x3f>, <&cpg CPG_MOD 0x40>,
            <&cpg CPG_MOD 0x41>, <&cpg CPG_MOD 0x42>;
    clock-names = "fck0", "fck1", "fck2", "fck3";
    resets = <&cpg 0x69>, <&cpg 0x6a>,
            <&cpg 0x6b>, <&cpg 0x6c>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 4-5 Configuration example of CMTW's required properties(RZ/V2N, RZ/V2H)

Required properties:

- compatible:
must be "renesas,rzv2n-cmtw".
must be "renesas,rzv2h-cmtw".
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
interrupt specifier for CMTW.
- clocks, resets:
phandle and clock/reset specifier pairs for RZ/V2N, RZ/V2H.
- power-domains:
specify the power-domain for CMTW.

CMTW device properties are shown as below of RZ/G3E.

```

cmtw0: timer@11C01800 {
    compatible = "renesas,rzg3e-cmtw";
    reg = <0 0x11C01800 0 0x1000>;
    interrupts = <GIC_SPI 455 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 456 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 457 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 458 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 59>, <&cpg CPG_MOD 0x60>,
            <&cpg CPG_MOD 0x61>, <&cpg CPG_MOD 0x62>;
    clock-names = "fck0", "fck1", "fck2", "fck3";
    resets = <&cpg 0x101>, <&cpg 0x102>,
            <&cpg 0x103>, <&cpg 0x104>;
    power-domains = <&cpg>;
    status = "disabled";
};

cmtw1: timer@13000C00 {
    compatible = "renesas,rzg3e-cmtw";
    reg = <0 0x13000C00 0 0x1000>;
    interrupts = <GIC_SPI 459 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 460 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 461 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 462 IRQ_TYPE_EDGE_RISING>;
    clocks = <&cpg CPG_MOD 0x63>, <&cpg CPG_MOD 0x64>,
            <&cpg CPG_MOD 0x65>, <&cpg CPG_MOD 0x66>;
    clock-names = "fck0", "fck1", "fck2", "fck3";
    resets = <&cpg 0x105>, <&cpg 0x106>,
            <&cpg 0x107>, <&cpg 0x108>;
    power-domains = <&cpg>;
    status = "disabled";
};

```

Figure 4-6 Configuration example of CMTW's required properties(RZ/G3E)

Required properties:

- compatible:
must be "renesas,rzg3e-cmtw".
- reg:
need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.
- interrupts:
interrupt specifier for CMTW.
- clocks, resets:
phandle and clock/reset specifier pairs for RZ/G3E.
- power-domains:
specify the power-domain for CMTW.

5. Integration

5.1 Directory Configuration

The directory configuration is shown below.

—— drivers/clocksource/	—— renesas-ostm.c	: GTM Driver source file
—— drivers/clocksource/	—— rz_cmtw.c	: CMTW Driver source file

Figure 5-1 Directory configuration

5.2 Integration Procedure

To enable the function of this module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  [*] Clock Source drivers --->
    <*> Renesas OSTM timer driver
```

Figure 5-2 Kernel configuration for OSTM

```
Device Drivers --->
  [*] Clock Source drivers --->
    <*> Renesas CMTW timer driver
```

Figure 5-3 Kernel configuration for CMTW

5.3 Option Setting

5.3.1 Module Parameters

There are no module parameters.

5.3.2 Kernel Parameters

There are no kernel parameters.

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Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2025	—	First Edition issued
1.01	Jul. 22, 2025	—	Add RZ/G3E support information
1.02	Nov. 28, 2025	—	Add RZ/G2L series, RZ/V2L, RZ/Five support information Add RZ/G3S support information
1.03	Dec. 19, 2025	—	Add RZ/V2H support information
1.04	Mar. 27, 2026	3	Update product number for RZ/V2N EVK boards
		7	Add CMTW clocksource usage.

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