

# Linux Interface Specification Device Driver RSCI

User's Manual: Software

RZ/G3E Group, RZ/V2N Group and RZ/V2H Group

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## General Precautions in the Handling of Micro processing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Micro processing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a micro processing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# How to Use This Manual

## 1. Purpose and Target Readers

This document is designed to provide the user with an understanding of the software development environment for RZ/G3E Group and RZ/V2H Group processors. It is intended for users developing software incorporating the processors. A basic knowledge of software development and Linux systems is necessary to use this document.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/G3E Group, RZ/V2N Group and RZ/V2H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description  Note: Refer to the application notes for details on using peripheral functions.	RZ/G3E Group User's Manual: Hardware	---
		RZ/V2N Group User's Manual: Hardware	---
		RZ/V2H Group User's Manual: Hardware	---
User's manual for Software	Software specifications (basic function of Linux kernel, memory maps, interrupt, clock, pins mux, device tree)	Linux interface Specification - Device Driver RSCI	This User's manual
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

3. Register Notation

#### 4. List of Abbreviations and Acronyms

Abbreviation	Full Form
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
Hi-Z	High Impedance
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase Locked Loop
UART	Universal Asynchronous Receiver-Transmitter
I2C	Inter-Integrated Circuit
SPI	Serial Peripheral Interface

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## 1. Overview

### 1.1 Overview

This manual explains the driver module that controls the RSCI (Renesas Serial Communications Interface) module on RZ/G3E Group, RZ/V2N Group and V2H Group.

**Note:** Currently, the devices that support this function are RZ/G3E Group, RZ/V2N Group and RZ/V2H Group.

### 1.2 Function

This module control is configurable to 3 interfaces:

- Asynchronous Communications Interface (UART).
- Simple I2C (master-only).
- Simple SPI.

#### 1.2.1 Asynchronous Communications Interface (UART)

- Number of channels: 10
- Data transmission and reception for RS232C.
- Control of communication settings
  - Baud rate 9600, 19200, 38400, 57600, 115200[bps], up to 3M[bps].
  - Parity bit (none/ODD/EVEN).
  - Stop bit (1bit or 2bit).
  - Data transfer bit length (7bit or 8bit).
- Each setting can be changed from the standard ioctl for tty.

#### 1.2.2 Simple I2C (master-only)

- Number of channels: 10.
- Driver functions:
  - Master-only mode.
  - Support transfer with 7-bit address.
  - Transfer rate: Up to 400[kbps].

#### 1.2.3 Simple SPI

- Number of channels: 10.
- Driver functions:
  - SPI transfer functions.



- Data format 8-bits
- Bit rate from 500Kbps to 25Mbps
- Buffer configuration.
- Support both master and slave modes.
- Interrupt sources.
- Loop back mode.
- PIO mode when data transmitted is less than 32 bytes.
- DMA mode when data transmitted is greater than 32 bytes.

## 1.3 Connected Port

### 1.3.1 Asynchronous Communications Interface (UART)

#### 1.3.1.1 RZ/G3E Board

- Table 1-1 describes port connected to UART function on the RZ/G3E SMARC Evaluation Board Kit.
- The sci2 channel is enabled when SW\_SER0\_PMOD=1 and SW\_SER2\_EN=0 in device tree.
- The sci4 channel is enabled when SW\_LCD\_EN=0 and SW\_SER0\_PMOD=1 in device tree.
- The sci9 channel is enabled when RSCI9\_SEL=0 and SW\_LCD\_EN=0 in device tree.

**Table 1-1 Connected port to UART (RZ/G3E Group) SMARC Evaluation Board Kit**

Channel	Connector	Support status	Remark
SCI0	–	No	–
SCI1	–	No	–
SCI2	SMARC module: CN4, SW4 SMARC Carrier-II: SW_OPT_MUX	Yes	Output as M2_KEY_E
SCI3	–	No	–
SCI4	SMARC module: CN4 SMARC Carrier-II: SW_OPT_MUX	Yes	Output as PMOD1_3A
SCI5	–	No	–
SCI6	–	No	–
SCI7	–	No	–
SCI8	–	No	–
SCI9	SMARC module: CN4, SW4	Yes	Output as SER1_UART

#### 1.3.1.2 RZ/V2H Boards

- Table 1-2 describes port connected to UART function on RZ/V2H-EVK-VER1/VER2 Boards.

**Table 1-2 Connected port to UART (RZ/V2H Group)**

Channel	Connector	Support status	Remark
SCI0	–	No	–
SCI1	–	No	–
SCI2	–	No	–
SCI3	–	No	–
SCI4	GP-EVK EXPANSION BOARD: CN1	Yes	–
SCI5	GP-EVK EXPANSION BOARD: CN1	Yes	–
SCI6	–	No	–
SCI7	–	No	–
SCI8	–	No	–
SCI9	GP-EVK EXPANSION BOARD: CN2	Yes	–

### 1.3.1.3 RZ/V2N Boards

- Table 1-23 describes port connected to UART function on RZ/V2N-EVK Boards.

**Table 1-3 Connected port to UART (RZ/V2N Group)**

Channel	Connector	Support status	Remark
SCI0	GP-EVK EXPANSION BOARD: CN3	Yes	–
SCI1	–	No	–
SCI2	–	No	–
SCI3	–	No	–
SCI4	GP-EVK EXPANSION BOARD: CN1	Yes	–
SCI5	GP-EVK EXPANSION BOARD: CN1	Yes	–
SCI6	–	No	–
SCI7	–	No	–
SCI8	–	No	–
SCI9	GP-EVK EXPANSION BOARD: CN2	Yes	–

### 1.3.2 Simple I2C (master-only)

#### 1.3.2.1 RZ/G3E Board

- Table 1-44 describes port connected to I2C function on the RZ/G3E SMARC Evaluation Board Kit.
- The rsci\_i2c9 channel is enabled when RSCI9\_SEL=1 in device tree

**Table 1-4 Connected port to I2C (RZ/G3E Group) SMARC Evaluation Board Kit**

Channel	Connector	Support status	Remark
rsci_i2c0	—	No	—
rsci_i2c1	—	No	—
rsci_i2c2	—	No	—
rsci_i2c3	—	No	—
rsci_i2c4	—	No	—
rsci_i2c5	—	No	—
rsci_i2c6	—	No	—
rsci_i2c7	—	No	—
rsci_i2c8	—	No	—
rsci_i2c9	SMARC module: CN4, SW4 SMARC Carrier-II: SW_M2_DIS	Yes	Output as PMOD1_6A

#### 1.3.2.2 RZ/V2H Boards

- Table 1-55 describes port connected to I2C function on RZ/V2H-EVK-VER1/VER2 Boards.

**Table 1-5 Connected port to I2C (RZ/V2H Group)**

Channel	Connector	Support status	Remark
rsci_i2c0	—	No	—
rsci_i2c1	—	No	—
rsci_i2c2	—	No	—
rsci_i2c3	—	No	—
rsci_i2c4	—	No	—
rsci_i2c5	GP-EVK EXPANSION BOARD: CN1	Yes	—
rsci_i2c6	—	No	—
rsci_i2c7	—	No	—
rsci_i2c8	—	No	—
rsci_i2c9	GP-EVK EXPANSION BOARD: CN2	Yes	—

### 1.3.2.3 RZ/V2N Boards

- Table 1-56 describes port connected to I2C function on RZ/V2N-EVK Boards.

**Table 1-6 Connected port to I2C (RZ/V2N Group)**

Channel	Connector	Support status	Remark
rsci_i2c0	GP-EVK EXPANSION BOARD: CN3	Yes	—
rsci_i2c1	—	No	—
rsci_i2c2	—	No	—
rsci_i2c3	—	No	—
rsci_i2c4	GP-EVK EXPANSION BOARD: CN1	Yes	—
rsci_i2c5	GP-EVK EXPANSION BOARD: CN1	Yes	—
rsci_i2c6	—	No	—
rsci_i2c7	—	No	—
rsci_i2c8	—	No	—
rsci_i2c9	GP-EVK EXPANSION BOARD: CN2	Yes	—

### 1.3.3 Simple SPI

#### 1.3.3.1 RZ/G3E Board

- Table 1-7 describes port connected to SPI function on the RZ/G3E SMARC Evaluation Board Kit.
- The rsci\_spi8 channel is enabled when RSPi0\_RSCI8\_SPI\_SEL=1 in device tree
- The rsci\_spi9 channel is enabled when RSCI9\_SEL=2 in device tree
- On RZ/G3E SMARC Evaluation Board Kit:
  - rsci\_spi8 channel output as PMOD0\_2A only supports a maximum speed of 12.5MHz. Moreover, PMOD0\_2A only supports master mode because TXU0304RUTR IC cannot support bidirectional transfer.
  - rsci\_spi9 channel can support a maximum speed of 25MHz with master or slave roles.

**Table 1-7 Connected port to SPI (RZ/G3E Group) SMARC Evaluation Board Kit**

Channel	Connector	Support status	Remark
rsci_spi0	—	No	—
rsci_spi1	—	No	—
rsci_spi2	—	No	—
rsci_spi3	—	No	—
rsci_spi4	—	No	—
rsci_spi5	—	No	—
rsci_spi6	—	No	—
rsci_spi7	—	No	—
rsci_spi8	SMARC module: CN4	Yes	Output as PMOD0_2A
rsci_spi9	SMARC module: CN4 SMARC Carrier-II: SW_M2_DIS	Yes	Output as PMOD0_2A and PMOD1_6A

### 1.3.3.2 RZ/V2H Boards

- Table 1-8 describes port connected to SPI function on RZ/V2H-EVK-VER1/VER2 Boards

**Table 1-8 Connected port to SPI (RZ/V2H Group)**

Channel	Connector	Support status	Remark
rsci_spi0	GP-EVK EXPANSION BOARD: CN3	Yes	—
rsci_spi1	—	No	—
rsci_spi2	—	No	—
rsci_spi3	—	No	—
rsci_spi4	—	No	—
rsci_spi5	—	No	—
rsci_spi6	—	No	—
rsci_spi7	—	No	—
rsci_spi8	—	No	—
rsci_spi9	GP-EVK EXPANSION BOARD: CN2	Yes	—

### 1.3.3.3 RZ/V2N Boards

- Table 1-9 describes port connected to SPI function on RZ/V2N-EVK Boards

**Table 1-9 Connected port to SPI (RZ/V2N Group)**

Channel	Connector	Support status	Remark
rsci_spi0	GP-EVK EXPANSION BOARD: CN3	Yes	—
rsci_spi1	—	No	—
rsci_spi2	—	No	—
rsci_spi3	—	No	—
rsci_spi4	—	No	—
rsci_spi5	—	No	—
rsci_spi6	—	No	—
rsci_spi7	—	No	—
rsci_spi8	—	No	—
rsci_spi9	GP-EVK EXPANSION BOARD: CN2	Yes	—

## 1.4 Reference

### 1.4.1 Standard

There is no reference document on standards.

### 1.4.2 Related Documents

The following table shows the document related to this module.

**Table 1-10 Related documents**

Number	Issue	Title	Edition	Date
-	-	-	-	-

## 1.5 Restrictions

Only one mode can run in a time. No support mode switching in runtime.

## 1.6 Notice

### 1.6.1 Simple I2C (master-only)

- This module: Supports enable the rsci\_i2c9 of RZ/G3E SMARC Evaluation Board Kit.
- Master-only transfer support.
- In the interrupt sources, the receive data full, transmit end and transmit data empty sources are supported by driver.

### 1.6.2 Simple SPI

- Master/Slave transfer are both supported.
- Support communication with flash-spi (Pmod SF3).
- Support speed change when transferring.

## 2. Terminology

The following table shows the terminology related to this module.

**Table 2-1 Terminology**

<b>Terms</b>	<b>Explanation</b>
SCI	Serial Communications Interface
UART	Universal Asynchronous Receiver-Transmitter
Tx	Transmit
Rx	Receive
I2C	Inter-Integrated Circuit
SCL	Serial Clock
SDA	Serial Data
SPI	Serial Peripheral Interface
SSL	Slave Select
CS	Chip Select
MOSI	Master Out Slave In
MISO	Master In Slave Out



## 3. Operating Environment

### 3.1 Hardware Environment

The following table shows the hardware needed to use this module.

**Table 3-1 Hardware Environment**

<b>Name</b>	<b>Product number</b>
RZ/G3E SMARC Evaluation Board Kit	RTK9947E57S01000BE
RZ/V2H Evaluation Board Kit	RTK0EF0168C04000BJ
RZ/V2N Evaluation Board Kit V1.0	RTK0EF0186C03000BJ
RZ/V2N Evaluation Board Kit V2.0	RTK0EF0186C03001BJ

## 3.2 Module Configuration

### 3.2.1 Asynchronous Communications Interface (UART)

The following Figure 3-1 shows the configuration of serial module.

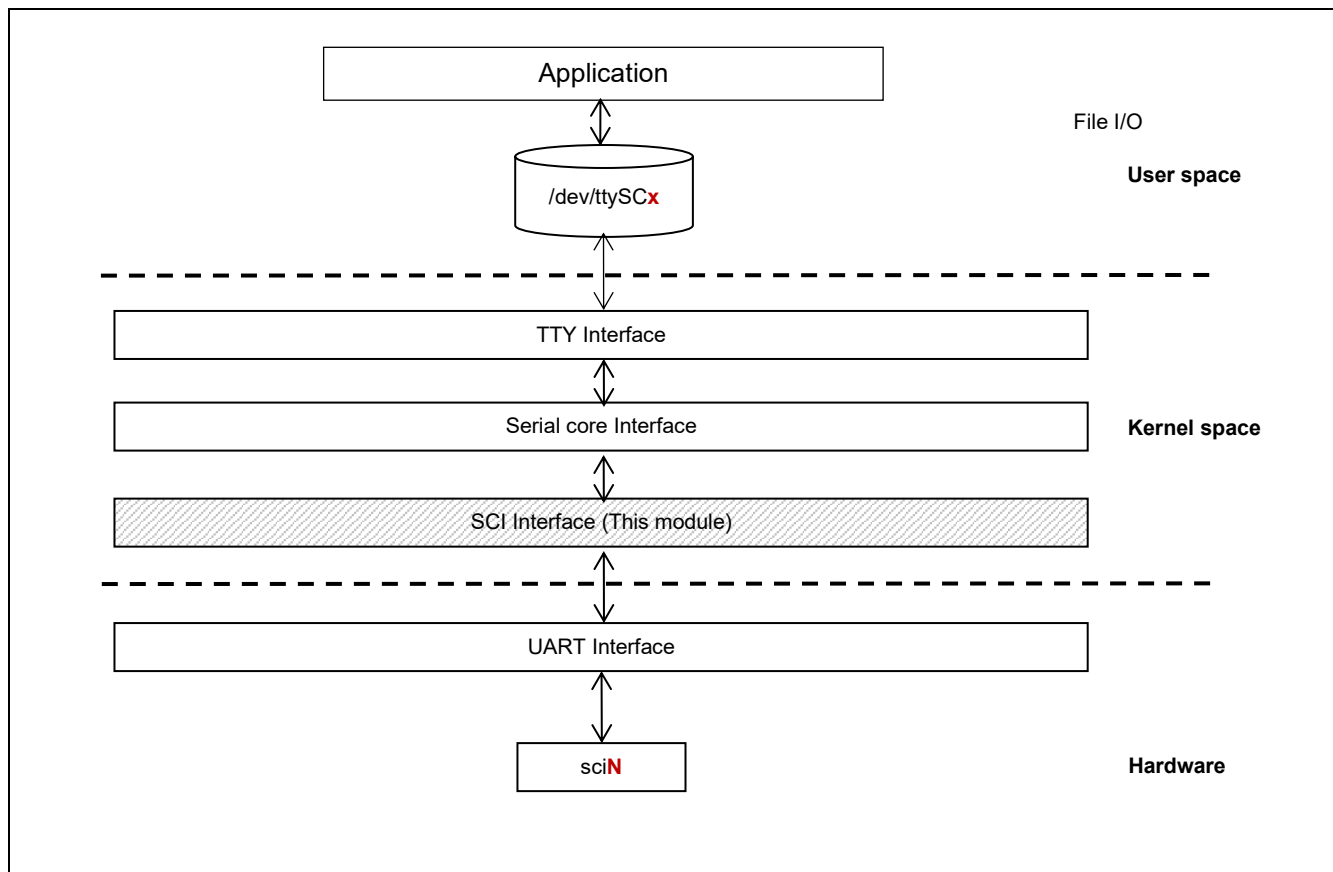


Figure 3-1 The UART from the user space to the hardware space

Note)

**x**: the serial device which enabled in device tree. (start: 1, 2, ...)

**N**: the number of sci channels (0, 1, 2, ..., 9)

### 3.2.2 Simple I2C (master-only)

The following Figure 3-2 shows the configuration of I2C module

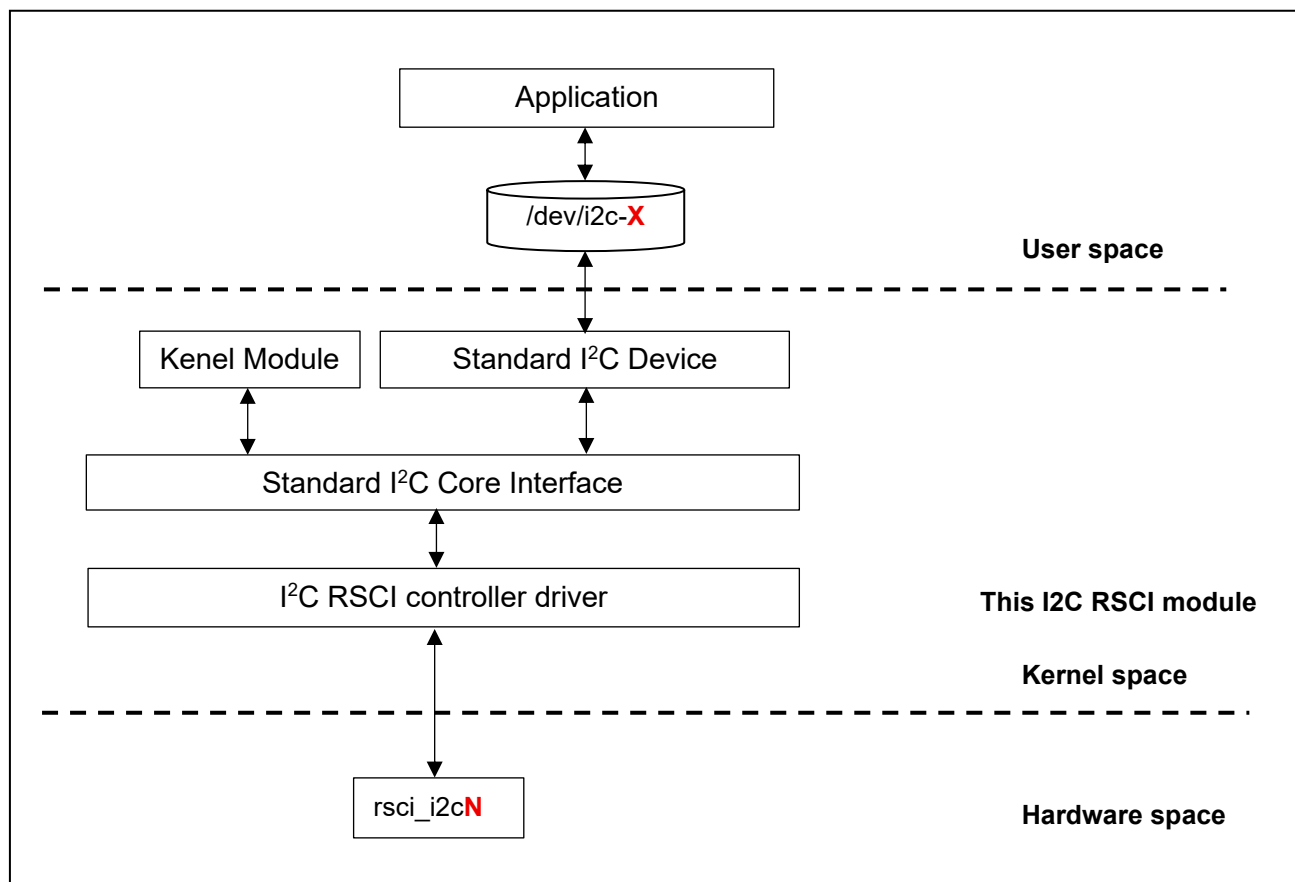


Figure 3-2 The I2C from the user space to the hardware space.

Note)

**X**: the I2C device number (start: 9, 10, 11, ...)

**N**: the number of rsci\_i2c channel. (0, 1, 2, ..., 9)

### 3.2.3 Simple SPI

The following Figure 3-3 shows the configuration of SPI module.

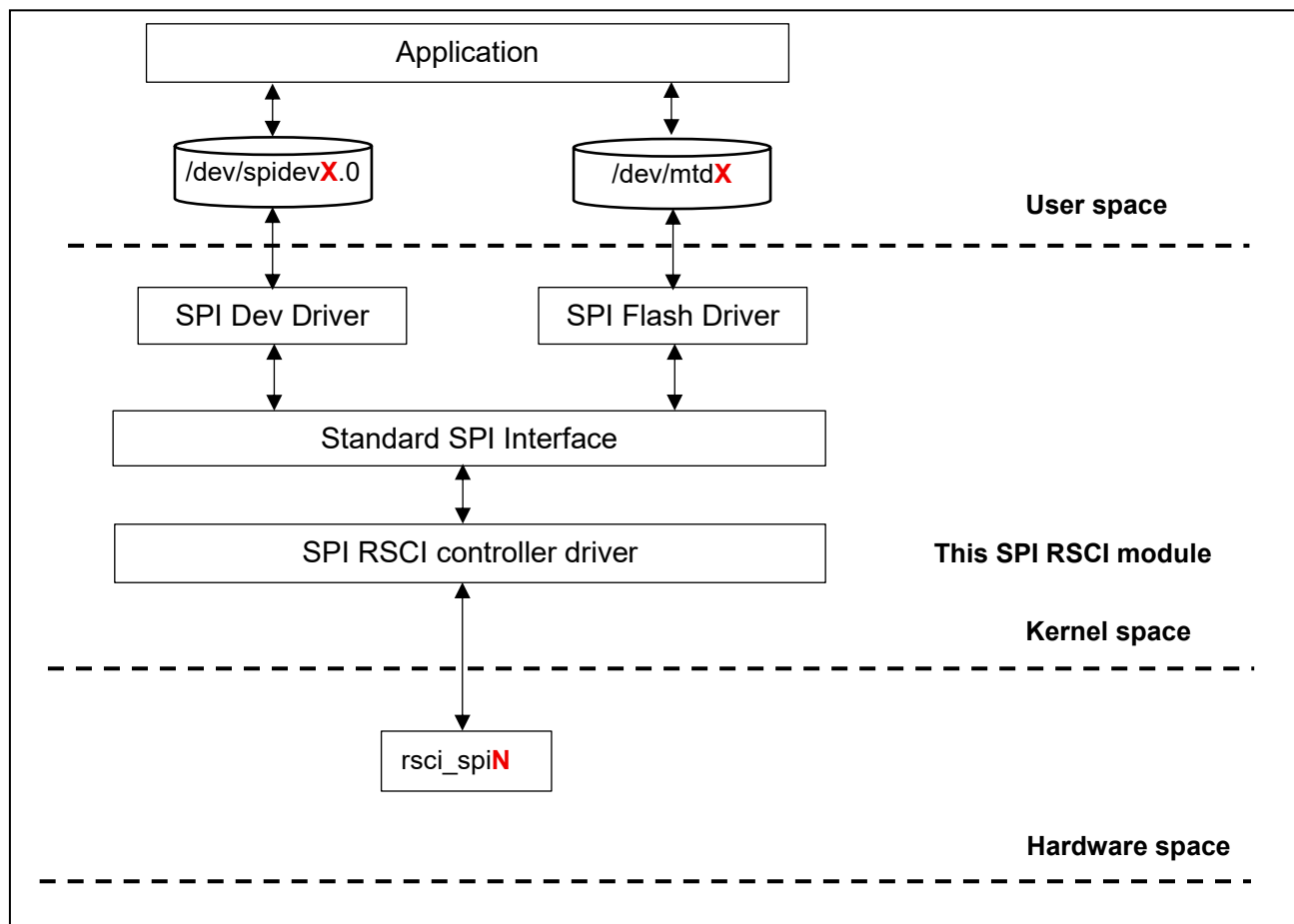


Figure 3-3 The SPI from the user space to the hardware space.

Note)

**X**: the SPI device number. (start: 0, 1, 2, ...)

For example: in case X=0,

- The /dev/spidev1.0 can be master or slave role if you configure the role in device tree.
- The /dev/mtd0 can communicate with flash device if you configure in device tree.

**N**: the number of rsci\_spi channel. (0, 1, 2, ..., 9)

## 3.3 State Transition Diagram

There is no state transition diagram for this module.

## 4. External Interface

### 4.1 Device Node

Device node of this module is shown below.

Table 4-1 Device Node (RZ/G3E Group, RZ/V2N Group and RZ/V2H Group)

Protocol	Device node	Remark
UART	/dev/ttySCx x: 1, 2, 3.	—
I2C	/dev/i2c-x x: 9, 10	—
SPI	/dev/spidev0.0 /dev/spidev1.0 /dev/mtd0	—

### 4.2 External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux

## 5. Integration

### 5.1 Directory Configuration

#### 5.1.1 Asynchronous Communications Interface (UART)

The directory configuration of UART is shown below.

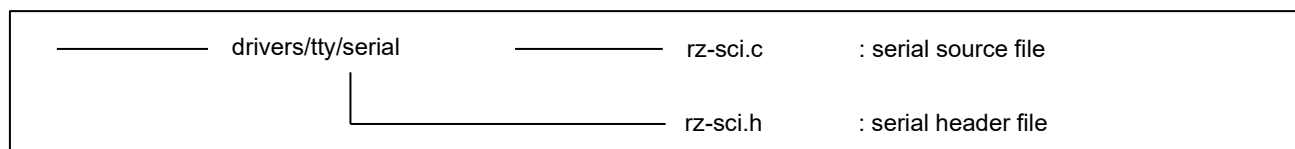


Figure 5-1 Directory Configuration of UART function

#### 5.1.2 Simple I2C (master-only)

The directory configuration of I2C is shown below.

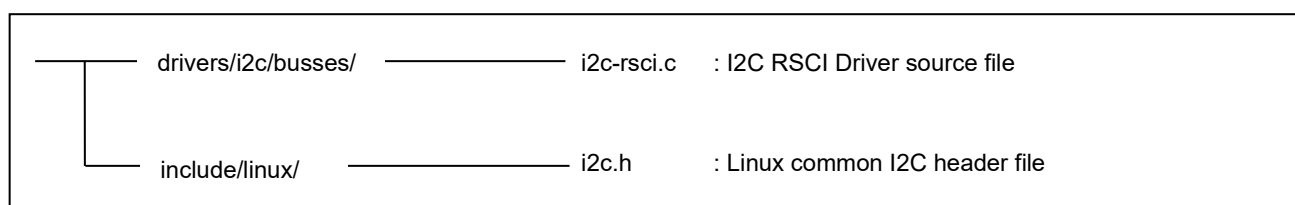


Figure 5-2 Directory Configuration of I2C function

#### 5.1.3 Simple SPI

The directory configuration of SPI is shown below.

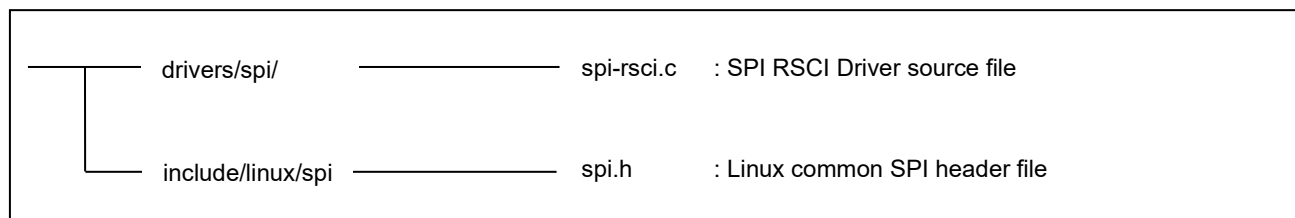


Figure 5-3 Directory Configuration of SPI function

## 5.2 Integration Procedure

### 5.2.1 Enable channel of RSCI module

#### 5.2.1.1 Asynchronous Communications Interface (UART)

##### (1) RZ/G3E Board

The following description explains how to enable sci2, sci4 and sci9 channel in RZ/G3E SMARC Evaluation Board Kit. (**supported on rz-6.1-cip28**)

**arch/arm64/boot/dts/renesas/rzg3e-smarc.dtsi**

```
aliases {  
  
    #if (!SW_LCD_EN)  
  
        serial1 = &sci4;  
  
    #if (RSCI9_SEL == RSCI_UART)  
  
        serial2 = &sci9;  
  
    #endif  
  
    #endif  
  
    #if ((SW_SER0_PMOD) && (!SW_SER2_EN))  
  
        serial3 = &sci2;  
  
    #endif  
  
};
```

**Figure 5-4 Aliases of sci channels on RZ/G3E SMARC**

- To enable sci2 channel. We need to set macro of SW\_SER2\_EN=0 and SW\_SER0\_PMOD=1. Additionally, we need to make sure that the corresponding switch on the board is correct.
- To enable sci4 channel. We need to set macro of SW\_LCD\_EN=0. Additionally, we need to make sure that the corresponding switch on the board is correct.
- To enable sci9 channel. We need to set macro of RSCI9\_SEL=0 and SW\_LCD\_EN=0. Additionally, we need to make sure that the corresponding switch on the board is correct.

For example, **Figure 5-5** enable 3 channels above.

**arch/arm64/boot/dts/renesas/r9a09g047e57-smarc.dts**

```
/* Switch selection settings */

#define SW_LCD_EN            0

#define SW_SER0_PMOD        1

#define SW_SER2_EN          0

#define RSCI9_SEL            0
```

**Figure 5-5 Enable SCI channels**

## (2) RZ/V2H Boards

The following description explains how to enable sci4, sci5 and sci5 channel in RZ/V2H Evaluation Board Kit. **(supported on rz-6.1-cip43)**

- To enable sci4 channel. Set macro of SEL\_CAN01\_HEADER=1 and SEL\_SCI4\_CAN01=1.
- To enable sci5 channel. Set macro of RSCI5\_SEL= RSCI\_UART.
- To enable sc9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_UART.

For example, **Figure 5-6** enable 3 channels above

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk.dts**

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk-ver2.dts**

```
/* Switch selection settings */

#define SEL_CAN01_HEADER      1

#define SEL_SCI4_CAN01       1

#define RSCI5_SEL             RSCI_UART

#define RSPI2_RSCI9_SEL       1

#define RSCI9_SEL             RSCI_UART
```

**Figure 5-6 Enable SCI channel (RZ/V2H-EVK-VER1/VER2)**



### (3) RZ/V2N Boards

The following description explains how to enable sci4, sci5 and sci5 channel in RZ/V2N Evaluation Board Kit. **(supported on rz-6.1-cip43)**

- To enable sci0 channel. Set macro of RSCI0\_SEL=RSCI\_UART.
- To enable sci4 channel. Set macro of CAN\_SPDIF\_SCI\_SEL=SCI\_SEL and RSCI4\_SEL=RSCI\_UART.
- To enable sci5 channel. Set macro of CAN\_SPDIF\_SCI\_SEL=SCI\_SEL and RSCI5\_SEL=RSCI\_UART.
- To enable sc9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_UART.

For example, **Figure 5-67** enable 4 channels above

**arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

```
/* Switch selection settings */  
  
#define CAN_SPDIF_SCI_SEL    SCI_SEL  
  
#define RSPI2_RSCI9_SEL      1  
  
#define RSCI0_SEL            RSCI_UART  
  
#define RSCI4_SEL            RSCI_UART  
  
#define RSCI5_SEL            RSCI_UART  
  
#define RSCI9_SEL            RSCI_UART
```

**Figure 5-7 Enable SCI channel (RZ/V2N-EVK)**

### 5.2.1.2 Simple I2C (master-only)

#### (1) RZ/G3E Board

The following description explains how to enable rsci\_i2c9 channel in RZ/G3E SMARC Evaluation Board Kit. (**supported on rz-6.1-cip28**)

- To enable rsci\_i2c9 channel. We need to set macro of RSCI9\_SEL=1 and SW\_LCD\_EN=0. Additionally, we need to make sure that the corresponding switch on the board is correct.

For example, **Figure 5-8** enable rsci\_i2c9 channel.

**arch/arm64/boot/dts/renesas/r9a09g047e57-smarc.dts**

```
/* Switch selection settings */
#define SW_LCD_EN            0
#define RSCI9_SEL            1
```

**Figure 5-8 Enable rsci\_i2c9 channel**

#### (2) RZ/V2H Boards

The following description explains how to enable rsci\_i2c5 and rsci\_i2c9 channel in RZ/V2H Evaluation Board Kit. (**supported on rz-6.1-cip43**)

- To enable rsci\_i2c5 channel. Set macro of RSCI5\_SEL= RSCI\_I2C.
- To enable rsci\_i2c9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_I2C.

For example, **Figure 5-9** enable channels

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk.dts**

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk-ver2.dts**

```
/* Switch selection settings */
#define RSCI5_SEL            RSCI_I2C
#define RSPI2_RSCI9_SEL      1
#define RSCI9_SEL            RSCI_I2C
```

**Figure 5-9 Enable rsci\_i2c channels (RZ/V2H-EVK-VER1/VER2)**

### (3) RZ/V2N Boards

The following description explains how to enable rsci\_i2c5 and rsci\_i2c9 channel in RZ/V2N Evaluation Board Kit. (**supported on rz-6.1-cip43**)

- To enable rsci\_i2c0 channel. Set macro of RSCI0\_SEL= RSCI\_I2C.
- To enable rsci\_i2c4 channel. Set macro of CAN\_SPDIF\_CAN\_SEL = SCI\_SEL and RSCI4\_SEL= RSCI\_I2C.
- To enable rsci\_i2c5 channel. Set macro of CAN\_SPDIF\_CAN\_SEL = SCI\_SEL and RSCI5\_SEL= RSCI\_I2C.
- To enable rsci\_i2c9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_I2C.

For example, **Figure 5--10** enable channels 4 channels above

**arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

```
/* Switch selection settings */  
  
#define CAN_SPDIF_SCI_SEL    SCI_SEL  
  
#define RSPI2_RSCI9_SEL      1  
  
#define RSCI0_SEL            RSCI_I2C  
  
#define RSCI4_SEL            RSCI_I2C  
  
#define RSCI5_SEL            RSCI_I2C  
  
#define RSCI9_SEL            RSCI_I2C
```

**Figure 5-10 Enable rsci\_i2c channels (RZ/V2N-EVK)**

### 5.2.1.3 Simple SPI

#### (1) RZ/G3E Board

The following description explains how to enable rsci\_spi8 and rsci\_spi9 channel in RZ/G3E SMARC Evaluation Board Kit. (**supported on rz-6.1-cip28**)

- To enable rsci\_spi8 channel. We need to set macro of RSPI0\_RSCI8\_SPI\_SEL=1. Additionally, we need to make sure that the corresponding switch on the board is correct.
- To enable rsci\_spi9 channel. We need to set macro of RSCI9\_SEL=2 and SW\_LCD\_EN=0. Additionally, we need to make sure that the corresponding switch on the board is correct.

For example, **Figure 5-11** enable rsci\_spi8 and rsci\_spi9 channels.

**arch/arm64/boot/dts/renesas/r9a09g047e57-smarc.dts**

```
/* Switch selection settings */
#define RSPI0_RSCI8_SPI_SEL      1
#define SW_LCD_EN                0
#define RSCI9_SEL                2
```

**Figure 5-11 Enable rsci\_spi channels**

#### (2) RZ/V2H Boards

The following description explains how to enable rsci\_spi0 and rsci\_spi9 channel in channel in RZ/V2H Evaluation Board Kit. (**supported on rz-6.1-cip43**)

- rsci\_spi0 channel was enabled (default)
- To enable rsci\_spi9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_SPI.

For example, **Figure 5-72** enable rsci\_spi0 and rsci\_spi9 channels

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk.dts**

**arch/arm64/boot/dts/renesas/r9a09g057h44-rzv2h-evk-ver2.dts**

```
/* Switch selection settings */
#define RSPI2_RSCI9_SEL          1
#define RSCI9_SEL                RSCI_SPI
```

**Figure 5-72 Enable rsci\_spi channels (RZ/V2H-EVK-VER1/VER2)**

#### (3) RZ/V2N Boards

The following description explains how to enable rsci\_spi0 and rsci\_spi9 channel in channel in RZ/V2N Evaluation Board Kit. (**supported on rz-6.1-cip43**)

- To enable rsci\_spi0 channel. Set macro of RSCI0\_SEL= RSCI\_SPI.
- To enable rsci\_spi9 channel. Set macro of RSPI2\_RSCI9\_SEL=1 and RSCI9\_SEL= RSCI\_SPI.

For example, **Figure 5-713** enable rsci\_spi0 and rsci\_spi9 channels

**arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

```
/* Switch selection settings */  
  
#define RSPi2_RSCI9_SEL          1  
  
#define RSCI0_SEL                RSCI_SPI  
  
#define RSCI9_SEL                RSCI_SPI
```

**Figure 5-83 Enable rsci\_spi channels (RZ/V2N-EVK)**

## 5.2.2 Enable function

### 5.2.2.1 Asynchronous Communications Interface (UART)

UART functions can work normally when we connect serial to this module through Tx and Rx pin.

#### (1) Kernel configuration settings

To enable the UART function of RSCI module, make the following setting with Kernel Configuration.

```
Device Drivers --->
  [*] Character devices --->
    Serial drivers --->
      <*> Renesas SCI serial port support
```

**Figure 5-94 Kernel configuration of UART function driver**

**Figure 5-105** lists the kernel config symbols to support UART function driver for RZ/G3E Group, RZ/V2N Group and RZ/V2H Group.

```
CONFIG_SERIAL_RZ_SCI=y
CONFIG_SERIAL_RZ_SCI_CONSOLE=y
```

**Figure 5-105 Kenel config symbols of UART function driver**

#### 5.2.2.2 Simple I2C (master-only)

The I2C function can work normally when we connect serial to this module through SCL and SDA pin.

#### (1) Kernel configuration settings

```
Device Drivers --->
  I2C support --->
    <*> I2C device interface
  I2C Hardware Bus support --->
    <*> Renesas RSCI I2C adapter
```

**Figure 5-116 Kernel configuration of I2C function driver**

**Figure 5-127** lists the kernel config symbols to support I2C function driver for RZ/G3E Group, RZ/V2N Group and RZ/V2H Group.

```
CONFIG_I2C_RSCI=y
```

**Figure 5-127 Kenel config symbols of I2C function driver**

### 5.2.2.3 Simple SPI

The SPI function can work normally when we connect serial to this module through MOSI, MISO, SCLK, and SSL/CS pin.

#### (1) Add User Space Interface

Add the compatible value of the Subnode to the file: drivers/spi/spidev.c

“maker name, slave device name”

```
static const struct spi_device_id spidev_spi_ids[] = {
    { .name = "slavedev" },
};
static const struct of_device_id spidev_dt_ids[] = {
    { .compatible = "maker,slavedev".data = &spidev_of_check},
    {}
};
```

← Add this line.

← Add this line.

Figure 5-138 Add slavedev compatible

#### (2) Add Subnode setting in device tree

##### (a) Master or Slave roles

Use the slave device name of the connection destination as the compatible value. The following form is ideal.  
“maker name, slave device name”.

Support transfer board to board through /dev/spidevX.0 on sysfs and spidev\_test tool.

After adding compatible above, we will add subnode to rsci\_spi node in device tree.

**Master mode:** adding content as below to rsci\_spi node in:

RZ/G3E SMARC: **arch/arm64/boot/dts/renesas/rzg3e-smarc.dtsi**

RZ/V2N-EVK: **arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

RZ/V2H-EVK-VER1/VER2: **arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi**

```
/* Add a subnode. */

    slavedev@0 {

        compatible = "maker,slavedev";

        reg = <0>;

        spi-max-frequency = <25000000>;

        spi-cpha;

        spi-cpol;

    };
```

Figure 5-19 The setting for master mode in rsci\_spi enable node

**Slave mode:** adding content as below to rsci\_spi node in:

RZ/G3E SMARC: **arch/arm64/boot/dts/renesas/rzg3e-smarc.dtsi**

RZ/V2N-EVK: **arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

RZ/V2H-EVK-VER1/VER2: **arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi**

```
spi-slave;

slave {
    compatible = "maker,slavedev";

    spi-cpha;

    spi-cpol;

};
```

**Figure 5-20** The setting for slave mode in rsci\_spi enables node



**(b) Connect to flash-SPI device**

Add Subnode of flash-spi device to rsci\_spi node in device tree.

For example, using Pmod SF3 connect to rsci\_spi pin. After adding Subnode as below:

RZ/G3E SMARC: **arch/arm64/boot/dts/renesas/rzg3e-smarc.dtsi**

RZ/V2N-EVK: **arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts**

RZ/V2H-EVK-VER1/VER2: **arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi**

```
flash0 {
    compatible = "micron,mt25ql256a","jedec,spi-nor";

    reg = <0>;

    spi-max-frequency = <12500000>; // => up to 25MHz

    spi-tx-bus-width = <1>;

    spi-rx-bus-width = <1>;

    m25p,fast-read;

    partitions {
        compatible = "fixed-partitions";

        #address-cells = <1>;

        #size-cells = <1>;

        partition@0000000 {
            label = "test-area0";

            reg = <0x00000000 0x00080000>;

        };

    };
};
```

**Figure 5-21 The setting for flash-spi device for rsci\_spi node**

### (3) Make spidev\_test tool

Steps to create **spidev\_test** tool are as below:

```
cd {CIP_WORK_DIR}/tools/spi$
source {SDK_DIR}/environment-setup-aarch64-poky-linux
{CIP_WORK_DIR}/tools/spi$ make
```

Figure 5-22 Step make spidev\_test tool

Then copy **spidev\_test** binary to rootfs. (Master or Slave Board).

**Note:** Please send the test command on Slave board before sending it on Master board.

### (4) Kernel configuration control

```
Device Drivers --->
    [*] SPI support --->
        <*> Renesas RSCI RZ/V2H controller
```

Figure 5-23 Kenel config symbols of SPI function driver

To use file system driver JFFS2, make the following setting with Kernel Configuration.

```
File Systems --->
    [*] Miscellaneous filesystems -->
        <*> Journaling Flash File System v2 (JFFS2) support
        [*] JFFS2 write-buffering support
```

Figure 5-24 File system configuration support for flash SPI

**Figure 5-5** lists the kernel config symbols to support SPI function driver for RZ/G3E Group, RZ/V2N Group and RZ/V2H Group

```
CONFIG_SPI_RZ_RSCI=y
```

Figure 5-25 Kenel config symbols of SPI function driver

Add the configuration to enable slave mode in: **arch/arm64/configs/defconfig**

```
CONFIG_SPI_SLAVE=y
```

Figure 5-26 Configuration support for slave mode

## 5.3 Device Tree Setting

### 5.3.1 SoC Device Tree

Basic configuration information of sci, rsci\_i2c, rsci\_spi node is defined at device tree:

RZ/G3E Group: **arch/arm64/boot/dts/renesas/r9a09g047.dtsi**

RZ/V2N Group: **arch/arm64/boot/dts/renesas/r9a09g056.dtsi**

RZ/V2H Group: **arch/arm64/boot/dts/renesas/r9a09g057.dtsi**

#### 5.3.1.1 Asynchronous Communications Interface (UART)

The initial reference information is shown below. An example here is sci9 channel

```
sci9: serial@12803000 {
    compatible = "renesas,r9a09g047-rz-rscif",
                "renesas,rz-rscif";

    reg = <0 0x12803000 0 0x400>;

    interrupts = <GIC_SPI 168 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 169 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 170 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 171 IRQ_TYPE_LEVEL_HIGH>;

    interrupt-names = "eri", "rxi", "txi", "tei";

    clocks = <&cpg CPG_MOD 138>,
            <&cpg CPG_MOD 139>;

    clock-names = "fck", "tclk";

    power-domains = <&cpg>;

    resets = <&cpg 147>,
            <&cpg 148>;

    reset-names = "presetn", "tresetn";

    status = "disabled";
};
```

Figure 5-27 Example of device tree initial references information of SCI9

**Required properties:****compatible:**

RZ/G3E Group: must be "renesas,r9a09g047-rz-rscif", "renesas,rz-rscif"

RZ/V2N Group: must be "renesas,r9a09g056-rz-rscif", "renesas,rz-rscif"

RZ/V2H Group must be "renesas,r9a09g057-rz-rscif", "renesas,rz-rscif"

**reg:** need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.

**interrupts:** interrupt specifier for the sci9 channel

**clocks, resets:** phandle + clock/reset specifier pairs

**5.3.1.2 Simple I2C (master-only)**

The initial reference information is shown below. An example here is rsci\_i2c9 channel

```
rsci_i2c9: i2c@12803000 {
    compatible = "renesas,r9a09g047-rz-rsci-i2c",
                "renesas,rsci-i2c";

    reg = <0 0x12803000 0 0x400>;

    interrupts = <GIC_SPI 168 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 169 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 170 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 171 IRQ_TYPE_LEVEL_HIGH>;

    interrupt-names = "eri", "rxi", "txi", "tei";

    clocks = <&cpg CPG_MOD 138>,
            <&cpg CPG_MOD 139>;

    clock-names = "fck", "tclk";

    clock-frequency = <100000>;

    power-domains = <&cpg>;

    resets = <&cpg 147>,
            <&cpg 148>;

    reset-names = "presetn", "tresetn";

    status = "disabled";
};
```

**Figure 5-28 Example of device tree initial references information of rsci\_i2c9**

**Required properties:**

**compatible:**

RZ/G3E Group: must be "renesas,r9a09g047-rz-rsci-i2c", "renesas,rsci-i2c"

RZ/V2N Group: must be "renesas,r9a09g056-rz-rsci-i2c", "renesas,rsci-i2c"

RZ/V2H Group: must be "renesas,r9a09g057-rz-rsci-i2c", "renesas,rsci-i2c"

**reg:** need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.

**interrupts:** interrupt specifier for the rsci\_i2c9 channel

**clocks, resets:** phandle + clock/reset specifier pairs

### 5.3.1.3 Simple SPI

The initial reference information is shown below. An example here is rsci\_spi9 channel

```
rsci_spi9: spi@12803000 {
    compatible = "renesas,r9a09g047-rz-rsci-spi",
                "renesas,rsci-spi";
    reg = <0 0x12803000 0 0x400>;
    interrupts = <GIC_SPI 168 IRQ_TYPE_LEVEL_HIGH>,
                <GIC_SPI 169 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 170 IRQ_TYPE_EDGE_RISING>,
                <GIC_SPI 171 IRQ_TYPE_LEVEL_HIGH>;
    interrupt-names = "eri", "rx", "tx", "te";
    clocks = <&cpg CPG_MOD 138>,
            <&cpg CPG_MOD 139>;
    clock-names = "fck", "tclk";
    dmas = <&dmac1 0x7F44AE>, <&dmac1 0x7F44AD>;
    dma-names = "tx", "rx";
    power-domains = <&cpg>;
    resets = <&cpg 147>,
            <&cpg 148>;
    reset-names = "presetrn", "tresetrn";
    num-cs = <1>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

**Figure 5-29 Example of device tree initial references information of rsci\_spi9**

**Required properties:****compatible:**

RZ/G3E Group: must be "renesas,r9a09g047-rz-rsci-spi", "renesas,rsci-spi"

RZ/V2N Group: must be "renesas,r9a09g056-rz-rsci-spi", "renesas,rsci-spi"

RZ/V2H Group: must be "renesas,r9a09g057-rz-rsci-spi", "renesas,rsci-spi"

**reg:** need two resources, first one mapped to register base address, second one mapped to extension resource registers base address.

**interrupts:** interrupt specifier for the rsci\_spi9 channel

**clocks, resets:** phandle + clock/reset specifier pairs

To enable DMA mode on SPI function, we need to add **dmass** and **dma-names** property to **rsci\_spi9** node in device tree as below:

```
&rsci_spi9{
    dmas = <&dmac1 0x7F44AE>, <&dmac1 0x7F44AD>;
    dma-names = "tx", "rx";
};
```

**Figure 5-30 Example of definition about DMA mode in SPI function**

**Note:** dmas number of SPI RSCI can refer at: **Table 4.7-22 DMA Transfer Request Detection Operation Setting Table** in Hardware Manual of RZ/V2H, RZ/V2N or RZ/G3E Group.

Example setting dmas (dmac1 channel) of all channels on RZ/G3E Group, RZ/V2N Group and RZ/V2H Group

**Table 5-1: Example setting dmas of all RSCI channels**

RSCI Channel	dmas
0	<&dmac1 0x7F4493>, <&dmac1 0x7F4492>;
1	<&dmac1 0x7F4496>, <&dmac1 0x7F4495>;
2	<&dmac1 0x7F4499>, <&dmac1 0x7F4498>;
3	<&dmac1 0x7F449C>, <&dmac1 0x7F449B>;
4	<&dmac1 0x7F449F>, <&dmac1 0x7F449E>;
5	<&dmac1 0x7F44A2>, <&dmac1 0x7F44A1>;
6	<&dmac1 0x7F44A5>, <&dmac1 0x7F44A4>;
7	<&dmac1 0x7F44A8>, <&dmac1 0x7F44A7>;
8	<&dmac1 0x7F44AB>, <&dmac1 0x7F44AA>;
9	<&dmac1 0x7F44AE>, <&dmac1 0x7F44AD>;

**Note:** Can change **dmac1** channel to other **dmac<sub>x</sub>** channels

### 5.3.2 Board Device tree

The following describes an example of UART, I2C, SPI function driver of RSCI module:

RZ/G3E SMARC Evaluation Board Kit in **arch/arm64/boot/dts/renesas/rzg3e-smarc.dtsi** (**supported on rz-6.1-cip28**)

RZ/V2N Evaluation Board Kit in **arch/arm64/boot/dts/renesas/r9a09g056n48-rzv2n-evk.dts** (**supported on rz-6.1-cip43**)

RZ/V2H Evaluation Board Kit in **arch/arm64/boot/dts/renesas/rzv2h-evk-common.dtsi** (**supported on rz-6.1-cip43**)

#### 5.3.2.1 Asynchronous Communications Interface (UART)

An example here is sci9 node

**Note:** Ensure sci9 node macro is enabled.

```
aliases {
    serial2 = &sci9;
};

&pinctrl {
    sci9_pins: sci9 {
        pinmux = <RZV2H_PORT_PINMUX(8, 3, 5)>, /* SCI9_TXD_MOSI_SDA */
               <RZV2H_PORT_PINMUX(8, 2, 5)>; /* SCI9_RXD_MISO_SCL */

        bias-pull-up;
    };
};

&sci9 {
    pinctrl-0 = <&sci9_pins>;

    pinctrl-names = "default";

    status = "okay";
};
```

Figure 5-31 Example of setting sci9 node in device tree



To enable UART hardware flow control, you need to add the **“uart-has-rtscts”** property, along with declaring the CTS and RTS pin in sci pinctrl node.

An example of how to enable hardware UART flow control on sci0

```
&pinctrl{  
    sci0_pins: sci0 {  
        pinmux = <RZV2N_PORT_PINMUX(5, 0, 1)>, /* SCI0_TXD_MOSI_SDA */  
        <RZV2N_PORT_PINMUX(5, 1, 1)>, /* SCI0_RXD_MISO_SCL */  
        <RZV2N_PORT_PINMUX(5, 2, 4)>, /* SCI0_CTS */  
        <RZV2N_PORT_PINMUX(5, 3, 2)>; /* SCI0_SS_CTS_RTS */  
        bias-pull-up;  
    };  
};  
  
&sci0 {  
    pinctrl-0 = <&sci0_pins>;  
    pinctrl-names = "default";  
    uart-has-rtscts;  
    status = "okay";  
};
```

**Figure 5-32 Example of setting hardware flow control on sci0 node in device tree**

### 5.3.2.2 Simple I2C (master-only)

An example here is rsci\_i2c9 node

**Note:** Ensure rsci\_i2c9 node macro is enabled.

```
&pinctrl {  
    rsci_i2c9_pins: rsci_i2c9 {  
        pinmux = <RZV2H_PORT_PINMUX(6, 6, 5)>, /* SCI9_TXD_MOSI_SDA */  
        <RZV2H_PORT_PINMUX(6, 5, 5)>; /* SCI9_RXD_MISO_SCL */  
        drive-open-drain = <1>;  
    };  
};  
  
&rsci_i2c9 {  
    pinctrl-0 = <&rsci_i2c9_pins>;  
    pinctrl-names = "default";  
    status = "okay";  
};
```

**Figure 5-33 Example of setting rsci\_i2c9 node in device tree**

**Notice** that RSCI module has multiple functions, so if we use I2C function, we need to add “**drive-open-drain = <1>;**” property to rsci\_i2c9\_pins node to module can work normally.

### 5.3.2.3 Simple SPI

An example here is `rsci_spi9` node. Furthermore, it can support master or slave role.

To use master or slave role of `rsci_spi9`, we will add Subnode to `rsci_spi9` node listed in **Add Subnode setting in device tree** section.

Master or Slave role will have **master\_sci9\_pins** or **slave\_sci9\_pins**. Default is **master\_sci9\_pins** when adding subnode Slave mode (“**spi-slave**” property has been added) will use **slave\_sci9\_pins**

**Note:** Ensure `rsci_spi9` node macro is enabled.

```
&pinctrl {
    master_sci9_pins: master_sci9 {
        pinmux = <RZV2H_PORT_PINMUX(6, 6, 5)>, /* SCI9_TXD_MOSI_SDA */
                <RZV2H_PORT_PINMUX(6, 5, 5)>, /* SCI9_RXD_MISO_SCL */
                <RZV2H_PORT_PINMUX(8, 4, 5)>; /* SCI9_SCLK */
    };
    slave_sci9_pins: slave_sci9 {
        pinmux = <RZV2H_PORT_PINMUX(6, 6, 5)>, /* SCI9_TXD_MOSI_SDA */
                <RZV2H_PORT_PINMUX(6, 5, 5)>, /* SCI9_RXD_MISO_SCL */
                <RZV2H_PORT_PINMUX(8, 4, 5)>, /* SCI9_SCLK */
                <RZV2H_PORT_PINMUX(8, 5, 5)>; /* SCI9_SSL */
    };
};

&rsci_spi9 {
    pinctrl-0 = <&master_sci9_pins>;
    pinctrl-1 = <&slave_sci9_pins>;
    pinctrl-names = "master", "slave";
    status = "okay";

    /* Using cs-gpios property when is master mode */
    cs-gpios = <&pinctrl RZV2H_GPIO(6, 4) GPIO_ACTIVE_HIGH>;

    /* Add subnode at here */
};
```

Figure 5-34 Example of setting `rsci_spi9` node in device tree

**Note)** In the SPI function driver of RSCI module support master/slave pins. Moreover, in master mode of SPI function don't support chip select pinfunction, so we use chip select pin of gpio with the name of property is cs-gpios.

## 5.4 Option Setting

### 5.4.1 Module Parameters

#### 5.4.1.1 Asynchronous Communications Interface (UART)

There are no parameters.

#### 5.4.1.2 Simple I2C (master-only)

We can set I2C transfer speed from 20KHz to 400KHz in "**clock-frequency**" property of device tree file. No setting means 100KHz.

RZ/G3E Group: in arch/arm64/boot/dts/r9a09g047.dtsi

RZ/V2N Group: in arch/arm64/boot/dts/r9a09g056.dtsi

RZ/V2H Group: in arch/arm64/boot/dts/r9a09g057.dtsi

#### 5.4.1.3 Simple SPI

There are no parameters.

### 5.4.2 Kernel Parameters

There are no kernel parameters.

REVISION HISTORY	Linux Interface Specification Device Driver RSCI User's Manual: Software
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		Page	Summary
1.00	Jul. 22, 2025	—	First Edition issued
1.01	Dec. 19, 2025	—	Add RZ/V2H support information
1.02	Mar. 27, 2026	—	Add RZ/V2N support information
		1	Update UART baudrate up to 3Mbps
		8	Remove 1.6.1 Asynchronous Communications Interface (UART)
		10	Update product name for RZ/V2N EVK boards
		34	Add figure 5-32

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RZ/G3E Group, RZ/V2N Group  
and RZ/V2H Group