On-Chip Debugger Functional Overview As for debugging function information of other emulators, visit each product's page from the following URL. <u>https://www.renesas.com/en/software-tool/chip-debuggers</u>

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E2 emulator Debugging Function (1)

	Target M	CU		Break Function			Trace Function	Memory			
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	reference&c hange while executing program	Performance measurement	Trigger	Hot plug–in
		RA8D1/M1		8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info)				
	RA8	RA8P1 CPU0	JTAG or SWD	8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area (CPU0/CPU1		Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info)				
		RA8P1 CPU1		8 points for an execution address, 4 points for a data access	shared)	can break CPU0/CPU1 separately or simultaneously	(CPU0/CPU1 shared)				
		RA6E2	SWD								
RA	RA6	Others than RA6xx	JTAG or SWD				Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)		Not supported; the time b/w Go and Stop is measurable.	Not supported	Supported
		RA4E2	SWD	6 points for an execution address, 4 points for a data access							
	RA4	RA4M1 RA4W1	JTAG or		2048 points for ROM/RAM area		Obtained information of branches is stored in a dedicated buffer 1KB. (both branch-source and branch-destination info)				
		Others than RA4xx	SWD		-		Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)				
	RA2 RA0	RA2xx RA0xx	SWD	4 points for an execution address, 2 points for a data access			Obtains the information of up to 2K branches *5 (both branch-source and branch-destination info)				
RE	RE0	RE01					Obtains the information of up to 4K branches *5 (both branch-source and branch-destination info)				Not supported
	RL78/G2x	RL78/G22 RL78/G23 RL78/G24		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				Not supported
	RL78/D1x	RL78/D1A RL78/F12 RL78/F13		1 point being shared by an execution address and data access	2000 points		Not supported	-			
	RL78/F1x	RL78/F14 RL78/F15 RL78/F15 RL78/F1E		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch–source info); the obtainable info is limited to 64 branches on some MCUs.				Supported
	RL78/F2x	RL78/F24 RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported	-	Not supported				
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				
RL78	RL78/G1x	RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G15 RL78/G16 RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G13A RL78/G1P	Single-wire Serial	1 point being shared by an execution address and data access	2000 points	Forcible break by selecting "Stop" on emulator debugger	Not supported	Supported	Not supported; the time b/w Go and Stop is measurable.		Not supported
	RL78/I1x	RL78/I1A RL78/I1B RL78/I1C RL78/I1D RL78/I1E		2 points being shared by an execution address and data access	-		Obtains the information of up to 256 branches (only branch-source info)				
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access]		Not supported]			
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				
	RL78/H1x RL RX700	RL78/H1D .78/FGIC RX72x RX71x	JTAG or Single-wire Serial	1 point being shared by an execution address and data access 8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.		-	Not supported Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)				
		RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *4		Supported *3
RX	RX600	Others than RX64x RX65x RX66x RX67x RX26T	JTAG or double-wire Serial *2 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation				
	Other	RX200 RX140 than RX26T RX100 than RX140	Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *1 Obtains the information of up to 32 branches or the information of up to 32 cycles		Not supported; the time b/w Go and Stop is		Not supported
RISC-V MCU	R9A02G021	R9A02G021	cJTAG	4 points being shared by an execution address and data access	2000 points for ROM/RAM area		on data-access operation Not supported		measurable. Not supported; the time b/w Go and Stop is measurable.		Not supported

Notes: *1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained. *2. The debugging function and the connection system vary by the MCU you use. *3. Available only when the emulator is connected via JTAG interface.

*4. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600." *5. The internal RAM of the microcomputer is used as the trace buffer.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator. This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e2

E2 emulator Debugging Function (2)

	Target MC	U		Break Function			Trace Function	Memory			
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	reference& change while executing program	Performance measurement	Trigger	Hot plug–in
	RH850/F1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH	LPD4-pin or LPD1-pin								
	RH850/E1x	RH850/E1M-S2					Between 2K and 4K of branch information can be acquired when this is the only target				
	RH850/C1x	RH850/C1H RH850/C1M	LPD4-pin				or Between 1K and 2K of cycle information				
	RH850/D1x	RH850/D1L RH850/D1M	LPD4-pin or				on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.				
RH850		RH850/P1M	LPD1-pin	12 points	2000 points for				euroneurte d	IN:2ch	Summaritad
КПОЭО		RH850/P1M-E		being shared by an execution address and data access	ROM/RAM area				supported	OUT:2ch	Supported
	RH850/P1x	RH850/P1H-C RH850/P1M-C RH850/P1L-C	LPD4-pin			Forcible break by selecting ″Stop″ on		Supported			
	RH850/E2x	RH850/E2M RH850/E2H RH850/E2UH	LPD4-pin				Between 4K and 8K of branch information can be acquired when this is the only target or				
	RH850/U2x	RH850/U2A RH850/U2B RH850/U2C	or JTAG			emulator debugger	on data-access operation can be acquired				
R–Car	R−Car S4	_	<g4mh> LPD−4pin or JTAG <cortex®−a,r> JTAG</cortex®−a,r></g4mh>	<g4mh> 12 points for an execution address/a data access <cortex®−a> 6 pints for an execution address <cortex®−r> 6 pints for an execution address 2 pints for a data address</cortex®−r></cortex®−a></g4mh>	2048 points for ROM/RAM area		<g4mh> Between 2K and 8K of branch information can be acquired when this is the only target or Between 2K and 4K of cycle information on data-access operation can be acquired when this is the only target <cortex®-a,r> Obtained information of branches is stored in a dedicated buffer 32KB. (both branch-source and branch-destination info)</cortex®-a,r></g4mh>		<g4mh> Supported <cortex®−a,r> Not supported; the time b/w Go and Stop is measurable.</cortex®−a,r></g4mh>	Not supported	Supported
	R−Car V4M	-	JTAG	<cortex®-a> 6 pints for an execution address <cortex®-r> 6 pints for an execution address</cortex®-r></cortex®-a>			Obtained information of branches is stored in a dedicated buffer 32KB.		Not supported; the time b/w Go and Stop is		
	R−Car V4H	-		6 pints for an execution address 2 pints for a data address			(both branch-source and branch-destination info)		measurable.		

Notes: *1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.

*2. The debugging function and the connection system vary by the MCU you use.
*3. Available only when the emulator is connected via JTAG interface.
*4. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600."
*5. The internal RAM of the microcomputer is used as the trace buffer.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator. This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes

available, check our website at: https://www.renesas.com/e2

E2 emulator Lite Debugging Function

	Target MCU			Break Function			Trace Function	Memory reference&ch	Performance					
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	ange while executing program	measurement	Hot plug–in				
		RA8D1/M1		8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info)							
	RA8	RA8P1 CPU0		8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger In this case, it can	Obtained information of branches is stored in a dedicated buffer 8KB.							
		RA8P1 CPU1		8 points for an execution address, 4 points for a data access	(CPU0/CPU1 shared)	break CPU0/CPU1 separately or simultaneously	(both branch-source and branch-destination info) (CPU0/CPU1 shared)							
RA	RA6	RA6xx	SWD				Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)		Not supported; the time b/w Go and Stop is measurable.	supported				
	RA4	RA4M1 RA4W1		6 points for an execution address, 2 points for a data access			Obtained information of branches is stored in a dedicated buffer 1KB. (both branch-source and branch-destination info)							
		Others than RA4xx			2048 points for ROM/RAM area		Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)							
	RA2	RA2xx		4 points for an execution address,			Obtains the information of up to 2K branches *6 (both branch-source and branch-destination info)							
	RAO	RA0xx		2 points for a data access			Obtains the information of up to 4K branches *6							
RE	RE0	RE01		2 points		-	(both branch-source and branch-destination info) Obtains the information of up to 256 branches	-						
	RL78/G2x RL78/D1x	RL78/G23 RL78/G24 RL78/D1A		being shared by an execution address and data access	-		(only branch-source info)			Not supported				
		RL78/F12		1 point being shared by an execution address and data access	2000 points		Not supported		_					
	RL78/F1x RL78/F2x	RL78/F13 RL78/F14 RL78/F15 RL78/F1E RL78/F23 RL78/F24		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.			Supported *3				
		RL78/G10 RL78/G1M RL78/G1N RL78/G1N		2 points for an execution address	Not supported	-	Not supported							
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access		Forcible break by selecting "Stop" on emulator debugger	Obtains the information of up to 256 branches (only branch-source info)							
RL78	RL78/G1x	RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G15 RL78/G15 RL78/G16 RL78/G10 RL78/G10 RL78/G10 RL78/G16 RL78/G13A RL78/G1P		1 point being shared by an execution address and data access	2000 points		Not supported		Not supported; the time b/w Go and Stop is measurable.	Not supported				
	RL78/I1x	RL78/I1A RL78/I1B RL78/I1C RL78/I1D RL78/I1D RL78/I1E		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)							
		RL78/L12 RL78/L13		1 point being shared by an execution address and data access	-		Not supported							
	RL78/L1x RL78/H1x	RL78/L1A RL78/L1C RL78/H1D		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)							
	<u> </u>	8/FGIC		1 point being shared by an execution address and data access	-	_	Not supported							
	RX700	RX72x RX71x	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)							
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *5	Supported *3 *4				
RX		Others than RX64x RX65x RX66x RX67x RX67x	JTAG or double–wire Serial *2 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation							
	R	X200 X140 han RX26T		4 points for an execution address +							Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *1			
		X100 han RX140	Single-wire Serial	2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation		Not supported; the time b/w Go and Stop is measurable.	Not supported				
RISC-V MCU	R9A02G021	R9A02G021	cJTAG	4 points being shared by an execution address and data access	2000 points for ROM/RAM area		Not supported		Not supported; the time b/w Go and Stop is measurable.	Not supported				

Notes: *1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained. *2. The debugging function and the connection system vary by the MCU you use. *3. Hot-plug Adapter for the E1 Emulator (optional) is required. *4. Available only when the emulator is connected via JTAG interface. *5. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600. *6. The internal RAM of the microcomputer is used as the trace buffer.

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■E1 emulator Debugging Function (1)

	Target MC	U		Break Function			Trace Function	Memory reference&c		
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	hange while executing program	measurement	Hot plug–in
	RH850/F1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH	LPD4-pin or LPD1-pin							
	RH850/E1x	RH850/E1M-S2	LPD4-pin							
RH850	RH850/C1x	RH850/C1H RH850/C1M		12 points	2000 points for		Between 2K and 4K of branch information can be acquired when this is the only target or Between 1K and 2K of cycle information		supported	Supported
KHOJU	RH850/D1x	RH850/D1L RH850/D1M	LPD4-pin or	being shared by an execution address and data access	ROM∕ RAM area		on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.		supported	*5
		RH850/P1M	LPD1-pin				Trace function isn't supported in some woo's.			
	RH850/P1x	RH850/P1M-E	LPD4-pin							
		RH850/P1H-C RH850/P1M-C RH850/P1L-C	LPD4-pin							
	RL78/D1x	RL78/D1A RL78/F12		1 point being shared by an execution address and data access			Not supported			Not supported
	RL78/F1x	RL78/F12 RL78/F13 RL78/F14 RL78/F15 RL78/F15		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.	-		Supported *5
		RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported			
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
RL78	RL78/G1x	RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G1G RL78/G13A RL78/G1P	Single-wire Serial	1 point being shared by an execution address and data access	2000 points			Not supported; the time b/w Go and Stop is measurable.	Not supported	
	RL78/I1x	RL78/I1A RL78/I1B RL78/I1C RL78/I1D RL78/I1E		2 points being shared by an execution address and data access		Forcible break by selecting "Stop" on emulator debugger	Obtains the information of up to 256 branches (only branch-source info)	Supported		
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported			
	RL78/H1x	RL78/L1A RL78/L1C RL78/H1D		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
		L78/FGIC		1 point being shared by an execution address and data access	-		Not supported	-		
	RX700	RX72x RX71x	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)			
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *7	Supported *5 *6
RX	RX600	Others than RX64x RX65x RX66x RX67x RX26T	JTAG or double−wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation			
	RX26T RX200 RX140 Other than RX26T	RX140		4 points for an execution address			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *3			
		RX100 r than RX140	Single−wire Serial	+ 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation		Not supported; the time b/w Go and Stop is measurable.	Not supported
V850		V850E1 V850ES V850E2	JTAG, double−wire or 4−wire Serial (data × 2, clock and handshake)	2 points being shared by an execution address and data access * Sequential breaks are specifiable.	4 points for ROM area 2000 points for RAM area				Not supported;	
V850 *1 *2		/850E2M /850E2S	Nexus or Single-wire Serial	[When using JTAG I/F][When using Serial I/F]Before-execution:Before-execution:4 points4 pointsAfter-execution:After-execution:8 pointsNot supportedAccess: 6 pointsAccess: 4 points* Sequential breaks are specifiable.	8 points for ROM area 2000 points for RAM area		Not supported		the time b/w Go and Stop is measurable.	Supported *5

Notes:

 $\ast 1.$ V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.

*2. The number of break points varies by the integrated development environment you use.

*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.

*4. The debugging function and the connection system vary by the MCU you use.*5. Hot-plug Adapter for the E1 Emulator (optional) is required.

*6. Available only when the emulator is connected via JTAG interface.

*7. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600.

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■E1 emulator Debugging Function (2)

	Target MCU			Break Function			Trace Function	Memory reference& change	Performance	
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	while executing program	measurement	Hot plug–in
	78K0R		Single-wire Serial or double-wire Serial (clock and data)	erial being shared by an execution address and data access ta)		Not supported				
	78K0 R8C/L35C, R8C/L36C, R8C/L38C and R8C/L3AC		double−wire Serial (clock and data)	ire Serial (only when software breaks are not used) 2000 points			Not supported			
R8C	R8C/L38C G R8C/L38M R8C/L38M G R8C/L38M G R8C/LA3A G R8C/JAAA R8C/32A, R8C R8C/3 R8C/32M, R8C R8C/34W, R8C/34W, R8C/34X, R8C/34X, R8C/34Z, R8C/34K, R8C and R8C/		Single-wire Serial	8 points for an address break + 2 points for a data condition break * Sequential breaks are specifiable.	256 points at the max	Forcible break by selecting "Stop" on emulator debugger	Obtains the information of 4 branches (sum of the branch-source and branch-destination PC) or the information of up to 8 cycles of specified data access	Supported	Not supported; the time b/w Go and Stop is measurable.	Not supported

Notes:

*1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
*2. The number of break points varies by the integrated development environment you use.

*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*4. The debugging function and the connection system vary by the MCU you use.
*5. Hot-plug Adapter for the E1 Emulator (optional) is required.
*6. Available only when the emulator is connected via JTAG interface.

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E20 emulator Debugging Function (1)

	Target MCL	J		Break Function			Trace F	Function	Memory reference&	Performance	Real-time	C0		
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	External Trace	change while executing program	measurement	Real-time RAM monitor	CU coverage	Hot plug-in	
RH850	RH850/F1x RH850/E1x RH850/C1x RH850/D1x RH850/P1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH RH850/E1M-S2 RH850/C1H RH850/C1H RH850/D1L RH850/D1L RH850/P1M-E RH850/P1M-E	LPD4-pin LPD4-pin or LPD1-pin	12 points being shared by an execution address and data access	2000 points for ROM/RAM area		Between 2K and 4K of branch info can be acquired when this is the only target or Between 1K and 2K of cycle info on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.	Not supported	bioPram	Supported			Supported	
		RH850/P1M-C RH850/P1L-C	LPD4-pin	4 1										
	RL78/D1x	RL78/D1A RL78/F12		1 point being shared by an execution address and data access			Not supported						Not supported	
	RL78/F1x	RL78/F13 RL78/F14 RL78/F15 RL78/F1E		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.						Supported	
		RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported							
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H RL78/G11		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				Not supported	Not supported		
RL78	RL78/G1x	RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G1A RL78/G1C RL78/G1D RL78/G1D RL78/G1G RL78/G13A RL78/G1P	Single−wire Serial	1 point being shared by an execution address and data access	2000 points		Not supported	Not supported		Not supported; the time b/w Go and Stop is measurable.			Not supported	
	RL78/I1x	RL78/I1A RL78/I1B RL78/I1C RL78/I1D RL78/I1E		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)	n of						
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported							
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access		Forcible break by	Obtains the information of up to 256 branches (only branch-source info)			4				
	RL78/H1x RL7	RL78/H1D 8/FGIC		1 point being shared by		selecting "Stop" on emulator debugger	Not supported		Supported					
			JTAG only or Single-wire Serial	an execution address and data access 8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	_			Not supported	Not supported		
	RX700	RX71x	JTAG + External Trace	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation (DMAC or DTC bus is selectable as a bus master)			Supported (Data- and Last-access attributes [Read/Write/N on-accessed])	Supported		
		RX64x RX65x RX66x RX67x RX26T	JTAG only or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	-			Not supported	Not supported	Supported *5	
RX	RX600	RX26T * Sequential breaks are specifiable. RX64x JTAG RX65x + RX66x 5 points for an execution address PX66x - State - RX66x - State - RX66x - State - State </td <td>256 points at the max</td> <td></td> <td>Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)</td> <td>Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation (DMAC or DTC bus is selectable as a bus master)</td> <td></td> <td>Supported *6</td> <td>Supported (Data- and Last-access attributes [Read/Write/N on-accessed])</td> <td>Supported</td> <td></td>	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation (DMAC or DTC bus is selectable as a bus master)		Supported *6	Supported (Data- and Last-access attributes [Read/Write/N on-accessed])	Supported				
		Others than RX64x RX65x	JTAG only or double–wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation	-			Not supported	Not		
		RX66x RX67x RX26T	JTAG or double−wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation			Supported (Data- and Last-access attributes [Read/Write/N on-accessed])	supported		
	R Other tl	X200 X140 han RX26T	Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation*3 Obtains the information of up to 32 branches	Not supported		Not supported;	Not supported	Not supported	Not supported	
		RX100 Other than RX140						or the information of up to 32 cycles on data-access operation			supported; the time b/w Go and Stop is measurable.			

Notes: *1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them. *2. The number of break points varies by the integrated development environment you use. *3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is

obtained. *4. The debugging function and connection system vary by the MCU you use.

*5. Available only when the emulator is connected via JTAG interface.*6. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator. This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e20

■E20 emulator Debugging Function (2)

	Target MCU	J		Break Fund	tion		Trace F	unction	Memory reference&c		Real-time		
Family	Series/Core	Group	Connection system	Hardware Break	Software Break	Special Break	Internal trace	External Trace	hange while executing program	Performance measurement	RAM monitor	C0 coverage	Hot plug–in
	V8	50E1 50ES 50E2	JTAG, double-wire or 4-wire Serial (data × 2, clock and handshake)	2 points being shared by an execution address and data access * Sequential breaks are specifiable.	4 points for ROM area 2000 points for RAM area								Not supported
V850 *1 *2		50E2M 50E2S	Nexus or Single-wire Serial	[When using JTAG I/F] [When using Serial I Before-execution: 4 points 4 points 4 points After-execution: 8 points Access: 6 points Access: 4 points * Sequential breaks are specifiable.	: 8 points for ROM area 2000 points for RAM		Not supported						Supported
	78K0R 78K0 78K0 R8C/L35C, R8C/L36C,		Single-wire Serial or double-wire Serial (clock and data)	1 point being shared by an execution address and data access	2000 painta								
			double-wire Serial (clock and data)	1 point for a before-execution break (only when software breaks are not used) + 1 point for an access break	2000 points								
R8C	R8C/L38C a Gr R8C/L35M R8C/L38M a Gr R8C/LA6A a Gr R8C/LA6A a Gr R8C/LA3A a Gr R8C/LA3A a Gr R8C/LA3A a Gr R8C/32C, R8C R8C/32C, R8C R8C/35C, R8C R8C/35C, R8C R8C/35C, R8C R8C/35M, R8C R8C/35M, R8C R8C/35M, R8C R8C/34W, I R8C/34W, I R8C/34W, I R8C/34W, I R8C/32 R8C/32G, R8C R8C/34C, R8C R8C/32G, R8C R8C/32G, R8C R8C/32G, R8C R8C/34C, R8C R8C/32C, R8C R8C/34C, R8C R8C	C, R8C/L36C, and R8C/L3AC roups 1, R8C/L36M, and R8C/L36M, and R8C/L36M roups and R8C/LA8A roups and R8C/LA5A roups APS Group C/5x /3xT-A C/33C, R8C/34C, C/5x /3xT-A C/33C, R8C/34C, C/5x /3xT-A C/33C, R8C/34C, C/36C, R8C/38M, 3GC and JC Groups C/33M, R8C/34M, C/36M, R8C/38M, 3GM and JM Groups R8C/36X and SX Groups R8C/36X and SX Groups R8C/36Z and SX Groups C/32H, R8C/33G, R8C/34P and AR Groups C/34U, R8C/3MK 3MU Groups	Single-wire Serial	8 points for an address break + 2 points for a data condition break * Sequential breaks are specifiable.	256 points at the max	Forcible break by selecting "Stop" on emulator debugger	Obtains the information of 4 branches (sum of the branch-source and branch-destination PC) or the information of up to 8 cycles of specified data access	Not supported	Supported	Not supported; the time b/w Go and Stop is measurable.	Not	Not supported	Not supported

Notes:

- $\ast 1.$ V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
- *2. The number of break points varies by the integrated development environment you use.
- *3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
- *4. The debugging function and connection system vary by the MCU you use.*5. Available only when the emulator is connected via JTAG interface.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator.

This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e20

MINICUBE2 Debugging Function

	Target MCU		Break Fun	ction			DMM	Time Measurement
Family	Series/ Core	Group	Hardware Break	Software Break	Forcible break	RAM Monitor	(Rewriting memories during RUN)	(from the start of execution to break)
V850	V85	50E1 50ES 50E2	2 points *1 (Shared by an execution and access)	ROM area: 4 points RAM area: 2000 points	Supported *2	Supported	Supported	Measurement resolution: 100 μ s
Voo		DE2M OE2S	Before-execution break : 4 points Access break : 4 points * Sequential breaks are specifiable.	ROM area: 8 points RAM area: 2000 points	Supported	Supported	Supported	Max. measurement time: Approx. 100 hours
	78K0R		1 point (Shared by an execution and access)	2000 points	Supported	Pseudo-Real RAM Monitor (RRM) : Supported	Supported	Measurement resolution: $100 \ \mu \ s$ Max. measurement time: Approx. 100 hours
	78K0		Before-execution break : 1 point (Not supported when software breaks are used) Access break : 1 point	2000 points	Supported	Pseudo-Real RAM Monitor (RRM) : Supported	Supported	Measurement resolution: 100 μ s Max. measurement time: Approx. 100 hours
	78K0S		Not supported	2000 points	Supported (Not supported while interrupts are inhibited)	Not supported	Not supported	Measurement resolution: 100 μ s Max. measurement time: Approx. 100 hours

Notes:

*1. The following MCUs have not been supported yet: V850ES/KE2, V850ES/KF2, V850ES/KG2, μ PD70F3733, and V850ES/IE2. *2. A forcible break is not possible in the following states.

- Interrupts are inhibited (DI).

- Interrupts from the serial interface used for communications between MINICUBE2 and the target device are masked.

- The device is on standby and triggering of release from standby by makeable interrupts is disabled.

- The main clock is stopped while the UART is being used as the communications interface between MINICUBE2 and the target device.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator.

This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at:

https://www.renesas.com/cs+ > "Functions Supported by CS+"(PDF)

E10A-USB(HS0005KCU01H/HS0005KCU02H)Debugging Function (1)

inter9 act does9		Target MCU		Break Function	-	Performance	Invalid External extension Mode	Trace	Function
InterpretationAdditional of 2000 Additional of 2000 Addit	Family	Series/ Core	Group	Hardware Break	Software Break	Measurement Function		Internal Trace	AUD Trace
Note Note:				condition break : 2 points + Address/R/W condition break : 4 points + Data/R/W condition break : 2 points + System bus condition break : 2 points		Supported	No Mode	8 branches ©	Up to 64K events *1 (Up to 32K of branch informatic can be acquired when branch trace is the only target ©
		SH-4	SH7751R	+ Address/R/W condition break : 4 points		Supported		8 branches	
$ \mathbf{k} = \frac{\left \mathbf{k} + \mathbf{k} + \mathbf{k} \right \\ \mathbf{k} = \frac{\left \mathbf{k} + \mathbf{k} + \mathbf{k} \right \\ \mathbf{k} = \frac{\left \mathbf{k} + \mathbf{k} + \mathbf{k} \right \\ \mathbf{k} = \frac{\left \mathbf{k} + \mathbf{k} $		SH-3	SH7721 SH7720 SH7712 SH7710 SH7705 SH7727	condition break : 1 point + Address/R/W condition break : 1 point		Supported	No Mode	8 branches	Up to 64K branches *1 (Only branch-destination information) ©
Image: state in the state is a second state is order in the state is			SH7706 SH7206 SH72AY SH72AW	-	-				Up to 26214 branches *1
99-07 (NOC)			SH72A2 SH7211 SH7216 (SH7216, SH7214) SH7231 SH7237 SH7239 SH7243				Supported	Select the target info from: Address/Data/Status/	Up to 64K events *1
Image: second	SuperH	(Except for Multi-core	SH7286 SH7670 SH726A SH726B SH7269 SH7268 SH7267 SH7266 SH7264 SH7264 SH7262 SH7203	Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point		Supported	No Mode	Select the target info from: Address/Data/Status/	(Up to 32K of branch informat can be acquired when branch trace is the only targe ⊚
No. Series		-	SH7201 SH7261 SH7256R					_	
Horizon Statistics Statistics No Mode 4 branches			SH7253	Address/Data/R/W/Execution-count			No Mode		_
High High Address brack : 4 paints Shift/12 Address brack : 4 paints Shift/144A SH-2 RF/144A RF/144A Address brack : 2 paints Address brack : 2 paints Address brack : 2 paints Address brack : 2 paints RF/144A RF/144A Address brack : 2 paints Address brack : 2 paints Address brack : 2 paints Address brack : 2 paints RF/144A				condition break : 1 point + Address/R/W condition break : 1 point	255 points	_	No Mode	4 branches	-
Bits Bits Bits Bits Bits Address/Data/R/W/Securitor-oution ondition break: 1 points Address/Data/R/W/Securitor-oution ondition break: 1 point Address/Data/R/W/Securitor-oution ondition break: 1 point Address/Data/R/W/Securitor-oution ondition break: 1 point Address/Data/R/W/Securitor-oution ondition break: 1 point Address/Data/R/W/Securitor-oution Signature Supported			SH7144F				_	-	Up to 64K events *2 (Up to 32K of branch informat can be acquired when branch trace is the only targe
$HSV = \frac{1}{185/2420} + \frac{1}{185/2421} $		SH-2	R5F71464A R5F70865A R5F70855A R5F70854A R5F70845A R5F70844A R5F70835A	+ Address/Data/R/W/Execution-count condition break : 1 point +		Supported	Supported	4 branches	_
$HSX = \frac{HSZ/1494R}{HSZ/100} + \frac{Address brak : 8 points}{Address brak : 1 point} + \frac{Address brak : 8 points}{Address/Data/R/W/Csecution-count} condition brak : 1 point} + \frac{Address/Data/R/W/Csecution-count}{Select the target info from: Select the target info from: Address/Data/Satisfaction-count} - +3 \\ HSX/1700 + \frac{HSX/1700}{HSX/1720} + \frac{Address/Data/Satisfaction-count}{Select the information track : 1 point} + \frac{HSX/100}{Supported} + \frac{HSX/1700}{RST0485R} + \frac{Address/Data/Satisfaction-count}{Supported} + \frac{1 + 3}{Supported} + \frac{1 + 3}{Sup$			SH7136 SH7125	* Sequential breaks are specifiable.		-			
HBSX/100 HBSX/120 HBSX/120 HBSX/120 HBSX/120 Address/Data/Salisfaction-count condition brask: 1 point * Sequential brasks are specifiable. Supported - *3 8 branches - HBSX/100 HBSX/120 HBS/2402 HBS/2403 Address/Data/Salisfaction-count condition brask: 1 point * Sequential brasks are specifiable. - - - 4 branch sources - HBS/2400 HBS/2401 HBS/2402 HBS/2402 Address/Data condition break: 2 points - - - 4 branch sources - HBS HBS/2420 HBS/2420 Address/Data condition break: 2 points + - - - 4 branch sources - - HBS HBS/2420 HBS/2420 HBS/2420 Address/Data condition break: 2 points - - 4 branch sources - - HBS/2200 HBS/2318 HBS/2318 Address/Data condition break: 2 points - - - - - - - HBS/2200 HBS/2201 HBS/2218 Address/Data condition break: 2 points - -			R5E71494R R5E71491R R5E71464R R5E70865R R5E70855R R5E70845R	+ Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point		Supported	Supported	Select the target info from: Address/Data/Status/	Up to 64K events *1 (Up to 32K of branch informat can be acquired when branch trace is the only targe ©
Image: H85X/150 H85X/150 Image: Condition break : 1 point * Sequential breaks are specifiable. Image: Condition break : 2 points Image: Condition break : 2 points H85 H85/2400 H85/2456 H85/2456 H85/2456 H85/2457 H85/2426 H85/2456 H85/2456 H85/2426 Address break : 6 points + Address/Data condition break : 2 points Image: Condition break : 2 points	H8SX		H8SX/1720	+ Address/Data/Satisfaction-count		Supported	- *3	8 branches	_
H85 H85/2463 H85/2450 H85/2450 H85/2420 H85/2420 H85/2420 H85/2427 H85/247 H85			(/1500		-	-			
H8S/2378 H8S/2378 Address/Data condition break : 2 points - 4 branch sources or Bus trace : 512 cycles H8S/2300 H8S/2339 *5 Address/Data condition break : 2 points Supported 4 branch sources H8S/2200 H8S/2218 Address/Data condition break : 2 points - - - 4 branch sources H8S/2200 H8S/2218 Address/Data condition break : 2 points - - - 4 branch sources -		H8S/2463 H8S/2462 H8S/2463 H8S/2456R H8S/2456R H8S/2456 H8S/2454 H8S/2454 H8S/2456R H8S/2454 H8S/2426R H8S/2426R H8S/2424 H8S/2426 H8S/2424 H8S/2427R H8S/2427 H8S/2427R			_	- Supported	4 branch sources or Bus trace : 1024 cycles	_	
H8S/2329 *6 Supported 4 branch sources H8S/2218 H8S/2215 *7 Address/Data condition break : 2 points - - 4 branch sources	H8S		H8S/2427R H8S/2427					8 branch sources	
H8S/2200 H8S/2215 *7 Address/Data condition break : 2 points 4 branch sources -	H8S	H8S/2300	H8S/2427R H8S/2427 H8S/2425 H8S/2378 H8S/2378R H8S/2378R H8S/2368 H8S/2319 *4	Address/Data condition break : 2 points	-		-	4 branch sources or Bus trace : 512 cycles	
	H8S		H8S/2427R H8S/2427 H8S/2425 H8S/2378 H8S/2378R H8S/2378R H8S/2368 H8S/2319 *4 H8S/2339 *5 H8S/2329 *6 H8S/2218		-		- Supported	4 branch sources or Bus trace : 512 cycles	

Notes:

*1. Not usable with HS0005KCU01H.

*2. Not usable with HS0005KCU01H. While using RAM monitor function with HS0005KCU02H, no trace information can be acquired.

*3. Supported only by H8SX/1651.

*4. Only H8S/2319EF is supported.

*5. Only H8S/2339EF is supported.

*6. Only H8S/2329EF is supported.*7. Only H8S/2215R and H8S/2215T are supported.

 \bigcirc Acquirable trace information:

Branch, Memory access within the specified range, and Software trace (Trace(x): variable x).

 \ast The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator. This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: $https://www.renesas.com/e10a_usb$

E10A-USB(HS0005KCU01H/HS0005KCU02H)Debugging Function (2)

	Target MCU		Break Function		Performance		Trace	Function
Family	Series/ Core	Group	Hardware Break	Software Break	Measurement Function	Invalid External extension Mode of Embedded ROM	Internal Trace	AUD Trace
H8S	H8S/2100	H8S/2168 H8S/2153 H8S/2164 H8S/2117 H8S/2117R H8S/2125 H8S/2116 H8S/2113 H8S/2112 H8S/2112R	Address break : 6 points + Address/Data condition break : 2 points	255 points	Not supported	No Mode	4 branch sources	Not supported
		H8S/2189R H8S/2114R	Address break : 6 points + Address/Data condition break : 2 points				4 branch sources or Bus trace : 512 cycles	

Notes:

*1. Not usable with HS0005KCU01H.

*2. Not usable with HS0005KCU01H. While using RAM monitor function with HS0005KCU02H, no trace information can be acquired.

*3. Supported only by H8SX/1651.

*4. Only H8S/2319EF is supported.

*5. Only H8S/2339EF is supported.

*6. Only H8S/2329EF is supported.

*7. Only H8S/2215R and H8S/2215T are supported.

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■E10A-USB(HS0005KCU01H/HS0005KCU02H + Debug MCU Board) Debugging Function

	Target MCU		Break Function		Performance	Invalid External extension Mode	Trace	Function
Family	Series/ Core	Group	Hardware Break	Software Break	Measurement Function	of Embedded ROM	Internal Trace	AUD Trace
SuperH	SH-4A	SH7456 SH7455 SH7451 SH7450	Address/Data/R/W/Execution-count condition break : 2 points + Address/R/W condition break : 4 points + Data/R/W condition break : 2 points + System bus condition break : 2 points * Sequential breaks are specifiable.		Supported	No Mode	8 branches ©	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ©
	SH-2	SH7125 SH7124	Address break : 8 points + Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point * Available to specify the sequential break	255 points	Supported	No Mode	1000 cycles Select the target one from Address/Data/Status/ Time stamp bus.	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target.) ©
H8S	H8S/2400	H8S/2456R H8S/2456 H8S/2454 H8S/2426R H8S/2426 H8S/2424	Address break : 6 points + Address/Data condition break : 2 points		Not supported	Supported	4 branch sources or Bus trace : 1024 cycles	Not supported

Note:

*1. Not usable with HS0005KCU01H.

O Acquirable trace information: Branch, Memory access within the specified range, and Software trace (Trace(x): variable x).

■E10A-USB(HS0005KCU14H) Debugging Function

		Target MCU		Break Function P		Performance		Trace Function	
Family	Family	Series/ Core	Group	Hardware Break	Software Break	Measurement Function	Invalid External extension Mode of Embedded ROM	Internal Trace	AUD Trace
		SH-4A (Multi-core MCU)	SH7786					60 sets of branch sources and destinations	Up to 128K events
SuperH	SH-2A (Multi-core MCU)	SH7205 SH7265	10 points (Using UBC module)	255 points (for each core Support in MCU)	Supported	orted No Mode	1024 cycles (When acquiring trace info by core in MCU, 512 cycles respectively.)	(Up to 64K of branch information can be acquired when branch trace is the only target) ⊚	

© Acquirable trace acquisition information: Branch, Memory access, and General register. (Conditions are settable by each CPU.)

■E8a Debugging Function

Target MCU			Break Function	Trace Function			
Family	Series/ Core	Group	Hardware Break	Software Break	Special Break	Internal Trace	
R8C	R8C/Lx		Address break : 8 points + Data condition break : 2 points * Sequential breaks are specifiable.			4 branches (sum of branch source PC and destination F or Up to 8 cycles of specified data access	
	R8C/Mx		Address break : 4 points + Data condition break : 1 point			3 branches (sum of branch source PC and destination PC) or 6 branches (branch source PC) or Up to 8 cycles of specified data access	
	R8C/3x	Other than R8C/3xD	Address break : 8 points + Data condition break : 2 points * Sequential breaks are specifiable.			4 branches (sum of branch source PC and destination PC) or Up to 8 cycles of specified data access	
	R8C/3xD		Address break : 4 points				
	R8C	C/2x	or Address break : 2 points + Data condition break : 1 point			The latest 4 branches (branch source PC)	
	R8C/1x	Other than R8C/10-13 R8C/10-13	Address break : 2 points				
	R32C/100		Address break . 2 points	-		_	
	M32C/80						
		M16C/62P M16C/6Nx M16C/6S	Address break : 8 points	255 points	Forcible break by selecting "Stop" on emulator debugger	_	
M16C	M16C/60	M16C/63 M16C/64A M16C/64C M16C/65 M16C/65C M16C/6C	Address break : 8 points			32 branches of order execution history (sum of branch source PC and destination PC) or Up to 64 cycles of specified data access	
		M16C/6S1 M16C/6B	+ Data condition break : 2 points * Sequential breaks are specifiable.			16 branches of order execution history (sum of branch source PC and destination PC) or Up to 32 cycles of specified data access	
	M16C/50					32 branches of order execution history (sum of branch source PC and destination PC) or Up to 64 cycles of specified data access	
	M16C/Tiny		Address break : 6 points]		-	
H8S	H8S/Tiny		Address break : 8 points + Address/Data condition break : 2 points			The latest 8 branch sources or The latest 4 branch sources + 4 branch destinations	
	H8/300H Tiny		Address/Data condition break : 1 point]			
H8	H8/300H Super Low Power		Address break : 1 point + Address/Data condition break : 1 point			The latest 4 branch sources	
	H8/300L Super Low Power		Address/Data condition break : 1 point	1			
	740		Address break : 2 points	1		-	

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator. This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e8a