On-Chip Debugger Functional Overview

◆As for debugging function information of other emulators, visit each product's page from the following URL.
https://www.renesas.com/en/software-tool/chip-debuggers

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■E2 emulator Debugging Function (1)

Target MCU			Connection system	Break Function			Trace Function	Memory reference&change while executing program	Performance measurement	Trigger	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace				
RA	RA8	RA8D1/M1	JTAG or SWD	8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info)	Supported	Not supported; the time b/w Go and Stop is measurable.	Not supported	Supported
		RA8P1 CPU0		8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area (CPU0/CPU1 shared)	Forcible break by selecting "Stop" on emulator debugger In this case, it can break CPU0/CPU1 separately or simultaneously	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info) (CPU0/CPU1 shared)				
		RA8P1 CPU1		8 points for an execution address, 4 points for a data access							
	RA6	RA6E2	SWD	6 points for an execution address, 4 points for a data access	2048 points for ROM/RAM area		Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)				
		Others than RA6xx	JTAG or SWD								
	RA4	RA4E2	SWD								
		RA4M1 RA4W1	JTAG or SWD				Obtained information of branches is stored in a dedicated buffer 1KB. (both branch-source and branch-destination info)				
		Others than RA4xx					Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)				
	RA2	RA2xx	SWD	4 points for an execution address, 2 points for a data access			Obtains the information of up to 2K branches *5 (both branch-source and branch-destination info)				
	RA0	RA0xx									
RE	RE0	RE01					Obtains the information of up to 4K branches *5 (both branch-source and branch-destination info)				Not supported
RL78	RL78/G2x	RL78/G22 RL78/G23 RL78/G24	Single-wire Serial	2 points being shared by an execution address and data access	2000 points	Forcible break by selecting "Stop" on emulator debugger	Obtains the information of up to 256 branches (only branch-source info)	Supported	Not supported; the time b/w Go and Stop is measurable.	Not supported	Not supported
	RL78/D1x	RL78/D1A		1 point being shared by an execution address and data access			Not supported				
	RL78/F1x	RL78/F12		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.				Supported
		RL78/F13 RL78/F14 RL78/F15 RL78/F1E									
	RL78/F2x	RL78/F23 RL78/F24									
	RL78/G1x	RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported				
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 256 branches (only branch-source info)				
		RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G15 RL78/G16 RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G1G RL78/G13A RL78/G1P		1 point being shared by an execution address and data access			Not supported				Not supported
	RL78/I1x	RL78/I1A		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				
		RL78/I1B RL78/I1C RL78/I1D RL78/I1E									
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported				
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)				
	RL78/H1x	RL78/H1D									
	RL78/FGIC			1 point being shared by an execution address and data access			Not supported				
RX	RX700	RX72x RX71x	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *4		Supported *3
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial								
		Others than RX64x RX65x RX66x RX67x RX26T	JTAG or double-wire Serial *2 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation				
	RX200 RX140 Other than RX26T		Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *1				Not supported
	RX100 Other than RX140						Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation		Not supported; the time b/w Go and Stop is measurable.		
RISC-V MCU	R9A02G021	R9A02G021	cJTAG	4 points being shared by an execution address and data access	2000 points for ROM/RAM area		Not supported		Not supported; the time b/w Go and Stop is measurable.		Not supported

Notes:
*1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*2. The debugging function and the connection system vary by the MCU you use.
*3. Available only when the emulator is connected via JTAG interface.
*4. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600."
*5. The internal RAM of the microcomputer is used as the trace buffer.

* The information provided only applies to MCUs where we have been able to confirm the specifications of the emulator.
This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e2

■E2 emulator Debugging Function (2)

Target MCU			Connection system	Break Function			Trace Function	Memory reference& change while executing program	Performance measurement	Trigger	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace				
RH850	RH850/F1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH	LPD4-pin or LPD1-pin	12 points being shared by an execution address and data access	2000 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Between 2K and 4K of branch information can be acquired when this is the only target or Between 1K and 2K of cycle information on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.	Supported	supported	IN:2ch OUT:2ch	Supported
	RH850/E1x	RH850/E1M-S2	LPD4-pin								
	RH850/C1x	RH850/C1H RH850/C1M									
	RH850/D1x	RH850/D1L RH850/D1M	LPD4-pin or LPD1-pin								
	RH850/P1x	RH850/P1M									
		RH850/P1M-E	LPD4-pin								
		RH850/P1H-C RH850/P1M-C RH850/P1L-C									
	RH850/E2x	RH850/E2M RH850/E2H RH850/E2UH	LPD4-pin or JTAG				Between 4K and 8K of branch information can be acquired when this is the only target or Between 2K and 4K of cycle information on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.				
	RH850/U2x	RH850/U2A RH850/U2B RH850/U2C									
R-Car	R-Car S4	-	<G4MH> LPD-4pin or JTAG <Cortex®-A,R> JTAG	<G4MH> 12 points for an execution address/a data access <Cortex®-A> 6 pints for an execution address <Cortex®-R> 6 pints for an execution address 2 pints for a data address	2048 points for ROM/RAM area		<G4MH> Between 2K and 8K of branch information can be acquired when this is the only target or Between 2K and 4K of cycle information on data-access operation can be acquired when this is the only target <Cortex®-A,R> Obtained information of branches is stored in a dedicated buffer 32KB. (both branch-source and branch-destination info)		<G4MH> Supported <Cortex®-A,R> Not supported; the time b/w Go and Stop is measurable.	Not supported	Supported
	R-Car V4M	-	JTAG	<Cortex®-A> 6 pints for an execution address <Cortex®-R> 6 pints for an execution address 2 pints for a data address			Obtained information of branches is stored in a dedicated buffer 32KB. (both branch-source and branch-destination info)		Not supported; the time b/w Go and Stop is measurable.		
	R-Car V4H	-									

Notes:
*1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*2. The debugging function and the connection system vary by the MCU you use.
*3. Available only when the emulator is connected via JTAG interface.
*4. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600."
*5. The internal RAM of the microcomputer is used as the trace buffer.

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■E2 emulator Lite Debugging Function

Target MCU			Connection system	Break Function			Trace Function	Memory reference&change while executing program	Performance measurement	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace			
RA	RA8	RA8D1/M1	SWD	8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info)	Supported	Not supported; the time b/w Go and Stop is measurable.	supported
		RA8P1 CPU0		8 points for an execution address, 8 points for a data access	2048 points for ROM/RAM area (CPU0/CPU1 shared)	Forcible break by selecting "Stop" on emulator debugger In this case, it can break CPU0/CPU1 separately or simultaneously	Obtained information of branches is stored in a dedicated buffer 8KB. (both branch-source and branch-destination info) (CPU0/CPU1 shared)			
		RA8P1 CPU1		8 points for an execution address, 4 points for a data access						
	RA6	RA6xx		6 points for an execution address, 2 points for a data access	2048 points for ROM/RAM area		Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)			
	RA4	RA4M1 RA4W1					Obtained information of branches is stored in a dedicated buffer 1KB. (both branch-source and branch-destination info)			
		Others than RA4xx					Obtained information of branches is stored in a dedicated buffer 2KB. (both branch-source and branch-destination info)			
	RA2	RA2xx		4 points for an execution address, 2 points for a data access			Obtains the information of up to 2K branches *6 (both branch-source and branch-destination info)			
	RA0	RA0xx								
RE	RE0	RE01					Obtains the information of up to 4K branches *6 (both branch-source and branch-destination info)			Not supported
RL78	RL78/G2x	RL78/G22 RL78/G23 RL78/G24	Single-wire Serial	2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 256 branches (only branch-source info)		Not supported; the time b/w Go and Stop is measurable.	
	RL78/D1x	RL78/D1A		1 point being shared by an execution address and data access			Not supported			
	RL78/F1x	RL78/F12								Supported *3
		RL78/F13 RL78/F14 RL78/F15 RL78/F1E		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.			
	RL78/F2x	RL78/F23 RL78/F24								
	RL78/G1x	RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported			Not supported
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 256 branches (only branch-source info)			
		RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G15 RL78/G16 RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G1G RL78/G13A RL78/G1P		1 point being shared by an execution address and data access			Not supported			
	RL78/I1x	RL78/I1A								
		RL78/I1B RL78/I1C RL78/I1D RL78/I1E		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported			
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
	RL78/H1x	RL78/H1D								
	RL78/FGIC			1 point being shared by an execution address and data access			Not supported			
RX	RX700	RX72x RX71x	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *5	Supported *3 *4
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)			
		Others than RX64x RX65x RX66x RX67x RX26T	JTAG or double-wire Serial *2 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation			
	RX200 RX140 Other than RX26T		Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *1			Not supported
	RX100 Other than RX140						Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation		Not supported; the time b/w Go and Stop is measurable.	
RISC-V MCU	R9A02G021	R9A02G021	cJTAG	4 points being shared by an execution address and data access	2000 points for ROM/RAM area		Not supported		Not supported; the time b/w Go and Stop is measurable.	Not supported

Notes:
*1. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*2. The debugging function and the connection system vary by the MCU you use.
*3. Hot-plug Adapter for the E1 Emulator (optional) is required.
*4. Available only when the emulator is connected via JTAG interface.
*5. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600.
*6. The internal RAM of the microcomputer is used as the trace buffer.

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■E1 emulator Debugging Function (1)

Target MCU			Connection system	Break Function			Trace Function	Memory reference&change while executing program	Performance measurement	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace			
RH850	RH850/F1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH	LPD4-pin or LPD1-pin	12 points being shared by an execution address and data access	2000 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Between 2K and 4K of branch information can be acquired when this is the only target or Between 1K and 2K of cycle information on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.	Supported	supported	Supported *5
	RH850/E1x	RH850/E1M-S2	LPD4-pin							
	RH850/C1x	RH850/C1H RH850/C1M								
	RH850/D1x	RH850/D1L RH850/D1M	LPD4-pin or LPD1-pin							
		RH850/P1M								
	RH850/P1x	RH850/P1M-E	LPD4-pin							
		RH850/P1H-C RH850/P1M-C RH850/P1L-C								
RL78	RL78/D1x	RL78/D1A	Single-wire Serial	1 point being shared by an execution address and data access	2000 points		Not supported		Not supported; the time b/w Go and Stop is measurable.	Not supported
	RL78/F1x	RL78/F12								
		RL78/F13 RL78/F14 RL78/F15 RL78/F1E		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.			Supported *5
	RL78/G1x	RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported			Not supported
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 256 branches (only branch-source info)			
		RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G1G RL78/G13A RL78/G1P		1 point being shared by an execution address and data access			Not supported			
	RL78/I1x	RL78/I1A								
		RL78/I1B RL78/I1C RL78/I1D RL78/I1E		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported			
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)			
	RL78/H1x	RL78/H1D								
	RL78/FGIC			1 point being shared by an execution address and data access			Not supported			
RX	RX700	RX72x RX71x	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)		Supported *7	Supported *5 *6
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)			
		Others than RX64x RX65x RX66x RX67x RX26T	JTAG or double-wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation			
	RX200 RX140 Other than RX26T		Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation *3			Not supported
	RX100 Other than RX140						Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation		Not supported; the time b/w Go and Stop is measurable.	
V850 *1 *2	V850E1 V850ES V850E2		JTAG, double-wire or 4-wire Serial (data × 2, clock and handshake)	2 points being shared by an execution address and data access * Sequential breaks are specifiable.	4 points for ROM area 2000 points for RAM area		Not supported		Not supported; the time b/w Go and Stop is measurable.	
	V850E2M V850E2S		Nexus or Single-wire Serial	[When using JTAG I/F] Before-execution: 4 points After-execution: 8 points Access: 6 points [When using Serial I/F] Before-execution: 4 points After-execution: Not supported Access: 4 points * Sequential breaks are specifiable.	8 points for ROM area 2000 points for RAM area					Supported *5

Notes:
*1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
*2. The number of break points varies by the integrated development environment you use.
*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*4. The debugging function and the connection system vary by the MCU you use.
*5. Hot-plug Adapter for the E1 Emulator (optional) is required.
*6. Available only when the emulator is connected via JTAG interface.
*7. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600.

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This includes MCUs and emulator software that are under development. For more information on support for these items as it becomes available, check our website at: https://www.renesas.com/e1

■E1 emulator Debugging Function (2)

Target MCU			Connection system	Break Function			Trace Function	Memory reference& change while executing program	Performance measurement	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace			
78K0R			Single-wire Serial or double-wire Serial (clock and data)	1 point being shared by an execution address and data access	2000 points		Not supported			
78K0			double-wire Serial (clock and data)	1 point for a before-execution break (only when software breaks are not used) + 1 point for Access break	2000 points		Not supported			
R8C	R8C/L35C, R8C/L36C, R8C/L38C and R8C/L3AC Groups R8C/L35M, R8C/L36M, R8C/L38M and R8C/L3AM Groups R8C/LA6A and R8C/LA8A Groups R8C/LA3A and R8C/LA5A Groups R8C/LAPS Group		Single-wire Serial	8 points for an address break + 2 points for a data condition break * Sequential breaks are specifiable.	256 points at the max	Forcible break by selecting "Stop" on emulator debugger	Obtains the information of 4 branches (sum of the branch-source and branch-destination PC) or the information of up to 8 cycles of specified data access	Supported	Not supported; the time b/w Go and Stop is measurable.	Not supported
	R8C/5x									
	R8C/3xT-A									
	R8C/32C, R8C/33C, R8C/34C, R8C/35C, R8C/36C, R8C/38C, R8C/3GC and R8C/3JC Groups R8C/32M, R8C/33M, R8C/34M, R8C/35M, R8C/36M, R8C/38M, R8C/3GM and R8C/3JM Groups R8C/33T, R8C/3JT and R8C/3NT Groups R8C/34W, R8C/36W and R8C/38W Groups R8C/34X, R8C/36X and R8C/38X Groups R8C/34Y, R8C/36Y and R8C/38Y Groups R8C/34Z, R8C/36Z and R8C/38Z Groups R8C/32G, R8C/32H, R8C/33G, R8C/33H, R8C/34P and R8C/34R Groups R8C/34K, R8C/34U, R8C/3MK and R8C/3MU Groups R8C/3MQ Group									

Notes:
*1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
*2. The number of break points varies by the integrated development environment you use.
*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*4. The debugging function and the connection system vary by the MCU you use.
*5. Hot-plug Adapter for the E1 Emulator (optional) is required.
*6. Available only when the emulator is connected via JTAG interface.

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■E20 emulator Debugging Function (1)

Target MCU			Connection system	Break Function			Trace Function		Memory reference& change while executing program	Performance measurement	Real-time RAM monitor	C0 coverage	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace	External Trace					
RH850	RH850/F1x	RH850/F1H RH850/F1M RH850/F1L RH850/F1K RH850/F1KM RH850/F1KH	LPD4-pin or LPD1-pin	12 points being shared by an execution address and data access	2000 points for ROM/RAM area	Forcible break by selecting "Stop" on emulator debugger	Between 2K and 4K of branch info can be acquired when this is the only target or Between 1K and 2K of cycle info on data-access operation can be acquired when this is the only target Trace function isn't supported in some MCU's.	Not supported	Supported	Supported	Not supported	Not supported	Supported
	RH850/E1x	RH850/E1M-S2	LPD4-pin										
	RH850/C1x	RH850/C1H RH850/C1M											
	RH850/D1x	RH850/D1L RH850/D1M	LPD4-pin or LPD1-pin										
	RH850/P1x	RH850/P1M											
		RH850/P1M-E	LPD4-pin										
		RH850/P1H-C RH850/P1M-C RH850/P1L-C											
RL78	RL78/D1x	RL78/D1A	Single-wire Serial	1 point being shared by an execution address and data access	2000 points		Not supported	Not supported	Supported	Not supported; the time b/w Go and Stop is measurable.	Not supported	Not supported	Not supported
	RL78/F1x	RL78/F12											
		RL78/F13 RL78/F14 RL78/F15 RL78/F1E		2 points being shared by an execution address and data access			Obtains the information of up to 128 branches (only branch-source info); the obtainable info is limited to 64 branches on some MCUs.						Supported
	RL78/G1x	RL78/G10 RL78/G1M RL78/G1N		2 points for an execution address	Not supported		Not supported						Not supported
		RL78/G14 (ROM: 96KByte and more) RL78/G1F RL78/G1H		2 points being shared by an execution address and data access	2000 points		Obtains the information of up to 256 branches (only branch-source info)						
		RL78/G11 RL78/G12 RL78/G13 RL78/G14 (ROM: 64KByte and less) RL78/G1A RL78/G1C RL78/G1D RL78/G1E RL78/G1G RL78/G13A RL78/G1P		1 point being shared by an execution address and data access			Not supported						
	RL78/I1x	RL78/I1A		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)						
		RL78/I1B RL78/I1C RL78/I1D RL78/I1E											
	RL78/L1x	RL78/L12 RL78/L13		1 point being shared by an execution address and data access			Not supported						
		RL78/L1A RL78/L1C		2 points being shared by an execution address and data access			Obtains the information of up to 256 branches (only branch-source info)						
	RL78/H1x	RL78/H1D											
	RL78/FGIC			1 point being shared by an execution address and data access			Not supported						
RX	RX700	RX71x	JTAG only or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.	256 points at the max		Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	-		Supported *6	Not supported	Not supported	Supported *5
			JTAG + External Trace	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation (DMAC or DTC bus is selectable as a bus master)			Supported (Data- and Last-access attributes [Read/Write/Non-accessed])	Supported	
	RX600	RX64x RX65x RX66x RX67x RX26T	JTAG only or Single-wire Serial	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	-			Not supported	Not supported	
		RX64x RX65x RX66x RX67x	JTAG + External Trace	8 points for an execution address + 4 points for a data access (DMAC or DTC bus is selectable as a bus master) * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation (DMAC or DTC bus is selectable as a bus master)	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation (DMAC or DTC bus is selectable as a bus master)			Supported (Data- and Last-access attributes [Read/Write/Non-accessed])	Supported	
		Others than RX64x RX65x RX66x RX67x RX26T	JTAG only or double-wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation	-			Not supported	Not supported	
			JTAG or double-wire Serial *4 (clock and data)	8 points for an execution address + 4 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 256 branches or the information of up to 256 cycles on data-access operation	Obtains the information of approx. 2M branches or the information of approx. 2M cycles on data access operation			Supported (Data- and Last-access attributes [Read/Write/Non-accessed])		
	RX200 RX140 Other than RX26T		Single-wire Serial	4 points for an execution address + 2 points for a data access * Sequential breaks are specifiable.			Obtains the information of up to 64 branches or the information of up to 64 cycles on data-access operation*3	Not supported			Not supported	Not supported	Not supported
	RX100 Other than RX140						Obtains the information of up to 32 branches or the information of up to 32 cycles on data-access operation			Not supported; the time b/w Go and Stop is measurable.			

Notes:
*1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
*2. The number of break points varies by the integrated development environment you use.
*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*4. The debugging function and connection system vary by the MCU you use.
*5. Available only when the emulator is connected via JTAG interface.
*6. 1 sections can be gauged with RX100. 2 sections can be gauged with RX600.

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■E20 emulator Debugging Function (2)

Target MCU			Connection system	Break Function			Trace Function		Memory reference&change while executing program	Performance measurement	Real-time RAM monitor	C0 coverage	Hot plug-in
Family	Series/Core	Group		Hardware Break	Software Break	Special Break	Internal trace	External Trace					
V850 *1 *2	V850E1 V850ES V850E2		JTAG, double-wire or 4-wire Serial (data × 2, clock and handshake)	2 points being shared by an execution address and data access * Sequential breaks are specifiable.	4 points for ROM area 2000 points for RAM area	Forcible break by selecting "Stop" on emulator debugger	Not supported	Not supported	Not supported	Not supported; the time b/w Go and Stop is measurable.	Not supported	Not supported	Not supported
	V850E2M V850E2S		Nexus or Single-wire Serial	[When using JTAG I/F] Before-execution: 4 points After-execution: 8 points Access: 6 points [When using Serial I/F] Before-execution: 4 points After-execution: Not supported Access: 4 points * Sequential breaks are specifiable.	8 points for ROM area 2000 points for RAM area								Supported
78K0R			Single-wire Serial or double-wire Serial (clock and data)	1 point being shared by an execution address and data access	2000 points								Not supported
78K0			double-wire Serial (clock and data)	1 point for a before-execution break (only when software breaks are not used) + 1 point for an access break									
R8C	R8C/L35C, R8C/L36C, R8C/L38C and R8C/L3AC Groups R8C/L35M, R8C/L36M, R8C/L38M and R8C/L3AM Groups R8C/LA6A and R8C/LA8A Groups R8C/LA3A and R8C/LA5A Groups R8C/LAPS Group		Single-wire Serial	8 points for an address break + 2 points for a data condition break * Sequential breaks are specifiable.	256 points at the max		Obtains the information of 4 branches (sum of the branch-source and branch-destination PC) or the information of up to 8 cycles of specified data access					
	R8C/5x												
	R8C/3xT-A												
	R8C/32C, R8C/33C, R8C/34C, R8C/35C, R8C/36C, R8C/38C, R8C/3GC and R8C/3JC Groups R8C/32M, R8C/33M, R8C/34M, R8C/35M, R8C/36M, R8C/38M, R8C/3GM and R8C/3JM Groups R8C/33T, R8C/3JT and R8C/3NT Groups R8C/34W, R8C/36W and R8C/38W Groups R8C/34X, R8C/36X and R8C/38X Groups R8C/34Y, R8C/36Y and R8C/38Y Groups R8C/34Z, R8C/36Z and R8C/38Z Groups R8C/32G, R8C/32H, R8C/33G, R8C/33H, R8C/34P and R8C/34R Groups R8C/34K, R8C/34U, R8C/3MK and R8C/3MU Groups R8C/3MQ Group												

Notes:
*1. V850E2/ME3 and V850E/ME2 cannot be used with the E1 emulator. Use the MINICUBE for them.
*2. The number of break points varies by the integrated development environment you use.
*3. For RX220 group, the information of 32 branches or the information of 32 cycles on data-access operation is obtained.
*4. The debugging function and connection system vary by the MCU you use.
*5. Available only when the emulator is connected via JTAG interface.

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■MINICUBE2 Debugging Function

Target MCU			Break Function			RAM Monitor	DMM (Rewriting memories during RUN)	Time Measurement (from the start of execution to break)
Family	Series/ Core	Group	Hardware Break	Software Break	Forcible break			
V850	V850E1 V850ES V850E2		2 points *1 (Shared by an execution and access)	ROM area: 4 points RAM area: 2000 points	Supported *2	Supported	Supported	Measurement resolution: 100 μs Max. measurement time: Approx. 100 hours
	V850E2M V850E2S		Before-execution break : 4 points Access break : 4 points * Sequential breaks are specifiable.	ROM area: 8 points RAM area: 2000 points	Supported			
78K0R			1 point (Shared by an execution and access)	2000 points	Supported	Pseudo-Real RAM Monitor (RRM) : Supported	Supported	Measurement resolution: 100 μs Max. measurement time: Approx. 100 hours
78K0			Before-execution break : 1 point (Not supported when software breaks are used) Access break : 1 point	2000 points	Supported	Pseudo-Real RAM Monitor (RRM) : Supported	Supported	Measurement resolution: 100 μs Max. measurement time: Approx. 100 hours
78K0S			Not supported	2000 points	Supported (Not supported while interrupts are inhibited)	Not supported	Not supported	Measurement resolution: 100 μs Max. measurement time: Approx. 100 hours

Notes:
*1. The following MCUs have not been supported yet: V850ES/KE2, V850ES/KF2, V850ES/KG2, μPD70F3733, and V850ES/IE2.
*2. A forcible break is not possible in the following states.
- Interrupts are inhibited (DI).
- Interrupts from the serial interface used for communications between MINICUBE2 and the target device are masked.
- The device is on standby and triggering of release from standby by makeable interrupts is disabled.
- The main clock is stopped while the UART is being used as the communications interface between MINICUBE2 and the target device.

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https://www.renesas.com/cs+ ＞ "Functions Supported by CS+"(PDF)

■E10A-USB (HS0005KCU01H/HS0005KCU02H) Debugging Function (1)

Target MCU			Break Function		Performance Measurement Function	Invalid External extension Mode of Embedded ROM	Trace Function	
Family	Series/ Core	Group	Hardware Break	Software Break			Internal Trace	AUD Trace
SuperH	SH-4A (Except for Multi-core MCUs)		Address/Data/R/W/Execution-count condition break : 2 points + Address/R/W condition break : 4 points + Data/R/W condition break : 2 points + System bus condition break : 2 points * Sequential breaks are specifiable.	255 points	Supported	No Mode	8 branches ◎	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ◎
	SH-4	SH7760 SH7751R	Address/Data/R/W : 2 points + Address/R/W condition break : 4 points * Sequential breaks are specifiable.		Supported	No Mode	8 branches	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ◎
		SH7750R				No Mode		-
	SH-3	SH7721 SH7720 SH7712 SH7710 SH7705	Address/Data/R/W/Execution-count condition break : 1 point + Address/R/W condition break : 1 point * Sequential breaks are specifiable.		Supported	No Mode	8 branches	Up to 64K branches *1 (Only branch-destination information) ◎
		SH7727 SH7709S SH7706				No Mode		Up to 26214 branches *1
	SH-2A (Except for Multi-core MCUs)	SH7206	Address break : 8 points + Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point * Sequential breaks are specifiable.		Supported	No Mode	1000 cycles Select the target info from: Address/Data/Status/ Time stamp bus.	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ◎
		SH72AY SH72AW SH72A0 SH72A2						
		SH7211 SH7216 (SH7216, SH7214) SH7231 SH7237 SH7239 SH7243 SH7285 SH7286				Supported		
		SH7670 SH726A SH726B SH7269 SH7268 SH7267 SH7266 SH7264 SH7262 SH7203 SH7263				No Mode	256 cycles Select the target info from: Address/Data/Status/ Time stamp bus.	
		SH7201 SH7261			-	No Mode	-	
		SH7256R SH7254R				Supported		
		SH7253				No Mode		-
	SH-2	SH7619 SH7618	Address/Data/R/W/Execution-count condition break : 1 point + Address/R/W condition break : 1 point * Sequential breaks are specifiable.		-	No Mode	4 branches	-
		SH7145F SH7144F SH7047F	Address break : 4 points * Sequential breaks are specifiable.			-	-	Up to 64K events *2 (Up to 32K of branch information can be acquired when branch trace is the only target)
		R5F71494A R5F71464A R5F70865A R5F70855A R5F70854A R5F70845A R5F70844A R5F70835A R5F70834A	Address break : 2 points + Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point * Sequential breaks are specifiable.		Supported	Supported	4 branches	-
		SH7137			-	Supported		
		SH7136 SH7125 SH7124				No Mode		
		R5E71494R R5E71491R R5E71464R R5E70865R R5E70855R R5E70845R R5E70835R	Address break : 8 points + Address/Data/R/W/Execution-count condition break : 1 point + Address/Data/R/W condition break : 1 point * Sequential breaks are specifiable.		Supported	Supported	1000 cycles Select the target info from: Address/Data/Status/ Time stamp bus.	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ◎
H8SX	H8SX/1700	H8SX/1720S H8SX/1720	Address break : 3 points + Address/Data/Satisfaction-count condition break : 1 point * Sequential breaks are specifiable.		Supported	- *3	8 branches	-
	H8SX/1600							
	H8SX/1500				-			
H8S	H8S/2400	H8S/2472 H8S/2463 H8S/2462	Address break : 6 points + Address/Data condition break : 2 points		-	-	4 branch sources	-
		H8S/2456R H8S/2456 H8S/2454 H8S/2426R H8S/2426 H8S/2424				Supported	4 branch sources or Bus trace : 1024 cycles	
		H8S/2427R H8S/2427 H8S/2425					8 branch sources	
	H8S/2300	H8S/2378 H8S/2378R H8S/2368 H8S/2319 *4	Address/Data condition break : 2 points			-	4 branch sources or Bus trace : 512 cycles	
		H8S/2339 *5 H8S/2329 *6				Supported	4 branch sources	
	H8S/2200	H8S/2218 H8S/2215 *7 H8S/2212	Address/Data condition break : 2 points		-	-	4 branch sources	-

Notes:
*1. Not usable with HS0005KCU01H.
*2. Not usable with HS0005KCU01H. While using RAM monitor function with HS0005KCU02H, no trace information can be acquired.
*3. Supported only by H8SX/1651.
*4. Only H8S/2319EF is supported.
*5. Only H8S/2339EF is supported.
*6. Only H8S/2329EF is supported.
*7. Only H8S/2215R and H8S/2215T are supported.

◎ Acquirable trace information:
Branch, Memory access within the specified range, and Software trace (Trace(x): variable x).

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■E10A-USB（HS0005KCU01H/HS0005KCU02H）Debugging Function (2)

Target MCU			Break Function		Performance Measurement Function	Invalid External extension Mode of Embedded ROM	Trace Function	
Family	Series/ Core	Group	Hardware Break	Software Break			Internal Trace	AUD Trace
H8S	H8S/2100	H8S/2168 H8S/2153 H8S/2164 H8S/2117 H8S/2117R H8S/2125 H8S/2116 H8S/2113 H8S/2112 H8S/2112R	Address break : 6 points ＋ Address/Data condition break : 2 points	255 points	Not supported	No Mode	4 branch sources	Not supported
		H8S/2189R H8S/2114R	Address break : 6 points ＋ Address/Data condition break : 2 points				4 branch sources or Bus trace : 512 cycles	

Notes:
*1. Not usable with HS0005KCU01H.
*2. Not usable with HS0005KCU01H. While using RAM monitor function with HS0005KCU02H, no trace information can be acquired.
*3. Supported only by H8SX/1651.
*4. Only H8S/2319EF is supported.
*5. Only H8S/2339EF is supported.
*6. Only H8S/2329EF is supported.
*7. Only H8S/2215R and H8S/2215T are supported.

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■E10A-USB（HS0005KCU01H/HS0005KCU02H ＋ Debug MCU Board） Debugging Function

Target MCU			Break Function		Performance Measurement Function	Invalid External extension Mode of Embedded ROM	Trace Function	
Family	Series/ Core	Group	Hardware Break	Software Break			Internal Trace	AUD Trace
SuperH	SH-4A	SH7456 SH7455 SH7451 SH7450	Address/Data/R/W/Execution-count condition break : 2 points ＋ Address/R/W condition break : 4 points ＋ Data/R/W condition break : 2 points ＋ System bus condition break : 2 points * Sequential breaks are specifiable.	255 points	Supported	No Mode	8 branches ◎	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target) ◎
	SH-2	SH7125 SH7124	Address break : 8 points ＋ Address/Data/R/W/Execution-count condition break : 1 point ＋ Address/Data/R/W condition break : 1 point * Available to specify the sequential break		Supported	No Mode	1000 cycles Select the target one from Address/Data/Status/ Time stamp bus.	Up to 64K events *1 (Up to 32K of branch information can be acquired when branch trace is the only target.) ◎
H8S	H8S/2400	H8S/2456R H8S/2456 H8S/2454 H8S/2426R H8S/2426 H8S/2424	Address break : 6 points ＋ Address/Data condition break : 2 points		Not supported	Supported	4 branch sources or Bus trace : 1024 cycles	Not supported

Note:
*1. Not usable with HS0005KCU01H.
◎ Acquirable trace information: Branch, Memory access within the specified range, and Software trace (Trace(x): variable x).

■E10A-USB（HS0005KCU14H） Debugging Function

Target MCU			Break Function		Performance Measurement Function	Invalid External extension Mode of Embedded ROM	Trace Function	
Family	Series/ Core	Group	Hardware Break	Software Break			Internal Trace	AUD Trace
SuperH	SH-4A (Multi-core MCU)	SH7786	10 points (Using UBC module)	255 points (for each core in MCU)	Supported	No Mode	60 sets of branch sources and destinations	Up to 128K events (Up to 64K of branch information can be acquired when branch trace is the only target) ◎
	SH-2A (Multi-core MCU)	SH7205 SH7265					1024 cycles (When acquiring trace info by core in MCU, 512 cycles respectively.)	

◎ Acquirable trace acquisition information: Branch, Memory access, and General register. (Conditions are settable by each CPU.)

■E8a Debugging Function

Target MCU			Break Function			Trace Function
Family	Series/ Core	Group	Hardware Break	Software Break	Special Break	Internal Trace
R8C	R8C/Lx		Address break : 8 points + Data condition break : 2 points * Sequential breaks are specifiable.	255 points	Forcible break by selecting "Stop" on emulator debugger	4 branches (sum of branch source PC and destination PC) or Up to 8 cycles of specified data access
	R8C/Mx		Address break : 4 points + Data condition break : 1 point			3 branches (sum of branch source PC and destination PC) or 6 branches (branch source PC) or Up to 8 cycles of specified data access
	R8C/3x	Other than R8C/3xD	Address break : 8 points + Data condition break : 2 points * Sequential breaks are specifiable.			4 branches (sum of branch source PC and destination PC) or Up to 8 cycles of specified data access
		R8C/3xD	Address break : 4 points or Address break : 2 points ＋ Data condition break : 1 point			The latest 4 branches (branch source PC)
	R8C/2x					
	R8C/1x	Other than R8C/10-13				
		R8C/10-13	Address break : 2 points			-
M16C	R32C/100		Address break : 8 points			-
	M32C/80					
	M16C/60	M16C/62P M16C/6Nx M16C/6S				
		M16C/63 M16C/64A M16C/64C M16C/65 M16C/65C M16C/6C	Address break : 8 points + Data condition break : 2 points * Sequential breaks are specifiable.			32 branches of order execution history (sum of branch source PC and destination PC) or Up to 64 cycles of specified data access
		M16C/6S1 M16C/6B				16 branches of order execution history (sum of branch source PC and destination PC) or Up to 32 cycles of specified data access
	M16C/50					32 branches of order execution history (sum of branch source PC and destination PC) or Up to 64 cycles of specified data access
	M16C/Tiny		Address break : 6 points			-
H8S	H8S/Tiny		Address break : 8 points ＋ Address/Data condition break : 2 points			The latest 8 branch sources or The latest 4 branch sources ＋ 4 branch destinations
H8	H8/300H Tiny		Address/Data condition break : 1 point			The latest 4 branch sources
	H8/300H Super Low Power		Address break : 1 point ＋ Address/Data condition break : 1 point			
	H8/300L Super Low Power		Address/Data condition break : 1 point			
740			Address break : 2 points			-

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