EL4340EVAL1

Evaluation Board User's Guide

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Introduction

The EL4340EVAL1 evaluation board contains all the circuitry needed to characterize critical performance parameters of the EL4340 triple 2:1 MUX-amplifier, over a variety of applications.

The EL4340 contains 3 separate 2 input multiplexers, each followed by a unity gain buffer controlled by a common set of logic inputs (Figure 1, Table 1). Control features include a high speed (20ns) HIZ output control for individual selection of MUX amps that share a common video output line. A control logic latch ($\overline{LE}$) enables multiple devices to share a common input control logic bus. The $\overline{ENABLE}$ control can be used to save power by powering the device down.

The evaluation board circuit and layout is optimized for either 50Ω or 75Ω terminations, and implements a basic R-G-B video 2 input MUX-amp. The board is supplied with 75Ω input signal terminations and a 75Ω back-termination resistor on each of the 3 outputs, making it suitable for driving video cable. The user has the option of replacing the 75Ω resistors with 50Ω resistors for other applications. The control lines contain 50Ω resistors to match the 50Ω output impedance of high speed pulse generators. Control line termination resistors are recommended for rise and fall times under 10ns to minimize unwanted transients. If DC is used for the control logic, the resistors may be removed; or the applied DC voltage can reduced to 2.5V to reduce the dissipation in the termination resistor.

The layout contains component options to include an output series resistor (R_S) followed by a parallel resistor (R_L) capacitor (C_L) network to ground. This option allows the user to select several different output configurations. Examples are shown in Figures 2A, 2B, and 2C. The evaluation board is supplied with the 75Ω back termination resistors shown in Figure 2C.

Amplifier Performance and Output Configurations

The EL4340 output amplifiers are designed for maximum gain-bandwidth performance when loaded with ~500Ω (R_L) in parallel with ~5pF (C_L) to ground, directly at the output pin (Figure 2A). They are ideally suited for driving high impedance high speed selectable-gain buffers when gain compensation is needed. In these applications, output trace capacitance to 5pF actually optimizes AC performance. For trace capacitance below 5pF, an additional capacitor between the output pin to ground may be added to achieve the 5pF optimum. GBW decreases slightly at the lower output load impedances typical of back-terminated cable driving applications.

High Frequency Layout Considerations

At frequencies of 500MHz and higher, circuit board layout may limit performance. The following layout guidelines are implemented on the evaluation board;

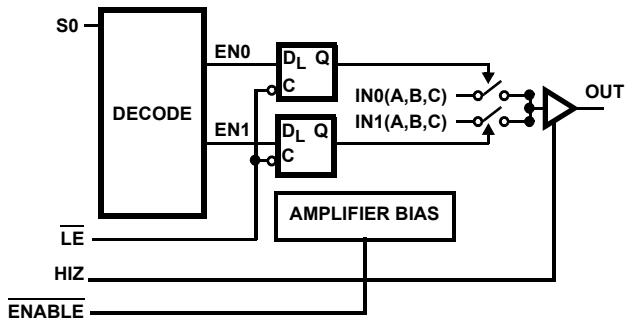
- Signal I/O lines are the same lengths and widths to match propagation delay and trace parasitics,
- No series connected vias are used in signal I/O lines, as they can add unwanted inductance,
- Signal trace lengths are minimized to reduce transmission line effects and the need for strip-line tuning of the signal traces.
- High frequency decoupling caps are places as close to the device power supply pin as possible - without series vias between the capacitor and the device pin.

Power Sequencing

Proper power supply sequencing is -V first, then +V. In addition, the +V and -V supply pin voltage rate-of-rise must be limited to ±1V/µs or less. The evaluation board contains parallel-connected low V_{ON} Shottky diodes on each supply terminal to minimize the risk of latch up due to incorrect sequencing. In addition, extra 10µF decoupling capacitors are added to each supply to aid in reducing the applied voltage rate-of-rise.

Reference Documents

1. EL4340 Data Sheet, FN7421.0

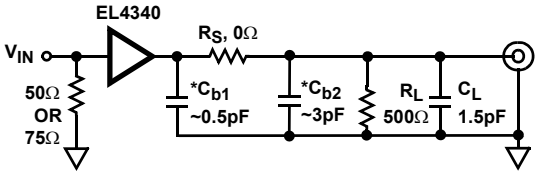


A logic high on $\overline{LE}$ will latch the last S0 state. This logic state is preserved when cycling HIZ or $\overline{ENABLE}$ functions.

FIGURE 1. EL4340 FUNCTIONAL BLOCK DIAGRAM (1 OF 3 CHANNELS)

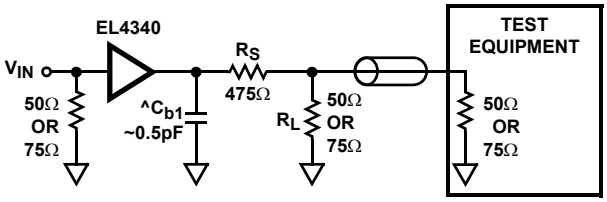
TABLE 1. LOGIC TABLE

S0	HIZ	ENABLE	LENABLE	OUTA,B,C
0	0	0	0	IN0A,B,C
1	0	0	0	IN1A,B,C
-	1	0	-	Hi Z
-	-	1	-	Power down
-	0	0	1	Last S0 selection



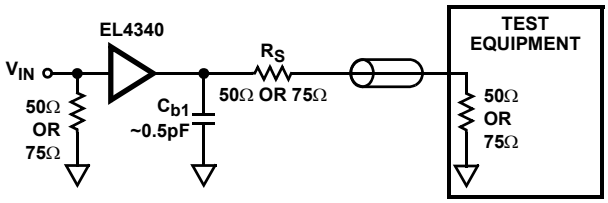
* C_{b1}, C_{b2} are approximate PCB trace capacitances.

FIGURE 2A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD



* C_{b1} is approximate PCB trace capacitance.

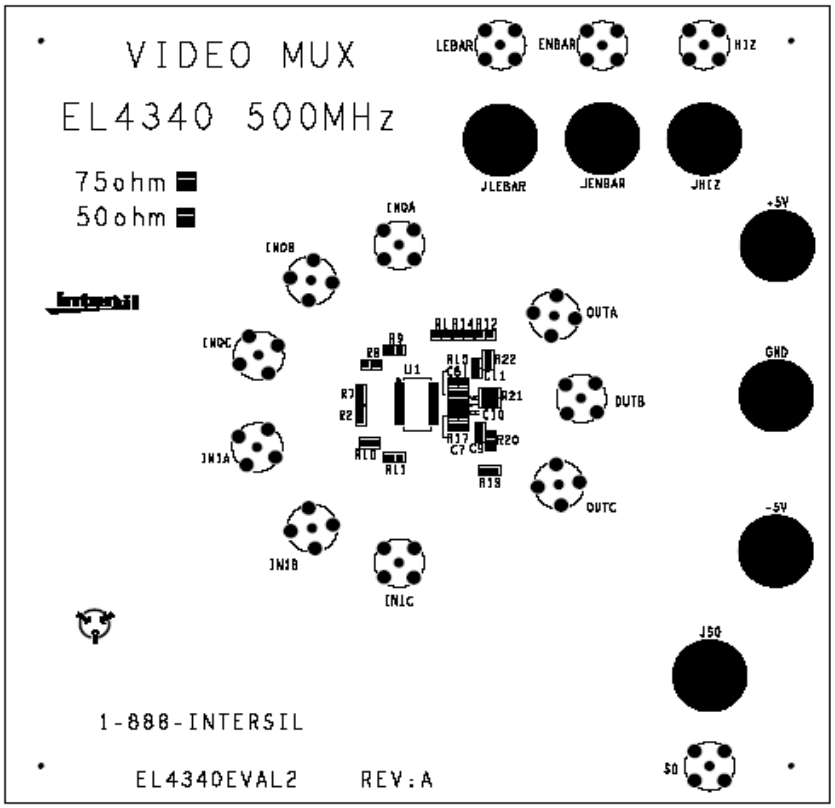
FIGURE 2B. TEST CIRCUIT FOR 50Ω OR 75Ω TERMINATIONS



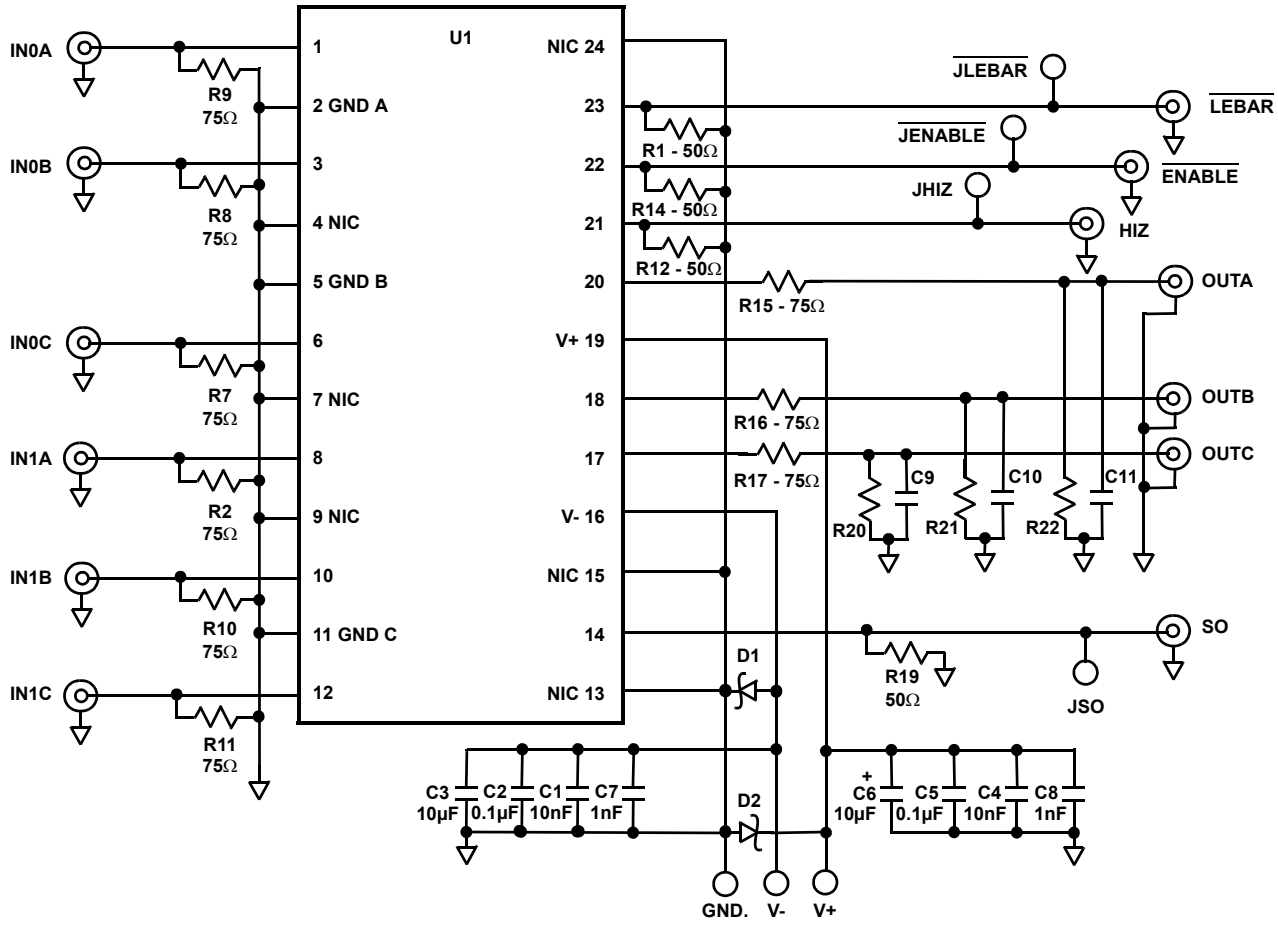
* C_{b1} is approximate PCB trace capacitance.

FIGURE 2C. BACK-TERMINATED TEST CIRCUIT FOR CABLE APPLICATION

EL4340EVAL1 Top View



EL4340EVAL1 Schematic Diagram



EL4340EVAL1 Components Parts List

DEVICE #	DESCRIPTION	COMMENTS
C7, C8	CAP, SMD, 0603, 1000pF, 25V, 10%, X7R	Power Supply Decoupling
C1, C4	CAP, SMD, 0603, 0.01µF, 25V, 10%, X7R	Power Supply Decoupling
C2, C5	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R	Power Supply Decoupling
C3, C6	CAP, SMD, 0805, 10µF, 6.3V, 10%, X5R	Power Supply Decoupling
D1, D2	Diode-Shottky, 2 Pin, 45V, 7.5A	MBR0550T (Motorola) Reverse Polarity Protection
R2, R7-R11, R15-R17	Resistor, SMD, 0603, 75Ω, 1/10W, 1%,	Signal Input/output Termination
R1, R12, R14, R19	Resistor, SMD, 0603, 49.9Ω, 1/16W, 1%,	Logic Input Termination
C9, C10, C11	Resistor, SMD, 0603	Optional, not populated
R20, R21, R22	Resistor, SMD, 0603	Optional, not populated
U1	EL4340IU -500MHz Multiplexing Amplifier, 24P, QSOP	Device Under Test

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