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1. Introduction

Device Overview

The FemtoClock® NG 5mm x 7mm devices are clock frequency sources with the capability to program the output frequency over a wide range and to a high resolution. They use the 4th generation fractional-feedback PLL technology from IDT and integrate the crystal within the package.

In contrast to the complex and expensive frequency control techniques of traditional oscillators, the IDT devices are configured by a simple and fast register write operation through a standard I^2C interface. Both in-field programming and factory pre-set configurations for the output frequency and VCXO pull range are supported.

This document gives the necessary information and procedures for in-field programming of the various devices in this family. For this purpose, the functionality and operation principles are explained, along with the complete set of configuration settings and optimization strategies that are required for a successful use.

The information given in this document applies to the following devices:

- IDT8N3Q001 revision G
- IDT8N3Q003 revision G
- IDT8N3QV01 revision G
- IDT8N4Q001 revision G
- IDT8N4Q003 revision G
- IDT8N4QV01 revision G
- IDT8N0Q001 revision G
- IDT8N0QV01 revision G
- IDT8N3SV75 revision C
- IDT8N3DV85 revision C
- IDT8N3S270 revision C
- IDT8N3S271 revision C
- IDT8N3S272 revision C
- IDT8N3S273 revision C
- IDT8N3D085 revision C
- IDT8N4SV75 revision C
- IDT8N4DV85 revision C
- IDT8N4S270 revision C
- IDT8N4S271 revision C
- IDT8N4S272 revision C
- IDT8N4S273 revision C

Document Conventions and Definitions

This manual uses the following conventions and terms:

- XO: Crystal oscillator
- VCXO: Voltage-controlled crystal oscillator
- Any-frequency device: device that supports the configuration of the output frequency with a high resolution and over a wide frequency range
- Integer-ratio device: device that supports the output frequency configuration to a range of discrete frequencies determined by integer dividers
- A register name in *italics* indicates a generic register
- A register name in normal font indicate an addressable register
- The prefix “n“ indicates the negative (inverted) signal of a differential pair, such as in “nQ” (the inverted output signal)
- The suffix “n“ indicates the index to a register. In example, INTn denominates a range of register bit positions INT0, INT1, INT2 etc.

Additional Resources

In addition to this programming guide, please refer to the following documents for related information:

- Individual device datasheets for electrical, mechanical and pinout information. Refer to www.idt.com or your sales representative
- FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information. This document contains the frequency order codes and explains the order scheme in detail. Refer to www.idt.com or your sales representative.
- IDT technical support at netcom@idt.com.

Selector Guide

Table 1. FemtoClock NG 5x7 Ceramic Base Part Numbers

Type	Part Number	Package		Output Levels			Int. XTAL		Output Frequency, Resolution				
		6 pin	10 pin	LVPECL	LVDS	LVCMOS	114.285 MHz	100 MHz	fmax (MHz)	0.2 ppm	#Default Freq.	I2C	Die Rev
XO	8N3Q001		Y	Y			Y	Y	1300	Y	4	Y	G
	8N3Q003		Y	Y			Y	Y	1300	Y	4	Y	G
	8N4Q001		Y		Y		Y	Y	1300	Y	4	Y	G
	8N4Q003		Y		Y		Y	Y	1300	Y	4	Y	G
	8N0Q001		Y			Y	Y	Y	260	Y	4	Y	G
	8N3D085	Y		Y			Y	Y	1300	Y	2		C
	8N3S270	Y		Y			Y	Y	1300	Y	1		C
	8N3S271	Y		Y			Y	Y	1300	Y	1		C
	8N3S272	Y		Y			Y	Y	1300	Y	1		C
	8N3S273	Y		Y			Y	Y	1300	Y	1		C
	8N4S270	Y			Y		Y	Y	1300	Y	1		C
	8N4S271	Y			Y		Y	Y	1300	Y	1		C
	8N4S272	Y			Y		Y	Y	1300	Y	1		C
VCXO	8N3QV01		Y	Y			Y		1300	Y	4	Y	G
	8N4QV01		Y		Y		Y		1300	Y	4	Y	G
	8N0QV01		Y			Y	Y		260	Y	4	Y	G
	8N3SV75	Y		Y			Y		1300	Y	1		C
	8N3DV85	Y		Y			Y		1300	Y	2		C
	8N4SV75	Y			Y		Y		1300	Y	1		C
	8N4DV85	Y			Y		Y		1300	Y	2		C

Pinout

Table 2. FemtoClock NG 5x7 Pinout Information

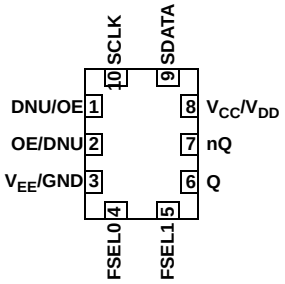
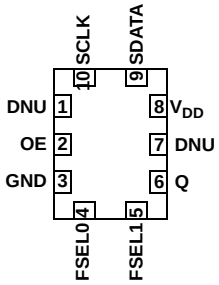
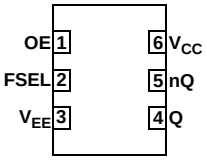
Type	Part Number	# Pins	Pinout	#	Name	Description
XO	8N3Q001 8N4Q001 8N3Q003 8N4Q003	10		1	DNU OE	8N3Q001: Do not use 8N4Q001: Do not use 8N3Q003: Output enable. LVCMOS/LVTTL levels. 8N4Q003: Output enable. LVCMOS/LVTTL levels.
				2	OE DNU	8N3Q001: Output enable. LVCMOS/LVTTL levels. 8N4Q001: Output enable. LVCMOS/LVTTL levels. 8N3Q003: Do not use 8N4Q003: Do not use
				3	V_{EE} GND	8N3Q001, 8N3Q003: (V_{EE}) Negative power supply. 8N4Q001, 8N4Q003: (GND) Negative power supply.
				4	FSEL0	Default frequency select pins. LVCMOS/LVTTL interface levels.
				5	FSEL1	
				6	Q	Differential clock output. 8N3Q001, 8N3Q003: LVPECL interface levels. 8N4Q001: 8N4Q003: LVDS interface levels.
				7	nQ	
				8	V_{CC} V_{DD}	8N3Q001: 8N3Q003: (V_{CC}) Positive power supply. 8N4Q001: 8N4Q003: (V_{DD}) Positive power supply.
				9	SDATA	I^2C Data I/O. LVCMOS/LVTTL interface levels when input. Open drain when output.
				10	SCLK	I^2C Clock Input. LVCMOS/LVTTL interface levels.
XO	8N0Q001	10		1	DNU	Do not use
				2	OE	Output enable pin. LVCMOS/LVTTL interface levels.
				3	GND	Negative power supply.
				4	FSEL0	Default frequency select pin. LVCMOS/LVTTL interface levels.
				5	FSEL1	
				6	Q	Clock output. LVCMOS/LVTTL interface levels.
				7	DNU	Do not use
				8	V_{DD}	Positive Power Supply.
				9	SDATA	I^2C Data I/O. LVCMOS/LVTTL interface levels when input. Open drain when output.
				10	SCLK	I^2C Clock Input. LVCMOS/LVTTL interface levels.
XO	8N3D085	6		1	OE	Output enable (OE).
				2	FSEL	Freqency select.
				3	V_{EE}	Negative power supply.
				4	Q	Differential clock output. LVPECL.
				5	nQ	
				6	V_{CC}	Positive power supply..

Table 2. FemtoClock NG 5x7 Pinout Information

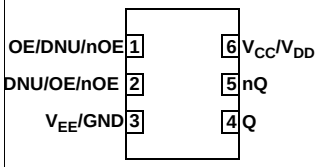
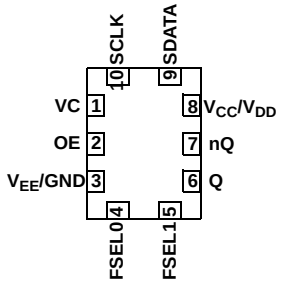
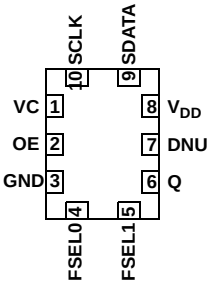
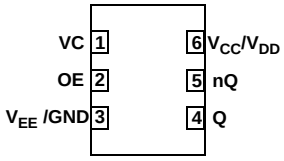
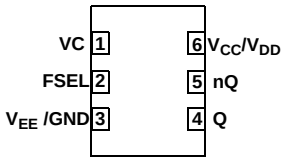
Type	Part Number	# Pins	Pinout	#	Name	Description
XO	8N3S270 8N3S271 8N3S272 8N3S273 8N4S270 8N4S271 8N4S272 8N4S273	6		1	OE DNU DNU nOE	8N3S270, 8N4S270: Output enable (OE). 8N3S271, 8N4S271: Do not use. 8N3S272, 8N4S272: Do not use. 8N3S273, 8N4S273: Output enable (nOE).
				2	DNU OE nOE DNU	8N3S270, 8N4S270: Do not use. 8N3S271, 8N4S271: Output enable (OE). LVCMOS/LVTTL. 8N3S272, 8N4S272: Output enable (nOE). LVCMOS/LVTTL. 8N3S273, 8N4S273: Do not use.
				3	V_{EE} GND	8N3S270, 8N3S272: (V_{EE}) Negative power supply. 8N3S271, 8N3S273: (V_{EE}) Negative power supply. 8N4S270, 8N4S271: (GND) Negative power supply. 8N4S272, 8N4S273: (GND) Negative power supply.
				4	Q	8N3S270, 8N3S271: Differential clock output. LVPECL. 8N3S272, 8N3S273: Differential clock output. LVPECL. 8N4S270: 8N4S271: Differential clock output. LVDS. 8N4S272, 8N3S273: Differential clock output. LVDS.
				5	nQ	
				6	V_{CC} V_{DD}	8N3S270, 8N3S271: (V_{CC}) Positive power supply. 8N3S272, 8N3S273: (V_{CC}) Positive power supply. 8N4S270: 8N4S271: (V_{DD}) Positive power supply. 8N4S272: 8N4S273: (V_{DD}) Positive power supply.
VCXO	8N3QV01 8N4QV01	10		1	VC	VCXO control voltage input.
				2	OE	Output enable pin. LVCMOS/LVTTL interface levels.
				3	V_{EE} GND	8N3QV01 (V_{EE}): Negative power supply. 8N4QV01 (GND): Negative power supply.
				4	FSEL0	Default frequency select pins. LVCMOS/LVTTL interface levels.
				5	FSEL1	
				6	Q	Differential clock output. 8N3QV01 LVPECL interface levels. 8N4QV01 LVDS interface levels.
				7	nQ	
				8	V_{CC} V_{DD}	8N3QV01 (V_{CC}): Positive power supply. 8N4QV01 (V_{DD}): Positive power supply.
				9	SDATA	I^2C Data I/O. LVCMOS/LVTTL interface levels when input. Open drain when output.
				10	SCLK	I^2C Clock Input. LVCMOS/LVTTL interface levels.

Table 2. FemtoClock NG 5x7 Pinout Information

Type	Part Number	# Pins	Pinout	#	Name	Description
VCXO	8N0QV01	10		1	VC	VCXO control voltage input.
				2	OE	Output enable pin. LVCMOS/LVTTL interface levels.
				3	GND	Negative power supply.
				4	FSEL0	Default frequency select pins. LVCMOS/LVTTL interface levels.
				5	FSEL1	
				6	DNU	Do not use
				7	Q	Clock output. LVCMOS/LVTTL interface levels.
				8	V_{DD}	Positive power supply.
				9	SDATA	I^2C Data I/O. LVCMOS/LVTTL interface levels when input. Open drain when output.
				10	SCLK	I^2C Clock Input. LVCMOS/LVTTL interface levels.
	8N3SV75 8N4SV75	6 pin		1	VC	VCXO control voltage input.
				2	OE	Output enable pin. LVCMOS/LVTTL interface levels.
				3	V_{EE} GND	8N3SV75 (V_{EE}): Negative power supply. 8N4SV75 (GND): Negative power supply.
				4	Q	8N3SV75: Differential clock output. LVPECL. 8N4SV75: Differential clock output. LVDS.
				5	nQ	
				6	V_{CC} V_{DD}	8N3SV75 (V_{CC}): Positive power supply. 8N4SV75 (V_{DD}): Positive power supply.
	8N3DV85 8N4DV85	6 pin		1	VC	VCXO Control Voltage input.
				2	FSEL	Frequency select pin. LVCMOS/LVTTL interface levels.
				3	V_{EE} GND	8N3DV85 (V_{EE}): Negative power supply. 8N4DV85 (GND): Negative power supply.
				4	Q	8N3DV85: Differential clock output. LVPECL. 8N4DV85: Differential clock output. LVDS.
				5	nQ	
				6	V_{CC} V_{DD}	8N3DV85 (V_{CC}): Positive power supply. 8N4DV85 (V_{DD}): Positive power supply.

XO and VCXO Programming

Introduction

This section begins with a description of the 10-pin crystal oscillator (XO) devices in the first part. Block diagram, the operating principle and programming guidelines are discussed. In the second part, the voltage controlled oscillator (VCXO) devices are described with the block diagram and operating principles where different from the XO. This second part also contains VCXO-specific information such as the VCXO pull range calculation. The third part focuses on the 6-pin XO and VCXO devices and describes their operating principles where different from the 10-pin devices. Device-specific programming information and the register map is shown for each individual device.

The programming information in this section is applicable to the following devices:

- 8N0Q001, 8N3Q001, 8N4Q001, 8N0Q003, 8N3Q003, 8N4Q003, (10 pin XO devices)
- 8N0QV01, 8N3QV01, 8N4QV01 (10 pin VCXO devices)
- 8N3SV75, 8N3DV85, 8N4V75, 8N4DV85 (6 pin VCXO devices)
- 8N3S270, 8N3S271, 8N3S272, 8N3S273, 8N4S270, 8N4S271, 8N4S272, 8N4S273 (6 pin XO devices)

Part 1: User-configurable XO devices in the 10-pin package

XO Block Diagram

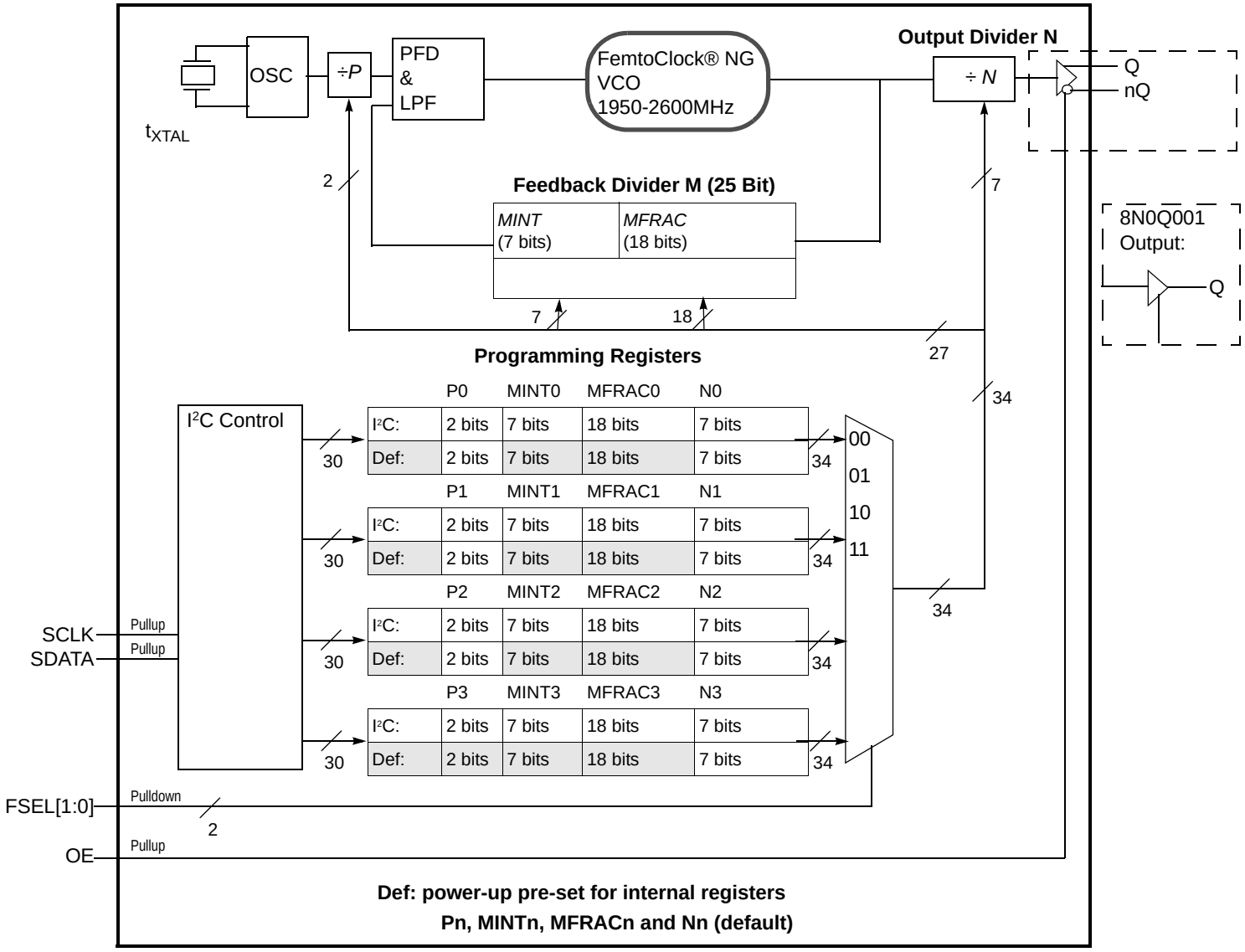


Figure 1: XO Block Diagram (8N3Q001, 8N4Q001, 8N0Q001)

The block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock f_{XTAL} of either 114.285 MHz or 100 MHz. The PLL includes the FemtoClock NG VCO along with the Pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the f_{XTAL} reference and must be configured correctly for proper operation. The feedback divider is fractional supporting a huge number of output frequencies. The configuration of the feedback divider to integer-only values results in an improved output phase noise characteristics at the expense of the range of output frequencies. For more information on integer-feedback, see section XO Integer-Feedback Programming on page 23.

In addition, internal registers are used to hold up to four different factory pre-set *P*, *M*, and *N* configuration settings. These default pre-sets are stored in the I2C registers at power-up. Each configuration is selected via the FSEL[1:0] pins and can be read back using the SCLK and SDATA pins.

The user may choose to operate the device at an output frequency different than that set by the factory. After power-up, the user may write new P, N and M settings into one or more of the four

configuration registers and then use the FSEL[1:0] pins to select the newly programmed configuration. Note that the I2C registers are volatile and a power supply cycle will reload the pre-set factory default conditions.

If the user does choose to write a different *P*, *M*, and *N* configuration, it is recommended to write to a configuration which is not currently selected by FSEL[1:0] and then change to that configuration after the I2C transaction has completed. Changing the FSEL[1:0] controls results in an immediate change of the output frequency to the selected register values. The *P*, *M*, and *N* frequency configurations support an output frequency range of 15.476MHz to 866.67MHz and 975MHz to 1,300MHz. See figure 1 for details.

XO Principles of Operation

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator.

The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right] \quad (1)$$

The four configuration registers for the *P, M (MINT & MFRAC)* and *N* dividers which are named Pn, MINTn, MFRACn and Nn with n=0 to 3. “n” denominates one of the four possible configurations.

As identified previously, the configurations of *P, M (MINT & MFRAC)* and *N* divider settings are stored the I^2C register, and the configuration loaded at power-up is determined by the FSEL[1:0] pins.

Table 3. Frequency Selection

Input		Selects	Register
FSEL1	FSEL0		
0 (def.)	0 (def.)	Frequency 0	P0, MINT0, MFRAC0, N0
0	1	Frequency 1	P1, MINT1, MFRAC1, N1
1	0	Frequency 2	P2, MINT2, MFRAC2, N2
1	1	Frequency 3	P3, MINT3, MFRAC3, N3

XO Frequency Configuration

The following procedure is suggested to obtain a valid frequency configuration (*P, MINT, MFRAC and N)* for a given output frequency f_{OUT}.

1. Determine the VCO frequency f_{VCO} and the post divider *N*:

Multiply the desired output frequency by the possible integer *N* dividers (the possible *N* dividers are shown in table 4). The resulting values are compared to the PLL lock range of 1950 MHz to 2600 MHz. Select the *N* divider that produces a value within that 1950MHz and 2600 MHz range.

Example: If an f_{OUT} = 625 MHz is desired.

- f_{OUT} * 2 = 1250 MHz (outside the 1950MHz to 2600 MHz range)
- f_{OUT} * 3 = 1875 MHz (outside the 1950MHz to 2600 MHz range)
- f_{OUT} * 4 = 2500 MHz (within the 1950MHz to 2600 MHz range)

A frequency divider of 4 is within the appropriate range. This results in a VCO frequency of f_{VCO} = 2500 MHz. A frequency divider of 4 corresponds to Nn[6:0] = 0x04 (see table 4 for the *N* value range).

2. Calculate the required multiplication value (*M*) and the pre-divider *P*:

Divide the f_{VCO} value calculated for step 1 by the PLL reference frequency f_{REF} and set P=1

$$M = \frac{f_{VCO}}{f_{REF}} \cdot P \quad (2)$$

Example: Value from step 1 = 2500 MHz

$$M = \frac{2500\text{MHz}}{114.285\text{MHz}} \cdot 1$$

$$M = 21.875136719$$

3. Determine the integer part (*MINT*) and the fractional part (*MFRAC*) of M

MINT has the length of six bits and is the integer portion of M:

MINT = integer(*M)*

The fractional portion *MFRAC* is base 2 and has the length of 18 bits:

$$\text{fractional}(M) = \frac{MFRAC}{2^{18}} + \frac{1}{2^{19}} \quad (3)$$

Resolve (3) for *MFRAC* in the following form:

$$MFRAC = 2^{18} \cdot \left[\text{fractional}(M) - \frac{1}{2^{19}} \right] \quad (4)$$

Example: *M*-value from step 2 = 21.875136719. Integer(*M*) = 21 and fractional(*M*) = 0.875136719. Calculate MFRAC by inserting fractional(*M*) into formula (4):

$$MFRAC = 2^{18} \cdot \left[0.875136719 - \frac{1}{2^{19}} \right]$$

$$MFRAC = 229,411.34$$

Rounding 229411.34 to the nearest integer, *MFRAC* = 229411 (0x38023). Because the MFRAC consists of 18 bits and is not infinitely long, some rounding error may occur which results in a output frequency error: the actual output frequency is somewhat different to the desired output frequency. Due to the size of *MFRAC* this rounding error is usually minimal, but should be checked to ensure desired operation is achieved. See also section XO Digital Frequency Synthesis Error on page 10.

4. Program the divider settings

Program any of the four Pn, MINTn, MFRACn, and Nn register sets with the calculated values. For the quad devices the number of register sets is four (n = 0, 1, 2, 3). For the dual frequency devices the number of register sets is two (n = 0, 1) while for the single devices there is only one register set available (n = 0).

Example:

- Value from step 1, load Nn[6:0] = 0x04
  (see table 4 for the *N* value coding)
- Value from step 2, load Pn[1:0] = 0x00
  (see table 7 for the *P* and *M* value coding)
- Value from step3, load MINTn[6:0] = 0x15
  (binary coding. See also table 7)
- Value from step 3, load MFRACn[17:0] = 0x38023
  (binary coding)

The Pn, MINTn, MFRACn and Nn register bits are located in the register file, which is described in table 5 on page 12.

5. PLL recalibration

Toggle the FSEL[1:0] bits in register 18 (See table 5 for the register map) or the FSEL[1:0] pins to force a PLL recalibration. PLL recalibration is required every time the PLL feedback register (*MINT, MFRAC*) is reprogrammed after power-up.

Table 4. PLL Post Divider N Coding

Frequency Divider *N*	Output frequency range		Register Bit
	f_{OUT_MIN} (MHz)	f_{OUT_MAX} (MHz)	N_n[6:0][1]
2	975	1300	000000X
2	975	1300	0000010
3	650	866.66	0000011
4	487.5	650	0000100
5	390	520	0000101
6	325	433.33	000011X
8	243.75	325	000100X
10	195	260	000101X
N (even integer)	(1950 ÷ *N*)	(2600 ÷ *N*)	...
124	15.73	20.97	111101X
126	15.48	20.63	111111X

1.X = 0 or 1 (don't care)

XO Digital Frequency Synthesis Error

The frequency error introduced by the rounding error in the fractional feedback divider is determined by using the calculated *MINT* and *MFRAC* values and finding the actual output frequency by using formula (1).

Example: f_{OUT} = 625 MHz. By step 3, MINT = 21 and MFRAC = 229411 and using formula (2):

$$\frac{229411}{2^{18}} + \frac{1}{2^{19}} = 0.875135421$$

So the actual *M* divider used is 21.875135421 and the output frequency calculates by formula (1) to:

$$f_{OUT} = 114.285\text{MHz} \cdot \frac{21.875135421}{1 \cdot 4}$$
$$f_{OUT} = 624.9999629\text{MHz}$$

The frequency error Δf is:

$$\Delta f = \frac{\Delta f_{OUT}}{f_{OUT}} \quad (5)$$
$$\Delta f = \frac{624.9999629\text{MHz} - 625\text{MHz}}{625\text{MHz}}$$
$$\Delta f = -5.936 \cdot 10^{-8}$$

Which is -0.059 parts per million, and is significantly less than the inaccuracy due to crystal characteristics. This example also hints at how to calculate the worst case ppm error for a given VCO frequency. The frequency resolution Δf (frequency step size) for a pre-divider P=1 is:

$$\Delta f = \left(\frac{114.285\text{MHz}}{2^{18}} + \frac{1}{2^{19}}\right) \div N \quad (6)$$
$$\Delta f = \frac{0.00043787\text{MHz}}{N}$$
$$\Delta f \approx \frac{438\text{Hz}}{N}$$

The worst case error will occur when the desired output frequency is half-way between these 438Hz steps because that is when the maximum round-off error will occur. So dividing this number by 2 results in 219÷*N* Hz and this is the worst case frequency error. This is an absolute error in Hz. The relative error in ppm will change with the VCO frequency and is higher at lower VCO frequencies. See also section Crystal Stability on page 11.

Crystal Stability

The XO devices use a 114.285 MHz or 100 MHz 3rd overtone crystal as frequency reference. VCXO devices always use a 114.285 MHz reference frequency. This reference frequency is not constant. Ambient temperature, supply voltage, crystal aging and the initial crystal accuracy result in a frequency error: the actual frequency is offset to the nominal 114.285MHz or 100MHz reference frequency. The frequency error is expressed in ppm (parts per million) and contains the following components:

f_I … Initial accuracy (see datasheet)

f_S … Crystal temperature stability

f_A … Crystal aging

The total stability f_T is the sum of these three components:

$$f_T = f_I + f_S + f_A \qquad \text{Crystal Stability} \qquad (7)$$

The individual components and the total stability are specified on the device datasheets. The temperature stability f_S is the largest contributor to the frequency error. f_S directly relates to the type and make (frequency cut) of the used crystal. The XO and VCXO family supports 20, 50 and 100 ppm XTAL options by order codes.

Comparing the crystal stability to the PLL digital synthesis error in a previous section, it is obvious that the crystal stability f_T is two orders of magnitude larger then the digital synthesis error. Therefore, the digital synthesis error can be neglected in device stability calculations.

Register Configuration

Table 5 shows the register map for the XO. Table 6 description of each register bit with recommended settings for users wanting to program and optimize the device. On power-up, the device loads pre-set frequency and optimized PLL parameters settings into all registers.

Table 5. I²C Register Map of the XO devices (8N3Q001, 8N4Q001, 8N0Q001)[1]

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	CP0[1]	CP0[0]	MINT0[4]	MINT0[3]	MINT0[2]	MINT0[1]	MINT0[0]	MFRAC0[17]
1	00001	CP1[1]	CP1[0]	MINT1[4]	MINT1[3]	MINT1[2]	MINT1[1]	MINT1[0]	MFRAC1[17]
2	00010	CP2[1]	CP2[0]	MINT2[4]	MINT2[3]	MINT2[2]	MINT2[1]	MINT2[0]	MFRAC2[17]
3	00011	CP3[1]	CP3[0]	MINT3[4]	MINT3[3]	MINT3[2]	MINT3[1]	MINT3[0]	MFRAC3[17]
4	00100	MFRAC0[16]	MFRAC0[15]	MFRAC0[14]	MFRAC0[13]	MFRAC0[12]	MFRAC0[11]	MFRAC0[10]	MFRAC0[9]
5	00101	MFRAC1[16]	MFRAC1[15]	MFRAC1[14]	MFRAC1[13]	MFRAC1[12]	MFRAC1[11]	MFRAC1[10]	MFRAC1[9]
6	00110	MFRAC2[16]	MFRAC2[15]	MFRAC2[14]	MFRAC2[13]	MFRAC2[12]	MFRAC2[11]	MFRAC2[10]	MFRAC2[9]
7	00111	MFRAC3[16]	MFRAC3[15]	MFRAC3[14]	MFRAC3[13]	MFRAC3[12]	MFRAC3[11]	MFRAC3[10]	MFRAC3[9]
8	01000	MFRAC0[8]	MFRAC0[7]	MFRAC0[6]	MFRAC0[5]	MFRAC0[4]	MFRAC0[3]	MFRAC0[2]	MFRAC0[1]
9	01001	MFRAC1[8]	MFRAC1[7]	MFRAC1[6]	MFRAC1[5]	MFRAC1[4]	MFRAC1[3]	MFRAC1[2]	MFRAC1[1]
10	01010	MFRAC2[8]	MFRAC2[7]	MFRAC2[6]	MFRAC2[5]	MFRAC2[4]	MFRAC2[3]	MFRAC2[2]	MFRAC2[1]
11	01011	MFRAC3[8]	MFRAC3[7]	MFRAC3[6]	MFRAC3[5]	MFRAC3[4]	MFRAC3[3]	MFRAC3[2]	MFRAC3[1]
12	01100	MFRAC0[0]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
13	01101	MFRAC1[0]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
14	01110	MFRAC2[0]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
15	01111	MFRAC3[0]	N3[6]	N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
16	10000	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
17	10001	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
18	10010	ADC_ENA	reserved	nPLL_BYP	FSEL[1]	FSEL[0]	reserved	reserved	reserved
19	10011	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
20	10100	P0[1]	P0[0]	MINT0[5]	DSM0[1]	DSM0[0]	DG0	DSM_ENA0	LF0
21	10101	P1[1]	P1[0]	MINT1[5]	DSM1[1]	DSM1[0]	DG1	DSM_ENA1	LF1
22	10110	P2[1]	P2[0]	MINT2[5]	DSM2[1]	DSM2[0]	DG2	DSM_ENA2	LF2
23	10111	P3[1]	P3[0]	MINT3[5]	DSM3[1]	DSM3[0]	DG3	DSM_ENA3	LF3

1.Registers labeled “Reserved“ are for future use. Access to reserved bits must write “0“. Read access results are not defined.

Table 6. I²C Register Function Descriptions of the XO devices (8N3Q001, 8N4Q001, 8N0Q001)

Bits	Name	Function	Recommended Setting
MINTn[5:0]	Integer Feedback Divider Register n (n = 0...3)	Sets the integer portion of the feedback divider value. Can be set to a value of 4 to 127. For binary values < 4, the value is x+4. So programming 0000000 would yield a feedback divider of ÷4, 0000001 = ÷5, etc. It should also be noted that with a reference of 114.285MHz and P=÷1, the minimum value loaded into this register should be 17 to remain above the minimum VCO frequency of 1950MHz. The six bits MINTn[5:0] can be programmed independently on any register setting, while the MSB of MINTn (MINT[6]) is configured in conjunction with the Pn[1:0] divider. See also table 7 on page 14.	According to the desired output frequency and the VCO frequency range. Set MINT to the lowest possible VCO frequency for best phase noise.
MFRACn[17:0]	Fractional Feedback Divider Register n (n = 0...3)	Sets the fractional value of the feedback divider resulting in a fraction of MFRAC0[17:0]÷2^{18}. From a 114.285MHz reference, this means the frequency is incremented by about 436Hz÷*N* for each LSB increment.	According to the desired output frequency. In fractional mode, phase noise is best for: MFRAC = 0.015 to 0.496 and MFRAC = 0.540 to 0.980
Nn[6:0]	Output Divider Register n (n = 0...3)	Sets the output divider. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See table 4 on page 10 for the output divider coding.	According to the desired output frequency
Pn[1:0]	Pre-Scaler Register n (n = 0...3)	Sets the PLL pre-scaler. The pre-scaler divider value has the range of 1, 2, 4 and 5. See table 7 on page 14 for the prescaler coding. Note the Pn[1:0] registers also set the Mn[6] bit of MINT (MINTn[6]).	P= ÷1 (P=00)
DG0	Dither Gain	Internal function.	1
DG1	Dither Gain	Internal function.	1
DG2	Dither Gain	Internal function.	1
DG3	Dither Gain	Internal function.	1
DSMn[1:0]	DSM Order (n = 0...3)	Internal function.	11
DSM_ENAn	DSM Enable (n = 0...3)	Delta Sigma Modulator Enable. 0 = DSM disabled. Use this setting for integer-PLL operation 1 = DSM enabled (default)	1
LFn	Loop Filter Value (n = 0...3)	Together with CPn[1:0] sets the PLL loop parameters. A higher value results in lower bandwidth.	1
CPn[1:0]	Charge Pump Current (n = 0...3)	Together with LFn sets the loop parameters. A higher value results in higher loop bandwidth (opposite of LFn).	if DSM_ENA=0, set CPn[1:0]=11 if DSM_ENA=1, set CPn[1:0]=00
FSEL[1:0]	Frequency Select	Selects from 4 available power-up default M and N combinations to provide 4 available power-up default output frequencies. The value of these bits are OR'ed with the Frequency Select pin values. Toggling the FSEL[1:0] bits also forces the PLL to recalibrate	None
nPLL_BYP	PLL Bypass	PLL Bypass. The output frequency = oscillator frequency (~114.285 MHz) divided by *N*. 0 = PLL Bypass 1 = PLL Enable (default)	1
ADC_ENA	ADC Enable	0 = ADC Disabled. Use for integer-PLL operation. 1 = ADC Enabled (default)	

Table 7. PLL Pre-Scaler P and Feedback Divider M6 Coding

Register Bit[1]		Pre-Scaler *P*	Feedback-Divider Bit $MINT_n[6]$
P_n1	P_n0		
0	0	1	0
0	1	2	0
1	0	4	1
1	1	5	1

1.The $P_n[1:0]$ bits control both the pre-scale P_n and the MSB of $MINT_n$ ($MINT_n[6]$).

Part 2: User-Configurable VCXO Devices in the 10-pin Package

VCXO Block Diagram

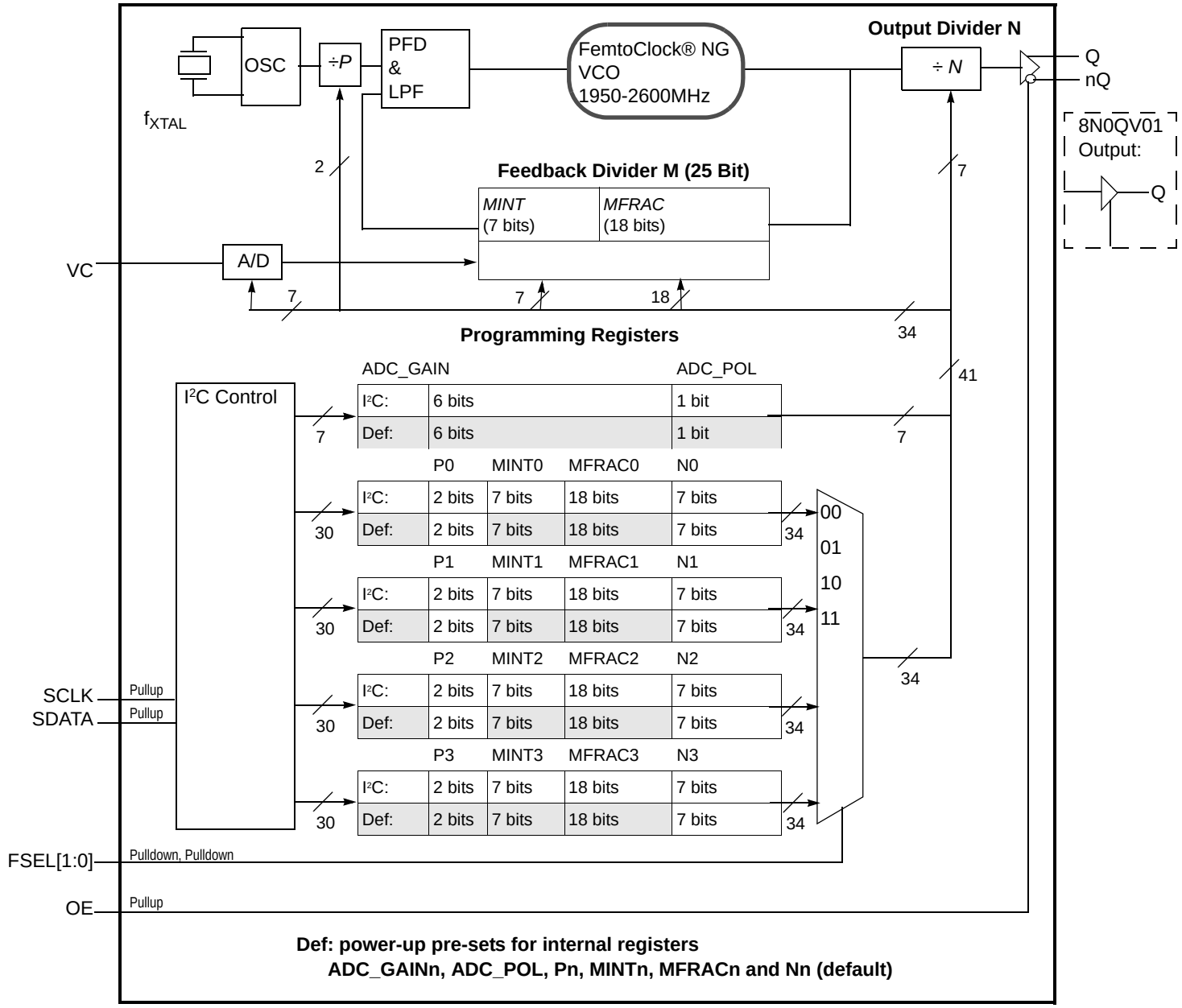


Figure 2: VCXO Block Diagram (8N3QV01, 8N4QV01, 8N0QV01)

The block diagram of the VCXO circuit shown in figure 2 is similar to the block diagram of the XO circuit in figure 1 and consists of the same basic blocks. The reference frequency (f_{XTAL}) is always equal to 114.285MHz. In addition to an XO, the VCXO has an analog VC control input for output frequency pulling. The VC input is internally connected to an analog-to-digital converter which samples the VC input at high speed. The sampled value is digitally added to the fractional feedback divider (*M*) of the VCXO for frequency control.

The configuration of a VCXO is equivalent to the configuration of the XO. The same I^2C registers hold the four possible *P*, *M*, and *N* settings. In addition, the VCXO includes I^2C registers for VCXO gain control (ADC_GAIN), and VCXO polarity (ADC_POL) that control the

pull range of the selected output frequency. The VCXO gain control and polarity are pre-set by the factory and are stored in the registers on power-up, but may be modified by the user after power-up by writing the registers via I^2C.

VCXO Frequency and Pull-Range Configuration

The following procedure is suggested to obtain a valid frequency configuration (*P, MINT, MFRAC and N)* for a given output frequency f_{OUT} and an approximate pull range Δfc. For a precise calculation of the VCXO pull range, such as for obtaining a minimum or maximum pull range requires the procedure in section Exact Calculation of the VCXO Pull Range on page 18.

Before starting to configure a device for a given pull range, it is recommended to read the section Crystal Stability on page 11

In an example, a VCXO will be configured to the nominal (center) frequency of 625 MHz and to the pull range Δfc of ±100ppm with a positive tuning slope: an increase of the voltage applied to VC increases the output frequency.

1. Determine the VCO frequency f_{VCO}, the pre-divider *P* and the post divider *N*:

VCO frequency and output divider *N* are determined as in step one in the previous paragraph (section XO Frequency Configuration on page 9): For f_{OUT}=625MHz, we obtain f_{VCO} = 2500 and *N*=4.

2. Calculate the required multiplication value (*M*):

For a *positive* tuning slope, *subtract* half of the desired pull range from the value for f_{VCO} obtained in step one. This will center the nominal output frequency (f_{OUT} at V_C=V_{CC}÷2) to the middle of the frequency pull range. Then, continue the calculation of *M* like in step 2 in the section XO Frequency Configuration on page 9.

Example: Value from step: *M* = 2500 MHz

Pull range Δfc = ±100 ppm

f_{VCO} = 2500MHz - 100ppm = 2499.75MHz

Using the formulas presented in step 2 of the XO frequency configuration, the *M* value for this example configuration calculates to *M* = 21.8729492049 (= 2499.75 MHz ÷ 114.285 MHz)

3. Determine the integer part (*MINT*) and the fractional part (*MFRAC*) of *M*

The calculation of *MINT* and *MFRAC* for a given VCO frequency is equivalent to step 3 in the XO frequency configuration. In our example, *M* is 21.8729492049 and the result of the calculation is:

- MINTn = 21 (0x15) and
- MFRACn = 228,837.90.

Then, MFRACn is rounded to the next integer:

- MFRACn = 228,838.

As identified previously, the rounding causes a frequency error. Refer to the section XO Digital Frequency Synthesis Error on page 10 for details, which also applies to the VCXO devices.

4. Determine the gain and polarity of the VCXO

The gain of the VCXO is the ratio the output frequency change per control voltage change. The VCXO gain is programmable in 12.5 ppm steps and used for programming the pull range. The VCXO gain for a given pull range can be looked up (see table 8 on page 17).

In our example, the pull range of ±100 ppm corresponds to the VCXO gain (ADC_GAIN) of 8 (binary 001000).

For a positive tuning slope, the ADC_POL bit is set to 0 and for a negative tuning slope, set ADC_POL to 1. In our example, the ADC_POL setting is 0.

5. Program the divider and register settings

Program any of the four Pn, MINTn, MFRACn, and Nn register sets with the calculated values. For the quad devices the number of register sets is four (n = 0, 1, 2, 3). For the dual frequency devices the number of register sets is two (n = 0, 1) while for the single devices there is only one register set available (n = 0). The Pn, MINTn, MFRACn and Nn register bits are located in the register file, which is described in table 5 on page 12.

Example:

- Value from step 1, Load Nn[6:0] = 0x04
  (see table 4 for the *N* value coding)
- Value from step 2, load Pn[1:0] = 0x00
  (see table 7 for the *P* and *M* value coding)
- Value from step3, load MINTn[6:0] = 0x15
  (binary coding. See also table 7)
- Value from step 3, load MFRACn[17:0] = 0x37DE6
  (binary coding)
- From step 4, load ADC_GAIN = 8

5. PLL recalibration

Toggle the FSEL[1:0] bits in register 18 (See table 5 for the register map) or the FSEL[1:0] pins to force a PLL recalibration. PLL recalibration is required every time PLL feedback register (*MINT, MFRAC*) is reprogrammed after power-up.

Negative Tuning Slope Configuration

Programming the *negative* tuning slope starts with the configuration of the programmed VCO frequency *higher* than the nominal frequency by half of the desired pull range. In an example of an output frequency of 625 MHz and a ±100ppm pull range with a negative slope, set the VCO frequency to 2500 MHz + 100 ppm = 2500.0025 MHz and the calculation would then proceed as in step 2 before. In step 4, set ADC_POL to 1.

From the above example, it should also be clear that it is also possible to program positive-only or negative-only deviation from nominal frequency (rather than ± deviation from nominal frequency).

In summary:

- positive pull range: decrease M by Δfc and set ADC_POL to 0
- negative pull range: decrease M by Δfc and set ADC_POL to 1

VCXO Pull Range and Absolute Pull Range (APR)

The absolute pull range (APR) is defined as the minimum guaranteed operating output frequency pull range for a full swing of the control voltage (VC=0 to VC=VCC). The XTAL frequency error reduces the pull range of the VCXO. In brief, the APR specifies how much of the programmed VCXO pull range is available to the application.

The APR can be calculated as the difference of the VCXO pull range and the total crystal stability:

APR = Pull range - Total Crystal stability (8)

APR = Pull range - f_T

In VCXO applications, the required APR is known and the pull range must be calculated and programmed. The following procedure is recommended to obtain the VCXO pull range:

- *add* the total crystal stability to the desired APR
- round to the next integer multiple of 12.5 ppm

Example:

- desired APR: ±200 ppm
- temperature stability of VCXO: f_S = ±50 ppm
  (these parameter are obtained from the datasheet of the selected VCXO: f_I = ±10 ppm, f_S = ±50 ppm, f_A = ±3 ppm)
  - $f_T = f_I + f_S + f_A$ = ±63 ppm, rounded up to ±75 ppm.
  - Pull range = APR + (±75 ppm)
  - Pull range = ±275 ppm
  - Looking up ADC_GAIN =22 (binary 10110) from table 8

Programming ADC_GAIN = 22 will result in the desired APR of ±200 ppm.

Table 8. APR, Pull Range and ADC_GAIN for devices with 20, 50 and 100 ppm crystals[1] [2]

APR[NOTE 1], (ppm), VC = 0V to VCC for a crystal of			Typical Pull Range[NOTE 2] (ppm) VC = 0V to VCC	ADC_GAIN					
f_S = 20 ppm	f_S = 50 ppm	f_S = 100 ppm		5	4	3	2	1	0
n/a	n/a	n/a	n/a	0	0	0	0	0	0
±0	±0	±0	±12.5	0	0	0	0	0	1
±0	±0	±0	±25.0	0	0	0	0	1	0
±4.5	±4.5	±0	±37.5	0	0	0	0	1	1
±17.0	±17.0	±0	±50.0	0	0	0	1	0	0
±29.5	±29.5	±0	±62.5	0	0	0	1	0	1
±42.0	±42.0	±0	±75.0	0	0	0	1	1	0
±54.5	±54.5	±0	±87.5	0	0	0	1	1	1
±67.0	±67.0	±0	±100.0	0	0	1	0	0	0
±79.5	±49.5	±0	±112.5	0	0	1	0	0	1
±92.0	±62.0	±12.0	±125.0	0	0	1	0	1	0
±104.5	±74.5	±24.5	±137.5	0	0	1	0	1	1
±117.0	±87.0	±37.0	±150.0	0	0	1	1	0	0
±(ADC_GAIN · 12.5) - 33	±(ADC_GAIN · 12.5) - 63	±(ADC_GAIN · 12.5) - 113	±(ADC_GAIN · 12.5)	...	...	...	...	...	...
±729.5	±669.5	±649.5	±762.5	1	1	1	1	0	1
±742.0	±712.0	±662.0	±775.0	1	1	1	1	1	0
±754.5	±724.5	±674.5	±787.5	1	1	1	1	1	1

1.The ADC gain is set through I^2C registers. APR (Absolute Pull Range) = Pull Range - Total stability. APR in table 8 is calculated for a XTAL with the temperature stability of ±20 ppm (option codes K and L), ±50 ppm (option codes E and F) and ±100 ppm (option code A and B), an aging of ±3ppm (10 years) and the initial accuracy (±10 ppm).
2.The Pull Range specification in table 8 contains typical APR values. For exact APR numbers, please see the section “Exact Calculation of the VCXO Pull Range”

Exact Calculation of the VCXO Pull Range

For most applications, the programming of the VCXO pull range by looking up ADC_GAIN in table 8 is sufficient. For an exact calculation, it must be taken into account that the feedback divider *(M)* depends on the VCXO pull range. An exact pull range calculation is applicable in applications that require to set a precise minimum or maximum APR. For these applications, ADCGAIN range should not be looked-up by table 8 but calculated as described below:

$$\text{Pullrange} = \pm\frac{1.27 \cdot 10^8}{2^{19}} \cdot \frac{\text{ADCGAIN}}{M} \quad (\text{ppm}) \quad (9)$$

$$\text{ADCGAIN} = \frac{2^{19}}{1.27 \cdot 10^8} \cdot M \cdot \pm\text{Pullrange} \quad (10)$$

The result, ADC_GAIN, is the binary value to be programmed.

Example calculation: find the ADC_GAIN setting for an output frequency of 622.08MHz and a desired APR of greater than ±100 ppm:

- determine *M* and *MINT* using the steps in the section “VCXO Block Diagram”: for f_{OUT} = 622.08, *M* equals 21.77075879 (f_{VCO}=2448.32MHz, *N*=4)
- By substitution of the pull range by APR and resolving for ADC_GAIN, we get:

$$\text{ADCGAIN} = \frac{2^{19}}{1.27 \cdot 10^8} \cdot M \cdot (\pm\text{APR} + f_I + f_S + f_A) \quad (11)$$

NOTE: ADC_GAIN: binary setting 1...63, step 1

f_I … Initial accuracy (see datasheet)

f_S … Crystal temperature stability (see datasheet)

f_A … Crystal aging (see datasheet)

In the example, the minimum APR of ±100ppm for an output frequency of 622.08 MHz and a 20 ppm crystal temperature stability and 10 year aging (±3 ppm) requires to set ADC_GAIN to:

ADC_GAIN = 0.00412825196 · 21.77075879 ·(±100 + (±10) + (±20) + (±3))

ADC_GAIN = 0.0898751 · (133) = 11.95, rounded up to 12 (binary: 001100)

Register configuration

Table 9 shows the register map for the XO. Table 6 description of each register bit with recommended settings for users wanting to program and optimize the device. On power-up, the device loads pre-set frequency and optimized PLL parameters settings into all registers

Table 9. I²C Register Map of the VCXO devices (8N3QV01, 8N4QV01, 8N0QV01)[1]

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	CP0[1]	CP0[0]	MINT0[4]	MINT0[3]	MINT0[2]	MINT0[1]	MINT0[0]	MFRAC0[17]
1	00001	CP1[1]	CP1[0]	MINT1[4]	MINT1[3]	MINT1[2]	MINT1[1]	MINT1[0]	MFRAC1[17]
2	00010	CP2[1]	CP2[0]	MINT2[4]	MINT2[3]	MINT2[2]	MINT2[1]	MINT2[0]	MFRAC2[17]
3	00011	CP3[1]	CP3[0]	MINT3[4]	MINT3[3]	MINT3[2]	MINT3[1]	MINT3[0]	MFRAC3[17]
4	00100	MFRAC0[16]	MFRAC0[15]	MFRAC0[14]	MFRAC0[13]	MFRAC0[12]	MFRAC0[11]	MFRAC0[10]	MFRAC0[9]
5	00101	MFRAC1[16]	MFRAC1[15]	MFRAC1[14]	MFRAC1[13]	MFRAC1[12]	MFRAC1[11]	MFRAC1[10]	MFRAC1[9]
6	00110	MFRAC2[16]	MFRAC2[15]	MFRAC2[14]	MFRAC2[13]	MFRAC2[12]	MFRAC2[11]	MFRAC2[10]	MFRAC2[9]
7	00111	MFRAC3[16]	MFRAC3[15]	MFRAC3[14]	MFRAC3[13]	MFRAC3[12]	MFRAC3[11]	MFRAC3[10]	MFRAC3[9]
8	01000	MFRAC0[8]	MFRAC0[7]	MFRAC0[6]	MFRAC0[5]	MFRAC0[4]	MFRAC0[3]	MFRAC0[2]	MFRAC0[1]
9	01001	MFRAC1[8]	MFRAC1[7]	MFRAC1[6]	MFRAC1[5]	MFRAC1[4]	MFRAC1[3]	MFRAC1[2]	MFRAC1[1]
10	01010	MFRAC2[8]	MFRAC2[7]	MFRAC2[6]	MFRAC2[5]	MFRAC2[4]	MFRAC2[3]	MFRAC2[2]	MFRAC2[1]
11	01011	MFRAC3[8]	MFRAC3[7]	MFRAC3[6]	MFRAC3[5]	MFRAC3[4]	MFRAC3[3]	MFRAC3[2]	MFRAC3[1]
12	01100	MFRAC0[0]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
13	01101	MFRAC1[0]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
14	01110	MFRAC2[0]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]

Table 9. I²C Register Map of the VCXO devices (8N3QV01, 8N4QV01, 8N0QV01)[1]

15	01111	MFRAC3[0]	N3[6]	N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
16	10000	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
17	10001	DBIT[0]	DBIT[1]	DBIT[2]	DBIT[3]	DBIT[4]	DBIT[5]	DBIT[6]	reserved
18	10010	ADC_ENA	ADC_POL	nPLL_BYP	FSEL[1]	FSEL[0]	reserved	reserved	reserved
19	10011	ADC_GAIN[5]	ADC_GAIN[4]	ADC_GAIN[3]	ADC_GAIN[2]	ADC_GAIN[1]	ADC_GAIN[0]	ADC_CLK[1]	ADC_CLK[0]
20	10100	P0[1]	P0[0]	MINT0[5]	DSM0[1]	DSM0[0]	DG0	DSM_ENA0	LF0
21	10101	P1[1]	P1[0]	MINT1[5]	DSM1[1]	DSM1[0]	DG1	DSM_ENA1	LF1
22	10110	P2[1]	P2[0]	MINT2[5]	DSM2[1]	DSM2[0]	DG2	DSM_ENA2	LF2
23	10111	P3[1]	P3[0]	MINT3[5]	DSM3[1]	DSM3[0]	DG3	DSM_ENA3	LF3

1.Registers labeled “Reserved“ are for future use. Access to reserved bits must write “0“. Read access results are not defined.

Table 10. I²C Function Descriptions of the VCXO devices (8N3QV01, 8N4QV01, 8N0QV01)

Bits	Name	Function	Recommended Setting
MINTn[5:0]	Integer Feedback Divider Register n (n = 0...3)	Sets the integer portion of the feedback divider value. Can be set to a value of 4 to 127. For binary values < 4, the value is x+4. So programming 0000000 would yield a feedback divider of ÷4, 0000001 = ÷5, etc. It should also be noted that with a reference of 114.285MHz and P=÷1, the minimum value loaded into this register should be 17 to remain above the minimum VCO frequency of 1950MHz. The six bits MINTn[5:0] can be programmed independently on any register setting, while the MSB of MINTn (MINT[6]) is configured in conjunction with the Pn[1:0] divider. See Pn[1:0] bit settings in this table.	According to the desired output frequency and the VCO frequency range. Set MINT to the lowest possible VCO frequency for best phase noise.
MFRACn[17:0]	Fractional Feedback Divider Register n (n = 0...3)	Sets the fractional value of the feedback divider resulting in a fraction of MFRAC0[17:0]÷2^{18}. From a 114.285MHz reference and P=÷1, this means the frequency is incremented by about 436Hz÷*N* for each LSB increment.	According to the desired output frequency. Best phase noise for: MFRAC = 0.015 to 0.496 and MFRAC = 0.540 to 0.980
Nn[6:0]	Output Divider Register n (n = 0...3)	Sets the output divider. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See table 4 on page 10 for the output divider coding.	According to the desired output frequency
Pn[1:0]	Pre-Scaler Register n (n = 0...3)	Sets the PLL pre-scaler and the Mn[6] bit of MINT (MINTn[6]). The supported pre-scaler divider value is ÷1 and the supported Mn[6] value is 0.	Always set Pn[1:0] to 00 for P=÷1 and Mn[6]=0
DG0	Dither Gain	Recommended setting = 1	1
DG1	Dither Gain	Recommended setting = 1	1
DG2	Dither Gain	Recommended setting = 1	1
DG3	Dither Gain	Recommended setting = 1	1
DSMn[1:0]	DSM Order (n = 0...3)	. Do not change the default value.	11
DBIT[6:0]	Test Bits	Do not change the default value.	
DSM_ENAn	DSM Enable (n = 0...3)	Delta Sigma Modulator Enable. 0 = DSM not enabled 1 = DSM Enabled (default)	1
LFn	Loop Filter Value (n = 0...3)	Together with CPn[1:0] sets the PLL loop parameters. A higher value results in lower bandwidth. Contact IDT for a recommendation for changing LFn.	1

Table 10. I²C Function Descriptions of the VCXO devices (8N3QV01, 8N4QV01, 8N0QV01)

CPn[1:0]	Charge Pump Current	Together with LFn sets the loop parameters. A higher value results in higher loop bandwidth (opposite of LFn). Contact IDT for a recommendation for changing LFn.	00
FSEL[1:0]	Frequency Select	Selects from 4 available power-up default M and N combinations to provide 4 available power-up default output frequencies. The value of these bits are OR'ed with the Frequency Select pin values. Toggling the FSEL[1:0] bits also forces a recalibration of the PLL.	None
nPLL_BYP	PLL Bypass	PLL Bypass. The output frequency = f_{XTAL} (114.285MHz) divided by *N*. 0 = PLL Bypass 1 = PLL Enable (default)	1 (enable)
ADC_ENA	ADC Enable	0 = ADC disabled 1 = ADC enabled (default)	1 (enable)
ADC_POL	ADC Polarity	0 = Positive slope. Increasing VC increases the output frequency (Default) 1 = Negative slope. Increasing VC decreases the frequency.	
ADC_GAIN[5:0]	ADC Gain	Sets the gain and therefore the pull range of the VCXO 000000 ADC Not used 000001 ±12.5ppm 000010 ±25.0ppm … *N* ±(12.5ppm * *N*) … 111110 ±775.0ppm 111111 ±787.5ppm Note that this does not take into account crystal variations which must be included to calculate Absolute Pull Range (APR) Default setting: TBD	
ADC_CLK[1:0]	ADC Clock Rate	00: f_{XTAL}÷8, 14.285625MHz 01: f_{XTAL}÷4 (default), 28.57125MHz 1x: reserved	pull range <150 ppm: 00 pull range >150 ppm: 01

Part 3: Factory-Programmable 6-Pin XO and VCXO Devices

Introduction

In contrast to the user-programmable devices, the 6-pin oscillators are designed for factory-programming only. All frequency and PLL parameters are as flexible as in the 10-Pin devices but need a final frequency specification from the customer. Devices are programmed in the factory. The operating principles of the 6-Pin and 10-Pin devices are essentially the same, including the architecture and register depth and length for all registers relevant for frequency and pull range programming. Block diagrams are somewhat different in the number of supported pre-set frequencies. A serial programming interface is not supported, the devices have either no or a single frequency select control pin. The pinouts of the 6-pin devices matches common industry-standard oscillator pinouts.

The generic part numbers of the factory-programmable XOs are 8N3S270, 8N4S270, 8N3S271, 8N4S271, 8NS3S272, 8N4S272, 8N3S273, 8N4S273 and 8N3D085. Part numbers 8N3DV85, 8N4DV85, 8N3SV75, 8N4SV75 are the factory-programmable VCXO devices. The part numbers with a “S” support a single, the part numbers with a “D” support two pre-set frequencies.

Single-Frequency XO

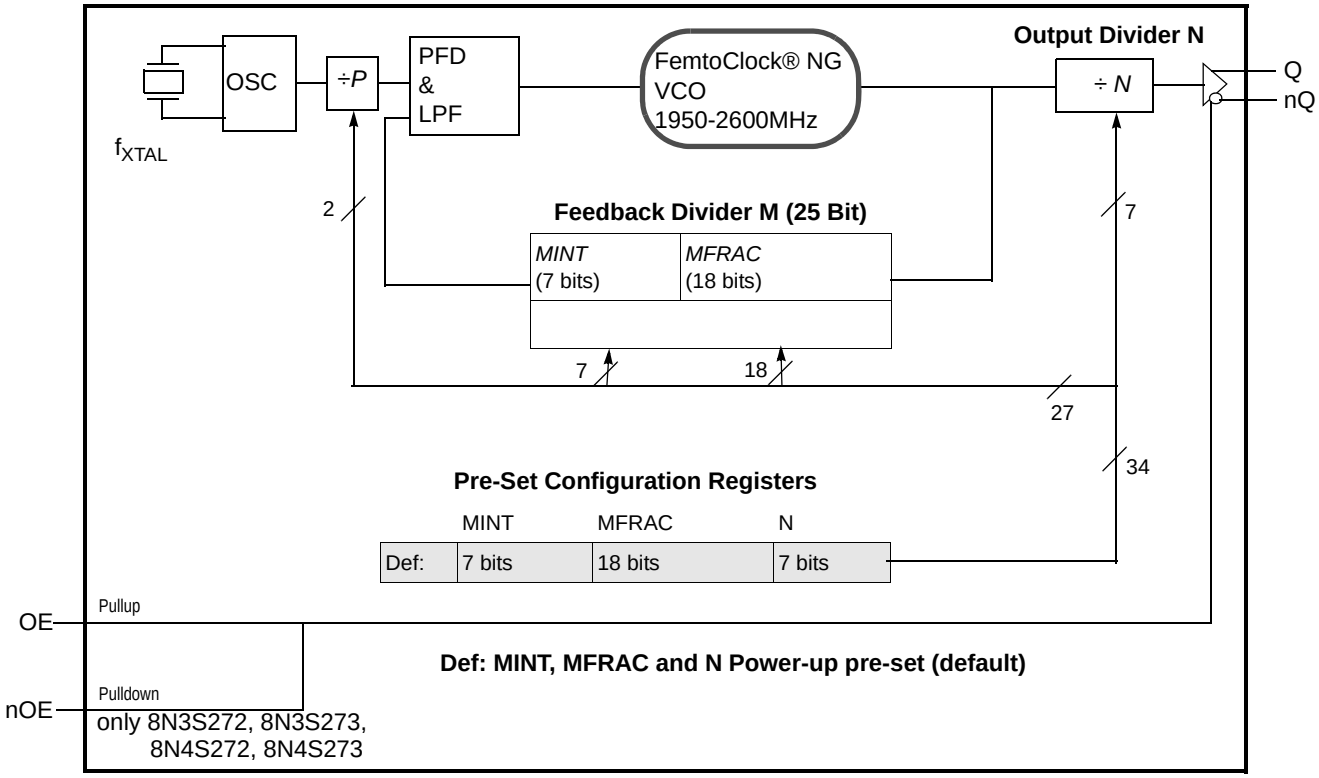


Figure 3: Single-Frequency XO Block Diagram (8N3S270, 8N3S271, 8N3S272, 8N3S273, 8N4S270, 8N4S271, 8N4S272, 8N4S273)

Similar to what was previously shown for the 10-pin devices, the block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock f_{XTAL} of 114.285 MHz or 100 MHz. The 100MHz XTAL is used for integer-mode frequency synthesis (see the section XO Integer-Feedback Programming on page 23 for details). The PLL includes the FemtoClock NG VCO along with the Pre-divider (*P*), the fractional feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the crystal reference frequency and are configured in the factory. The internal registers are used to hold one *P*, *M*, and *N* configuration setting. The *P*, *M*, and *N* frequency configurations support an output frequency range of 15.476MHz to 866.67MHz and 975MHz to 1,300MHz. See figure 3 for block diagram details. The frequency pre-set and desired XTAL frequency parameters are specified by the order code. For order details, please refer to the device datasheet.

Single and Dual Frequency VCXO

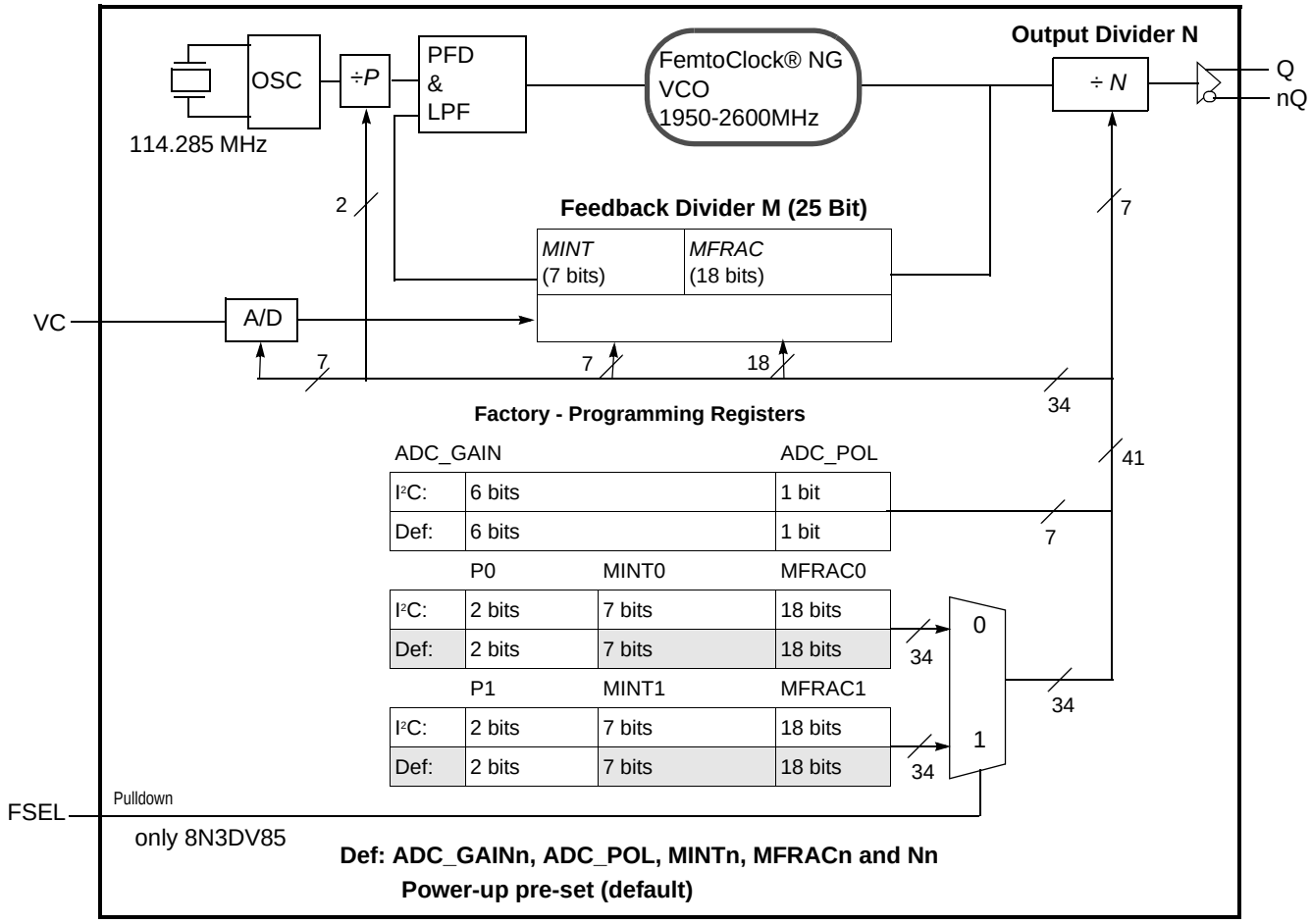


Figure 4: VCXO Block Diagram (8N3DV85, 8N3SV75, 8N4DV85, 8N4SV75)

The block diagrams of the 8N3DV85/8N4DV85 and 8N3SV75/8N4SV75 are similar to the 8N3QV01/8N4QV01 quad-frequency block diagrams, except the aforementioned number of frequency pre-sets. In the case the 8N3DV85/8N4DV85, the selection the two pre-set frequencies is controlled by a single FSEL pin.

The 8N3DV85/8N4DV85 and 8N3SV75/8N4SV75 support the same level of flexibility than the other VCXO devices, but do not offer an I2C serial interface for in-field re-programming of the output frequencies. Consult the section VCXO Frequency and Pull-Range Configuration on page 16 for details on frequency and pull range programming capabilities. The section “Crystal Stability” applies as well. Factory pre-set programming involves the specification of the desired output frequencies and VCXO pull range by an order code. Contact IDT sales for obtaining order codes.

XO Integer-Feedback Programming

Introduction

Each XO device supports frequency synthesis with the digital PLL limited to using an integer PLL-feedback divider. The advantage of the integer-feedback is the low output phase noise (typically 0.267 ps RMS for a 156.25 MHz output clock, 12kHz-20MHz integration range) compared to using the fractional PLL-feedback divider (about 0.8 ps RMS). Programming the XO to the integer PLL-feedback involves using *MINT* for synthesis, setting *MFRAC* to zero and disabling the DSM in the devices register for each pre-set frequency. The disadvantage of integer-feedback is a limited flexibility in frequency programming. The frequency resolution Δf of the synthesizer is a function of the length of the *M (MINT + FRAC)* register. With *MFRAC* = 0, the resolution is limited to a small range of output frequencies compared to using the full fractional-feedback capabilities of the synthesizer core. Note that the digital synthesis error is zero when *MFRAC*=0.

Integer-feedback works with any of the two available crystal reference frequencies of 100 and 114.285 MHz. IDT recommends to order XO devices with a 100 MHz XTAL for the wider range of popular industry frequencies that can be accomplished with that reference frequency. Devices ordered with pre-set integer PLL feedback use the order codes dddd = 1xxx.

VCXO devices do not support integer-feedback: frequency pulling requires the fractional-feedback divider.

Principles of Operation

The integer-only mode uses the synthesizer integer core rather than the fractional-feedback. *MFRAC* must set to zero and the DSM disabled. Output frequencies are derived from a 100 MHz reference frequency by using integer multiplication and division. The 2-bit prescaler (*P*), 7-bit integer feedback divider (*MINT*) and the 7-bit output divider (*N*) are available for frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{MINT}{P \cdot N} \qquad (12)$$

or by using the recommend XTAL frequency:

$$f_{OUT} = 100MHz \cdot \frac{MINT[4:0]}{P[4:0] \cdot N[6:0]}$$

Register configuration, crystal stability and the selection of pre-set frequency characteristics and features remains the same also for integer-feedback. It is recommended to follow to following procedure for obtaining a valid configuration:

Frequency Configuration

1. In integer-feedback mode, the device supports the output frequencies that satisfy *all* of these criteria:
- f_{OUT} = 100.00 MHz ÷ *P* · *MINT* ÷ *N*
- 1950 MHz <= (f_{OUT} · *N*) <= 2600 MHz
- *P* is either 1, 2, 4 or 5
- *N* is in the range of 2, 3, 4, 5, 6 or
  N is in the range of 8, 10, 12..., 124, 126 (increment 2)
- *MINT* is in the range of 1...127 and is an integer

2. Determine the VCO frequency and output divider *N*:
Multiplying the desired output frequency f_{OUT} by some integer *N* (*N* is the output divider value and has the range of 2, 3, 4, 5, 6, 8, 10,...,126, see table 11) that will situate the VCO frequency within the PLL lock range (1950MHz to 2600MHz). For example, if an output frequency of 400MHz is desired, the output divider must be set to *N* = 5, which will result in a VCO frequency of 2000MHz. 2000MHz satisfies the PLL lock frequency range criteria. The setting for the N registers can be looked-up from table 11: *N* = 5 corresponds to the register setting of 0x05.

3. Calculate the required multiplication value M in conjunction with the pre-scaler P:
Divide the VCO frequency from step 2 by the PLL reference frequency f_{REF} ÷ *P*. *P* can be equal to 1, 2, 4 or 5. Set P to 1, 2, 4 or 5 (in this order) and check with the conditions under step 1 to achieve a valid *P*, *M* and *N* combination.

If multiple *P*, *M* and *N* configurations are available for a given output frequency, select the one with the smallest P divider and smallest possible M divider. For instance, to achieve an output frequency of 400 MHz, the configuration P=1, M=20 and N=5 is preferred over P=2, M=48 and N=6. The highest possible phase detector frequency and the smallest possible feedback divider ensures the best possible phase noise characteristics. The PLL reference frequency is the frequency of the internal crystal oscillator (100.00MHz).

4. Program any of the Pn, MINTn and Nn register sets (n = 0, 1, 2 or 3) with the calculated values: MINTn = 20 (0x14), N = 5 (0x05)). The devices have one, two or four frequency sets. In the case multiple frequency sets, the FSEL[1:0] pin(s) select(s) the register set that sets the output frequency. For correct operation, set both the DSM_ENAn and ADC_ENA bits to zero (disable).

5. PLL recalibration (10 pin devices)
Toggle the FSEL[1:0] bits in register 18 (See table 5 for the register map) or the FSEL[1:0] pins to force a PLL recalibration. PLL recalibration is required every time PLL feedback register (*MINT*) is reprogrammed after power-up.

Table 11. PLL Post Divider N Coding[1]

Register Bit	Frequency Divider *N*	Output frequency range	
N_N[6:0]		$f_{OUT,MIN}$ (MHz)	$f_{OUT,MAX}$ (MHz)
000000X	2	975	1300
0000010	2	975	1300
0000011	3	650	866.66
0000100	4	487.5	650
0000101	5	390	520
000011X	6	325	433.33
000100X	8	243.75	325
000101X	10	195	260
000110X	12	162.5	216.66
000111X	14	139.29	185.71
001000X	16	121.87	162.5
...	N (even integer)	(1950 ÷ *N*)	(2600 ÷ *N*)
111101X	124	15.73	20.97
111111X	126	15.48	20.63

1.NOTE: “X” can be either 0 or 1 (don’t care).

Example Configurations

The following configurations are examples for the generation of popular standard industry frequencies. All frequencies are generated with zero-ppm deviation from the internal reference frequency of 100MHz. The stability of the output frequency only depends only the stability of the internal 100.00 MHz crystal.

Table 12. Ethernet Configurations

Configuration			f_{OUT} (MHz)
P	M	N	
1	20	80	25
1	20	16	125
1	25	16	156.25
1	25	8	312.5

Table 13. Configurations for FibreChannel

Configuration			f_{OUT} (MHz)
P	M	N	
2	85	20	106.25
2	51	10	212.5

Table 14. Configurations for PCIe

Configuration			f_{OUT} (MHz)
P	M	N	
1	20	20	100
1	20	10	200
1	20	8	250

Table 15. Configurations for Processor and DSP Clocks

Configuration			f_{OUT} (MHz)
P	M	N	
5	99	60	33
1	20	60	33.3333
1	20	40	50
5	99	30	66
1	20	30	66.6666
1	20	20	100
1	21	14	150
1	20	12	166.6666
1	20	10	200

Table 16. Other example Frequency Configurations

Configuration			f_{OUT} (MHz)
P	M	N	
1	20	2	1000
1	24	3	800
1	24	4	600
1	20	4	500
1	20	5	400
2	45	12	187.5
2	45	6	375
1	24	20	120
5	112	14	160

Serial Interface Description

The FemtoClockNG Ceramic 5x7 Modules have an I²C-compatible configuration interface to access any of the internal registers for frequency and PLL parameter programming. The devices act as a slave device on the I²C bus and has the address 0b1101110. The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address. See table as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, Table 18 and table Table 19). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate I²C the read or write transfer after accessing byte #23.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Table 17. I²C Device Slave Address

1	1	0	1	1	1	0	R/W

Table 18. Block Write Operation

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W(0)	ACK	Address Byte P	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 19. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte P	ACK	Repeated START	Slave Address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

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