ForgeFPGA

SLG7SC1 Socket Card #1

Description

ForgeFPGA™ Socket Card #1 is designed for emulation and prototyping of ForgeFPGA integrated circuits.

Specifications

The ForgeFPGA Socket Card #1 provides a connection between the pins of a ForgeFPGA and a development board. This board can be used for design prototyping with various boot modes. The Socket Card supports the PMOD standard, allowing the connection of different PMOD adapters.

Features

- STQFN-24 package compatibility
- Programming and emulation
- Standalone boot option
- Onboard 4-Mbit SPI flash
- PMOD connectors
- Clock generator from 2.5kHz to 200MHz
- Standalone power connectors

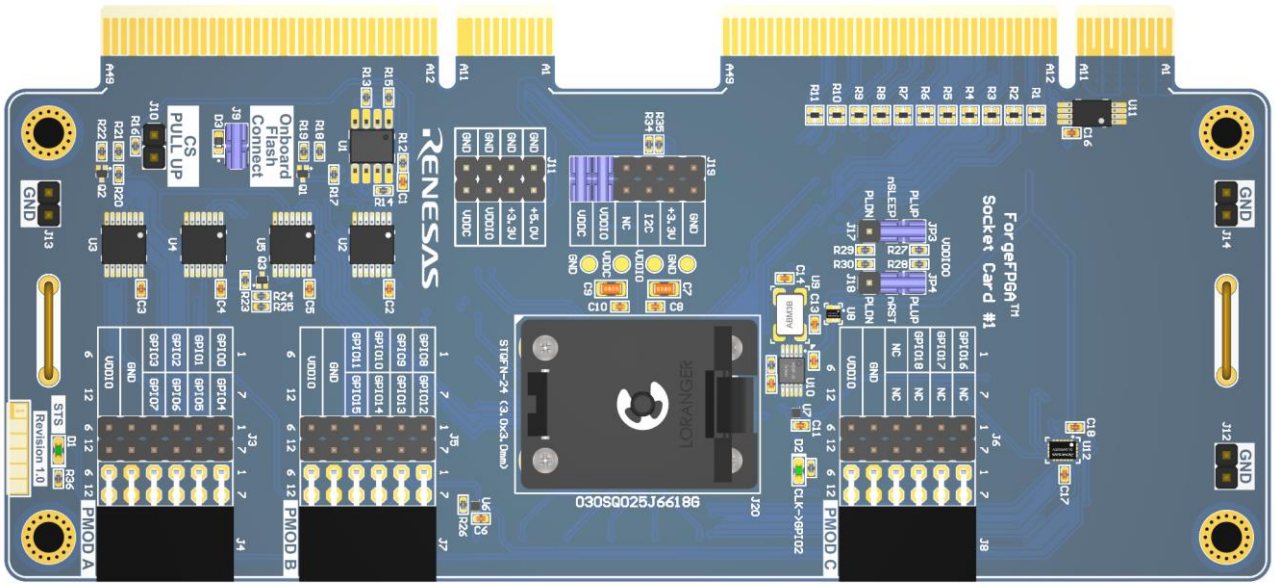


Figure 1. ForgeFPGA Socket Card #1

Contents

Figures

Tables

1. Functional Description

Figure 2 shows the board view and identifies its main components. This board can be used in conjunction with the Go Configure Development Board using the Dual Interaction Connector to transmit and process signals. It can also operate as a standalone unit. The chip can be powered either by the development board or through the External Power connector, and signals on the GPIO are accessible through the 12-pin GPIO connectors or PMOD connectors.

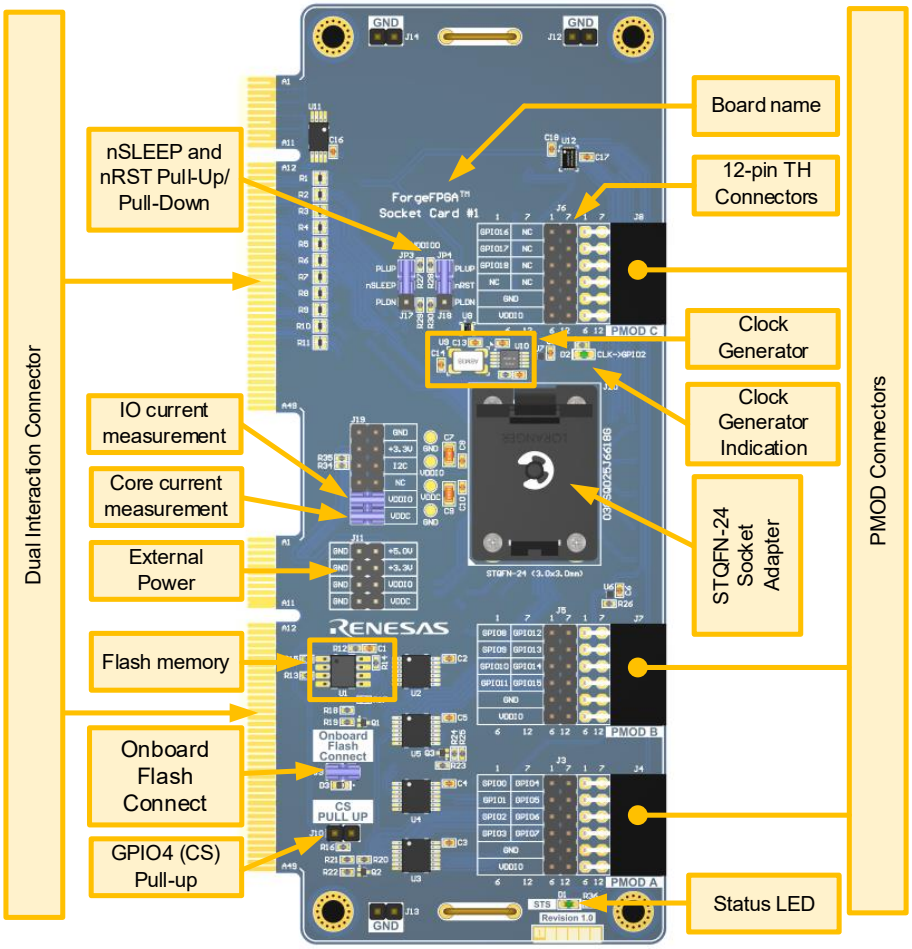


Figure 2. ForgeFPGA Socket Card #1 Components

1.1 PMOD and GPIO Connectors

Access to the socket pins is provided through the GPIO and PMOD connectors, both of which share the same pinout. *Note:* Programming signals from the Interaction Connector to the GPIO/PMOD are gated during programming and emulation entry sequences.

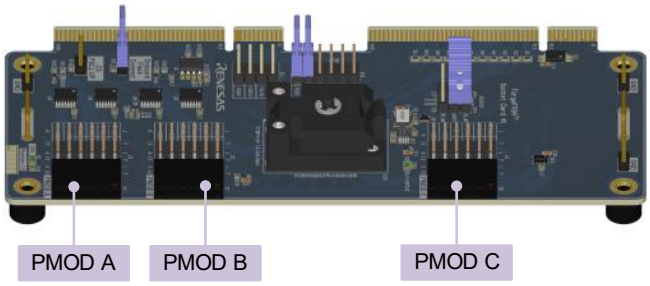


Figure 3. PMOD and GPIO Connector

Table 1 and **Table 2** show the PMOD and external connectors pinout and characteristics.

Table 1. PMOD A-C and External Connectors Pinout

PMOD PIN #	PIN Name		
	GPIO/PMOD A	GPIO/PMOD B	GPIO/PMOD C
1	GPIO0	GPIO8	GPIO16
2	GPIO1	GPIO9	GPIO17
3	GPIO2	GPIO10	GPIO18
4	GPIO3	GPIO11	-
5	GND	GND	GND
6	VDDIO0	VDDIO0	VDDIO0
7	GPIO4	GPIO12	-
8	GPIO5	GPIO13	-
9	GPIO6	GPIO14	-
10	GPIO7	GPIO15	-
11	GND	GND	GND
12	VDDIO0	VDDIO0	VDDIO0

Table 2. GPIO and PMOD Connector Characteristics

Parameter	Description	Min	Typ	Max	Unit
I_L	Input leakage current	-	2	-	µA
C_{IO}	Input-Output Pin Capacitance	-	7	-	pF
R_{ON}	Series Resistance	-	25	52	Ω
V_{IN}	Input Voltage	-0.5	-	VDDIO	V

1.2 ForgeFPGA Current Measuring

ForgeFPGA Socket Card #1 also includes an option for measuring IC power consumption. To perform this measurement, remove the jumpers (as shown on **Figure 4**) and connect a current meter in their place. The typical load should not exceed 200 mA. Under normal operation, when current measurement is not required, the jumpers should remain installed on the board.

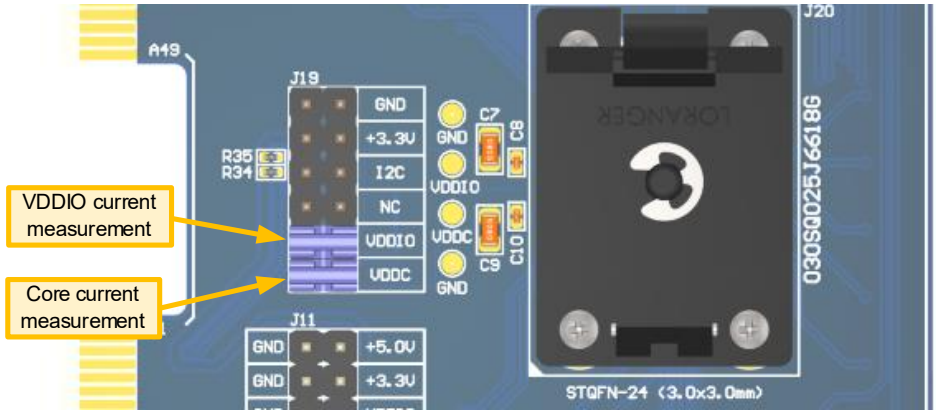


Figure 4. ForgeFPGA Current Measurement Setup

1.3 SPI Interface between ForgeFPGA and Flash Memory

Figure 5 shows the SPI flash interface connection between ForgeFPGA IC and Flash Memory.

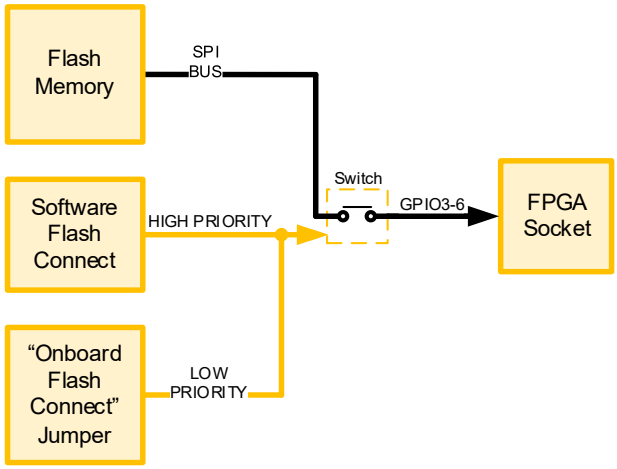
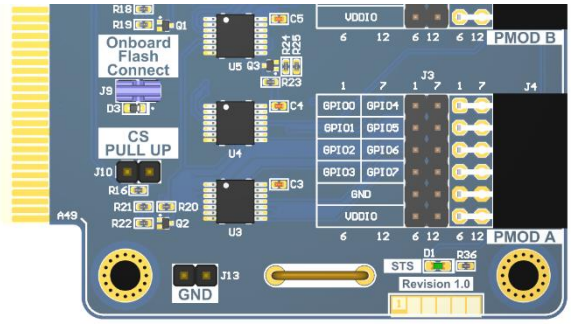


Figure 5. SPI interface Connection

The Onboard Flash Connect and CS PULL UP jumpers should be installed when using the board with the development board. *Note:* Jumper removal or configuration changes are overridden and controlled by the development board. The table in **Figure 6** shows the correct jumper setup for standalone operation.



Mode	Onboard Flash Connect	CS PULL UP
Internal OTP Memory	0	0
SPI FLASH Memory	1	X
EXT Flash Memory	0	1

Figure 6. Memory Selection Table for Boot Configuration

External Flash Memory can be connected to Socket Card by using PMOD A.

Figure 7 shows how to connect External Flash Memory to PMOD A.

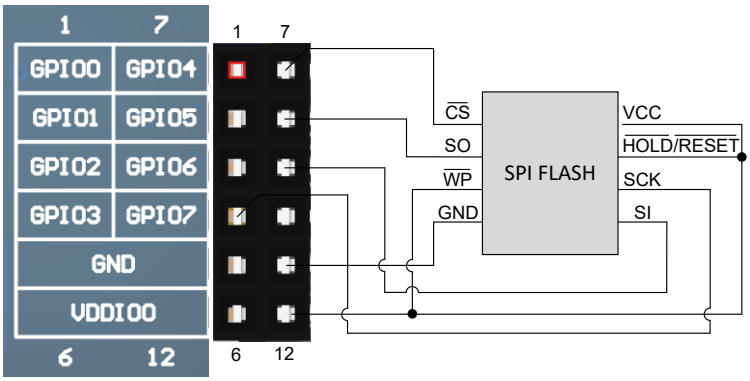


Figure 7. Connection of External Flash Memory to PMOD A

1.4 External Power Connector

ForgeFPGA Socket Card #1 can also operate with an external power supply. In this case, four separate power supply channels must be connected to the External Power (J11) connector (shown in **Figure 8**). The voltage and current levels for VDDIO0, VDDIO1, and VDDC must comply with the ForgeFPGA IC specifications. The 5.0V terminal should be supplied with 5.0V to power the commutation switches. The external power supply option can only be used when the Socket Card is not connected to the Go Configure Development Board.

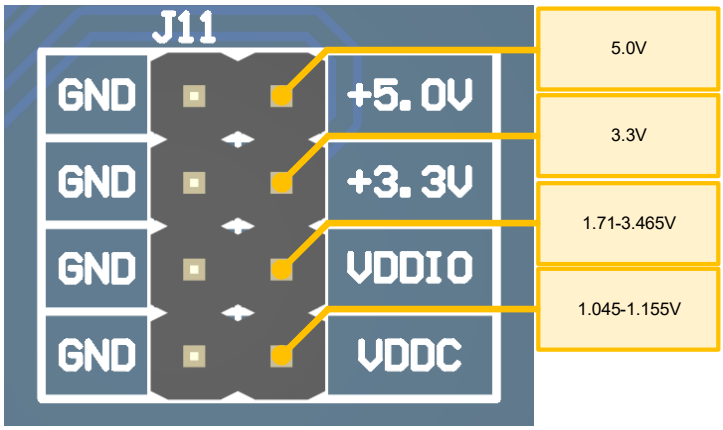


Figure 8. External Power Connector Pinout

1.5 Clock Generator

ForgeFPGA Socket Card #1 has I²C Programmable CMOS Clock Generator – Si5351A-B-GTR.

It is used to drive PLL input of ForgeFPGA – GPIO2.

Table 3 shows the main characteristics of the Clock Generator.

Table 3. Main Characteristics of Clock Generator

Parameter	Description	Min	Typ	Max	Unit
F_{CLK}	Frequency Range	0.0025	-	200	MHz
J_{PER}	Period Jitter	-	70	155	ps, pk-pk
V_{DDX}	Output Buffer Voltage	-	VDDIO	-	V
I_{DDX}	Output Buffer Supply Current (Per Output)	-	2.2	5.6	mA

1.6 Status LED

The status LED indicates the current operation being performed on the chip (see Table 4).

Table 4. Status LED Description

Chip Standard Operations	Flash Operations
Read	Read
Program	Program
Emulation	Erase
Test Mode	Test Mode

The position of the Status LED (D1) is shown on **Figure 9**.

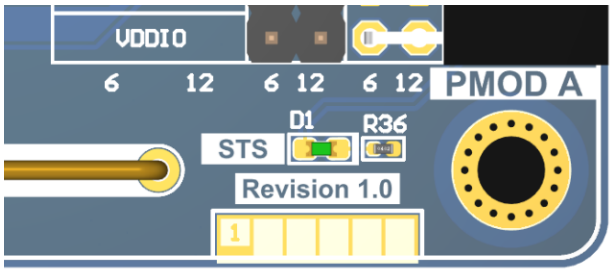


Figure 9. Status LED

2. Working with ForgeFPGA Products

To start working with ForgeFPGA products using the Socket Card, two methodologies are available:

- Using the Go Configure Development Board.
- In standalone mode, where the ForgeFPGA configuration is downloaded from the onboard SPI flash.

2.1 Standalone Working Mode

As previously described, ForgeFPGA can boot from onboard flash as an SPI host. There are two ways of programming onboard flash: program with the development board or program the flash IC manually. The programming pins for the flash chip are accessible through the PMOD A connector. To program manually, the Socket Card must be powered using the EXT Power connector. If the VDDIO voltage is equal to or greater than 3.0 V, the 5V and VDDIO pins can be powered from the same source.

For these operations, the ForgeFPGA must be disabled by applying logic LOW (to the nRST pins. Additionally, the Onboard Flash Connect and CS PULL UP jumpers must be installed. If the SPI flash is programmed correctly, setting logic HIGH to both the nRST and nSLEEP pins allows the ForgeFPGA to boot from the SPI flash.

2.2 Configuration with Go Configure Development Board

To begin working with ForgeFPGA products, connect the platform to a PC using a USB Type-C cable and apply power.

Important: Connect the USB cable directly to the PC. Avoid using USB hubs or docking stations. Ensure the Socket Card is properly connected to the Go Configure Development Board as shown on **Figure 10**.

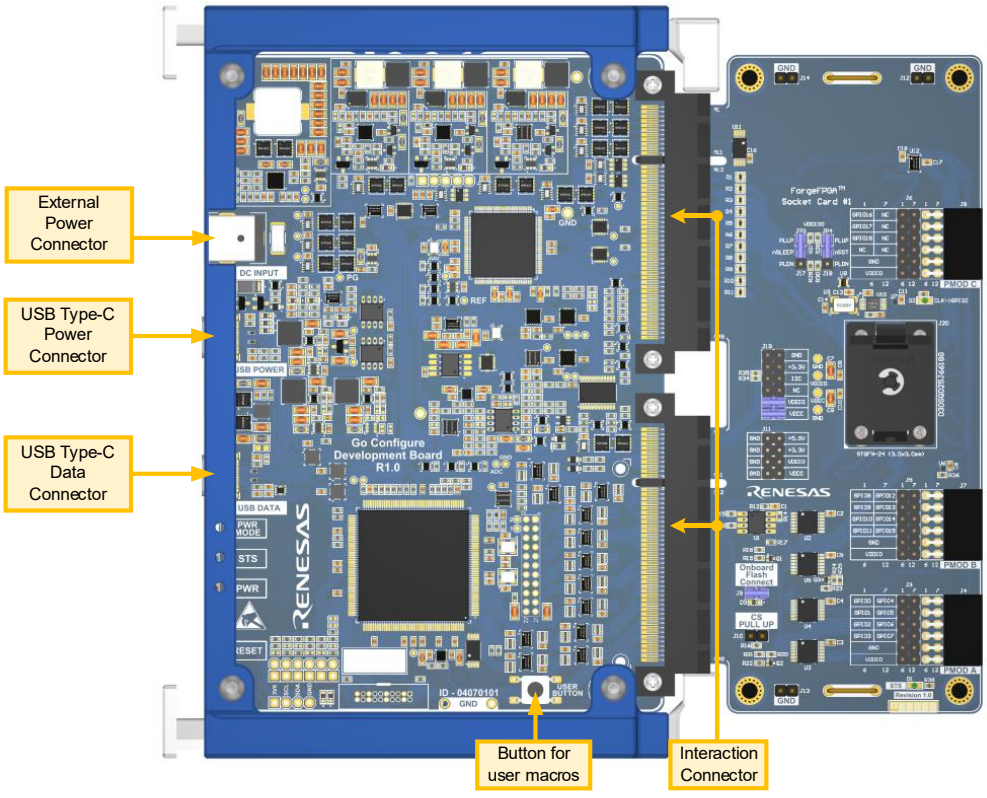


Figure 10. Development Kit

If all the connections are correct, the red LED (PWR) automatically turn on. After selecting **Go Configure Development Board** in Go Configure **Debug** tab, the blue LED blinks several times, and the HW-FW version appear in the bottom-left corner of the debugging control window.

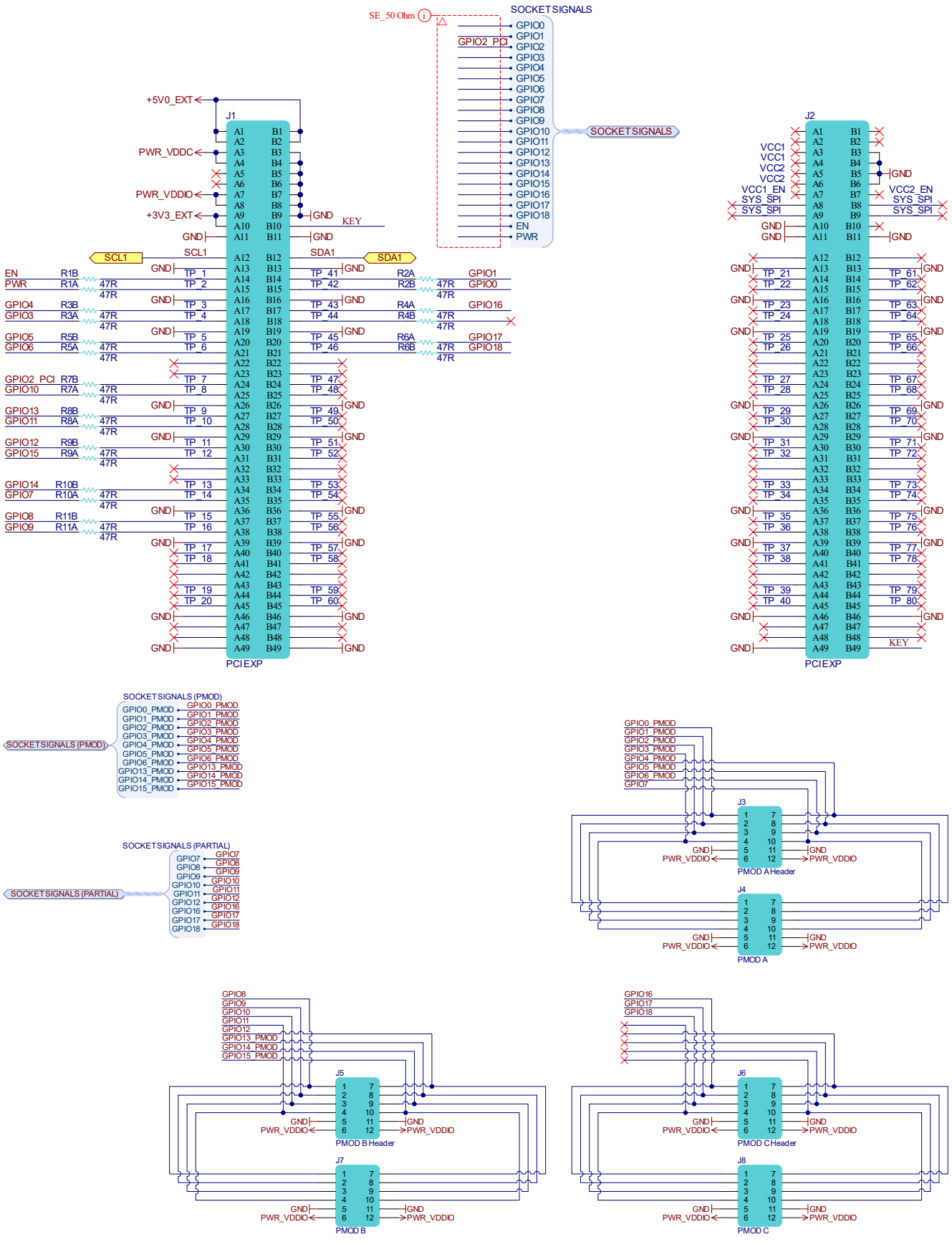
The following debug options are available:

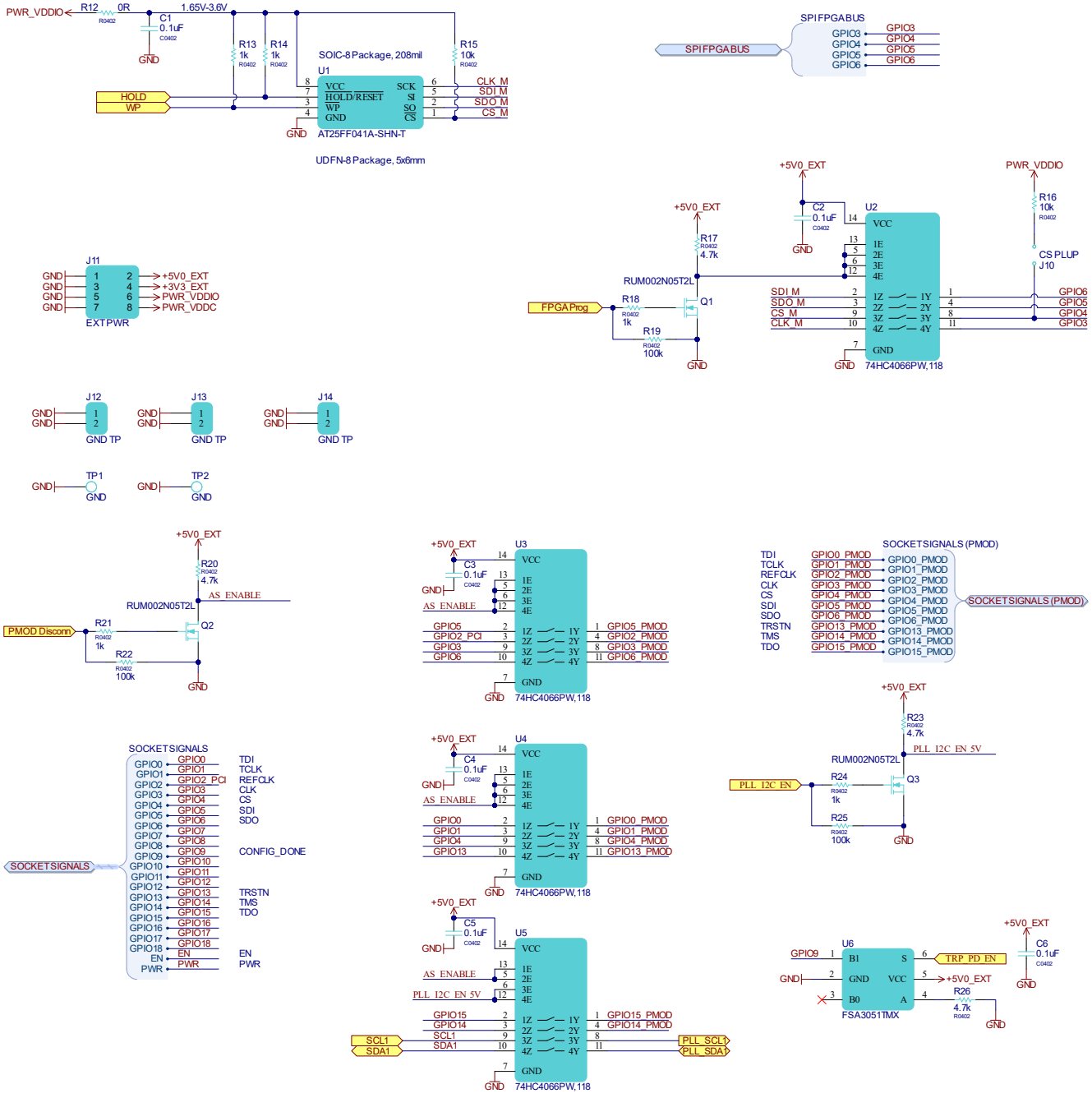
- Emulation – allows debugging of the current project. This mode is available only after synthesis and bitstream generation in the FPGA Editor.
- Test Mode – enables debugging of a programmed project.
- Test Mode* – used to debug a project loaded from SPI Flash.
- Read – reads the configuration from the programmed chip and opens the project in a new software instance or in the Project Data window of the current instance.
- Program – programs the chip with the current project.
- TP Map – displays the test point map in the workspace, reflecting the physical test points on the development platform.

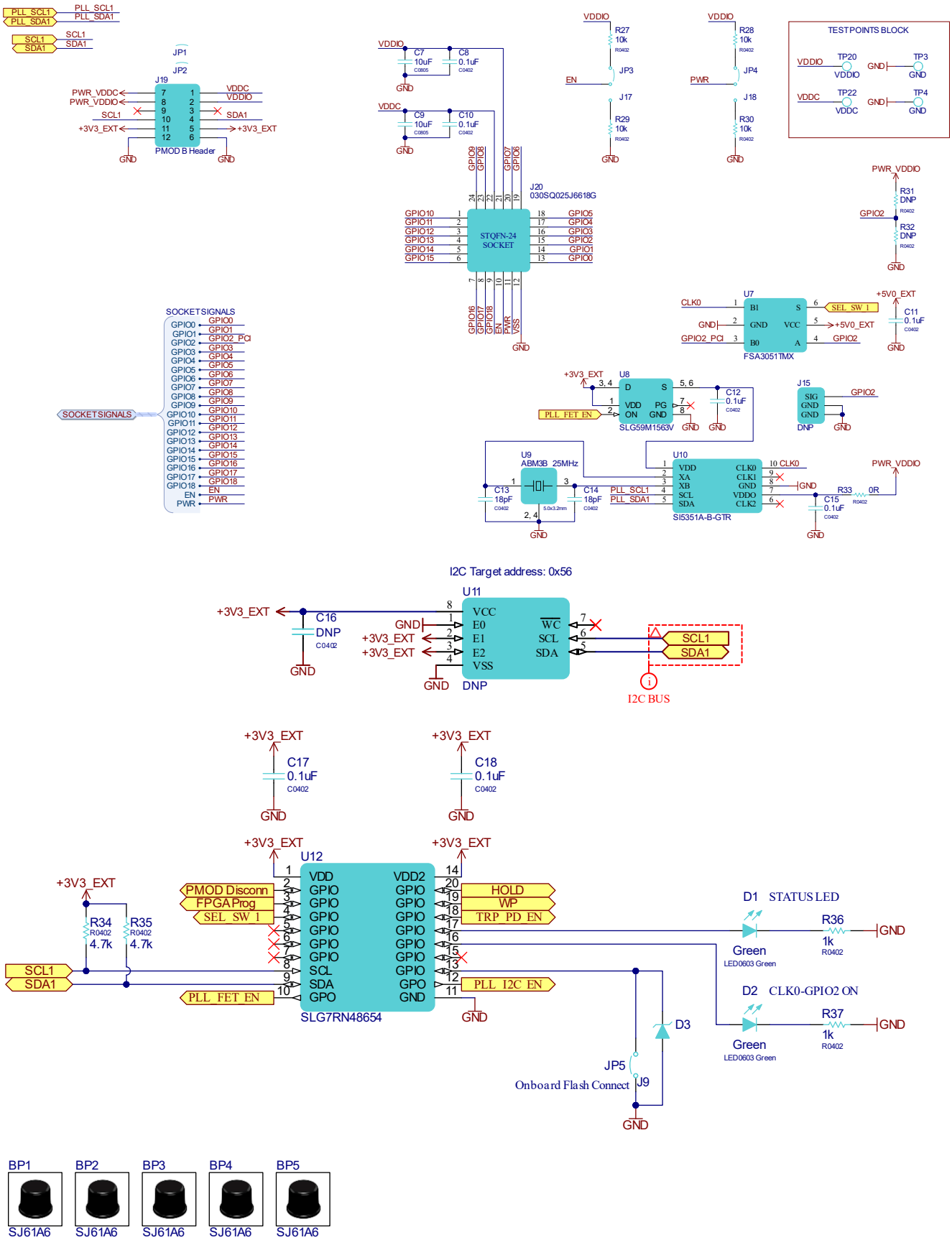
More detailed information about Go Configure software can be found in *Go Configure™ Software Hub User Guide*.

3. Board Design

3.1 Schematic Diagrams




PWR_VDDIO
R12
0R
1.65V-3.6V
C1
0.1uF
GND
R13
1k
R14
1k
SOIC-8 Package, 208mil
U1
R15
10k
HOLD
WP
VCC
HOLD/RESET
WP
GND
SCK
SI
SO
CS
CLK_M
SDI_M
SDO_M
CS_M
AT25FF041A-SHN-T
UDFN-8 Package, 5x6mm
SPI FPGA BUS
GPIO3
GPIO4
GPIO5
GPIO6
J11
EXT PWR
+5V0_EXT
+3V3_EXT
PWR_VDDIO
PWR_VDDC
+5V0_EXT
R17
4.7k
RUM002N05T2L
FPGA Prog
R18
1k
R19
100k
Q1
C2
0.1uF
U2
74HC4066PW,118
R16
10k
CS PLUP
J10
J12
J13
J14
GND TP
TP1
TP2
R20
4.7k
AS_ENABLE
PMOD Disconn
R21
1k
R22
100k
Q2
U3
U4
U5
C3
C4
C5
SOCKET SIGNALS (PMOD)
TDI
TCLK
REFCLK
CLK
CS
SDI
SDO
TRSTN
TMS
TDO
SOCKET SIGNALS
CONFIG_DONE
EN
PWR
R23
4.7k
PLL_I2C_EN_5V
PLL_I2C_EN
R24
1k
R25
100k
Q3
U6
FSA3051TMX
TRP_PD_EN
C6
0.1uF
R26
4.7k
SCL1
SDA1
PLL_SCL
PLL_SDA


PLL_SCL1
PLL_SDA1
SCL1
SDA1
JP1
JP2
J19
PMOD B Header
PWR_VDDC
PWR_VDDIO
VDDC
VDDIO
+3V3_EXT
GND
J20
030SQ025J6618G
STQFN-24
SOCKET
SOCKETSIGNALS
R27
R28
R29
R30
JP3
JP4
J17
J18
EN
PWR
TEST POINTS BLOCK
TP20
TP3
TP22
TP4
R31
R32
DNP
U7
FSA3051TMX
SEL_SW_1
+5V0_EXT
U8
SLG59M1563V
PLL_FET_EN
J15
U9
ABM3B 25MHz
U10
SI5351A-B-GTR
I2C Target address: 0x56
U11
C16
C17
C18
0.1uF
U12
SLG7RN48654
PMOD Disconn
FPGAProg
SEL_SW_1
HOLD
WP
TRP_PD_EN
PLL_I2C_EN
R34
R35
4.7k
D1 STATUS LED
D2 CLK0-GPIO2 ON
D3
Green
LED0603 Green
R36
R37
1k
JP5
J9
Onboard Flash Connect
I2C BUS
BP1
BP2
BP3
BP4
BP5
SJ61A6

3.2 Bill of Materials

Item #	Designator	Manufacturer Part Number	Manufacturer	Quantity
1	BP1, BP2, BP3, BP4, BP5	SJ61A6	3M	5
2	C1-C6, C8, C10-C12, C15, C17, C18	GCM155R71C104KA55D	Murata	13
3	C7, C9	GRM21BR61C106KE15L	Murata	2
4	C13, C14	CL05C180JB5NNNC	Samsung	2
5	C16	DNP	DNP	1
6	D1, D2	150060GS75000	Wurth Electronics	2
7	D3	DESD5V0U1BB-7	Diodes	1
8	J3, J5, J6, J19	67996-212HLF	Amphenol ICC / FCI	4
9	J4, J7, J8	PPPC062LJBN-RC	Sullins	3
10	J9, J10	68000102HLF	Amphenol ICC / FCI	2
11	J11	10129381-908001BLF	Amphenol ICC / FCI	1
12	J12, J13, J14	68000102HLF	Amphenol ICC / FCI	3
13	J15	DNP	DNP	1
14	J17, J18	68000103HLF	Amphenol ICC / FCI	2
15	J20	030SQ025J6618G	Renesas Electronics America Inc	1
16	JP1, JP2, JP3, JP4, JP5	NPC02SXON-RC	Sullins	5
17	Q1, Q2, Q3	RUM002N05T2L	Rohm	3
18	R1-R11	S41X043470JP	CTS	11
19	R12, R33	RC0402JR-070RL	Yageo	2
20	R13, R14, R18, R21, R24, R36, R37	RC0402JR-071KL	Yageo	7
21	R15, R16, R27, R28, R29, R30	RC0402JR-0710KL	Yageo	6
22	R17, R20, R23, R26, R34, R35	RC0402JR-074K7L	Yageo	6
23	R19, R22, R25	RC0402JR-07100KL	Yageo	3
24	R31, R32	DNP	DNP	2
25	U1	AT25FF041A-SHN-T	Renesas	1
26	U2, U3, U4, U5	74HC4066PW,118	Nexperia	4
27	U6, U7	FSA3051TMX	ON Semiconductor / Fairchild	2
28	U8	SLG59M1563V	Renesas Electronics America Inc	1
29	U9	ABM3B-25.000MHZ-D2Y-T	Abracon	1
30	U10	SI5351A-B-GTR	Skyworks Solutions	1
31	U11	DNP	DNP	1
32	U12	SLG7RN48654	Renesas Electronics America Inc	1

4. Revision History

Revision	Date	Description
1.00	Dec 9, 2025	Initial release.