

ForgeFPGA

SLG7SC3 Socket Card #3

Description

ForgeFPGA™ Socket Card #3 is designed for emulation and prototyping of ForgeFPGA integrated circuits.

Specifications

The ForgeFPGA Socket Card #3 provides a connection between the pins of a ForgeFPGA and a development board. This board can be used for design prototyping with various boot modes. The Socket Card supports the PMOD standard, allowing the connection of different PMOD adapters.

Features

- QFN-48 package compatibility
- Programming and emulation
- Standalone boot option
- Onboard 4-Mbit SPI flash
- PMOD connectors
- Clock generator from 2.5kHz to 200MHz
- Standalone power connectors

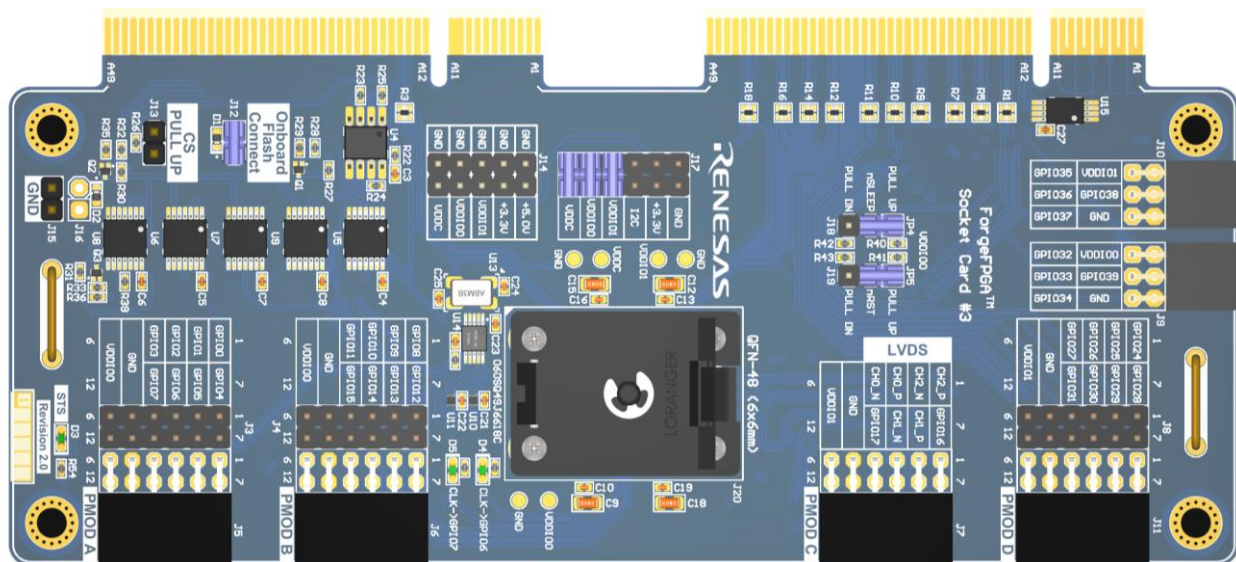


Figure 1. ForgeFPGA Socket Card #3

Contents

1. Functional Description	3
1.1 PMOD and GPIO Connectors.....	3
1.2 ForgeFPGA Current Measuring.....	4
1.3 SPI Interface between ForgeFPGA and Flash Memory.....	5
1.4 External Power Connector.....	6
1.5 Clock Generator.....	6
1.6 Status LED	7
2. Working with ForgeFPGA Products	8
2.1 Standalone Working Mode	8
2.2 Configuration with Go Configure Development Board	8
3. Board Design	10
3.1 Schematic Diagrams.....	10
4. Bill Of Materials.....	14
5. Revision History	15

Figures

Figure 1. ForgeFPGA Socket Card #3.....	1
Figure 2. ForgeFPGA Socket Card #3 Components	3
Figure 3. PMOD and GPIO Connector	4
Figure 4. ForgeFPGA Current Measurement Setup	5
Figure 5. SPI interface Connection.....	5
Figure 6. Memory Selection Table for Boot Configuration	5
Figure 7. Connection of External Flash Memory to PMOD A.....	6
Figure 8. External Power Connector Pinout	6
Figure 9. Status LED	7
Figure 10. Development Kit.....	8

Tables

Table 1. PMOD A-D and External Connectors Pinout	4
Table 2. GPIO and PMOD Connector Characteristics.....	4
Table 3. Main Characteristics of Clock Generator	6
Table 4. Status LED Description.....	7

1. Functional Description

Figure 2 shows the board view and identifies its main components. This board can be used in conjunction with the Go Configure Development Board using the Dual Interaction Connector to transmit and process signals. It can also operate as a standalone unit. The chip can be powered either by the development board or through the External Power connector, and signals on the GPIO are accessible through the 12-pin GPIO connectors or PMOD connectors.

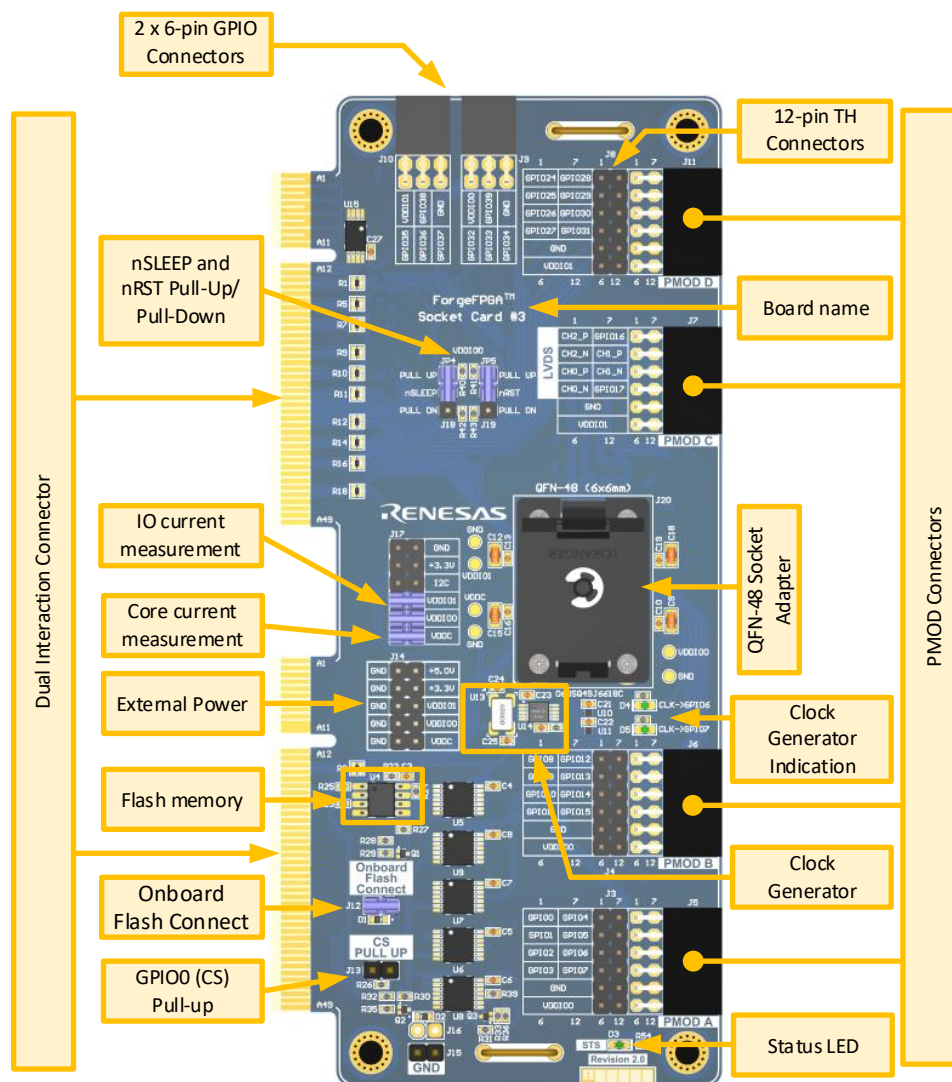
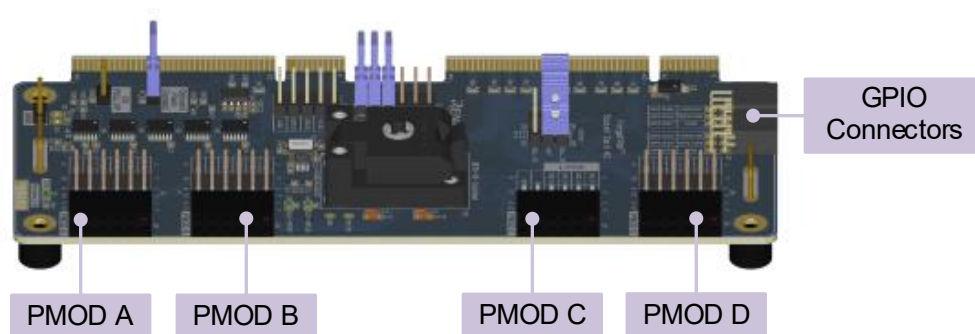


Figure 2. ForgeFPGA Socket Card #3 Components

1.1 PMOD and GPIO Connectors

Access to the socket pins is provided through the GPIO and PMOD connectors, both of which share the same pinout. *Note:* Programming signals from the Interaction Connector to the GPIO/PMOD are gated during programming and emulation entry sequences.



6	5	4	3	2	1
12	11	10	9	8	7

Figure 3. PMOD and GPIO Connector

Table 1 and Table 2 show the PMOD and external connectors pinout and characteristics.

Table 1. PMOD A-D and External Connectors Pinout

PMOD PIN #	PIN Name					
	GPIO/PMOD A	GPIO/PMOD B	GPIO/PMOD C	GPIO/PMOD D	GPIO CONN J9	GPIO CONN J10
1	GPIO0	GPIO8	LVDS_2_P/GPIO23	GPIO24	GPIO32	GPIO35
2	GPIO1	GPIO9	LVDS_2_N/GPIO22	GPIO25	GPIO33	GPIO36
3	GPIO2	GPIO10	LVDS_0_P/GPIO19	GPIO26	GPIO34	GPIO37
4	GPIO3	GPIO11	LVDS_0_N/GPIO18	GPIO27	VDDIO0	VDDIO1
5	GND	GND	GND	GND	GPIO39	GPIO38
6	VDDIO0	VDDIO0	VDDIO1	VDDIO1	-	-
7	GPIO4	GPIO12	GPIO16	GPIO28	-	-
8	GPIO5	GPIO13	LVDS_1_P/GPIO21	GPIO29	-	-
9	GPIO6	GPIO14	LVDS_1_N/GPIO20	GPIO30	-	-
10	GPIO7	GPIO15	GPIO17	GPIO31	-	-
11	GND	GND	GND	GND	-	-
12	VDDIO0	VDDIO0	VDDIO1	VDDIO1	-	-

Table 2. GPIO and PMOD Connector Characteristics

Parameter	Description	Min	Typ	Max	Unit
I_L	Input leakage current	-	2	-	μA
C_{IO}	Input-Output Pin Capacitance	-	7	-	pF
R_{ON}	Series Resistance	-	25	52	Ω
V_{IN}	Input Voltage	-0.5	-	VDDIO	V

1.2 ForgeFPGA Current Measuring

ForgeFPGA Socket Card #3 also includes an option for measuring IC power consumption. To perform this measurement, remove the jumpers (as shown on Figure 4) and connect a current meter in their place. The

typical load should not exceed 200mA. Under normal operation, when current measurement is not required, the jumpers should remain installed on the board.

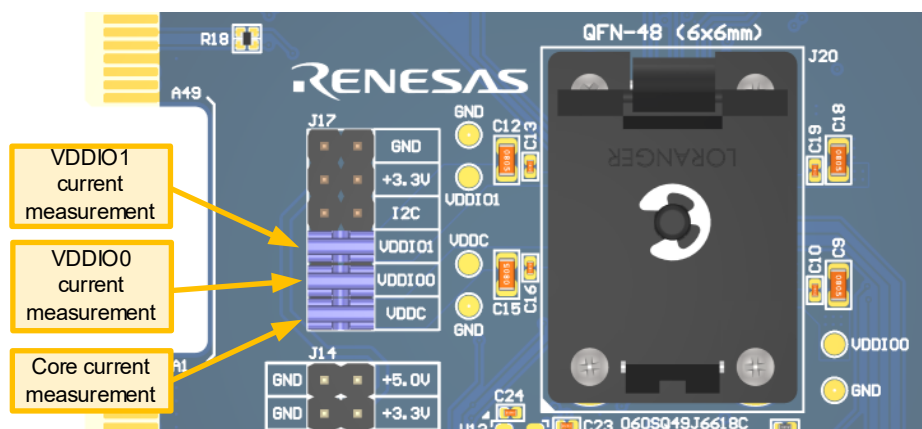


Figure 4. ForgeFPGA Current Measurement Setup

1.3 SPI Interface between ForgeFPGA and Flash Memory

Figure 5 shows the SPI flash interface connection between ForgeFPGA IC and Flash Memory.

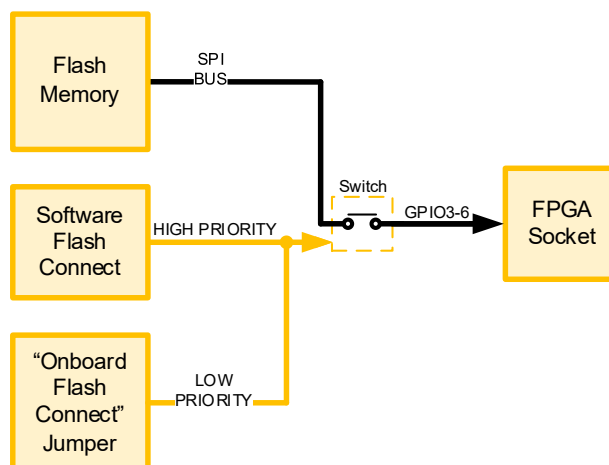
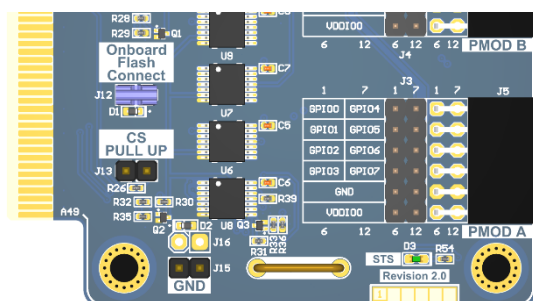


Figure 5. SPI interface Connection

The Onboard Flash Connect and CS PULL UP jumpers should be installed when using the board with the development board. *Note:* Jumper removal or configuration changes are overridden and controlled by the development board. The table in Figure 6 shows the correct jumper setup for standalone operation.



Mode	Onboard Flash Connect	CS PULL UP
Internal OTP Memory	0	0
SPI FLASH Memory	1	X
EXT Flash Memory	0	1

Figure 6. Memory Selection Table for Boot Configuration

External Flash Memory can be connected to Socket Card by using PMOD A.

Figure 7 shows how to connect External Flash Memory to PMOD A.

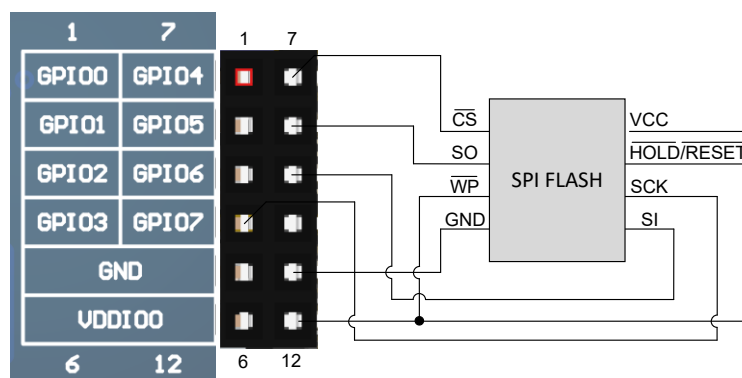


Figure 7. Connection of External Flash Memory to PMOD A

1.4 External Power Connector

ForgeFPGA Socket Card #3 can also operate with an external power supply. In this case, four separate power supply channels must be connected to the External Power (J14) connector (shown in **Figure 8**). The voltage and current levels for VDDIO0, VDDIO1, and VDDC must comply with the ForgeFPGA IC specifications. The 5.0V terminal should be supplied with 5.0V to power the commutation switches. The external power supply option can only be used when the Socket Card is not connected to the Go Configure Development Board.

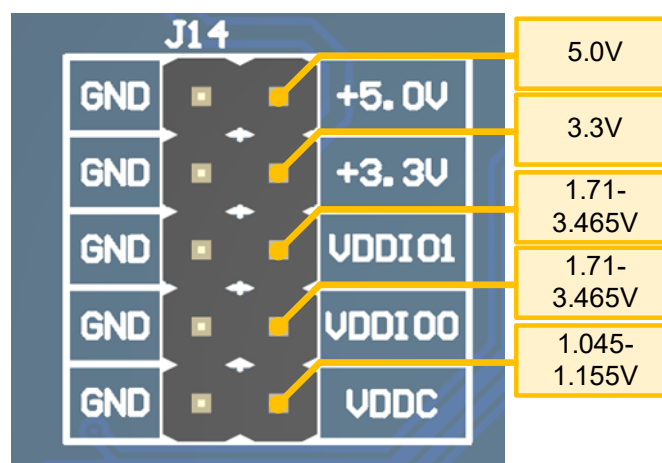


Figure 8. External Power Connector Pinout

1.5 Clock Generator

ForgeFPGA Socket Card #3 has I²C Programmable CMOS Clock Generator – Si5351A-B-GTR.

It is used to drive PLL input of ForgeFPGA – GPIO6 and GPIO7.

Table 3 shows the main characteristics of the Clock Generator.

Table 3. Main Characteristics of Clock Generator

Parameter	Description	Min	Typ	Max	Unit
F _{CLK}	Frequency Range	0.0025	-	200	MHz
J _{PER}	Period Jitter	-	70	155	ps, pk-pk
V _{DDX}	Output Buffer Voltage	-	VDDIO	-	V
I _{DDX}	Output Buffer Supply Current (Per Output)	-	2.2	5.6	mA

1.6 Status LED

The status LED indicates the current operation being performed on the chip (see **Table 4**).

Table 4. Status LED Description

Chip Standard Operations	Flash Operations
Read	Read
Program	Program
Emulation	Erase
Test Mode	Test Mode

The position of the Status LED (D1) is shown on **Figure 9**.



Figure 9. Status LED

2. Working with ForgeFPGA Products

To start working with ForgeFPGA products using the Socket Card, two methodologies are available:

- Using the Go Configure Development Board.
- In standalone mode, where the ForgeFPGA configuration is downloaded from the onboard SPI flash.

2.1 Standalone Working Mode

As previously described, ForgeFPGA can boot from onboard flash as an SPI host. There are two ways of programming onboard flash: program with the development board or program the flash IC manually. The programming pins for the flash chip are accessible through the PMOD A connector. To program manually, the Socket Card must be powered using the EXT Power connector. If the VDDIO voltage is equal to or greater than 3.0V, the 5V and VDDIO pins can be powered from the same source.

During this operation, the ForgeFPGA must be disabled by applying logic LOW to the nRST pin. Additionally, the Onboard Flash Connect and CS PULL UP jumpers must be installed. If the SPI flash is programmed correctly, setting logic HIGH to both the nRST and nSLEEP pins allows the ForgeFPGA to boot from the SPI flash.

2.2 Configuration with Go Configure Development Board

To begin working with ForgeFPGA products, connect the platform to a PC using a USB Type-C cable and apply power.

Important: Connect the USB cable directly to the PC. Avoid using USB hubs or docking stations. Ensure the Socket Card is properly connected to the Go Configure Development Board as shown on **Figure 10**.

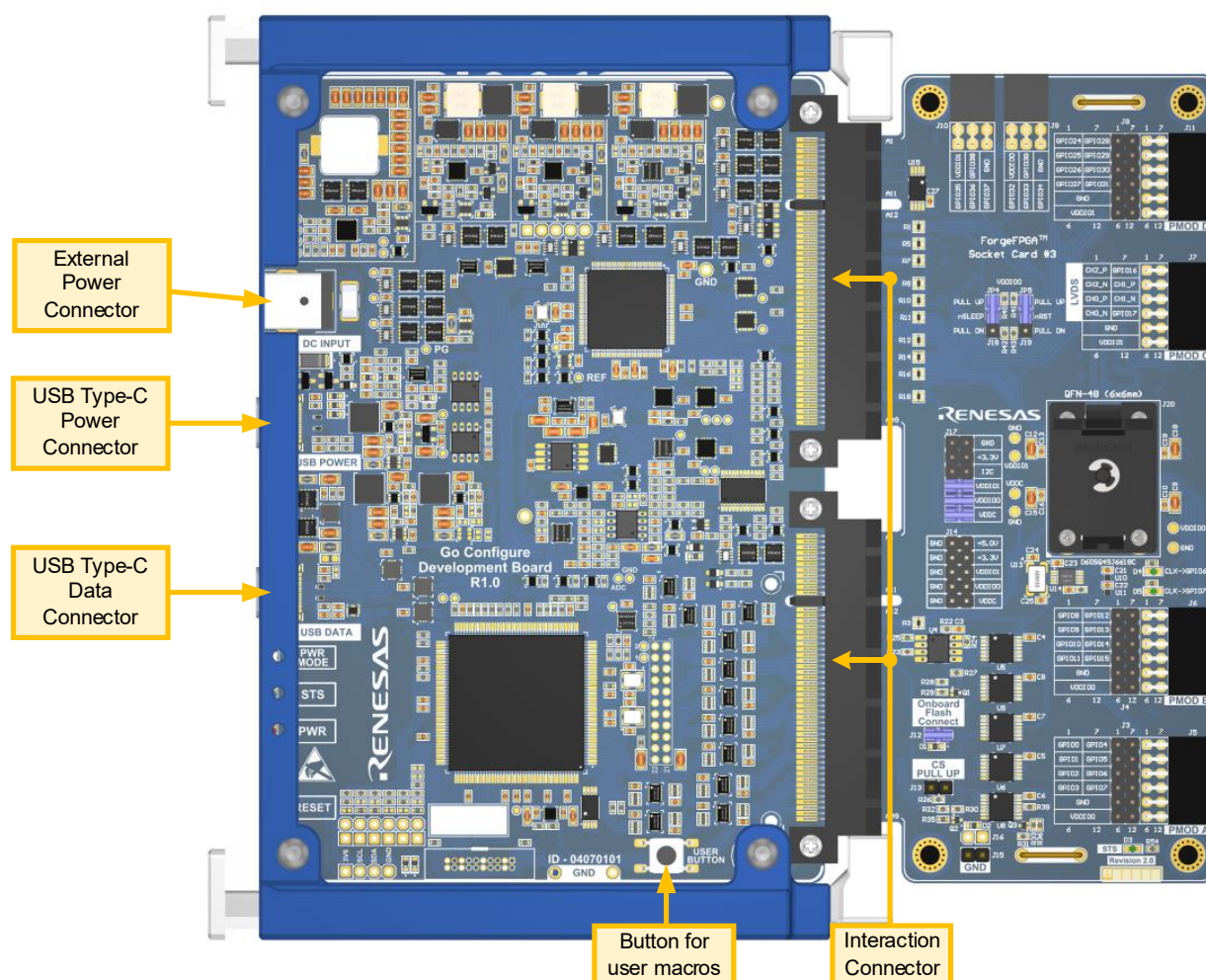


Figure 10. Development Kit

If all the connections are correct, the red LED (PWR) automatically turn on. After selecting **Go Configure Development Board** in Go Configure **Debug** tab, the blue LED blinks several times, and the HW-FW version appear in the bottom-left corner of the debugging control window.

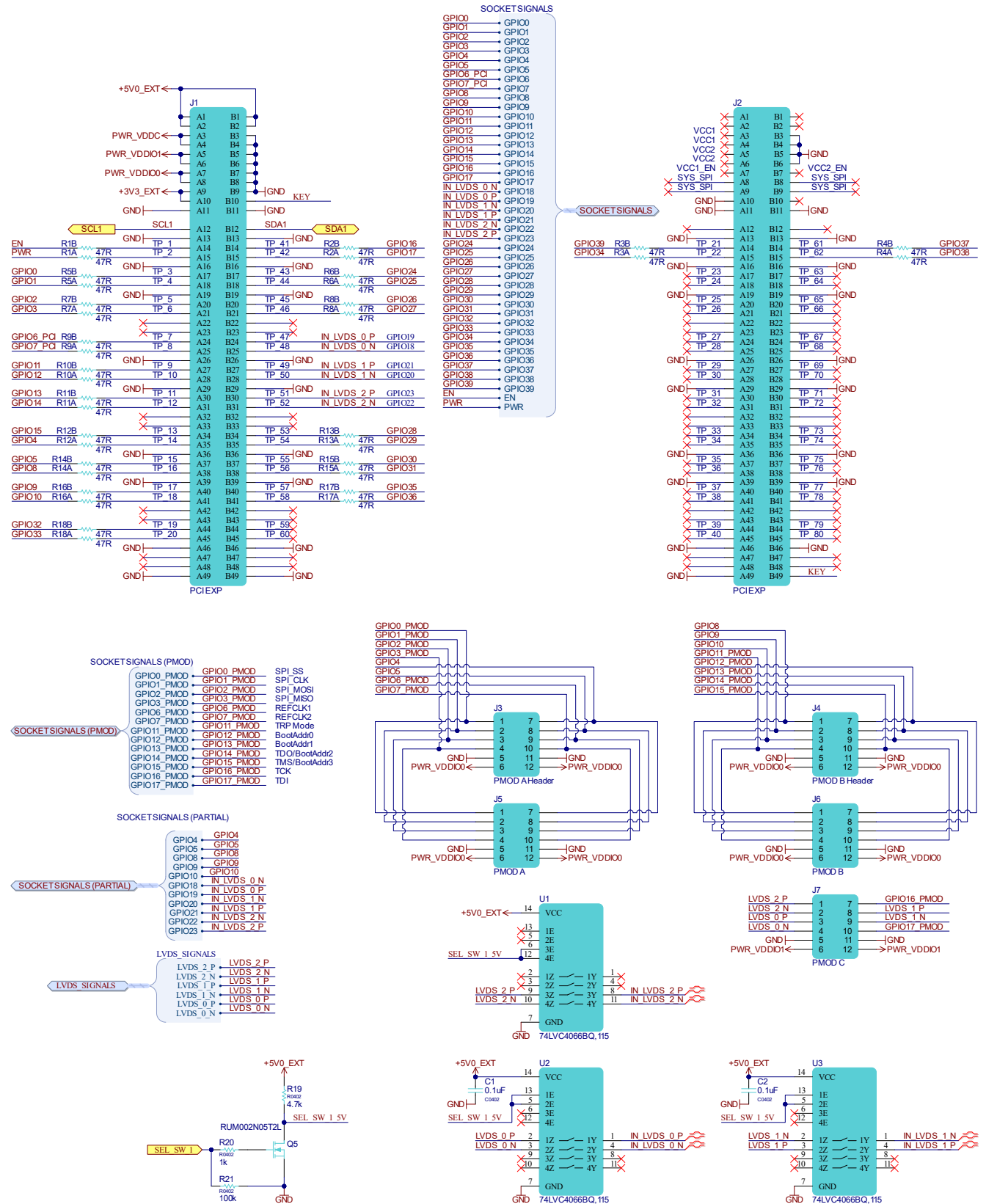
The following debug options are available:

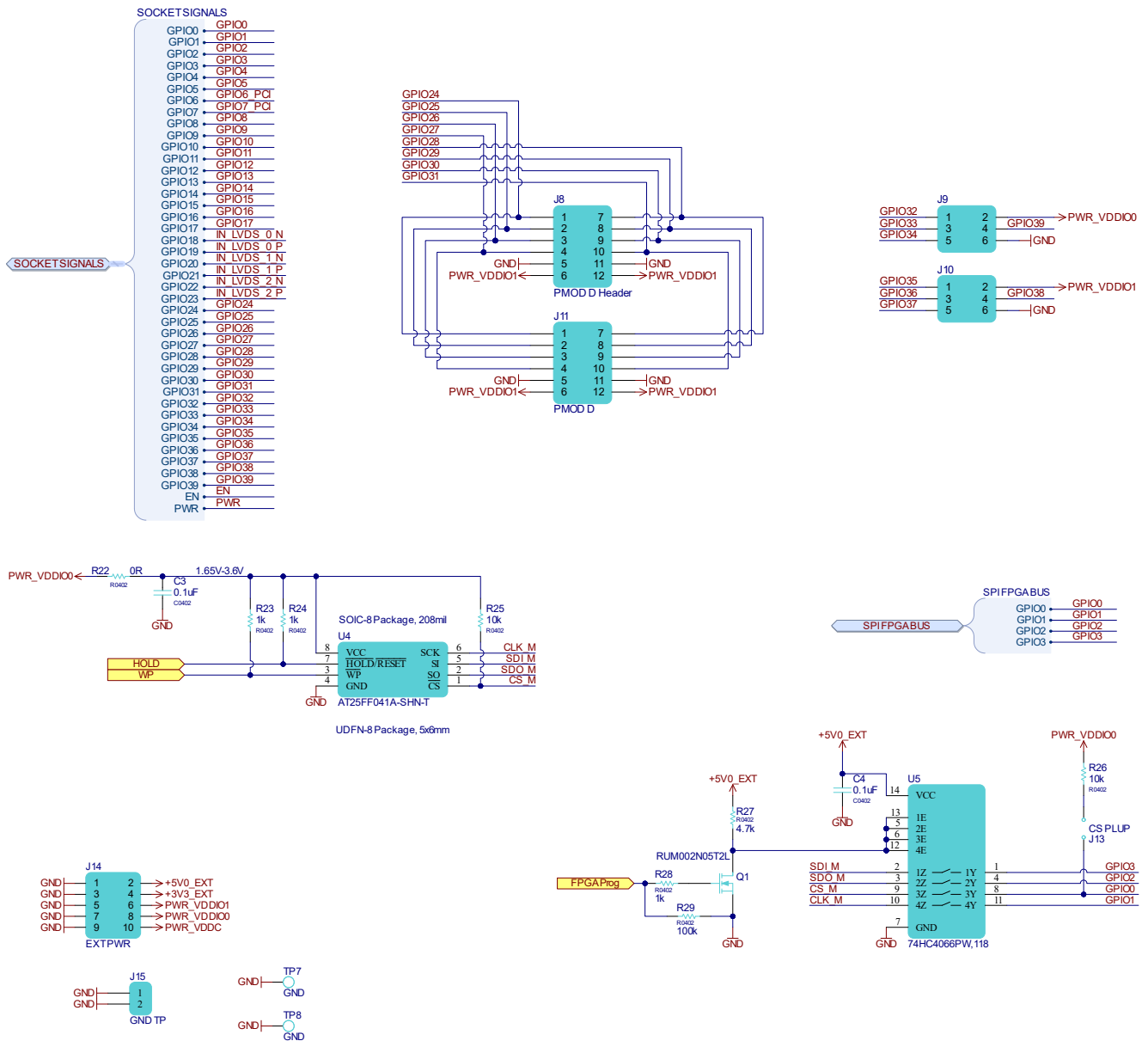
- Emulation – allows debugging of the current project. This mode is available only after synthesis and bitstream generation in the FPGA Editor.
- Test Mode – enables debugging of a programmed project.
- Test Mode* – used to debug a project loaded from SPI Flash.
- Read – reads the configuration from the programmed chip and opens the project in a new software instance or in the Project Data window of the current instance.
- Program – programs the chip with the current project.
- TP Map – displays the test point map in the workspace, reflecting the physical test points on the development platform.

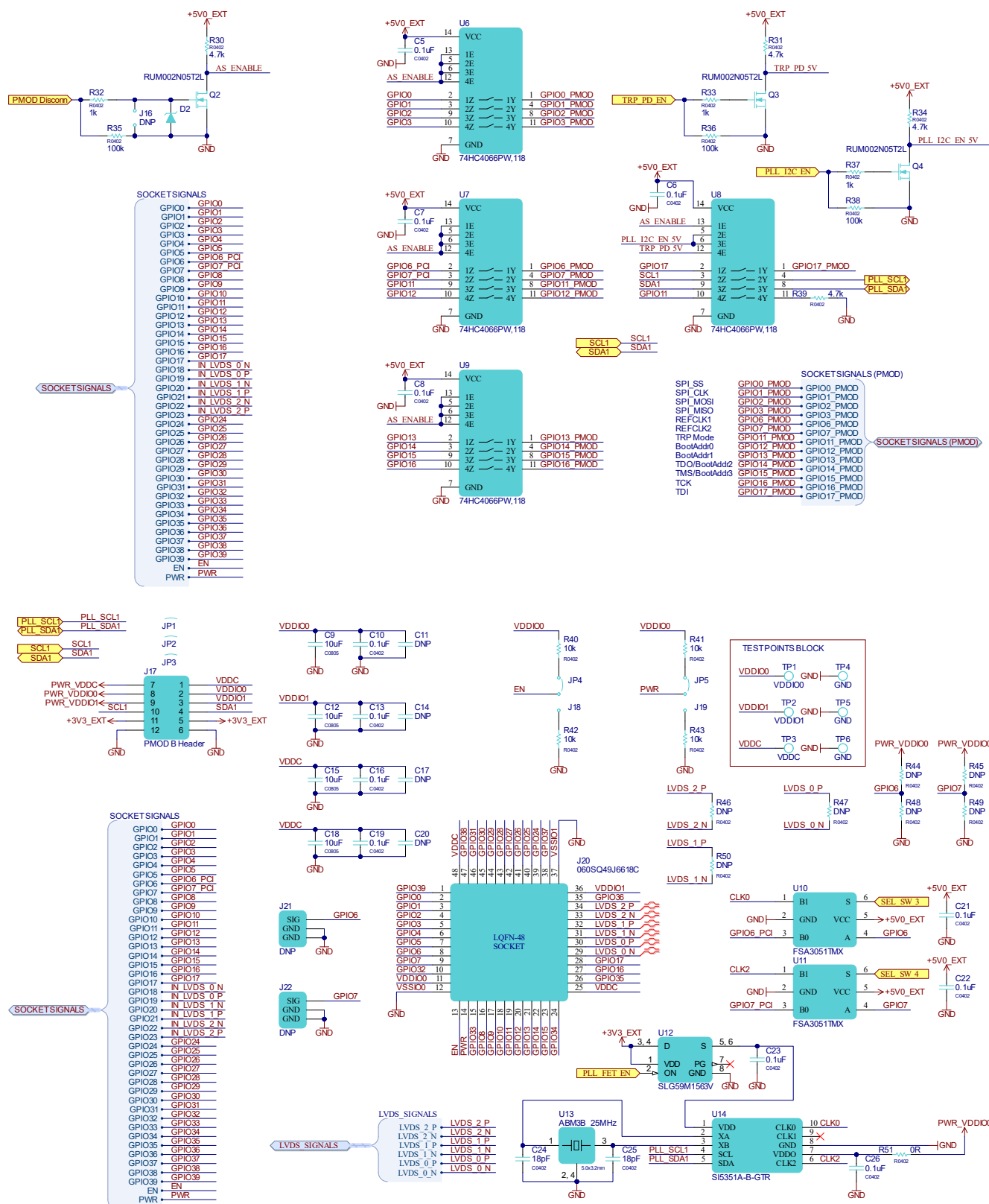
More detailed information about Go Configure software can be found in [Go Configure™ Software Hub User Guide](#).

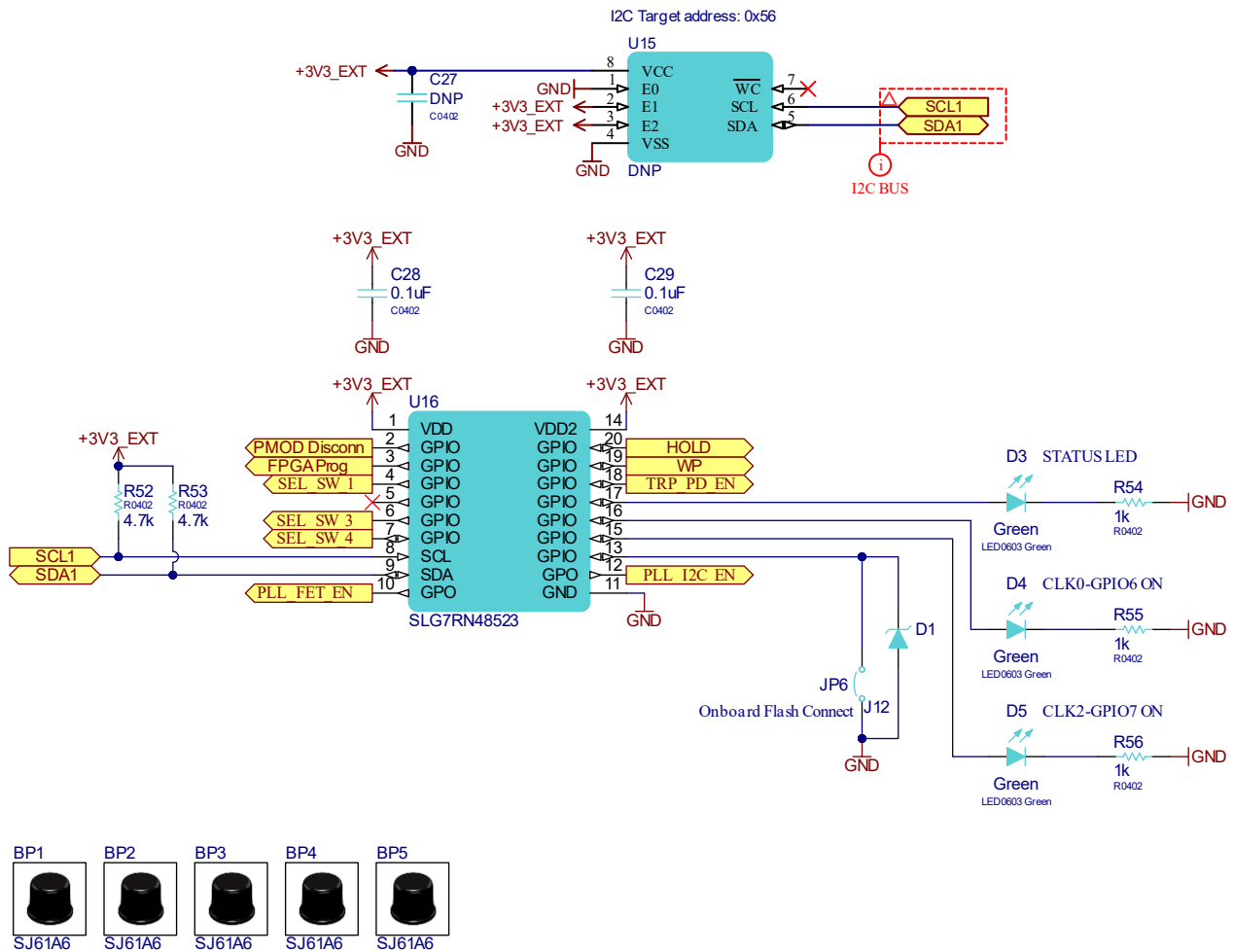
3. Board Design

3.1 Schematic Diagrams









4. Bill Of Materials

#	Designator	Manufacturer Part Number	Manufacturer	Quantity
1	BP1, BP2, BP3, BP4, BP5	SJ61A6	3M	5
2	C1-C8, C10, C13, C16, C19, C21-C23, C26, C28, C29	GCM155R71C104KA55D	Murata	18
3	C9, C12, C15, C18	GRM21BR61C106KE15L	Murata	4
4	C11, C14, C17, C20, C27	DNP	DNP	5
5	C24, C25	CL05C180JB5NNNC	Samsung	2
6	D1, D2	DESD5V0U1BB-7	Diodes	2
7	D3, D4, D5	150060GS75000	Wurth Electronics	3
8	J3, J4, J8, J17	67996-212HLF	Amphenol ICC / FCI	4
9	J5, J6, J7, J11	PPPC062LJBN-RC	Sullins	4
10	J9, J10	PPPC032LJBN-RC	Sullins	2
11	J12, J13	68000102HLF	Amphenol ICC / FCI	2
12	J14	67997210HLF	Amphenol ICC / FCI	1
13	J15	68000102HLF	Amphenol ICC / FCI	1
14	J16	DNP	DNP	1
15	J18, J19	HTSW-103-07-T-S	Samtec	2
16	J20	060SQ49J6618C	Renesas Electronics	1
17	J21, J22	DNP	DNP	2
18	JP1, JP2, JP3, JP4, JP5, JP6	NPC02SXON-RC	Sullins	6
19	Q1, Q2, Q3, Q4, Q5	RUM002N05T2L	Rohm	5
20	R1- R18	S41X043470JP	CTS	18
21	R19, R27, R30, R31, R34, R39, R52, R53	RC0402JR-074K7L	Yageo	8
22	R20, R23, R24, R28, R32, R33, R37, R54, R55, R56	RC0402JR-071KL	Yageo	10
23	R21, R29, R35, R36, R38	RC0402JR-07100KL	Yageo	5
24	R22, R51	RC0402JR-070RL	Yageo	2
25	R25, R26, R40, R41, R42, R43	RC0402JR-0710KL	Yageo	6
26	R44, R45, R46, R47, R48, R49, R50	DNP	DNP	7
27	U1, U2, U3	74LVC4066BQ,115	Nexperia	3
28	U4	AT25FF041A-SHN-T	Renesas	1
29	U5, U6, U7, U8, U9	74HC4066PW,118	Nexperia	5
30	U10, U11	FSA3051TMX	ON Semiconductor / Fairchild	2
31	U12	SLG59M1563V	Renesas Electronics America Inc	1
32	U13	ABM3B-25.000MHZ-D2Y-T	Abracon	1
33	U14	SI5351A-B-GTR	Skyworks Solutions	1
34	U15	DNP	DNP	1
35	U16	SLG7RN48523	Renesas Electronics America Inc	1

5. Revision History

Revision	Date	Description
1.00	Dec 9, 2025	Initial release.