User's Manual

# RA0L1 Group

## Fast Prototyping Board for RA0L1 Microcontroller Group
## FPB-RA0L1 v1
## User's Manual

Renesas RA Family
RA0 Series



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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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# Precautions

This Fast Prototyping Board is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

# Proprietary Notice

Renesas RA Family

# FPB-RA0L1 v1

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## Glossary

**Table 1. List of Abbreviations and Acronyms**

| | |
|---|---|
| BoM | Bill of Materials |
| FPB | Fast Prototyping Board |
| FSP | Flexible Software Package |
| GPIO | General Purpose Input Output |
| $I^2C$ (or IIC) | Inter-Integrated Circuit |
| IDE | Integrated Development Environment |
| I/O | Input/Output |
| IRQ | Interrupt Request |
| LDO | Low Dropout |
| LED | Light Emitting Diode |
| LFQFP | Lead Free Quad Flat Pack |
| MCU | Micro Controller Unit |
| MISO | SPI Master In Slave Out |
| MOSI | SPI Master Out Slave In |
| NC | Not Connected |
| PMOD™ | Peripheral Module |
| RWM | Pulse Width Modulation |
| RXD | Receive Data |
| SCI | Serial Clock Line |
| SCL | Serial Clock Line |
| SDA | Serial Data Line |
| SMD | Surface Mount Device |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| SWD | Serial Wire Debug |
| TXD | Transmit Data |
| UART | Universal Asynchronous Receiver-Transmitter |
| USB | Universal Serial Bus |

# 1. Board Overview

The FPB-RA0L1, a Fast Prototyping Board for the RA0L1 MCU Group, enables users to seamlessly evaluate the features of the RA0L1 MCU group and develop embedded systems applications using Flexible Software Package (FSP) and the e$^2$ studio IDE. Users can use on-board features along with their choice of popular ecosystems add-ons to bring their big ideas to life.

The key features of the FPB-RA0L1 board are categorized in three groups (consistent with the architecture of the board) as follows:

**MCU and MCU Native Pin Access**

- R7FA0L1074CFL MCU (referred to as RA MCU)
- 32 MHz, Arm® Cortex®-M23 core
- 64 KB Code Flash, 16 KB SRAM, 1 KB Data Flash
- 48-pin LFQFP package
- Native pin access through 24 x 2-pin male headers (not fitted)
- MCU's VCC current measurement point for precision current consumption measurement

  Multiple clock sources – Oscillators for high-speed, medium-speed, and low-speed on-chip clock signals are available in the RA MCU. Signals from crystal oscillators at 32.768 kHz and 20.000 MHz (not fitted) can also be used for the sub-clock and main clock, respectively.

**System Control and Ecosystem Access**

- USB Full Speed Device (USB 2.0 Type-C™ connector)
- Two 5 V input sources
  - USB (Debug, Full Speed)
  - External power supply (using 2-pin header) (not fitted)
- On-board debugger (SWD)
- User LEDs and buttons
  - User LEDs (green) x 2
  - Power LED (green) indicating availability of regulated power
  - Debug/Power LED (yellow) indicating power and the debug connection
  - User button x 1
  - Reset button x 1
- Two popular ecosystem expansions
  - Digilent Pmod™ (SPI, UART, and I$^2$C) connectors x 2
  - Arduino® (Uno R3) connectors

**Special Feature Access**

- Capacitive touch button x 2
- Touch button LED (green) x 2

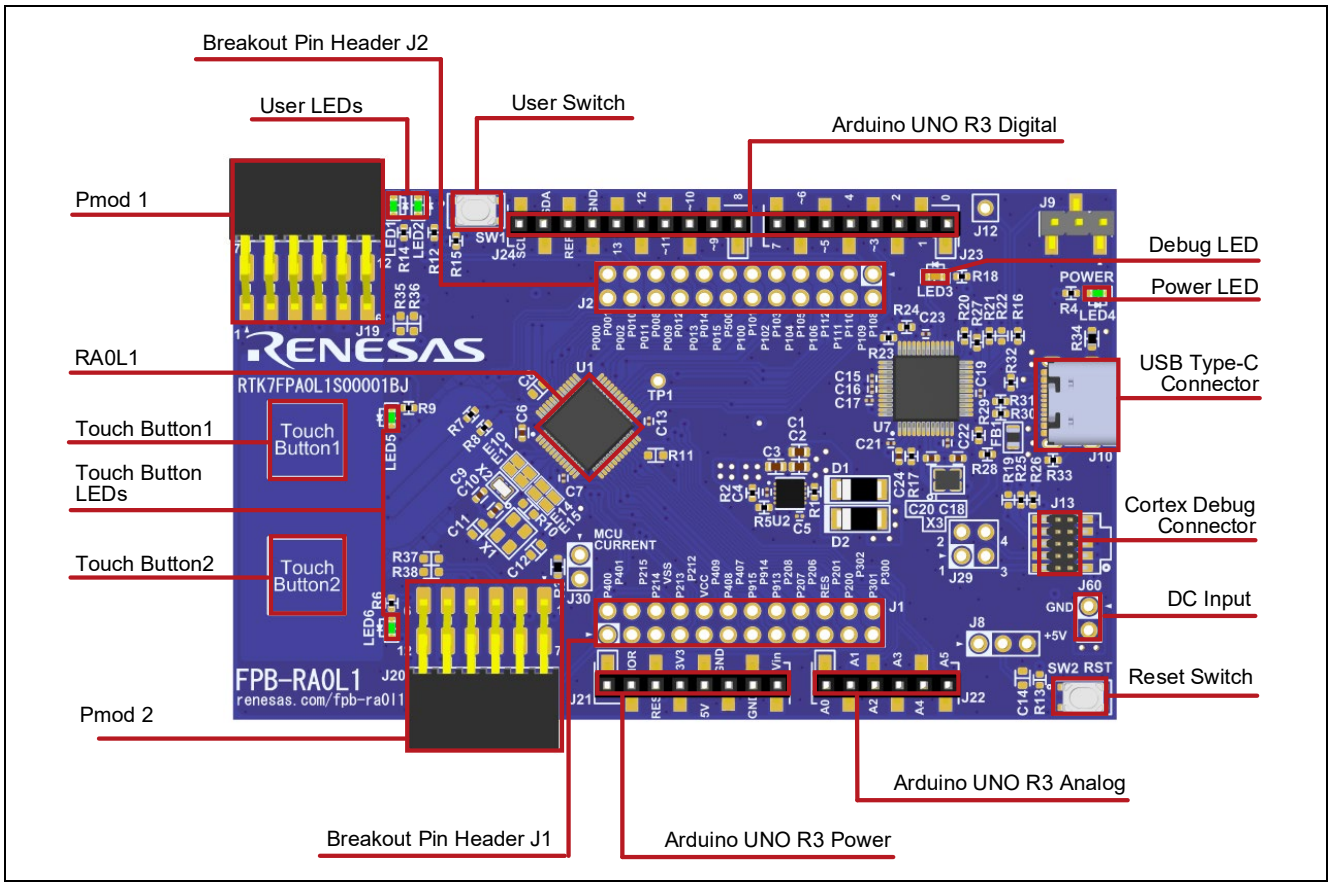



**Figure 1. FPB-RA0L1 Board (Top View)**

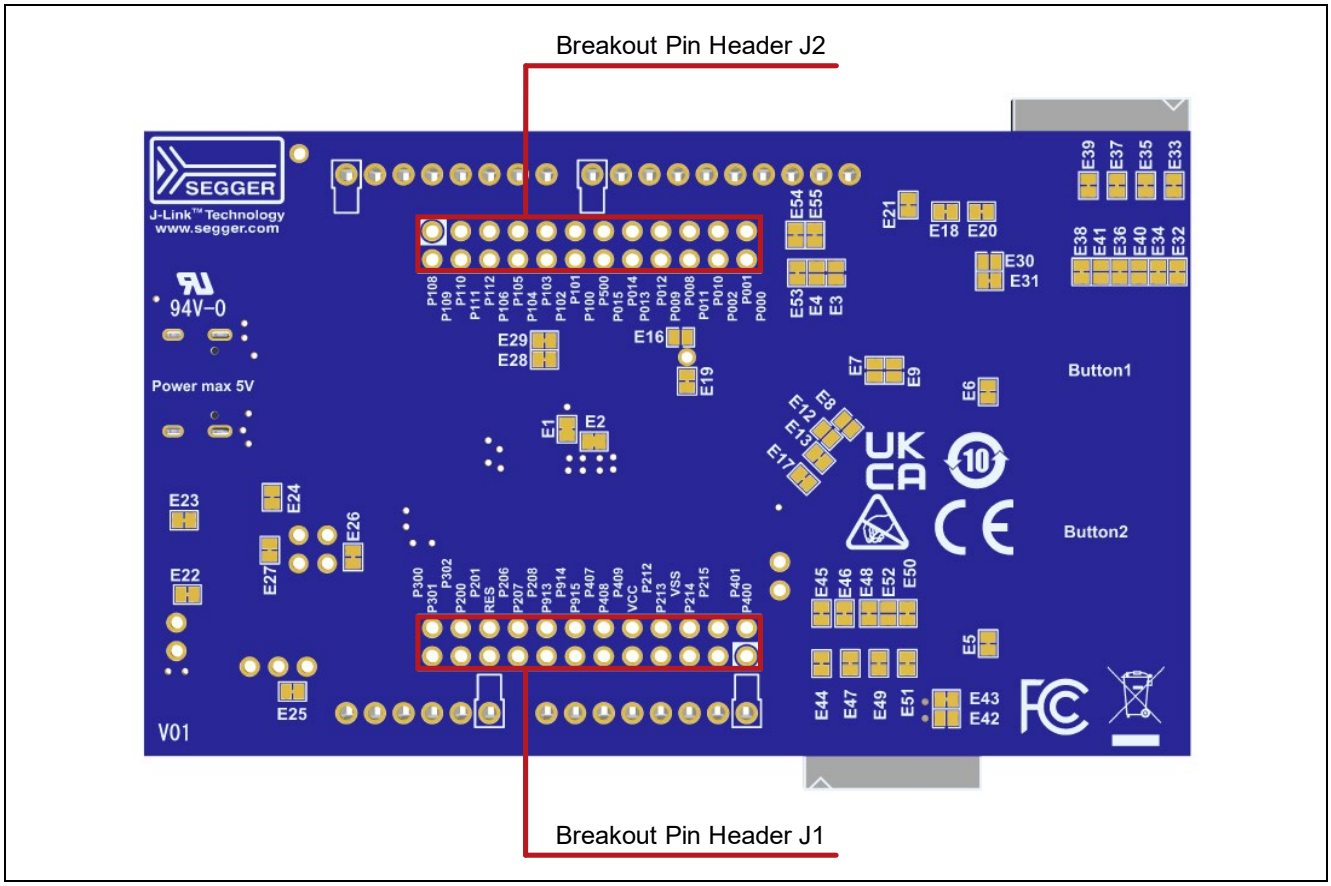



**Figure 2. FPB-RA0L1 Board (Bottom View)**

## 1.1 Assumptions and Advisory Notes

(1) It is assumed that the user has a basic understanding of microcontrollers and embedded systems hardware.

(2) It is recommended that the user refers to the *FPB-RA0L1 Quick Start Guide* to get acquainted with the board.

(3) Flexible Software Package (FSP) and Integrated Development Environment (IDE) such as e² studio are required to develop embedded applications on FPB-RA0L1 board.

(4) Instructions to download and install software, create example projects, build them and program the FPB-RA0L1 board can be found in the FPB-RA0L1 tutorial and Getting Started with Fast Prototyping Board for RA Family.

(5) The MCU fitted to the FPB-RA0L1 board may not contain the latest version of the firmware.

## 2. Box Contents

The following components are included in the box.

(1) FPB-RA0L1 v1 board
(2) USB 2.0 Type-C™ cable (Type-C male to Type-C male)
(3) Printed Quick Start Guide and China RoHS document

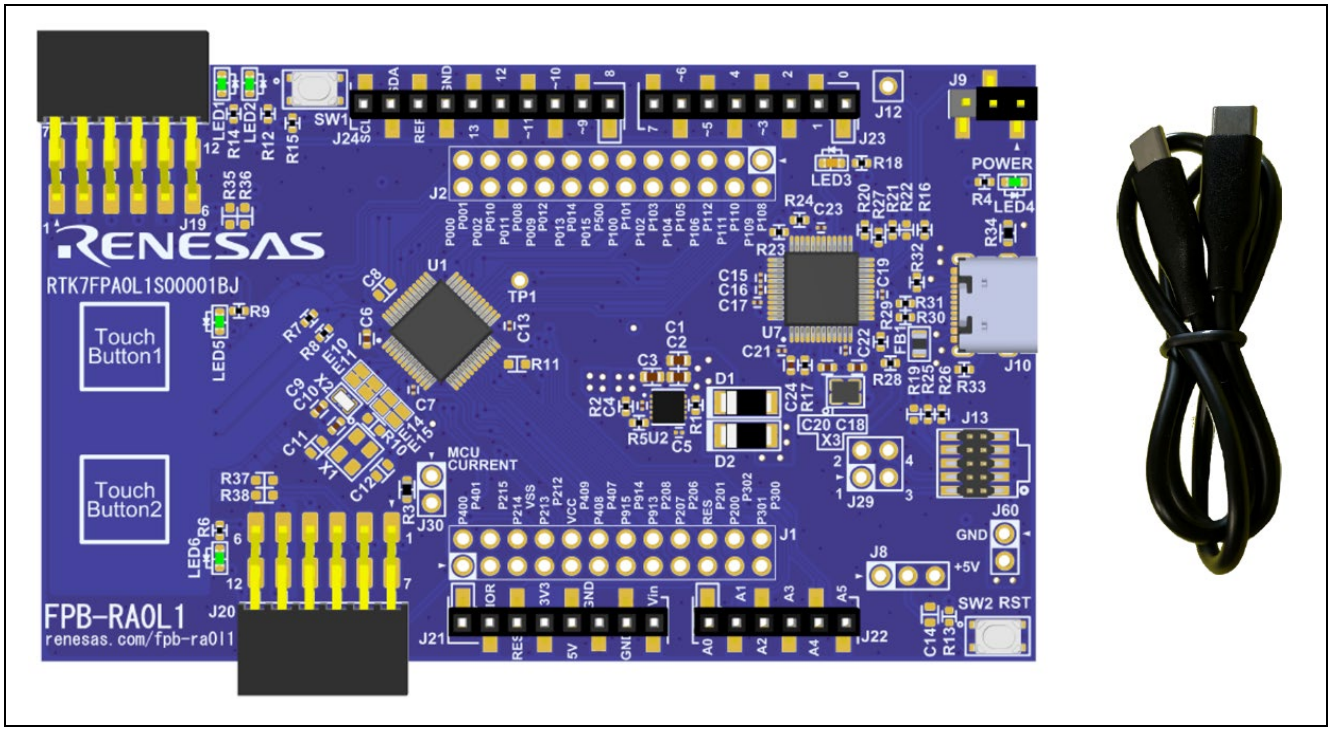



**Figure 3. Configuration of the FPB-RA0L1 v1 Evaluation Kit**

## 3. Ordering Information

- FPB-RA0L1 v1 orderable part number: RTK7FPA0L1S00001BJ

  Note: The underlined character in the orderable part number represents the kit version.

- FPB-RA0L1 board dimensions: 56.00 mm (width) x 93.00 mm (length)

# 4. Hardware Architecture and Default Configuration

## 4.1 Board Architecture

The FPB-RA0L1 board is designed with a similar architecture to other boards in the FPB series. Alongside the RA MCU there is an on-board programmer, pin headers for access to all the pins on the RA MCU, a power supply regulator, some LEDs, switches, capacitive touch buttons, and several ecosystem I/O connectors (Pmod and Arduino).

**Table 2. Kit Architecture**

| Board Functionality | Features | Function present on all similar boards | Functionality is: |
|---|---|---|---|
| MCU Native Pin Access | RA MCU, all MCU I/Os and power, and breakout pin headers for current measurement | Yes | RA MCU dependent |
| System Control and Ecosystem Access | Power, debugger, user LEDs and switches, reset switch, and ecosystem connectors | Yes | Same or similar across other FPB boards |
| Special Feature Access | Capacitive touch buttons | No | RA MCU dependent |

## 4.2 Block Diagram

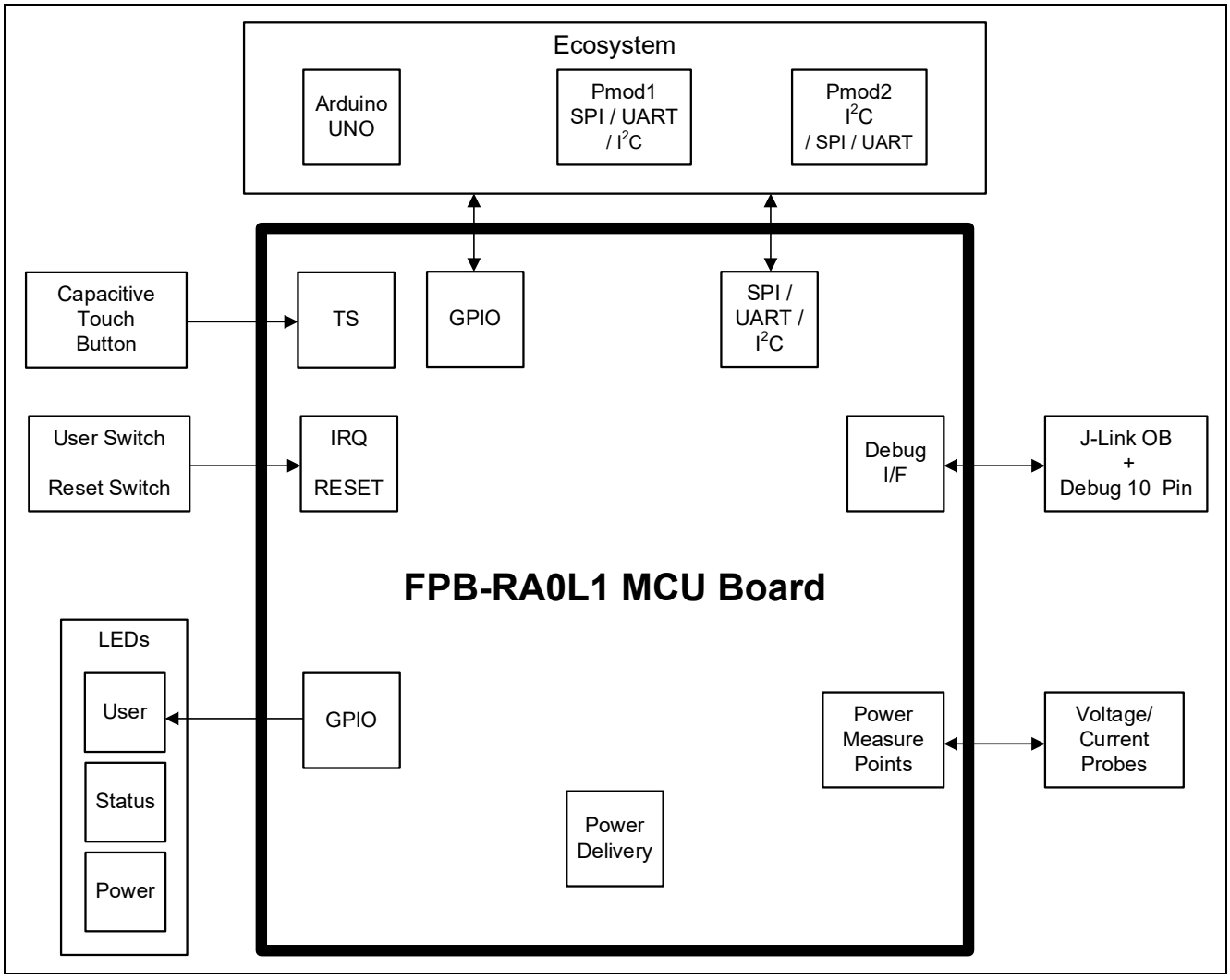



**Figure 4. FPB-RA0L1 Board Block Diagram**

## 4.3 Jumper Settings

Two types of jumpers are provided on the FPB-RA0L1 board.

(1) Copper jumpers (**Jumper Trace Cut(closed)** and **Jumper Solder Bridge(open)**)
(2) Traditional pin header jumpers

The following sections describe each type and their default configuration.

### 4.3.1 Copper Jumpers

Copper jumpers are of two types, designated **Jumper Trace Cut (closed)** and **Jumper Solder Bridge (open)**.

A **Jumper Trace Cut (closed)** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **Jumper Solder Bridge (open)** is provided with two isolated pads that may be joined together by one of three methods:

Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
A small wire may be placed across the two pads and soldered in place.
A SMD resistor, inch size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for the Jumper Trace Cut**(closed)**.) The connection is considered **open** if there is no electrical connection between the pads (default for the Jumper Solder Bridge**(open)**).

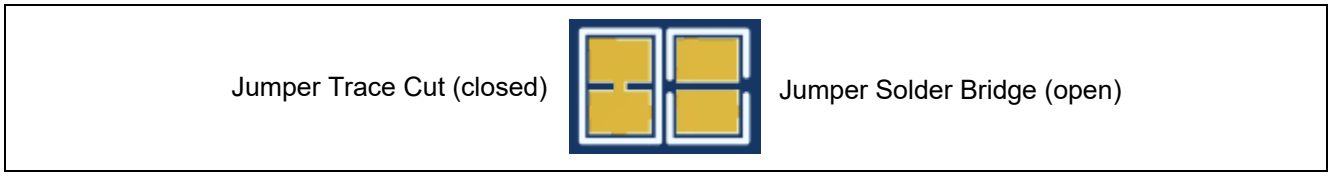



**Figure 5. Copper Jumpers**

### 4.3.2 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The traditional pin header jumpers on the FPB-RA0L1 board are 0.1” (2.54 mm) pitch headers and require compatible 2.54 mm shunt jumpers.

### 4.3.3 Default Jumper Configuration

The following table describes the default settings for each jumper on the FPB-RA0L1 board. This includes copper jumpers (Ex designation) and traditional pin jumpers (Jx).

The circuit group for each jumper is the designation found in the board schematic (FPB-RA0L1 - Design Package). Functional details for many of the listed jumpers may be found in sections associated with each functional area of the kits.

**Table 3. Default Jumper Settings**

| Location | Circuit Group | Default Open/Closed | Function |
|---|---|---|---|
| E1 | Power | Closed | Connects 3.3 V to +3V3JLOB. |
| E2 | Power | Closed | Connects 3.3 V to VCC. |
| E3 | Power | Open | Connects P010/VREFH0 to VCC. |
| E4 | Power | Open | Connects P011/VREFL0 to GND. |
| E53 | Power | Closed | Connects P011/VREFL0 to J2-20. |
| E54 | Power | Closed | Connects P010/VREFH0 to J2-21. |
| E20 | User LED | Closed | Connects P002 to LED1. |
| E18 | User LED | Closed | Connects P104 to LED2. |
| E6 | Touch Button LED | Closed | Connects P401 to LED5. |
| E5 | Touch Button LED | Closed | Connects P400 to LED6. |
| E7 | Touch Button | Open | Connects P000/TS23 to J2-24. |
| E9 | Touch Button | Open | Connects P001/TS22 to J2-23. |
| E16 | Touch Button | Open | Connects P112/TSCAP to J2-5. |
| E19 | Touch Button | Closed | Connects P112/TSCAP to 10 nF. |
| E8 | Clock | Open | Connects P215/XCIN to J1-4. |
| E10 | Clock | Closed | Connects P215/XCIN to the sub-clock. |
| E11 | Clock | Closed | Connects P214/XCOUT to the sub-clock. |
| E12 | Clock | Open | Connects P214/XCOUT to J1-5. |
| E13 | Clock | Closed | Connects P213/X2/EXCLK to J1-7. |
| E14 | Clock | Open | Connects P213/X2/EXCLK to the main clock. |
| E15 | Clock | Open | Connects P212/X1 to the main clock. |
| E17 | Clock | Closed | Connects P212/X1 to E52 and J1-8. |
| E21 | User Switch | Closed | Connects P200 to SW1. |
| E22 | Debugger | Closed | Connects VCC to J13-1. |
| E23 | Debugger | Closed | Connects GND to J13-9. |
| E24 | Debugger | Closed | Connects U7-P100 to J13-6. |
| E25 | Debugger | Closed | Connects RES to U7-P112 and J13-10. |
| E26 | Debugger | Closed | Connects P108/SWDIO to U7-P101 and J13-2. |
| E27 | Debugger | Closed | Connects P300/SWCLK to U7-P102 and J13-4. |
| E28 | Debugger | Closed | Connects P106/TXDA1_B to U7-P301. |
| E29 | Debugger | Closed | Connects P105/RXDA1_B to U7-P302. |
| E31 | Pmod1 | Closed | Connects VCC to J19-6 and J19-12. |
| E32 | Pmod1 | Closed | Connects P103/SSI00_A to J19-1. |

| Location | Circuit Group | Default Open/Closed | Function |
|---|---|---|---|
| E34 | Pmod1 | Closed | Connects P101/SO00_A/TXDA0_D to J19-2. |
| E36 | Pmod1 | Closed | Connects P100/SI00_A/RXDA0_D to J19-3. |
| E38 | Pmod1 | Closed | Connects P102/SCK00_A to J19-4. |
| E33 | Pmod1 | Closed | Connects P201/IRQ5_B to J19-7. |
| E35 | Pmod1 | Closed | Connects P013 to J19-8. |
| E37 | Pmod1 | Closed | Connects P012 to J19-9. |
| E39 | Pmod1 | Closed | Connects P009 to J19-10. |
| E40 | Pmod1 | Open | Connects P110/SCLA0_C to J19-3. |
| E41 | Pmod1 | Open | Connects P109/SDAA0_C to J19-4. |
| E43 | Pmod2 | Closed | Connects VCC to J20-6 and J20-12. |
| E44 | Pmod2 | Closed | Connects P409/IRQ6_B to J20-1. |
| E46 | Pmod2 | Closed | Connects P213 to J20-2. |
| E48 | Pmod2 | Closed | Connects P408/SCLA1_F to J20-3. |
| E50 | Pmod2 | Closed | Connects P407/SDAA1_F to J20-4. |
| E45 | Pmod2 | Closed | Connects P206 to J20-7. |
| E47 | Pmod2 | Closed | Connects P915 to J20-8. |
| E49 | Pmod2 | Closed | Connects P302 to J20-9. |
| E51 | Pmod2 | Closed | Connects P301 to J20-10. |
| E52 | Pmod2 | Open | Connects P212/SI11_A to J20-3. |
| E55 | Arduino | Closed | Connects P010/VREFH0 to the Arduino® connector. |
| J8 | Debugger | Not fitted | 1-2 closed: Connects RES to U7-P112 and J13-10.<br>2-3 closed: Connects RES to GND. |
| J9 | Debugger | 1-2 closed | 1-2 closed: Pulls up U7-RES (on-board debug).<br>2-3 closed: Connects U7-RES to GND (MCU alone or debug in). |
| J29 | Debugger | Not fitted | 1-2 closed: Connects P108/SWDIO to U7-P101 and J13-2.<br>3-4 closed: Connects P300/SWCLK to U7-P102 and J13-4. |

Note: J1 and J2: Breakout Pin Header
J13: Debug connector
U7: RA4M2 (J-Link OB)
J19: Pmod 1
J20: Pmod 2

# 5. System Control and Ecosystem Access

The FPB-RA0L1 board provides a power supply regulator, an on-board debugger, simple I/O (switches and LEDs), and popular I/O ecosystem connectors. These are all described in detail below.

## 5.1 Power

The FPB-RA0L1 board is designed for 5 V operation. An on-board Low Dropout (LDO) regulator is used to convert the 5 V supply to a 3.3 V supply. The 3.3 V supply is used to power the RA MCU and other peripheral features.

### 5.1.1 Power Supply Options

This section describes the different ways in which FPB-RA0L1 board can be powered.

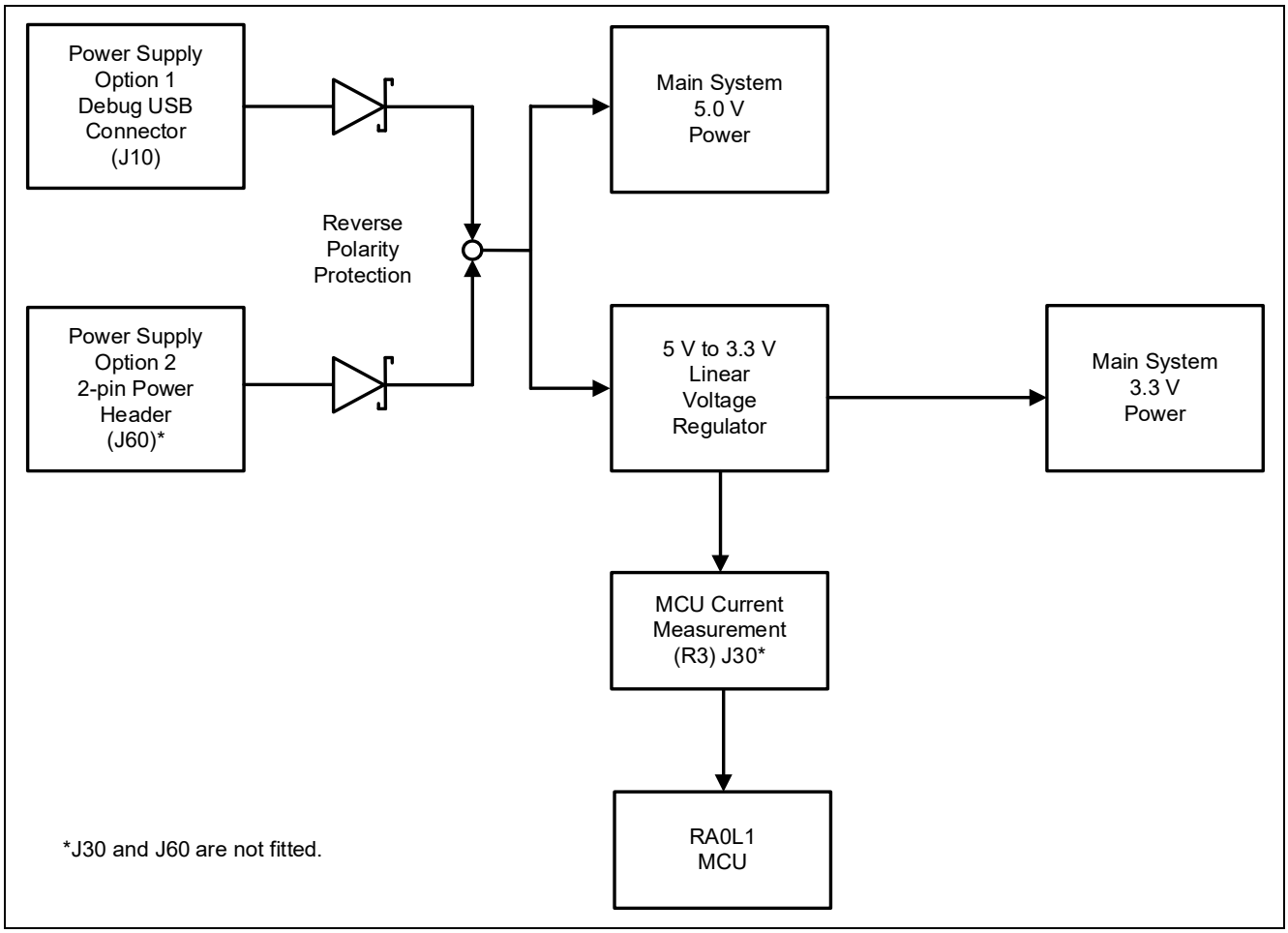



**Figure 6. Power Supply Options**

#### 5.1.1.1 Option 1: Debug USB (Default Setting)

5 V may be supplied from an external USB host to the USB debug connector (J10). Power from this source is connected to the main system 5 V power. Reverse current protection is provided between this connector and the main system 5 V power.

#### 5.1.1.2 Option 2: Header Connector J60

5 V may be supplied from an external power supply to the header connector (J60) on the board. J60 (not fitted) is a 2-pin through-hole that can accommodate a 0.1” (2.54 mm) pin header or connector. Power from this source is connected to the main system 5 V power. Reverse current protection is provided between the 5 V header connector and the main system 5 V power supply.

### 5.1.2 Power Supply Considerations

The on-board LDO regulator which supplies 3.3 V has a built-in current limit of 2.0 A. Make sure the total current required by the RA MCU, any active on-board features, and any connected peripheral devices does not exceed this limit.

Note: The total current available from a typical USB host is 500 mA maximum. Depending on the configuration of the kit, multiple power sources may be required.

### 5.1.3 Power-up Behavior

When power is supplied, green LED4 marked POWER will illuminate. Yellow LED3 (DEBUG LED) will also illuminate.

## 5.2 Debug

The FPB-RA0L1 board can be programmed and debugged by using the built-in SEGGER J-Link® on-board debugger and can support the two debug modes listed below.

**Table 4. Debug Modes**

| Debug Mode | Debug MCU* | Target MCU (MCU to be Debugged) | Debug Interface | Connector Used |
|---|---|---|---|---|
| On-Board Debug | RA4M2 (on-board) | RA0L1 (on-board) | SWD | USB 2.0 Type-C™ connector (J10) |
| Debug In | External debug tools | RA0L1 (on-board) | SWD | 10-pin connector (J13) |

* MCU to be connected to an IDE running on a PC

The following table summarizes the pin-header jumper configurations for each of the debug modes.

**Table 5. Pin-header Jumper Configurations for Each of the Debug Modes**

| Debug Mode | J9 |
|---|---|
| On-Board Debug | 1-2 |
| Debug In | 2-3 |

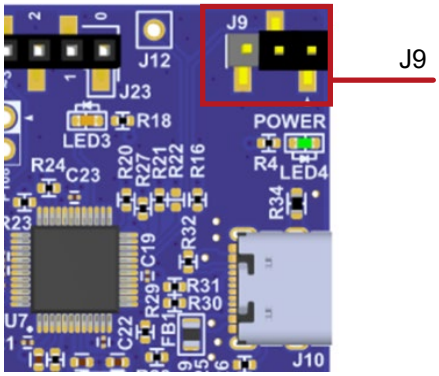



**Figure 7. Jumper for Debug Modes**

### 5.2.1 On-Board Debug

The on-board debug functionality is provided using RA4M2 (J-Link OB) and SEGGER J-Link® firmware. The USB 2.0 Type C™ connector (J10) for debugging connects the RA4M2 (J-Link OB) to an external USB full speed host, allowing re-programming and debugging of the target RA MCU firmware. This connection is the default debug mode for the FPB-RA0L1 board.
The RA4M2 (J-Link OB) is connected to the target MCU through the SWD interface.

**Table 6. Debug USB Connector**

| Debug USB Connector J10 | | FPB-RA0L1 |
|---|---|---|
| **Pin** | **Description** | **Signal/Bus** |
| A4, B4, A9, B9 | +5VDC | +5V_USB_DBG |
| A7, B7 | Data- | USB_JL_OB_DM (U7 pin 14) |
| A6, B6 | Data+ | USB_JL_OB_DP (U7 pin 15) |
| CC1, CC2 | USB ID, jack internal switch, cable inserted | Pull down |
| SH1, SH2, SH3, SH4 | Shell | VSS |
| A1, B1, A12, B12 | Ground | VSS |

Signal/Bus names are shown on the board schematic (FPB-RA0L1 - design package) and are compliant with that.

Yellow indicator LED3 shows the status of the debug interface. When the FPB-RA0L1 board is powered on and LED3 is blinking, it indicates that the RA4M2 (J-Link OB) is not connected to the host PC. When LED3 is lit, it indicates that the RA4M2 (J-Link OB) is connected to the host PC.
When LED3 is blinking while connected to the host PC, it indicates that data is being transferred between the RA4M2 (J-Link OB) and the host PC.

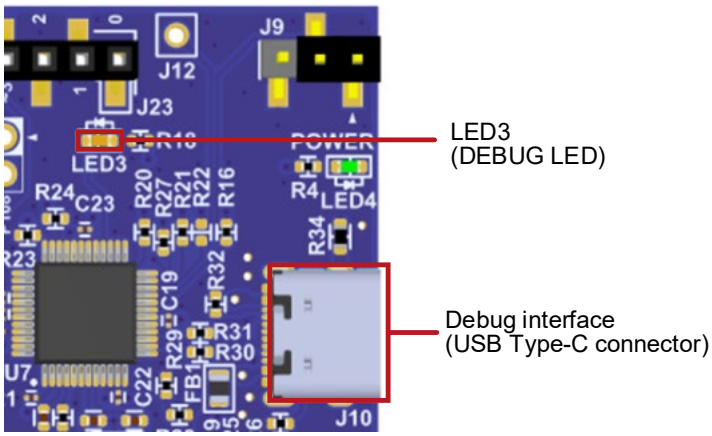



**Figure 8. FPB-RA0L1 Debug Interface (FPB-RA0L1 Top View)**

### 5.2.2 Debug In

The 10-pin Cortex® debug connector J13 supports the SWD(Serial Wire Debug) interface, allowing debugging of the target RA0L1 using an external debug tool.

To configure the FPB-RA0L1 board to use the Debug In mode, configure the pin-header jumpers using Table 5.

**Table 7. 10-pin Debug Connector**

| Debug Connector J13 | | FPB-RA0L1 |
|---|---|---|
| **Pin** | **SWD Pin Name** | **Signal/Bus** |
| J13-1 | Vtref | 3.3 V |
| J13-2 | SWDIO | P108/SWDIO |
| J13-3 | GND | VSS |
| J13-4 | SWCLK | P300/SWCLK |
| J13-5 | GND | VSS |
| J13-6 | - | NC |
| J13-7 | Key | NC |
| J13-8 | - | NC |
| J13-9 | GND Detect | VSS |
| J13-10 | nRESET (sSRST) | RES |

### 5.2.3 Debugger Settings in e² studio

Figure 9 shows the settings for e² studio when creating a new project for the FPB-RA0L1 board.

[Debug hardware]: Select [J-Link (ARM)].
[Target Device]: Select [R7FA0L107].

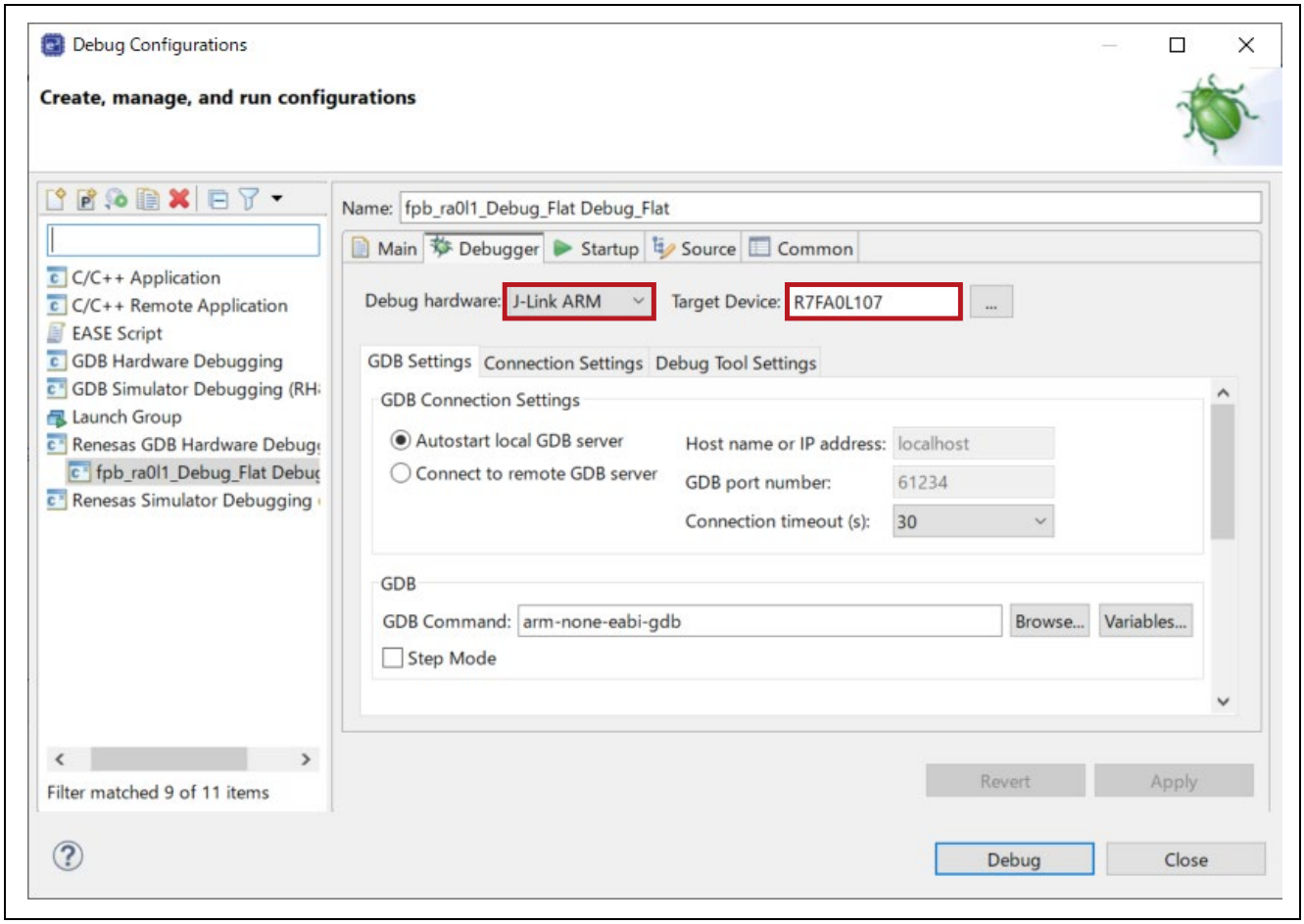



**Figure 9. e² studio Debugger Settings**

### 5.2.4 VCOM port

The FPB-RA0L1 board can perform USB-UART conversion by using the RA4M2 (J-Link OB). It is recognized by the host as the VCOM port (J-Link CDC UART Port) and connected to the RA0L1 UART by using the FPB-RA0L1 board (refer to Table 8).

**Table 8. UART Assignments**

| RA0L1 Pin | RA0L1 Signal |
|---|---|
| U1-31 | P105/RXDA1_B |
| U1-30 | P106/TXDA1_B |

The RxD (RA4M2: P301) pin on the J-Link OB side is pulled up for the input direction. When this pin is not to be used for the J-Link UART and pulling up of this pin would affect the connected P106/TXDA1_B, reset the RA4M2 (by short-circuiting J9).

## 5.3 Ecosystem

The Ecosystem connectors allow users to simultaneously connect several third-party add-on modules compatible with two popular ecosystems using the following connectors:

(1) Digilent Pmod™ (SPI, UART, and I²C) connector x 2
(2) Arduino® (Uno R3) connector

### 5.3.1 Digilent Pmod™ Connectors

Two 12-pin connectors are provided to support Pmod modules where the RA MCU acts as the master, and the connected module acts as a slave device.

These interfaces may be configured in firmware to support several Pmod types such as Type 2A (expanded SPI), Type 3A (expanded UART), and Type 6A (I²C).

The default 12-pin Pmod interface supports 3.3-V devices. Please ensure that any Pmod device installed is compatible with a 3.3-V supply.

Note that both Pmods use the SAU peripheral in “Simplified SPI” mode and so do not offer the full functionality of the SCI peripheral. Please see the hardware manual for full details of the SAU “Simplified SPI” mode.

#### 5.3.1.1 Pmod 1

A 12-pin right angle connector is fitted at Pmod 1. The connections support Pmod Type 2A (expanded SPI), Type 3A (expanded UART), and Type 6A (I²C). Type 2A and Type 3A are used for the connections by default. Type 6A can be used by changing copper jumper settings (E*x* designation). This interface may additionally be re-configured in firmware as several other Pmod types.

UARTA0 (TXDA0_D and RXDA0_D) of Pmod 1 is used in common with the Arduino® connector. If the signals are simultaneously to be used with the Arduino® connector, use TXD0_A and RXD0_A of the SAU for Pmod 1.

IICA0 (SCLA0_C and SDAA0_C) of Pmod 1 is also used in common with the Arduino® connector.

**Table 9. Pmod 1 Connector**

| **Pmod 1 Connector** | | | **FPB-RA0L1** | **Pmod 1 Configuration** | |
|---|---|---|---|---|---|
| **Pin** | **Option Type 2A/3A (Default)** | **Option Type 6A** | **Signal/Bus** | **Short** | **Open** |
| J19-1 | CS/CTS | INT | P103/SSI00_A/IRQ5_A | E32 | - |
| J19-2 | MOSI/TXD | RESET | P101/SO00_A/TXDA0_D/TXD0_A | E34 | - |
| J19-3 | MISO/RXD | - | P100/SI00_A/RXDA0_D/RXD0_A | E36 | E40 |
| | - | SCL | P110/SCLA0_C | E40 | E36 |
| J19-4 | SCK/RTS | - | P102/SCK00_A | E38 | E41 |
| | - | SDA | P109/SDAA0_C | E41 | E38 |
| J19-5 | GND | | VSS | - | - |
| J19-6 | VCC | | 3.3 V | E31 | - |
| J19-7 | INT/GPIO | GPIO | P201/IRQ5_B | E33 | - |
| J19-8 | RESET/GPIO | GPIO | P013 | E35 | - |
| J19-9 | CS2/GPIO | GPIO | P012 | E37 | - |
| J19-10 | CS3/GPIO | GPIO | P009 | E39 | - |
| J19-11 | GND | | VSS | - | - |
| J19-12 | VCC | | 3.3 V | E31 | - |

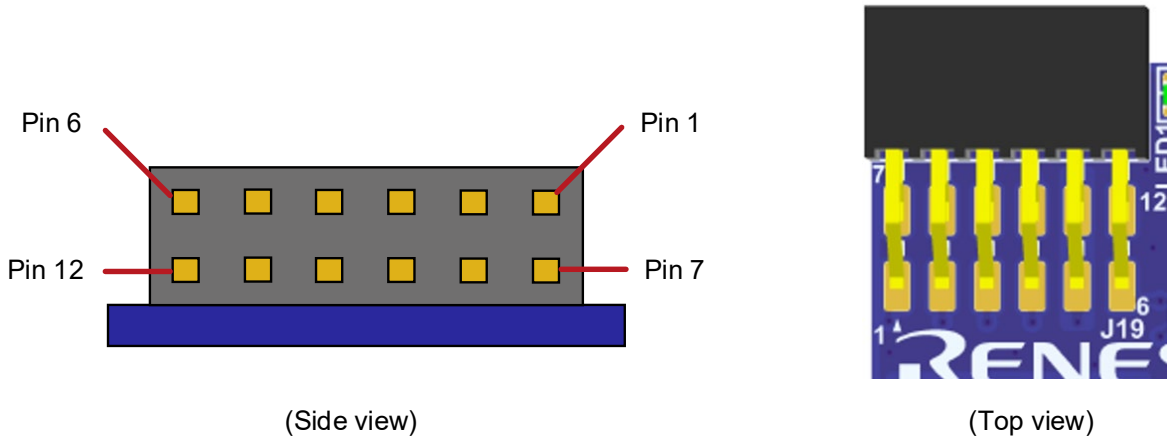



**Figure 10. Pmod 1 Connector**

The Pmod 1 interface supports 3.3-V devices by default. Ensure that any Pmod device installed is compatible with a 3.3-V supply.

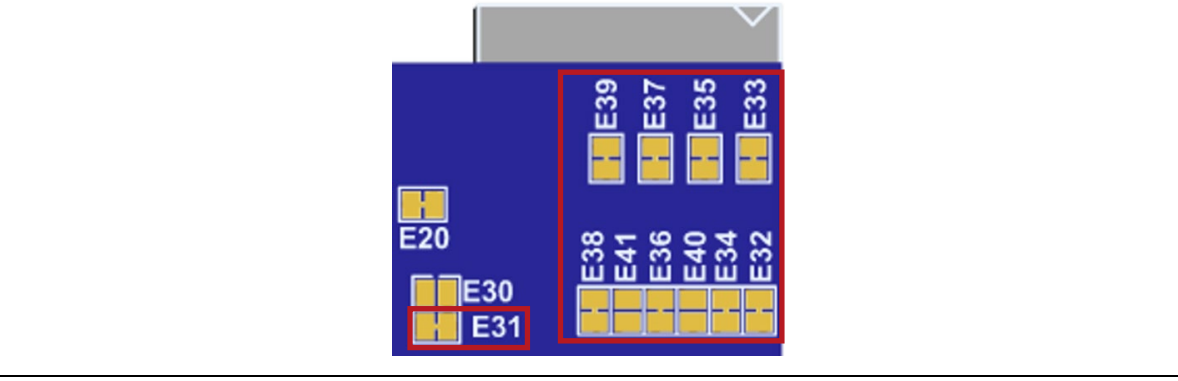



**Figure 11. Pmod 1 Copper Jumpers (FPB-RA0L1 Bottom View)**

### 5.3.1.2 Pmod 2

A 12-pin right angle connector is fitted at Pmod 2. The connections support Pmod Type 2A (expanded SPI), Type 3A (expanded UART), and Type 6A ($I^2C$). Type 6A is used for the connections by default. Type 2A and Type 3A can be used by changing copper jumper settings (E*x* designation). This interface may additionally be re-configured in firmware as several other Pmod types.

SPI11 (SO11_A, SI11_A, and SCK11_A) of Pmod 2 is used in common with the Arduino® connector.

**Table 10. Pmod 2 Connector**

| Pmod 2 Connector | | | FPB-RA0L1 | Pmod 2 Configuration | |
|---|---|---|---|---|---|
| Pin | Option Type 2A/3A | Option Type 6A (Default) | Signal/Bus | Short | Open |
| J20-1 | CS/CTS | INT | P409/IRQ6_B | E44 | - |
| J20-2 | MOSI/TXD | RESET | P213/SO11_A/TXDA0_B | E46 | - |
| J20-3 | - | SCL | P408/SCLA1_F | E48 | E52 |
| | MISO/RXD | - | P212/SI11_A/RXDA0_B | E52 | E48 |
| J20-4 | SCK/RTS | SDA | P407/SDAA1_F/SCK11_A | E50 | - |
| J20-5 | GND | | VSS | - | - |
| J20-6 | VCC | | 3.3 V | E43 | - |
| J20-7 | INT/GPIO | GPIO | P206/IRQ0_C | E45 | - |
| J20-8 | RESET/GPIO | GPIO | P915 | E47 | - |
| J20-9 | CS2/GPIO | GPIO | P302 | E49 | - |
| J20-10 | CS3/GPIO | GPIO | P301 | E51 | - |
| J20-11 | GND | | VSS | - | - |
| J20-12 | VCC | | 3.3 V | E43 | - |

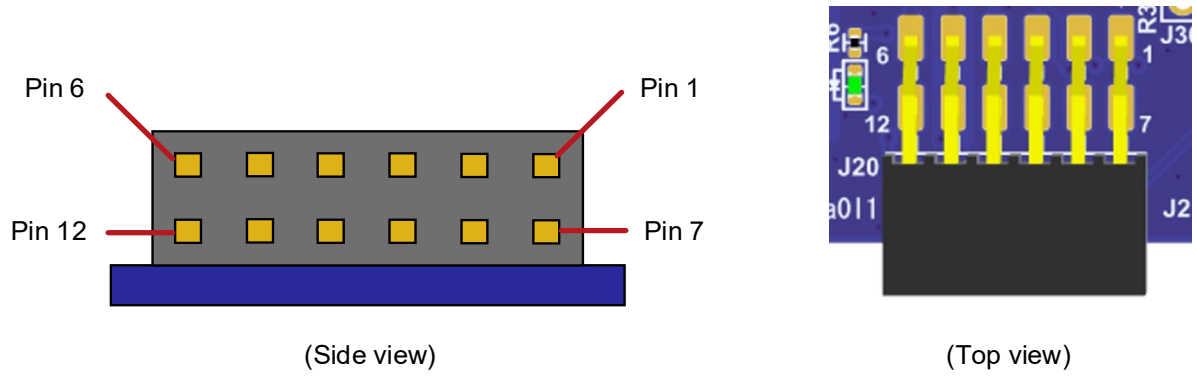



**Figure 12. Pmod 2 Connector**

The Pmod 2 interface supports 3.3-V devices by default. Ensure that any Pmod device installed is compatible with a 3.3-V supply.

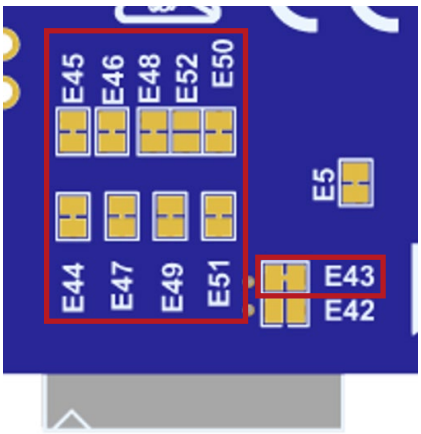



**Figure 13. Pmod 2 Copper Jumpers (FPB-RA0L1 Bottom View)**

### 5.3.2 Arduino® Connector

An Arduino® Uno R3 compatible connector interface is provided.

However, we do not guarantee connection to all types of Arduino® shield. Confirm the specifications of this product against any Arduino® shield you intend to use.

IICA0 (SCLA0_C and SDAA0_C) of the Arduino® connector is used in common with Pmod 1.

SPI11 (SO11_A, SI11_A, and SCK11_A) of the Arduino® connector is used in common with Pmod 2.

**Table 11. Arduino® Connector**

| **Arduino® Connector** | | **FPB-RA0L1** |
|---|---|---|
| **Pin** | **Description** | **Signal/Bus** |
| J21-1 | NC | NC |
| J21-2 | IOREF | 3.3 V |
| J21-3 | RESET | RES |
| J21-4 | 3V3 | 3.3 V |
| J21-5 | 5V | 5.0 V |
| J21-6 | GND | VSS |
| J21-7 | GND | VSS |
| J21-8 | VIN | NC |
| J22-1 | A0 | P015/AN007 |
| J22-2 | A1 | P014/AN006 |
| J22-3 | A2 | P013/AN005 |
| J22-4 | A3 | P012/AN004 |
| J22-5 | A4 | P009/AN003 |
| J22-6 | A5 | P008/AN002 |
| J23-1 | RX/D0 | P207/RXDA0_A |
| J23-2 | TX/D1 | P208/TXDA0_A |
| J23-3 | 2 | P111/IRQ1_C |
| J23-4 | ~3 | P201/TO05_B |
| J23-5 | 4 | P100 |
| J23-6 | ~5 | P101/TO07_A |
| J23-7 | ~6 | P500/TO03_D |
| J23-8 | 7 | P103 |
| J24-1 | 8 | P109 |
| J24-2 | ~9 | P301/TO06_B |
| J24-3 | ~10 | P110/TO01_A |
| J24-4 | ~11 | P213/SO11_A/TO02_B |
| J24-5 | 12 | P212/SI11_A |
| J24-6 | 13 | P407/SCK11_A |
| J24-7 | GND | VSS |
| J24-8 | AREF | P010/VREFH0 |
| J24-9 | SDA | P913/SDAA0_A |
| J24-10 | SCL | P914/SCLA0_A |

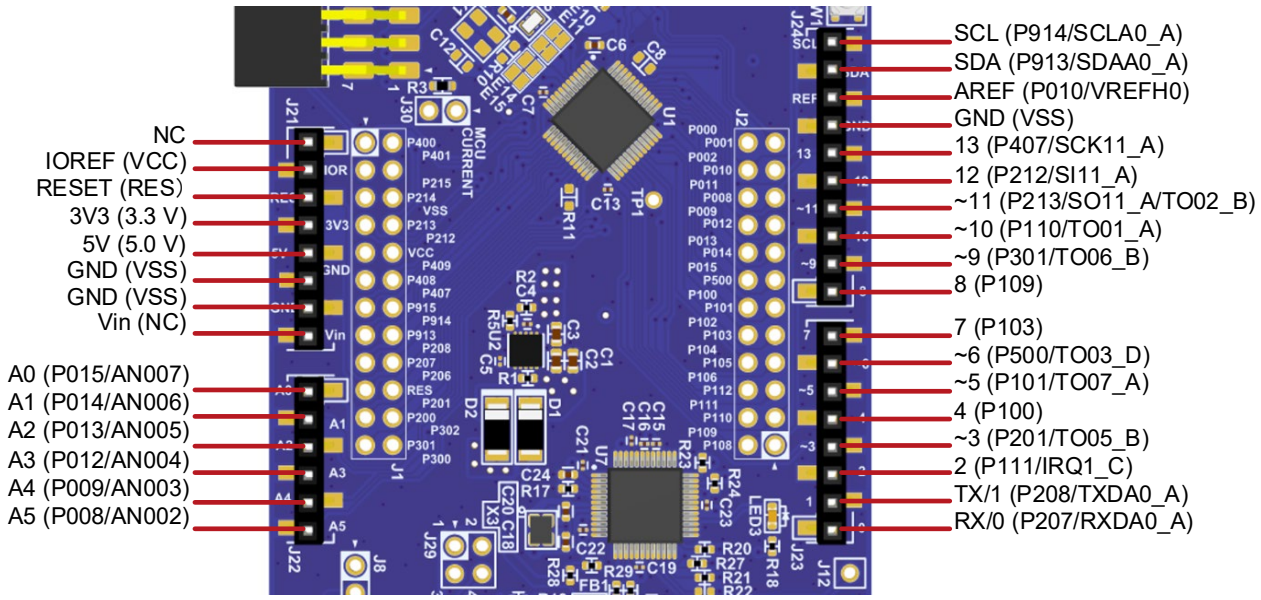



**Figure 14. Arduino® Connectors (FPB-RA0L1 Top View)**

## 5.4 Miscellaneous

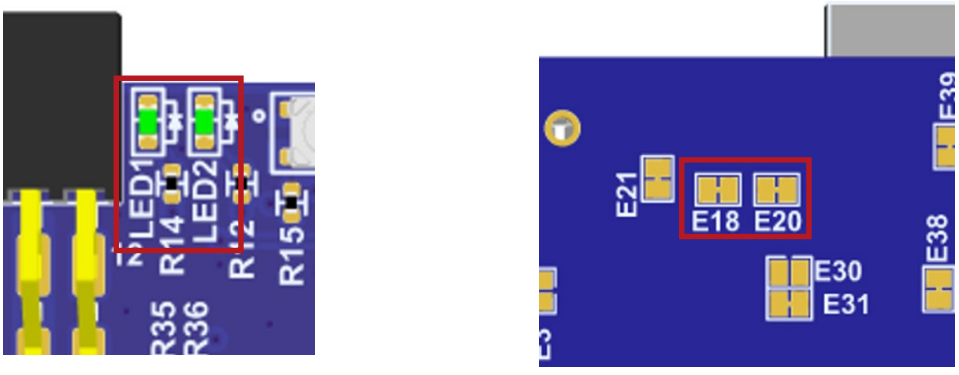
### 5.4.1 User, Debug, and Power LEDs

Two user LEDs, one debug LED, and one power LED are provided on the FPB-RA0L1 board. Behavior of the LEDs on the FPB-RA0L1 board is described in the following table.

**Table 12. FPB-RA0L1 Board LED Functions**

| Designator | Color | Function | RA MCU Control Port |
|---|---|---|---|
| LED1 | Green | User LED | P002 (illuminated by the high level) |
| LED2 | Green | User LED | P104 (illuminated by the high level) |
| LED3 | Yellow | Debug LED | Port for the RA4M2 (J-Link OB) |
| LED4 | Green | Power on indicator | VCC |

The user and touch-button LEDs can be isolated from the RA MCU so that the associated ports can be used for other purposes. To disconnect LED1 from P002, Jumper Trace Cut (closed) E20 must be open. To disconnect LED2 from P104, Jumper Trace Cut (closed) E18 must be open.




(Top view) (Bottom view)

**Figure 15. User LEDs and Jumpers for User LEDs**

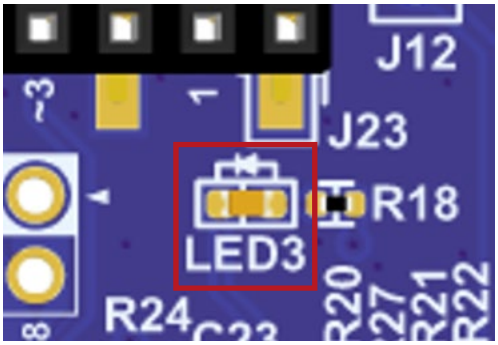



**Figure 16. Debug LED (FPB-RA0L1 Top View)**


**Figure 17. Power LED (FPB-RA0L1 Top View)**

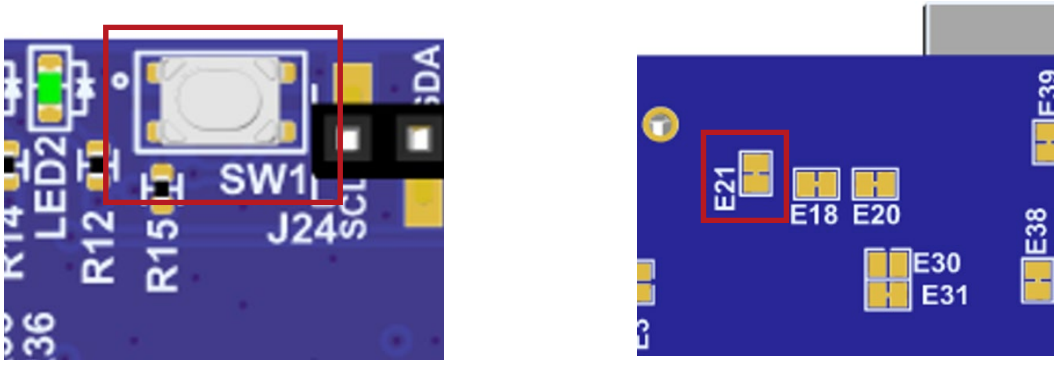
### 5.4.2 User and Reset Switches

Two miniature, momentary, mechanical push-button type SMD switches are mounted on the FPB-RA0L1 board.
Pressing the reset switch (SW2) generates a reset signal to restart the RA MCU.

**Table 13. FPB-RA0L1 Board Switches**

| Designator | Function | RA MCU Control Port |
|---|---|---|
| SW1 | User Switch | P200/NMI/IRQ0_A |
| SW2 | RA MCU Reset Switch | RES |

User switch SW1 may be isolated from the RA MCU, so that the associated port can be used for other purposes. To disconnect SW1 from P200, Jumper Trace Cut (closed) E21 must be open.




(Top view) (Bottom view)

**Figure 18. User Switch (SW1) and Jumper Trace Cut (Closed) E21**

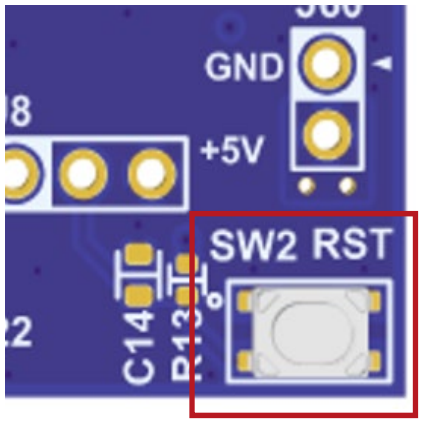



**Figure 19. Reset Switch (SW2)**

### 5.4.3 MCU Clocks

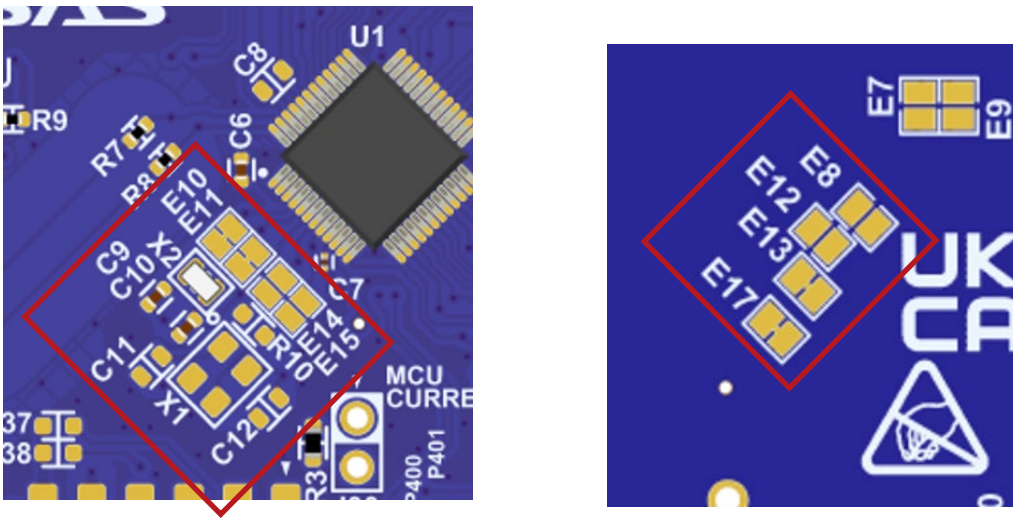
The FPB-RA0L1 board is fitted with a sub-clock oscillator crystal (X2: SC20S-7PF20PPM from Seiko Instruments), providing a precision 32.768 kHz reference clock. The option has also been provided to fit an RA MCU oscillator crystal (X1: not fitted), providing a precision 20.000 MHz reference clock.

A recommended component for X1 is ABM8-20.000MHZ-10-B1U-T from Abracon.

Table 14 lists the settings of jumpers and fitted components for use with the sub-clock and main clock.

**Table 14. Settings of the Main Clock and Sub-clock for the FPB-RA0L1 Board**

| Designator | Additional Component | Jumper Setting (Closed) | Jumper Setting (Open) |
|---|---|---|---|
| X1 | X1, R10, C11, C12 | E14, E15 | E13, E17 |
| X2 | None | E10, E11 | E8, E12 |




(Top view) (Bottom view)

**Figure 20. Main-clock and Sub-clock Oscillation Circuits and Jumpers**

# 6. Special Feature Access

## 6.1 Capacitive Touch Buttons

Two capacitive touch buttons are provided on the FPB-RA0L1 board.

Table 15 lists the port assignments of the capacitive touch buttons on the FPB-RA0L1 board.

**Table 15. Capacitive Touch Buttons on the FPB-RA0L1 Board**

| Designator | RA MCU Control Port |
|---|---|
| Touch Button1 | P001/TS22 |
| Touch Button2 | P000/TS23 |

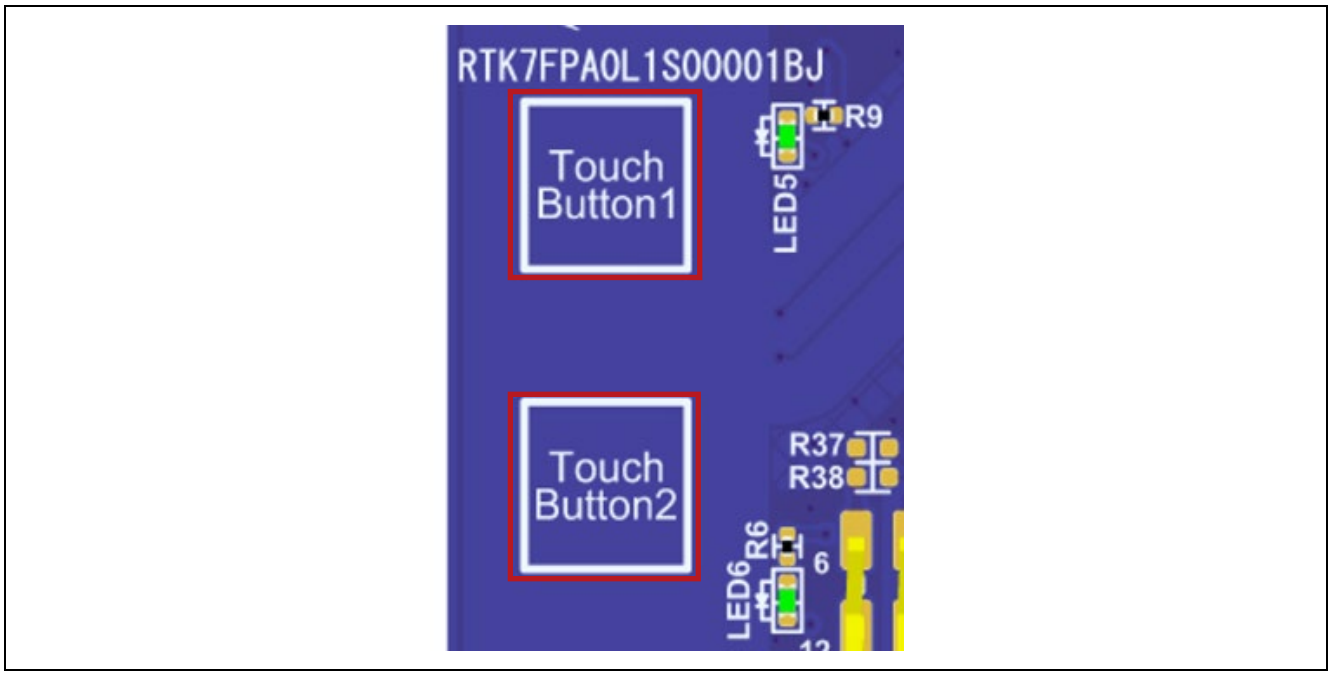



**Figure 21. Capacitive Touch Buttons (FPB-RA0L1 Top View)**

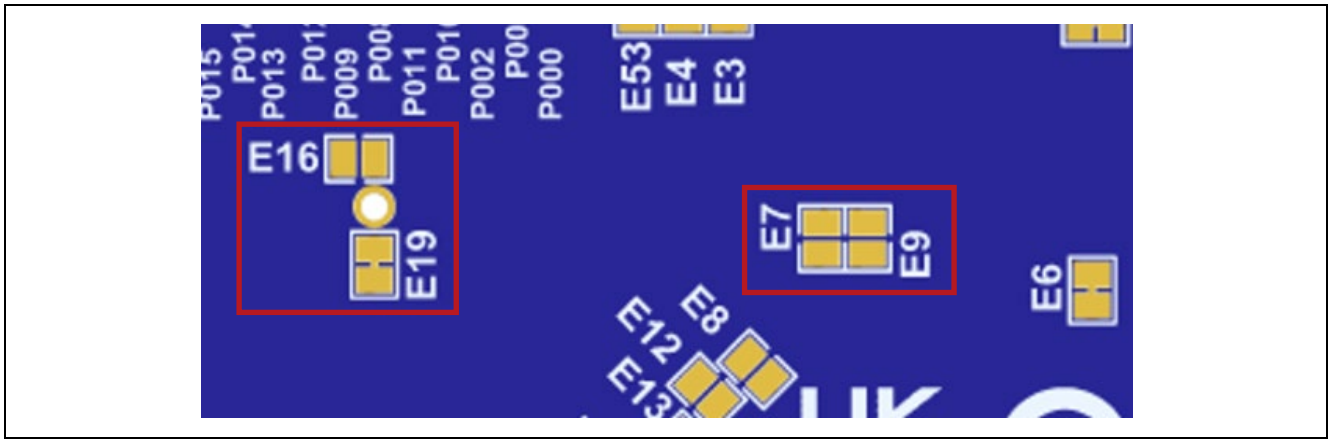



**Figure 22. Jumpers for Capacitive Touch Buttons (FPB-RA0L1 Bottom View)**

To use P001 as a normal port, Jumper Solder Bridge (open) E7 must be closed.

To use P000 as a normal port, Jumper Solder Bridge (open) E9 must be closed.

P112 is used as TSCAP by default and is connected to a 10-nF capacitor.

To use P112 as a normal port, Jumper Solder Bridge (open) E16 must be closed and Jumper Trace Cut (closed) E19 must be open.

## 6.2 Touch-button LEDs

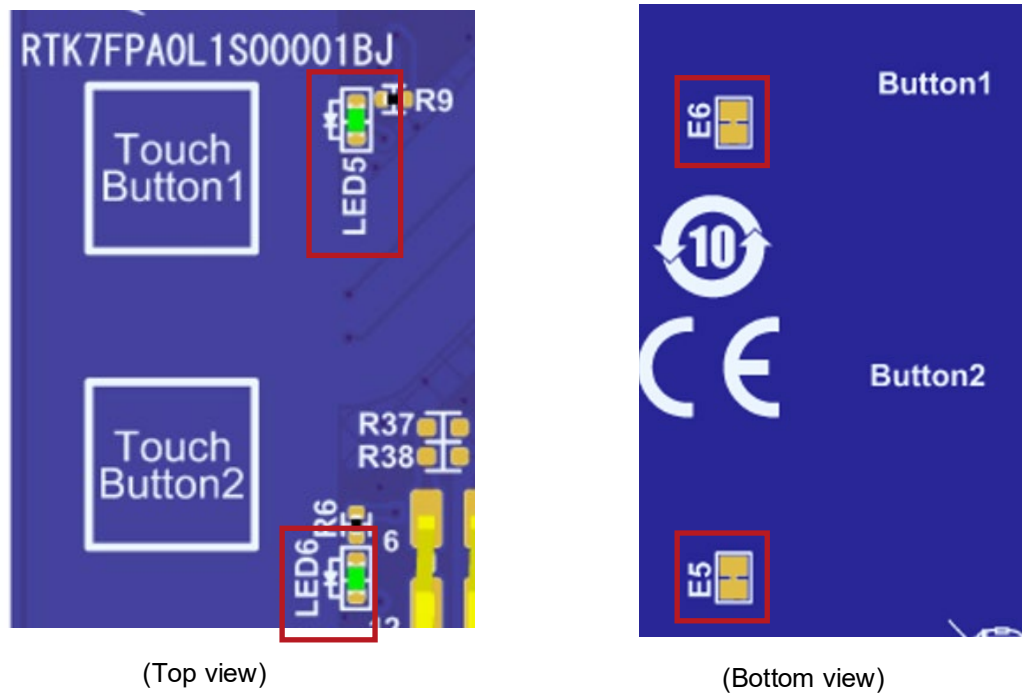
Touch-button LEDs are provided near the two touch buttons on the FPB-RA0L1 board as indicators for those buttons.

Table 16 lists the port assignments of the touch-button LEDs on the FPB-RA0L1 board.

**Table 16. Touch-button LEDs on the FPB-RA0L1 Board**

| Designator | Color | RA MCU Control Port |
|---|---|---|
| LED5 | Green | P401 (illuminated by the low level) |
| LED6 | Green | P400 (illuminated by the low level) |

The touch-button LEDs can be used for any desired purpose in addition to the usage as indicators for the touch buttons. The LEDs can also be isolated from the RA MCU so that the associated ports can be used for other purposes. To disconnect LED5 from P401, Jumper Trace Cut (closed) E6 must be open. To disconnect LED6 from P400, Jumper Trace Cut (closed) E5 must be open.




(Top view) (Bottom view)

**Figure 23. Touch-button LEDs and Jumpers for Touch-button LEDs**

## 7. MCU Native Pin Access

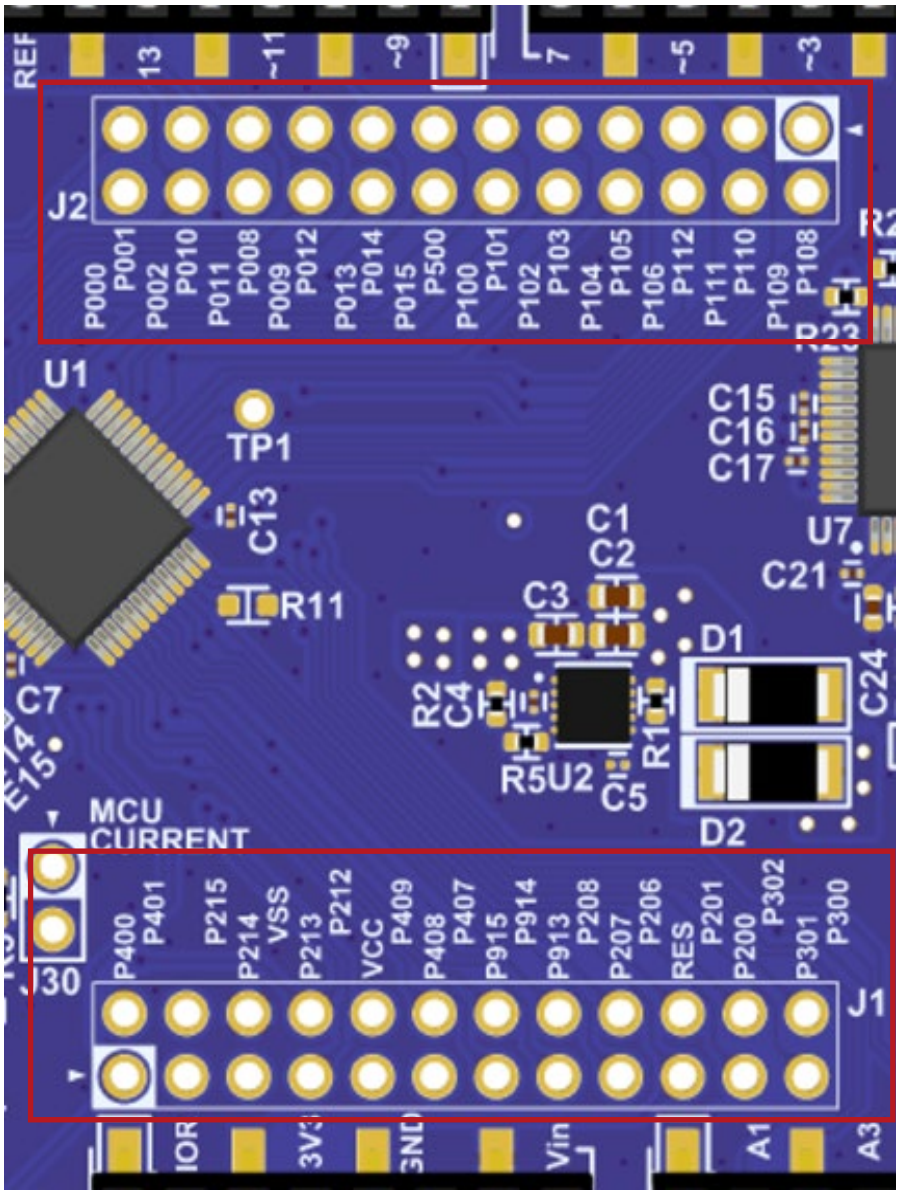



**Figure 24. Native Pin Access (Breakout Pin Headers J1 and J2) (FPB-RA0L1 Top View)**

## 7.1 Breakout Pin Headers

The FPB-RA0L1 board pin headers, J1 (not fitted) and J2 (not fitted), provide access to all RA MCU interface signals, and to voltages for all RA MCU power ports. Each header pin is labelled with the voltage or port connected to that pin. Refer to the RA0L1 Group User's Manual for details of each port function, and the FPB-RA0L1 board schematic for pin header port assignments.

The placement of the breakout pin headers allows for a standard 0.100" (2.54 mm) center breadboard to be placed on both pin headers simultaneously. This can be used for prototyping and testing of custom circuitry for use with the RA MCU.

**Table 17. Breakout Pin Header J1**

| J1 Pin No. | Circuit Net Name | RA0L1 MCU | J1 Pin No. | Circuit Net Name | RA0L1 MCU |
|---|---|---|---|---|---|
| 1 | P400 | U1-1 | 2 | P401 | U1-2 |
| 3 | - | - | 4 | P215 | U1-4 |
| 5 | P214 | U1-5 | 6 | VSS | - |
| 7 | P213/SO11_A/TXDA0B/TO02_B | U1-7 | 8 | P212/SI11_A/RXDA0_B | U1-8 |
| 9 | VCC | - | 10 | P409 | U1-10 |
| 11 | P408/SCLA1_F | U1-11 | 12 | P407/SCK11_A/SDAA1_F | U1-12 |
| 13 | P915 | U1-13 | 14 | P914/SCLA0_A | U1-14 |
| 15 | P913/SDAA0_A | U1-15 | 16 | P208/TXDA0_A | U1-16 |
| 17 | P207/RXDA0_A | U1-17 | 18 | P206/IRQ0_C | U1-18 |
| 19 | RES | U1-19 | 20 | P201/IRQ5_B/TO05_B | U1-20 |
| 21 | P200/IRQ0/NMI | U1-21 | 22 | P302/TS0 | U1-22 |
| 23 | P301/TO06_B | U1-23 | 24 | P300/SWCLK | U1-24 |

**Table 18. Breakout Pin Header J2**

| J2 Pin No. | Circuit Net Name | RA0L1 MCU | J2 Pin No. | Circuit Net Name | RA0L1 MCU |
|---|---|---|---|---|---|
| 1 | P108/SWDIO | U1-25 | 2 | P109/SDAA0_C | U1-26 |
| 3 | P110/SCLA0_C/TO01_A | U1-27 | 4 | P111/IRQ1_C | U1-28 |
| 5 | P112/TSCAP | U1-29 | 6 | P106/TXDA1_B | U1-30 |
| 7 | P105/RXDA1_B | U1-31 | 8 | P104 | U1-32 |
| 9 | P103/SSI00_A/IRQ5_A | U1-33 | 10 | P102/SCK00_A | U1-34 |
| 11 | P101/SO00_A/TXDA0_D/TXD0_A/ TO07_A | U1-35 | 12 | P100/SI00_A/RXDA0_D/RXD0_A | U1-36 |
| 13 | P500/TO03_D | U1-37 | 14 | P015/AN007 | U1-38 |
| 15 | P014/AN006 | U1-39 | 16 | P013/AN005 | U1-40 |
| 17 | P012/AN004 | U1-41 | 18 | P009/AN003 | U1-42 |
| 19 | P008/AN002 | U1-43 | 20 | P011/VREFL0 | U1-44 |
| 21 | P010/VREFH0 | U1-45 | 22 | P002 | U1-46 |
| 23 | P001/TS22 | U1-47 | 24 | P000/TS23 | U1-48 |

## 7.2 MCU Current Measurement

Included near the RA0L1 is resistor R3 and test connector J30 (not fitted) to measure the VCC current of the RA0L1.

Resistor R3 is 0 Ω (SMD 0603). It should be removed in order to measure the current consumption using an ammeter connected between J30 (not fitted) pins 1 and 2.

Alternatively, it could be removed and replaced with a suitable low value resistor, and then a voltmeter used to measure the voltage between J30 pins 1 and 2. The current drawn by RA0L1 can then be calculated using Ohm's Law.

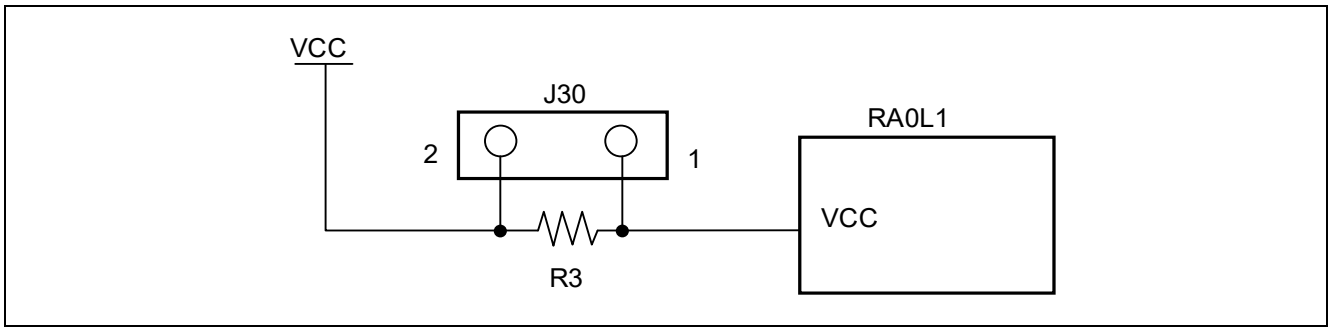



**Figure 25. RA0L1 VCC Current Measurement Circuit Diagram**

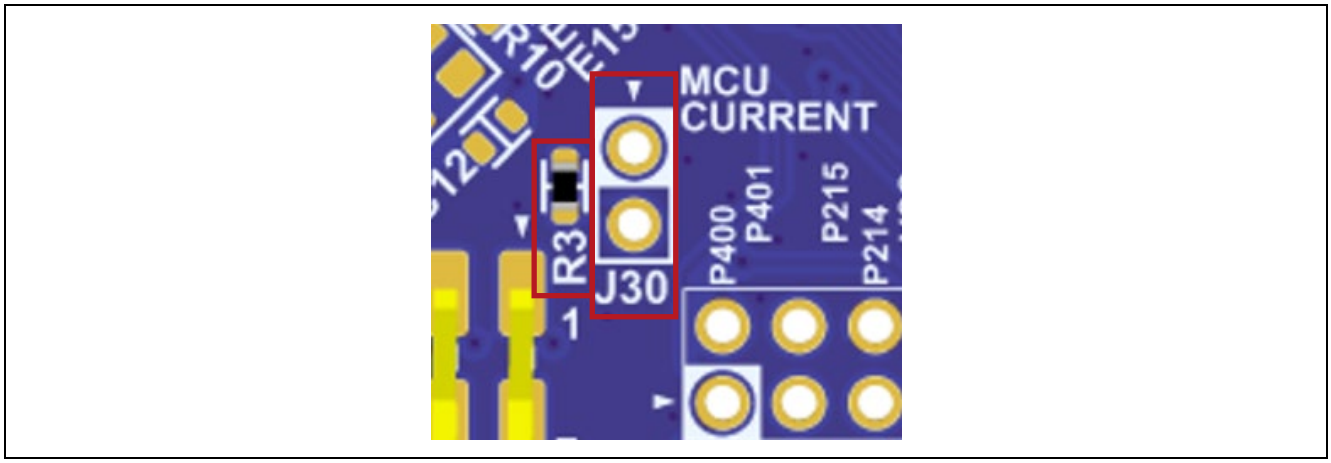



**Figure 26. RA0L1 VCC Current Measurement Point (J30) and R3 (FPB-RA0L1 Top View)**

## 8. Recommended Parts

Table 19 lists recommended part numbers for optional components that can be fitted as required.

**Table 19. Optional Components**

| Designator(s) | Description | Manufacturer | Part Number |
|---|---|---|---|
| X1 | 20 MHz Crystal | ABRACON | ABM8-20.000MHZ-10-B1U-T |
| J1, J2 | 24-pin dual pin header | Parts with 12 x 2 pins and 2.54-mm pitch, which fit into the board holes with a diameter of 1.10 mm | |
| J60, J30 | 2-pin male header | Parts with 2.54-mm pitch, which fit into the board holes with a diameter of 1.10 mm | |

# 9. Certifications

The FPB-RA0L1 board meets the following certifications/standards. See the beginning of this user's manual for the disclaimer and precautions.

## 9.1 EMC/EMI Standards

FCC Notice (Class A)

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

— Reorient or relocate the receiving antenna.
— Increase the separation between the equipment and receiver.
— Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
— Consult the dealer or an experienced radio/television technician for help.

Innovation, Science and Economic Development Canada ICES-003 Compliance:

CAN ICES-3 (A)/NMB-3(A)

CE Class A (EMC)

This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

**Warning** – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)

This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

**Warning** – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

Taiwan: Chinese National Standard 13438, C6357 compliance, Class A limits

Australia/New Zealand AS/NZS CISPR 32:2015, Class A

## 9.2 Material Selection, Waste, Recycling and Disposal Standards

EU RoHS
China SJ/T 113642014, 10-year environmental protection use period.
WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013

The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at;
https://www.renesas.com/eu/en/support/regional-customer-support/weee

## 9.3 Safety Standards

UL 94V-0

## 10. Design and Manufacturing Information

The design and manufacturing information for the FPB-RA0L1 v1 board is available in the “FPB-RA0L1 v1 Design Package” available on renesas.com/fpb-ra0l1.

Design package file name: fpb-ra0l1-v1-designpackage.zip
Design package contents:

**Table 20. FPB-RA0L1 Board Design Package Contents**

| File Type | Content | File/Folder Name |
|---|---|---|
| File (PDF) | Schematics | fpb-ra0l1-v1-schematics |
| File (PDF) | Mechanical Drawing | fpb-ra0l1-v1-mechdwg |
| File (PDF) | BoM | fpb-ra0l1-v1-bom |
| File (PDF) | 3D Drawing | fpb-ra0l1-v1-3d |
| Folder | Manufacturing Files | Manufacturing Files |
| Folder | Design Files | Design Files–Altium |

## 11. Website and Support

Visit the following URLs to learn about the kit and the RA family of microcontrollers, download tools and documentation, and get support.

| | |
|---|---|
| FPB-RA0L1 Resources | renesas.com/fpb-ra0l1 |
| RA Kit Information | renesas.com/ra/kits |
| RA Product Information | renesas.com/ra |
| RA Product Support Forum | renesas.com/ra/forum |
| RA Videos | renesas.com/ra/videos |
| Renesas Support | renesas.com/support |

## 12. Note on Usage

The FPB-RA0L1 v1 board has the following notes.

1. When connecting an external debugger to J13, check the position of pin 1 of the connector to be connected.

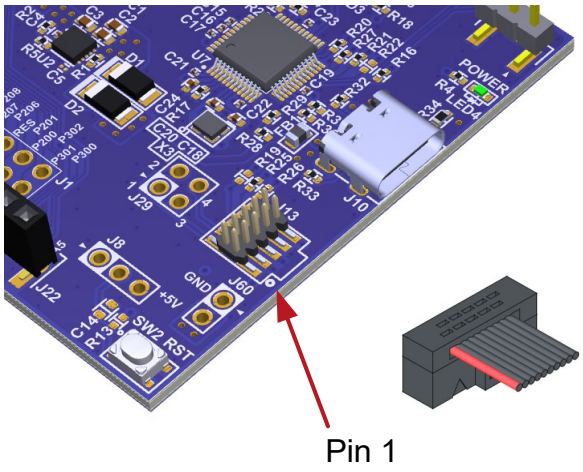



**Figure 27. Position of J13-1 (FPB-RA0L1 Top View)**

2. P106/TXDA1_B and P105/RXD1A_B are connected to the RA4M2 (J-Link OB). When these components are not used as the VCOM port of J-Link, cut E28 and E29 of the Jumper Trace Cut (closed).

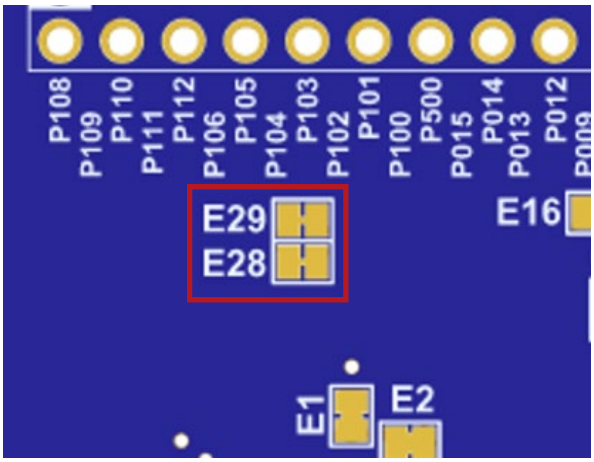



**Figure 28. Jumper Trace Cut (Closed) for the VCOM Port (FPB-RA0L1 Bottom View)**

# 13. Appendix

## 13.1 Layout Diagram of Components on the FPB-RA0L1 Board

The layout diagram of components on the FPB-RA0L1 board is shown below.

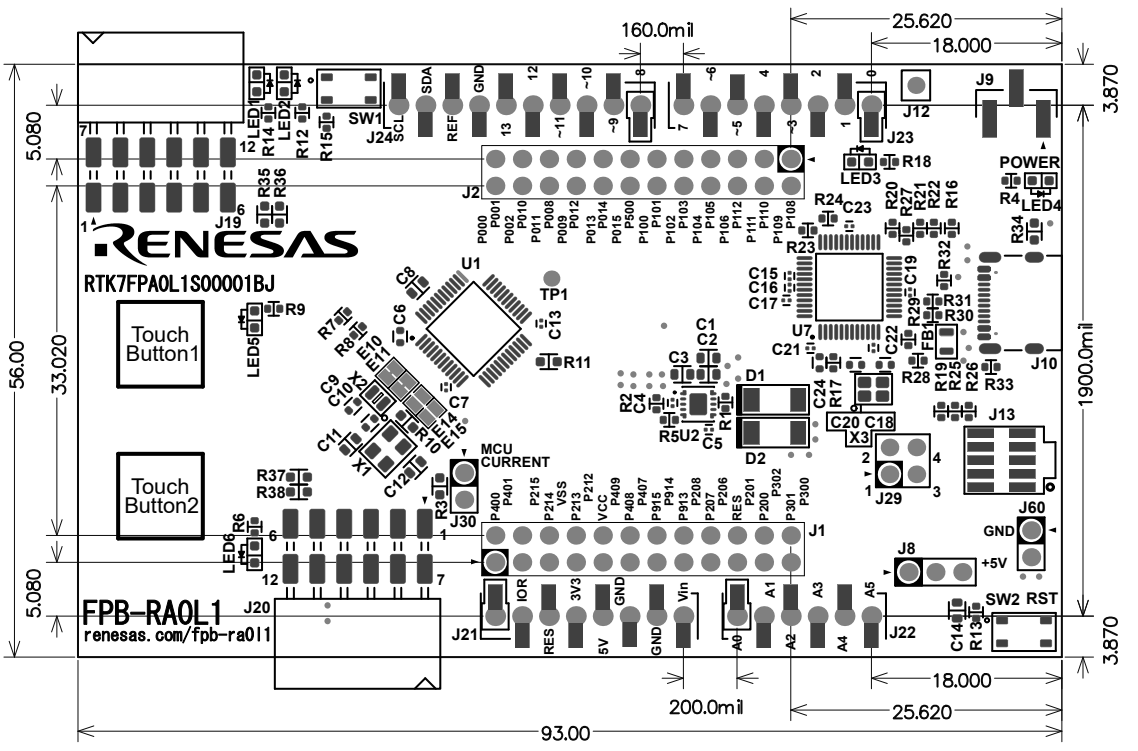



**Figure 29. Layout Diagram of Components on the FPB-RA0L1 Board (Top View)**

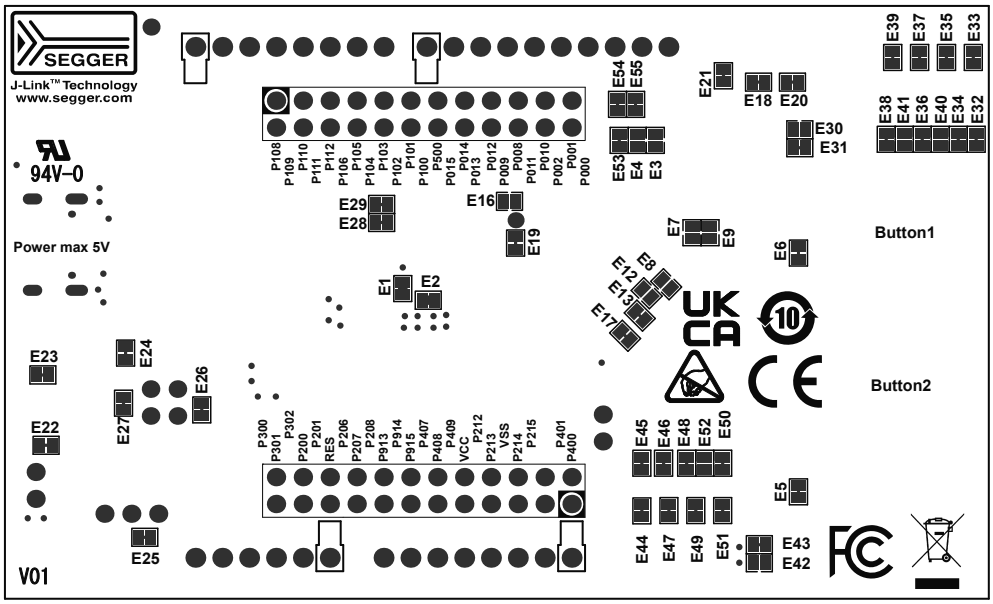



**Figure 30. Layout Diagram of Components on the FPB-RA0L1 Board (Bottom View)**

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jul.05.25 | — | First Edition issued |

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