HSP50415EVAL1

HSP50415EVAL1 Evaluation Kit

FN4859
Rev 0.00
Apr 2000

The HSP50415EVAL1 is an evaluation kit for the HSP50415 wideband programmable modulator. The kit consists of an evaluation Circuit Card Assembly (CCA) complete with the HSP50415 device and additional circuitry to provide for control via a computer parallel port. Windows based demonstration software is provided for full user programmability and control of all HSP50415 operational modes. The evaluation board provides digital outputs which are accessible through a standard logic analyzer header. It also provides both single ended and differential analog outputs via standard SMA connectors. Documentation includes a user's manual, full evaluation board schematics and PCB layout materials. Special filter files, pattern files and example configuration script files are included for quickly configuring the board.

Features

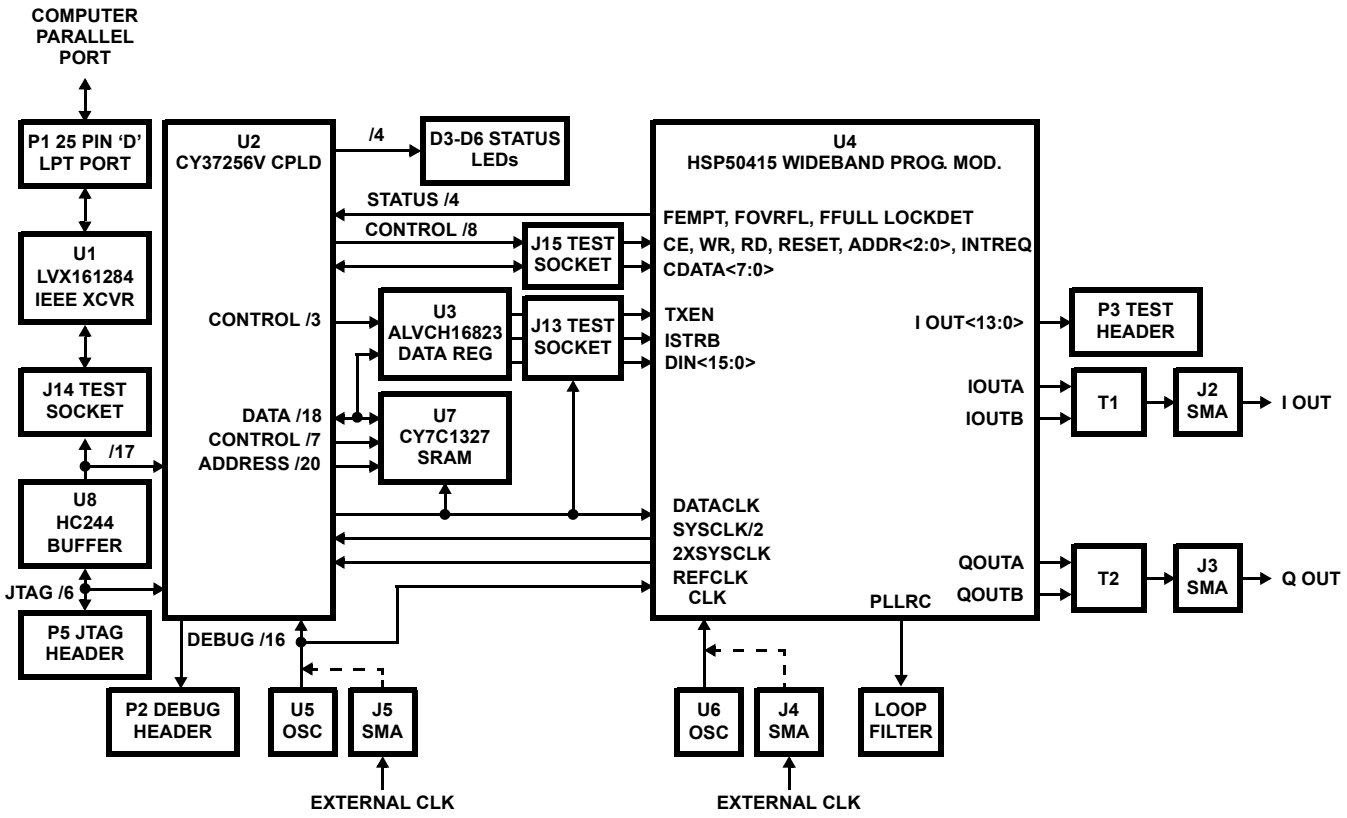
- Evaluation CCA Complete With HSP50415 Wideband Programmable Modulator
- Windows Based Demonstration Software
- Example Files For Common Modulation Techniques

Reference Documents

- HSP50415EVAL1 Demonstration Software in File HSP50415.exe
- Example Configuration Files in *.js, filter files in *.coe, and Pattern Files in *.pat
- HSP50415EVAL1 Schematics in File sch415bx.pdf
- HSP50415EVAL1 Layout in File fab415bx.pdf
- HSP50415EVAL1 Bill of Material in File bom415bx.pdf

The latest version for all reference materials and programs is available via the Intersil internet website: www.intersil.com

Block Diagram



Getting Started

Installation Requirements

1. A personal computer running Windows 95, Windows 98, or Windows NT with a bidirectional parallel port.
2. A $5V_{DC}$ power supply capable of supporting the evaluation CCA by sourcing 1.0 amps.

Software Installation

Obtain the latest version of the downloadable software from 'www.intersil.com/commlink/download/hsp50415eval1'. The software is packaged into an executable zip file format. Copy the file onto the target computer from the website.

Windows 95

1. Execute the 'HSP50415.exe' installation program. This program will create folder HSP50415 and install the required files.
2. Select and execute 'ste51en.exe.' This program will install the required Windows scripting host.

Windows 98

1. Execute the 'HSP50415.exe' installation program. This program will create folder HSP50415 and install the required files.
2. If the target computer's operating system was loaded with the default system configuration, it is not necessary to select and execute "ste51en.exe." This program would have been part of the default. If scripting errors are encountered, execute 'ste51en.exe.'

Windows NT

1. Execute the 'HSP50415.exe' installation program. This program will create folder HSP50415 and install the required files.
2. Select and execute 'ste51en.exe.' This program will install the required Windows scripting host.
3. Execute 'TDLPortIO.exe' from the disk. 'TDLPortIO.exe' installs the parallel port driver, a necessary component for running the software under Windows NT. In order to run 'TDLPortIO.exe' successfully you must have administrator privileges on your NT machine, and have the 'DLLPortIO.dll' and 'DLLPortIO.sys' files in the same directory from which you are executing 'TDLPortIO.exe'. Upon completion, you must reboot in order for the driver to take effect.

Hardware Description

Board Components

The evaluation board consists of three major components as depicted in the block diagram:

1. HSP50415 (U4): This is the wideband programmable modulator device.
2. SRAM (U7). The board uses a 256K x 18 bits synchronous RAM to store digital data patterns for the In-phase and Quadrature inputs to the HSP50415. The SRAM is clocked with the same clock that strobes data into the HSP50415 (DATACLK). The RAM can hold I/Q stimulus patterns that are repeatable with no overhead.
3. CPLD (U2): The CPLD's main function is to interface between the HSP50415, the PC's parallel port, and the SRAM. The CPLD is in system re-programmable, allowing for CCA configuration fielded upgrades.

Communication with the PC is achieved using the 'EPP' (Standard Parallel Port) handshake. Each of the evaluation board's two clocks can be either driven internally by U5 and U6, or externally via SMA connectors J4 and J5. When providing these clocks externally, 50Ω terminators for the external clock sources must be enabled through jumpers JP6 and JP7.

CPLD Registers

The CPLD contains three groups of registers, the first group contains an Address register and a Data register for implementing the EPP handshake. Note that the PC doesn't necessarily require an EPP, as the evaluation software will emulate the EPP handshake. The second group of CPLD registers is shown in Table 2. These registers can be accessed from the evaluation software using the console commands "pldread" and "pldwrite" or using scripts. The third group of registers is shown in Table 3. These registers can be accessed from the evaluation software using the console commands "read" and "write" or using scripts. For more details refer to the 'Software Description' section.

Hardware Configuration

Verify the following default jumper configurations per Table 1:

1. JP1 in position 1-2. (programming 'norm' mode).
2. JP-2 and JP-3 in position 1-2. (board address to 00).
3. JP4 has no jumper. (software controls the source of DATACLK).
4. JP5 in position 1-2. (HSP50415 REFLO enabled as the 1.2V internal reference).
5. JP6 has no jumper (for using the internal REFCLK).
6. JP7 has no jumper (for using the internal Clk).
7. Connect the 5V power supply to the evaluation board connector J1 using the supplied power cable. Ensure the power supply can source 1.0 amps regulated at $5V_{DC}$±5%.

WARNING: Ensure care is utilized to prevent the application of reverse polarity power to the CCA.

8. Connect the supplied ribbon cable from the PC's parallel port to the evaluation board's P1 connector ensuring the arrow indicating pin one on the ribbon cable connector J1 and the CCA P1 are correctly mated.

Software Description

The evaluation software provides a graphical user interface that allows full control over the HSP50415 evaluation board. Through the software, all operational modes of the HSP50415 can be exerted, via the CPLD and SRAM. The software also implements functions for loading stimulus patterns into external memory, loading coefficient files for the internal FIR filters, and

loading constellation map files into the internal constellation map RAM. The software supports dumping any of the internal memory contents into a file for review and editing. Controlling the board can be done by using the forms provided in the software, by using the active command window to execute commands pertaining to accessing registers directly in a peek/poke manner, or by running scripts. The software contains six forms, each controlling a specific part of the board. For example, the PLL form controls the digital and analog phase locked loops. The software has a pull-down menus through which the user can execute various commands. These commands include running scripts, recording macros, dumping memory contents, …etc. These functions are discussed in more details in the following sections.

Running the Software

1. Turn on the power supply.
2. Execute ‘modulator.exe’.
3. Select ‘File’ then ‘Load Configuration’.
4. Select the desired configuration file, then select OK.
5. The ‘modulator.exe’ active window will display the execution results of the selected configuration and the evaluation CCA will be operational.”

Controlling the HSP50415

Software Forms

The software provides five different forms for controlling the HSP50415 device, and one form for controlling the evaluation CCA. These forms can set or clear various register bits, and load associated memories. For more information concerning the interpretations of the bit fields inside these forms, refer to the HSP50415 data sheet. Switching between forms can be done using the Tab toolbar. A brief discussion of the software forms follows:

NCO/Status: This form controls the Carrier Frequency (0x0A), Symbol Rate (0x0B), Memory Control Register (0x00), Interrupt Enable Register (0x09), and the Interrupt Status Register (0x08). Note that the Clk Pin field doesn’t control the Clk going into the HSP50415, it is only used internally by the software for calculating the frequencies in Hz from the hex values stored in registers 0x0A, and 0x0B. The user has to make sure the value in this field is equal to the U6 oscillator value installed, or the external clock frequency, if being input via connector J4.

FIFO/IO: This form controls bits in the FIFO Control Register (0x02), I Channel Control Register (0x03), and the Q channel Control Register (0x04). The user can control the FIFO, I/O pin polarities, I/O pin assignments, DAC enables, and various output enables.

DataFlow: This form controls I Calibration (0x03), Q Calibration (0x04), Gain Control Register (0x05), Shaping Filter DC Offset (0x11) and the Device Configuration Register (0x01).

PLL: This form controls the Digital PLL, which includes the Upper Limit Register (0x0c), Lower Limit Register (0x0d), the REFCLK divider/NCO divider (0x05), and gain control (0x06). This form also controls the Lock Detect/Analog PLL Register (0x07).

Filter: This form displays the contents of the coefficient RAMs, and the constellation map RAM. Contents of the coefficient RAMs can be changed by specifying a file and then clicking on the appropriate load button. It is possible to load the I Coefficient RAM, the Q Coefficient RAM, or both at the same time from the same coefficient file. Note that the loader needs to know the interpolation rate, whether the coefficient file is symmetric, and whether two bit mode will be used or not. Also if the scale Best-Fit box is not checked, the scaling factor for the coefficient file must be known. Clicking the Refresh button will update the memory contents. This is useful when the user specifies a file to load and then decides not to load it, in which case the contents of the File Name box will not reflect the actual memory contents. Loading the constellation map is done similarly.

Board: The form can be used to select the source for DATACLK, and the source for the DIN<15:0> bus. The source for DATACLK can be REFCLK, 2XSYMCLK, SYSCLK/2, or it can be three-stated. The source for the DIN<15:0> can be pattern memory, ground, or it can be three-stated for using an external pattern generator. The board form also shows the contents of the pattern memory. The contents of pattern memory can either be from the software pattern generator, or from a file. If the Pattern Memory Contents box displays ‘Pattern’, it means that the pattern memory was loaded with a pattern according to the parameters shown in the ‘Pattern Parameters’ box. Loading the pattern memory from a file can be done by browsing and selecting a file name, and then clicking on the ‘Load File’ button.

Command Line Window

The Command Line Window is an alternative way to control the HSP50415. There are 7 commands that can be used to control the HSP50415 device, and 4 commands that can be use to control the board:

HSP50415 Device Commands

peek ADDRESS: Reads one of the HSP50415’s control registers specified by ADDRESS.

poke ADDRESS DATA: Writes DATA to the one of the HSP50415 control registers specified by ADDRESS.

setbits ADDRESS MASK: Sets the bits of the control register specified by ADDRESS according to the specified MASK.

resetbits ADDRESS MASK: Clears the bits of the control register specified by ADDRESS according to the specified MASK.

modifybits ADDRESS DATA MASK: Changes the bits specified by MASK of the control register specified by ADDRESS to the value specified by DATA.

read ADDRESS: Reads one of the eight HSP50415 interface registers, if the ADDRESS doesn't exceed 0x07. If the address exceeds 0x07, then this command will read a CPLD register.

write ADDRESS DATA: Writes to one of the HSP50415 interface registers if the ADDRESS is between 0x00 and 0x07.

Board Commands:

pldwrite ADDRESS DATA: Writes DATA to the CPLD register specified by ADDRESS.

pldread ADDRESS: Reads from the CPLD register specified by ADDRESS.

read ADDRESS: Reads the CPLD's Status Register, or Clock Control Register, if the ADDRESS is 0x08 or 0x09 respectively.

write ADDRESS DATA: Writes to the CPLD Clock Control Register, if the address is 0x09. Note that CPLD register 8 is read only. It returns the status pins of the HSP50415. While CPLD register 9 selects the DATACLK source. Writing '0' selects REFCLK, writing '1' selects 2XSYMCLK, writing '2' selects SYSCLK/2, and writing '3' three-states the DATACLK.

All ADDRESS, DATA, and MASK values are expressed in HEXADECIMAL. Additional insight on the command line window can be obtained by using the forms to change bit fields and observing the corresponding commands being echoed in the command line window.

Pull Down Menus

File Menu

Run Script: Allows the user to select and load a script file.

New Script: Opens a scripting window in Notepad.

Start Recording: Begins recording the user's actions that pertain to the evaluation board into a Java script file. To end the recording, click on File, and deselect Recording.

Save Configuration: Saves the contents of all the form register contents into a configuration script file. This file will contain all necessary steps for initializing the evaluation board registers to the present values displayed on all forms.

Load Configuration: Allows the user to select and load a configuration script file.

Dump Menu

This function is used to verify the contents of the external RAM, I coefficient RAM, Q coefficient RAM, Constellation RAM, or FIFO memories for debug purposes. Any of the HSP50415 memories can be dumped into a file using the Dump menu item, and then selecting a file to dump to when prompted. A file comparison can then be done to compare the dumped file to the original file loaded.

Actions Menu

Soft Reset: Issues a reset to the HSP50415 Device.

Board Reset: Issues a reset to both the HSP50415 and the evaluation board.

Send Memory Data: Begins sending the contents of the external RAM to the HSP50415 DIN<15:0> inputs by setting the source for DIN<15:0> as Pattern Memory.

Stop Sending: Stops sending the external RAM data to the HSP50415 DIN<15:0> inputs by setting the source for DIN<15:0> to Gnd.

File Formats

Script files

Scripts can be used to configure the evaluation board and for programming a sequential set of actions. Java scripts (*.js) and Visual Basic scripts (*.vbs), created with any text editor, are supported. Specific file formats are required for each type of file, with examples provided in the evaluation software:

*Configuration Files *.js or *.vbs*

Configuration files contain the scripting host set-up information, followed by the reset commands and the software form registers output commands.

*Coefficient Files *.coe or *.imp*

The coefficient files contain seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing one floating point coefficient per line.

*Constellation RAM Files *.hex*

The constellation RAM file contains only one hexadecimal number per line, with each number containing four digits. The first two digits represent the 8-bit address, while the second two digits represent the 8-bit data.

*Pattern Files *.pat or *.imp*

The pattern file contains seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing two floating point numbers with values <1. The first number is for the I data, and the second is for the Q data.

DUMP FILES *.RAM

The I or Q Coefficient RAM file contains one binary number per line. The first 8-bits are the RAM memAddr<7:0>, the remaining 72-bits contain the RAM memBuf<71:0> contents for the specified address.

TABLE 1. JUMPER CONFIGURATION

JUMPER	TYPE	POSITION	DEFAULT	FUNCTION
JP1	3-point	1-2 Norm/Off	1-2	Selects CPLD normal mode
		2-3 Prog		Selects CPLD programming mode
JP2, JP3	3-point	1-2=0, 2-3=1	1-2	Specify the board address 0 and 1
JP4	3-point	Off	Off	Software selects source for DATACLK
		1-2		DATACLK = REFCLK
		2-3		DATACLK = 2XSYMCLK
JP5	3-point	1-2	1-2	REFLO = Gnd
		2-3		REFLO = Vcca
JP6	On/Off	On	Off	Enables CLK's 50Ω terminator
		Off		Disables CLK's 50Ω terminator
JP7	On/Off	On	Off	Enables REFCLK 's 50Ω terminator
		Off		Disables REFCLK's 50Ω terminator
SJMP 1-4	Solder Jumpers		N.C.	Specify the board revision

TABLE 2. GROUP 2 CPLD REGISTERS

ADDRESS	REGISTER	DESCRIPTION
0x0	MemoryDataOut Register [7:0]	Outputs of this register are the Memory Data Pins.
0x1	MemoryDataOut Register [15:8]	
0x2	MemoryDataOut Register [17:16]	
0x3	MemoryDataIn Register [7:0]	Inputs to this register are the Memory Data Pins.
0x4	MemoryDataIn Register [15:8]	
0x5	MemoryDataIn Register [17:16]	
0x6	MemoryAddress Register [7:0]	Bits [17:0] are the Memory Address pins. Bit 18 is the R/$\overline{W}$ bit. Writing to register 0x8 initiates a memory access transaction (read if Bit 18=1).
0x7	MemoryAddress Register [15:8]	
0x8	MemoryAddress Register [18:16]	
0x9	MemoryStartAddress Register [7:0]	This register is used for the start address of the pattern loaded in memory. The end Address is 0x3ffff (256 K).
0xA	MemoryStartAddress Register [15:8]	
0xB	MemoryStartAddress Register [17:16]	
0xC	MemoryControl Register [0]	Asserting this bit will send the pattern in the memory to the HSP50415.
Note: Memory Data [15:0] are the actual I or Q data. Bit 16 goes to the ISTRB pin in the HSP50415. Bit 17 goes to the TXEN pin in the HSP50415.		

TABLE 3. GROUP 3 CPLD REGISTERS

ADDRESS	REGISTER	DESCRIPTION
0x00 to 0x07	HSP50415 Interface Registers	
0x08	StatusRegister [4:0]	Read only, Bit 0 = FFULL, Bit 1 = FOVERFL, Bit 2 = FEMPT, Bit 3 = LOCKDET, Bit 4 = Interrupt
0x09	ClockControlRegister [1:0]	Bits[1:0] select the source for DATACLK: 00 selects REFCLK, 01 selects 2XSYMCLK, 10 selects SYSCLK/2, 11 DATACLK three-stated

© Copyright Intersil Americas LLC 2000. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com