USER'S MANUAL

ISL70002SEHEVAL1Z

Evaluation Board

AN1732
Rev.1.00
December 6, 2016

Circuit Comments

The ISL70002SEHEVAL1Z evaluation board is designed to demonstrate the features of the ISL70002SEH, a TID and SEE hardened 12A synchronous buck regulator IC with integrated MOSFETs intended for space applications. For more detailed information about the ISL70002SEH, refer to the ISL70002SEH datasheet.

The ISL70002SEHEVAL1Z evaluation board accepts a nominal 3V to 5.5V input voltage and provides a regulated output voltage ranging from 0.8V to 85% of the input voltage at output currents ranging from 0A to 12A. The output can be quickly set to a preset voltage of 1.0V, or adjusted to an alternate voltage using the onboard potentiometer. A Power-Good (PGOOD) signal goes high and lights a red LED to indicate that the output voltage is within a ±11% typical regulation window. A toggle switch is provided to conveniently enable or disable the output voltage.

The ISL70002SEHEVAL1Z evaluation board can be set to run from the nominal 500kHz or 1MHz internal oscillator of the ISL70002SEH or synchronized to a 500kHz to 1MHz ±20% external clock. Two ISL70002SEH ICs can be synchronized to each other in a master/slave configuration, providing nearly twice the output current while switching 180° out-of-phase with respect to each other. See AN1953, "Dual Phase Current Share Evaluation Board User Guide".

Related Literature

- For a full list of related documents, visit our website
  - ISL70002SEH product page

Schematic and BOM

A photograph, schematic, and BOM of the ISL70002SEHEVAL1Z evaluation board are shown in Figure 1, Figure 20 on page 6, and Table 1 on page 7, respectively. The schematic indicates the test points, which allow many nodes of the evaluation circuit to be monitored directly. The BOM shows components that are representative of the types needed for a design, but these components are not space-qualified. Equivalent space-qualified components would be required for flight applications. A 1µH inductor is recommended for 500kHz and a 500µH inductor is recommended for 1MHz.

Recommended Test Equipment

- A 0V to 6V power supply with at least 20A current capability
- An electronic load capable of sinking current up to 12A
- Two Digital Multimeters (DMMs)
- A 500MHz dual-trace oscilloscope

Ordering Information

PART NUMBER	DESCRIPTION
ISL70002SEHEVAL1Z	ISL70002SEHEVAL1Z Evaluation Board

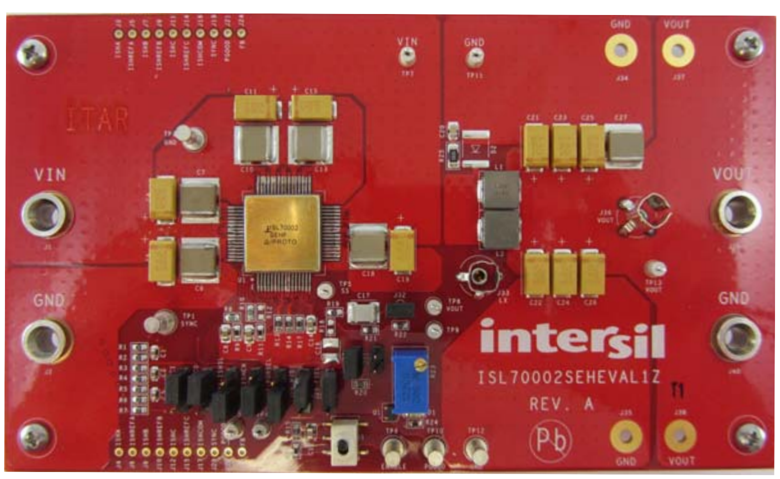

FIGURE 1. ISL70002SEHEVAL1Z TOP VIEW

Quick Start

1. Toggle S1 to the down (OFF) position.
2. Turn on the power supply. Set the output voltage to 3.3V and set the output current limit to 20A. Turn off the power supply.
3. Connect the positive lead of the power supply to J1 and the negative lead of the power supply to J2.
4. Turn on the electronic load and set the output current to 6A.
5. Connect the positive lead of the electronic load to J39 and connect the negative lead of the electronic load to J40.
6. Configure one DMM to monitor the input voltage from TP7 to TP11.
7. Configure another DMM to monitor the output voltage from TP13 to TP11.
8. Connect Channel 1 of the oscilloscope to J6 (or from TP33 to TP28) to monitor the rectangular waveform on the LXx pins.
9. Connect Channel 2 of the oscilloscope to J14 (or from TP36 to TP37) to monitor the output voltage. Ripple voltage is customarily measured with 20MHz bandwidth limiting.
10. Toggle S1 to the up (ON) position.
11. Verify the output voltage is 1.0V ±3% and the frequency of the LXx waveform is 1MHz ±10%.

Layout Guidelines

1. Use an eight-layer PCB with 2 ounce (70µm) copper or equivalent in thinner layers.
2. Two layers should be dedicated for ground plane.
3. Top and bottom layers should be used primarily for signals, but can also be used to increase the VIN, VOUT, and ground planes as required.
4. Connect all AGND, DGND, and PGNDx pins directly to the ground plane. Connect all PVINx pins directly to the VIN portion of the power plane.
5. Locate ceramic bypass capacitors as close as possible to U1. Prioritize the placement of the bypass capacitors on the pins of U1 in the order shown: PVINx, REF, AVDD, DVDD, SS, EN, PGOOD.
6. Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the load and the bottom leg of the resistive divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.
7. Use a small island of copper to connect the LXx pins of U1 to the inductor(s), L1 and L2, to minimize the routing capacitance that degrades efficiency. Separate the island from ground and power planes as much as possible.
8. Keep all signal traces as short as possible.
9. A small series snubber (R_{25} and C_{20}) connected from the LXx pins to the PGNDx pins may be used to dampen ringing on the LXx pins if desired.
10. For optimum thermal performance, place a pattern of vias on the top layer of the PCB directly underneath U1. Connect the vias to the ground planes, which serve as a heatsink. Thermal interface material such as a Sil-Pad should be used to fill the gap between the vias and the bottom of U1 to ensure good thermal contact. Using a Sil-Pad has the added benefit of raising the bottom of U1 from the PCB surface so that a slight bend can be added to the leads for strain relief.

ISL70002SEHEVAL1Z Efficiency Curves

The efficiency data presented in Figures 2 through 17 was taken with the ISL70002SEHEVAL1Z immersed in a temperature-calibrated liquid bath to ensure the notated IC case temperature.

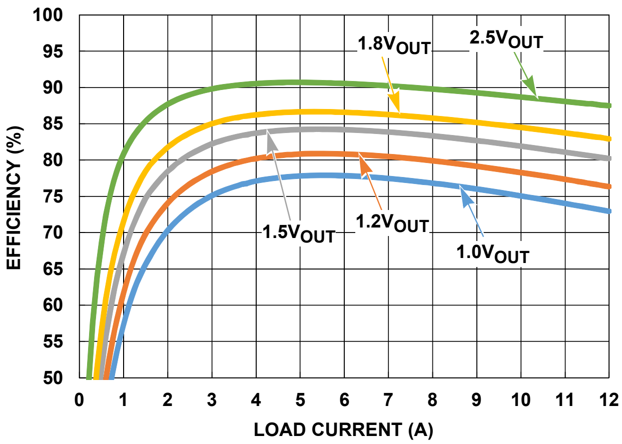

FIGURE 2. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 500kHz, -55°C CASE TEMPERATURE

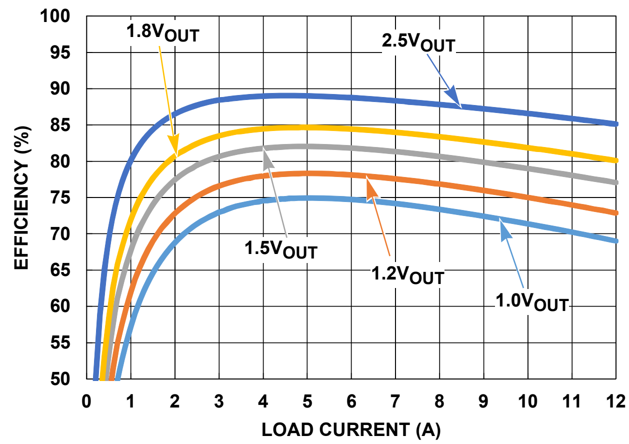

FIGURE 3. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 1MHz, -55°C CASE TEMPERATURE

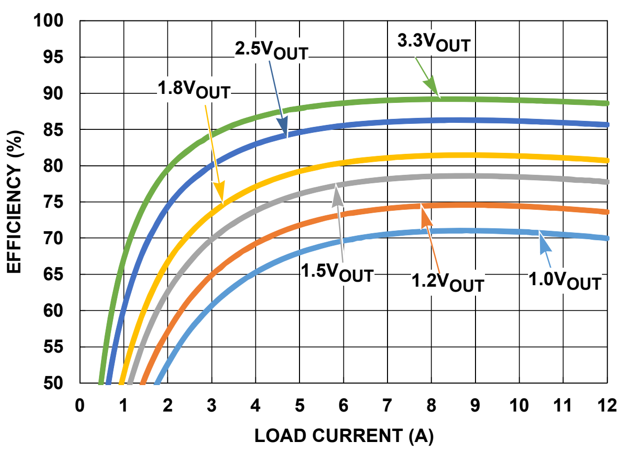

FIGURE 4. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW}= 500kHz, -55°C CASE TEMPERATURE

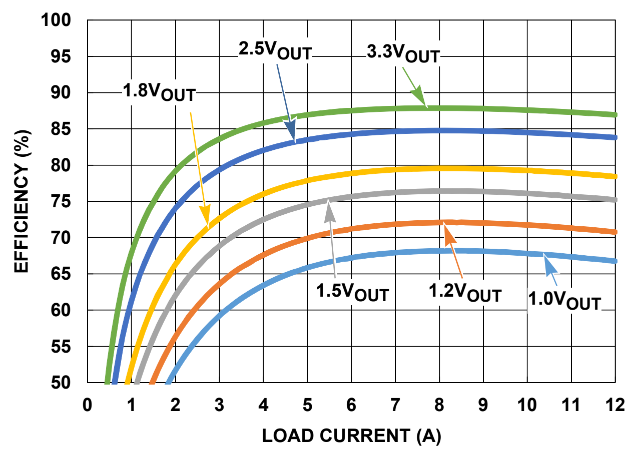

FIGURE 5. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW} = 1MHz, -55°C CASE TEMPERATURE

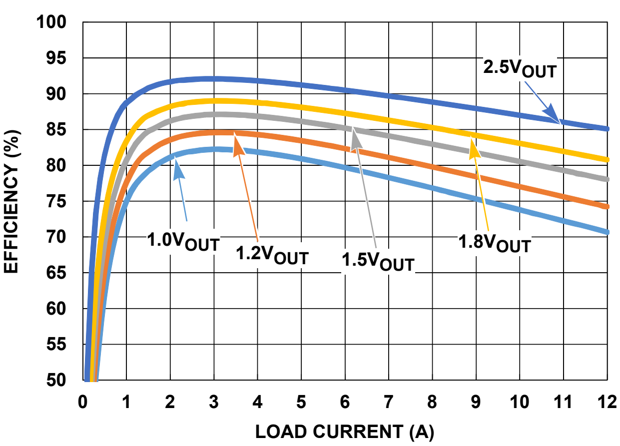

FIGURE 6. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 500kHz, +25°C CASE TEMPERATURE

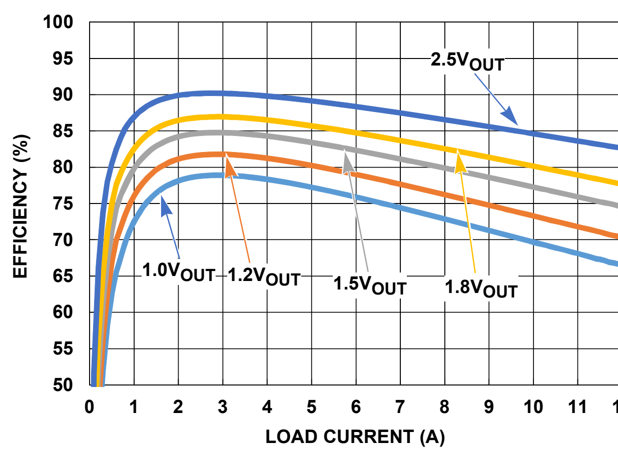

FIGURE 7. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 1MHz, +25°C CASE TEMPERATURE

ISL70002SEHEVAL1Z Efficiency Curves

The efficiency data presented in Figures 2 through 17 was taken with the ISL70002SEHEVAL1Z immersed in a temperature-calibrated liquid bath to ensure the notated IC case temperature. **(Continued)**

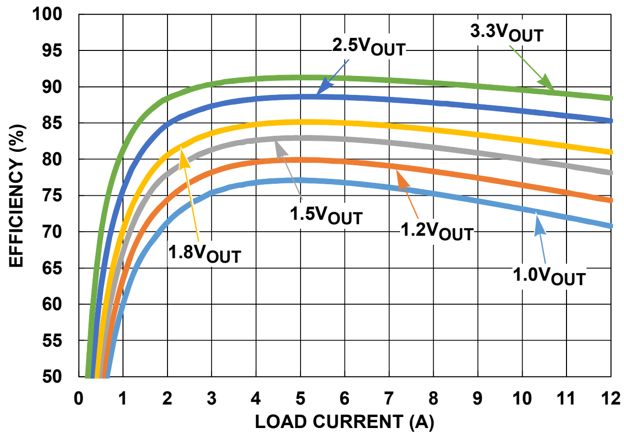

FIGURE 8. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 500kHz, +25°C CASE TEMPERATURE

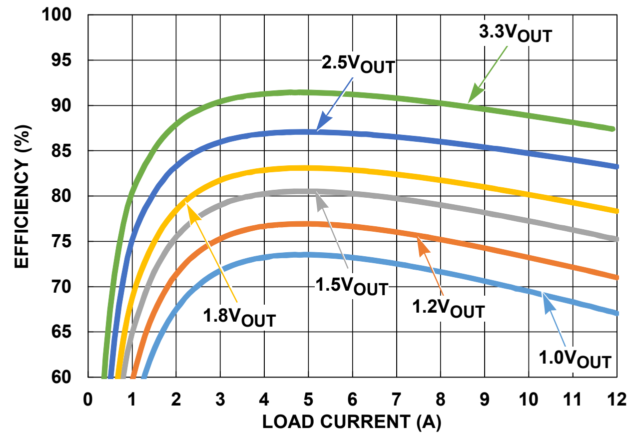

FIGURE 9. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 1MHz, +25°C CASE TEMPERATURE

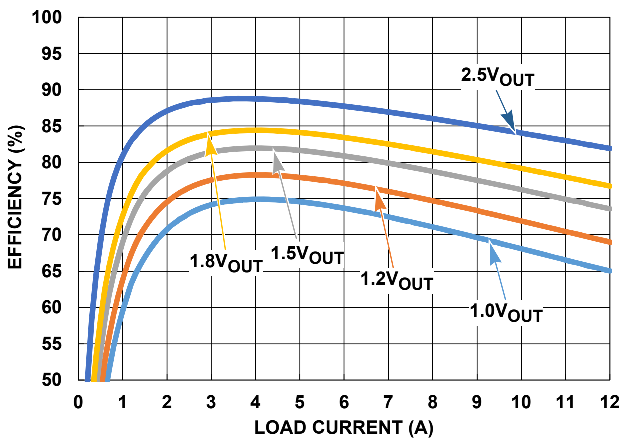

FIGURE 10. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 500kHz, +85°C CASE TEMPERATURE

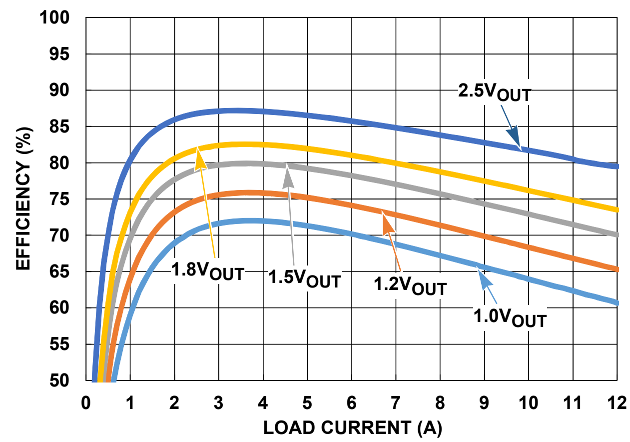

FIGURE 11. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 1MHz, +85°C CASE TEMPERATURE

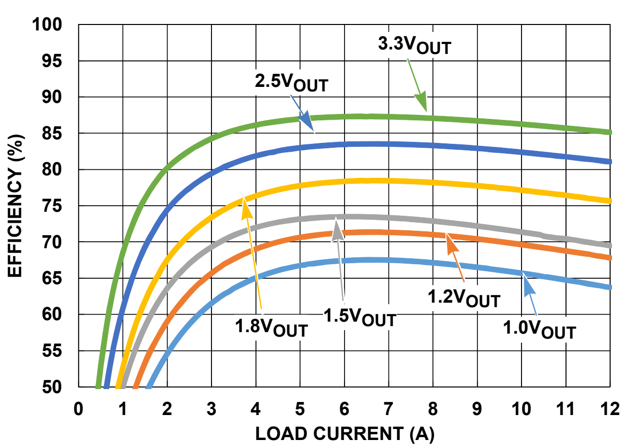

FIGURE 12. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 500kHz, +85°C CASE TEMPERATURE

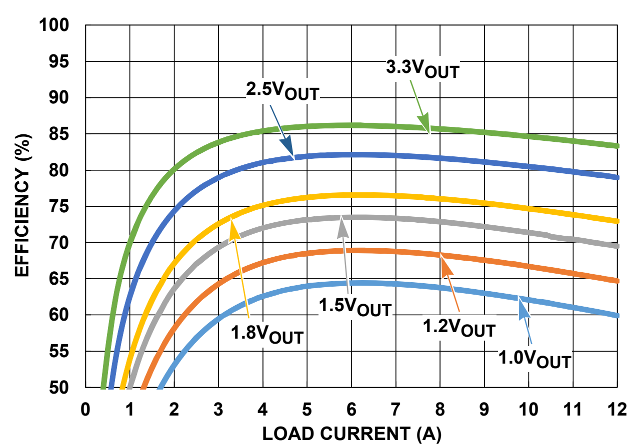

FIGURE 13. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 1MHz, +85°C CASE TEMPERATURE

ISL70002SEHEVAL1Z Efficiency Curves

The efficiency data presented in Figures 2 through 17 was taken with the ISL70002SEHEVAL1Z immersed in a temperature-calibrated liquid bath to ensure the notated IC case temperature. **(Continued)**

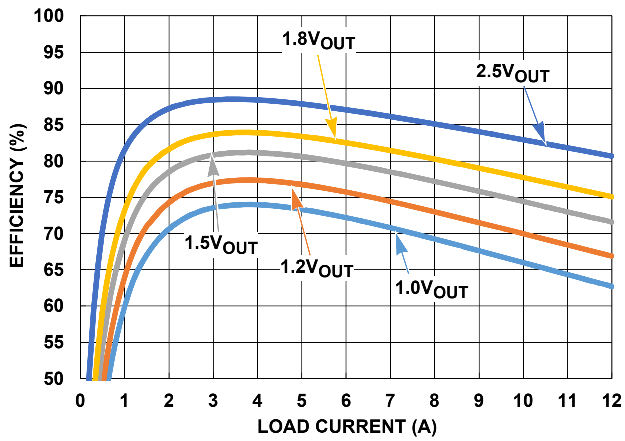

FIGURE 14. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE, V_{IN} = 3.3V, f_{SW} = 500kHz, +125°C CASE TEMPERATURE

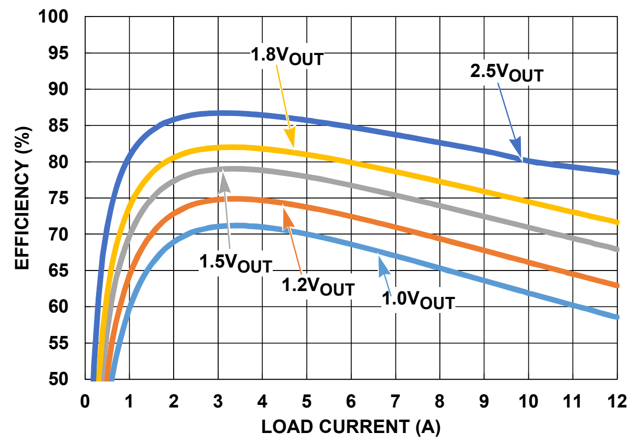

FIGURE 15. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 1MHz, +125°C CASE TEMPERATURE

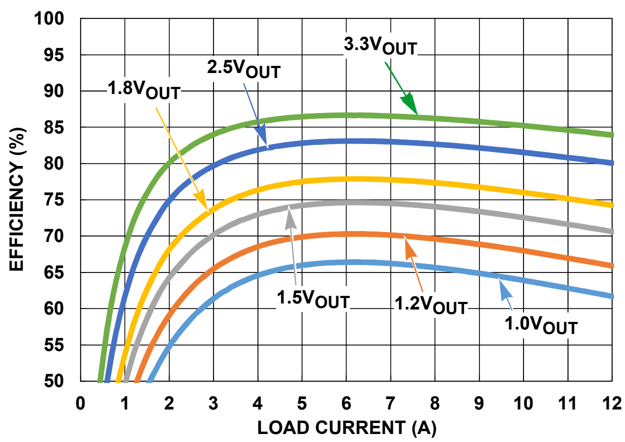

FIGURE 16. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW}= 500kHz, +125°C CASE TEMPERATURE

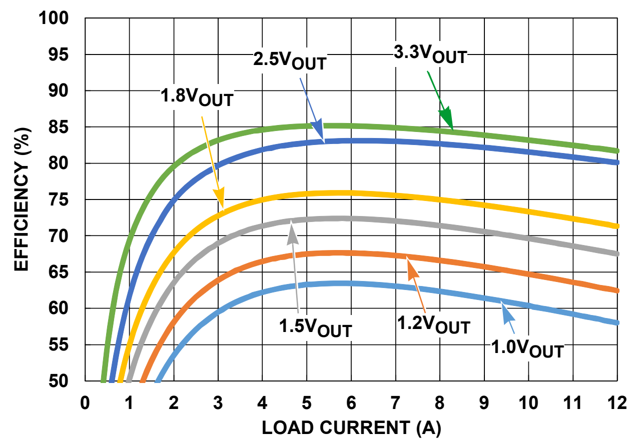

FIGURE 17. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 1MHz, +125°C CASE TEMPERATURE

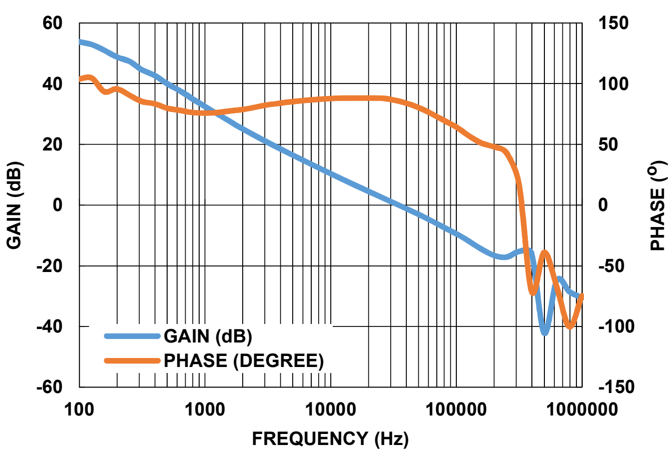

FIGURE 18. GAIN/PHASE PLOT, V_{IN} = 5V, f_{SW} = 500kHz, +25°C AMBIENT TEMPERATURE

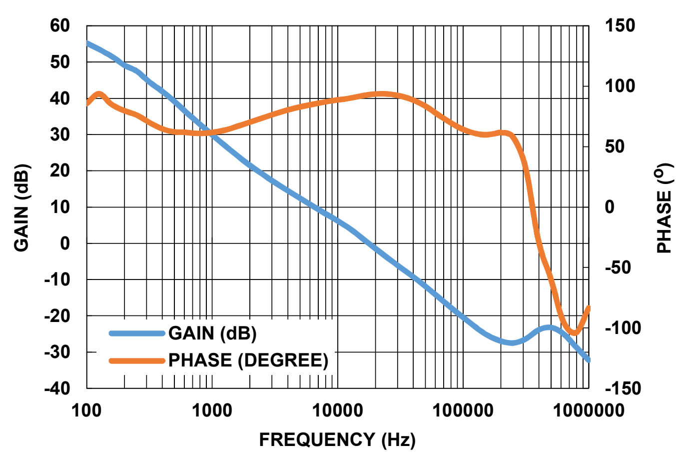

FIGURE 19. GAIN/PHASE PLOT, V_{IN} = 5V, f_{SW} = 1MHz, +25°C AMBIENT TEMPERATURE

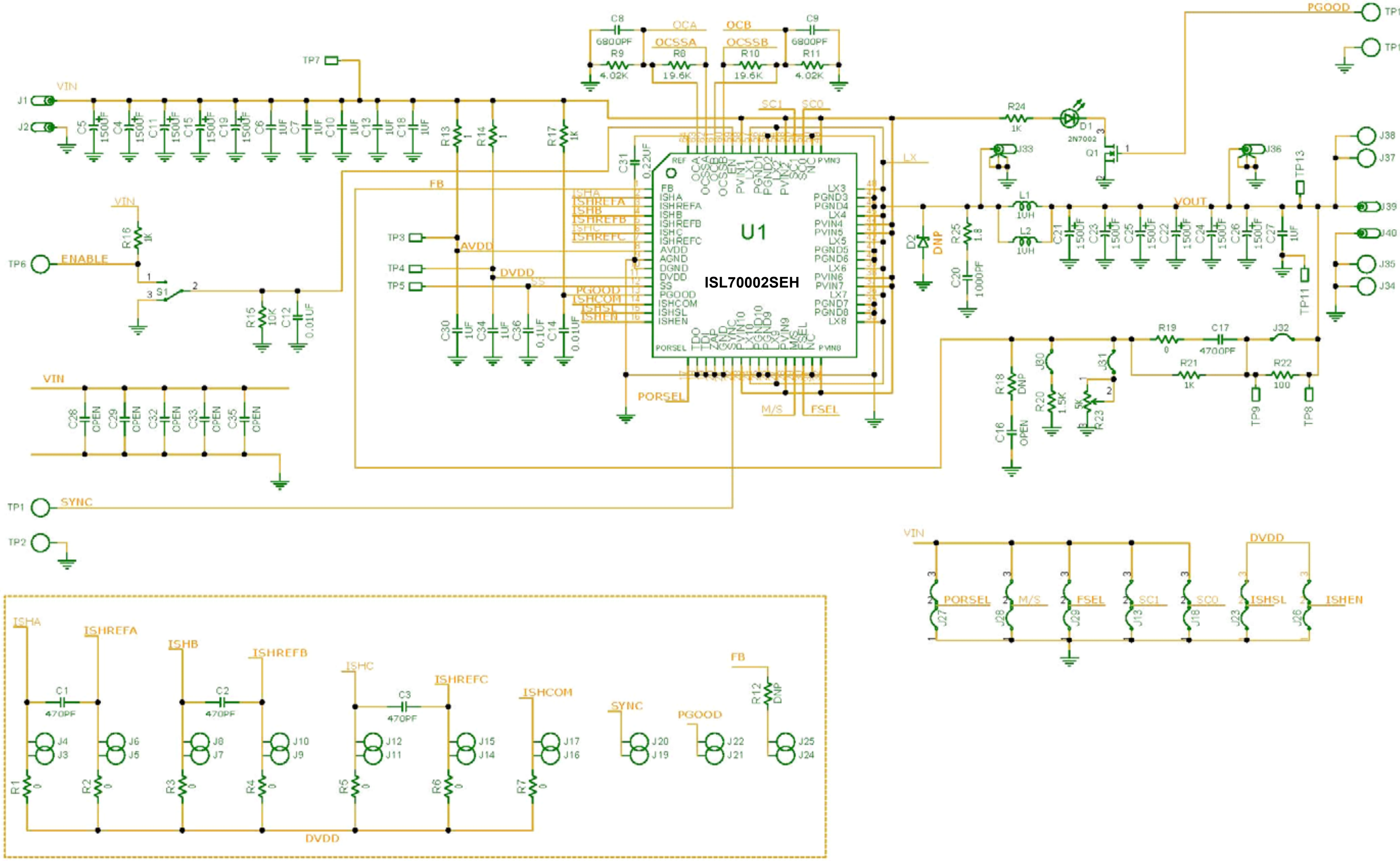

FIGURE 20. ISL70002SEHEVAL1Z BOARD SCHEMATIC

TABLE 1. ISL70002SEHEVAL1Z BILL OF MATERIALS

PART NUMBER	REF DES	QTY	VALUE	TOL	VOLTAGE	POWER	PACKAGE TYPE	JEDEC TYPE	MANUFACTURER	DESCRIPTION
C0805C103K2RAC	C12, C14	2	0.01µF	10%	200V		805	CAP_0805	KEMET	Ceramic Chip Cap
H1082-OPEN	C16	1	OPEN	10%	OPEN		1210	CAP_1210	GENERIC	Ceramic Chip Cap
C1812C472F2GAC	C17	1	4700pF	1%	200V		1812	CAP_1812	KEMET	Multilayer Cap
H1045-00471-25V20	C1-C3	3	470pF	20%	25V		603	CAP_0603	GENERIC	Multilayer Cap
C0805C102K2RAC	C20	1	1000pF	10%	200V		805	CAP_0805	KEMET	Ceramic Chip Cap
H1045-OPEN	C28, C29, C32, C33, C35	5	OPEN	5%	OPEN		603	CAP_0603	GENERIC	Multilayer Cap
C1825C224K2RAC	C31	1	0.22µF	10%	200V		1825	CAP_1825	KEMET	Ceramic Chip Cap
C1210C104K2RAC	C36	1	0.1µF	10%	200V		1210	CAP_1210	KEMET	Ceramic Chip Cap
T530D157M010AHE006	C4, C5, C11, C1, C19, C21-C26	11	150µF	20%	10V		SMD	CAP_7343_31	KEMET	High Capacitance Ultra-Low ESR Tantalum SMD Cap
C2225C105K2RAC	C6, C7, C10, C13, C18, C27, C30, C34	8	1µF	10%	200V		2225	CAP_2225	KEMET	Multilayer Cap
C0805C682K2RAC	C8, C9	2	6800pF	10%	200V		805	CAP_0805	KEMET	Multilayer Cap
LTST-C170CKT	D1	1					SMD	LTST_C170CKT	LITEON	AlGaAs on GaAs Red LED
1N5822US	D2	0					SMD2	DIO_CASE_D-5B	MICROSEMI	3A 40V SCHOTTKY BARRIER RECTIFIER
575-4	J1, J2, J39, J40	4					CONN	CON_BAN_575	KEYSTONE	SOLDER MOUNT BANANA PLUG
JUMPER-3-100	J13, J18, J23, J26-J29	7					THOLE	JUMPER-3	GENERIC	Three Pin Jumper
JUMPER2_100	J30-J32	3					THOLE	JUMPER-1	GENERIC	Two Pin Jumper
131-4353-00	J33, J36	2					CONN	TEK131-4353-00	TEKTRONIX	Scope Probe Test Point PCB Mount
IHLP-2525CZ-ER-1R0-M-01	L1, L2	2	1µH	20%		11A	SMD	IND_IHLP-2525CZ-01	VISHAY	LOW PROFILE HIGH CURRENT INDUCTOR (RoHS COMPLIANT)
2N7002-7-F	Q1	1					SOT23	SOT23	FAIRCHILD	N-Channel EMF Effect Transistor (Pb-Free)
H2505-DNP-DNP-1	R12, R18	2	DNP	1%		DNP	603	RES_0603	GENERIC	Metal Film Chip Resistor (Do Not Populate)
S0603CPZ1R00F10	R13, R14	2	1	1%		1/10W	603	RES_0603	State of the Art	100ppm Thick Film Chip Resistor
S0603CA1002BEZ	R15	1	10k	0.10%		1/10W	603	RES_0603	State of the Art	25ppm Thin Film Chip Resistor
MCR03EZPFX1001	R16	1	1k	1%		1/10W	603	RES_0603	ROHM	Metal Film Chip Resistor
S0603CPZ1001F10	R17	1	1k	1%		1/10W	603	RES_0603	State of the Art	100ppm Thick Film Chip Resistor

TABLE 1. ISL70002SEHEVAL1Z BILL OF MATERIALS (Continued)

PART NUMBER	REF DES	QTY	VALUE	TOL	VOLTAGE	POWER	PACKAGE TYPE	JEDEC TYPE	MANUFACTURER	DESCRIPTION
H2511-00R00-1/16W1	R19	1	0	1%		1/16W	603	RES_0603	GENERIC	Thick Film Chip Resistor
ERJ3GEY0R00V	R1-R7	7	0	0%		1/10W	603	RES_0603	PANASONIC	Thick Film Chip Resistor
S0603CA1501BEZ	R20	1	1.5k	0.10%		1/10W	603	RES_0603	State of the Art	25ppm Thin Film Chip Resistor
S0603CA1001BEZ	R21	1	1k	0.10%		1/10W	603	RES_0603	State of the Art	25ppm Thin Film Chip Resistor
S0603CPZ1000F10	R22	1	100	1%		1/10W	603	RES_0603	State of the Art	100ppm Thick Film Chip Resistor
3299W-1-502-LF	R23	1	5k	10%		1/2W	RADIAL	RES_POT_3299W	BOURNS	TRIMMER POTENTIOMETER (RoHS COMPLIANT)
H2511-01001-1/16W1	R24	1	1k	1%		1/16W	603	RES_0603	GENERIC	Thick Film Chip Resistor
H2513-001R8-1/8W1	R25	1	1.8	1%		1/8W	1206	RES_1206	GENERIC	Thick Film Chip Resistor
S0603CA1962BEZ	R8, R10	2	19.6k	0.10%		1/10W	603	RES_0603	State of the Art	25ppm Thin Film Chip Resistor
S0603CA4021BEZ	R9, R11	2	4.02k	0.10%		1/10W	603	RES_0603	State of the Art	25ppm Thin Film Chip Resistor
GT11MSCBE-T	S1	1					SMT	GT13MSCKE	C&K	SPDT On-None-On SMT Ultraminiature Toggle Switch (RoHS compliant)
1514-2	TP1, TP2, TP6, TP10, TP12	5					THOLE	TP-150C100P	KEYSTONE	Test Point Turret 0.150 Pad 0.100 Thole
5002	TP3-TP5, TP7-TP9, TP11, TP13	8					THOLE	MTP500X	KEYSTONE	Miniature White Test Point 0.100 Pad 0.040 Thole
ISL70002SEHVF	U1	1					CQFP	CQFP64_555X555_635	INTERSIL	12A SYNCHRONOUS BUCK REGULATOR W/MOSFET
SP2000-0.020-AC-1212		1							Bergquist	Thermal Interface Material, Sil-Pad, 12inx12inx0.020in, with adhesive, cut to 0.4inx0.4in and placed on underside of U1

Board Layout

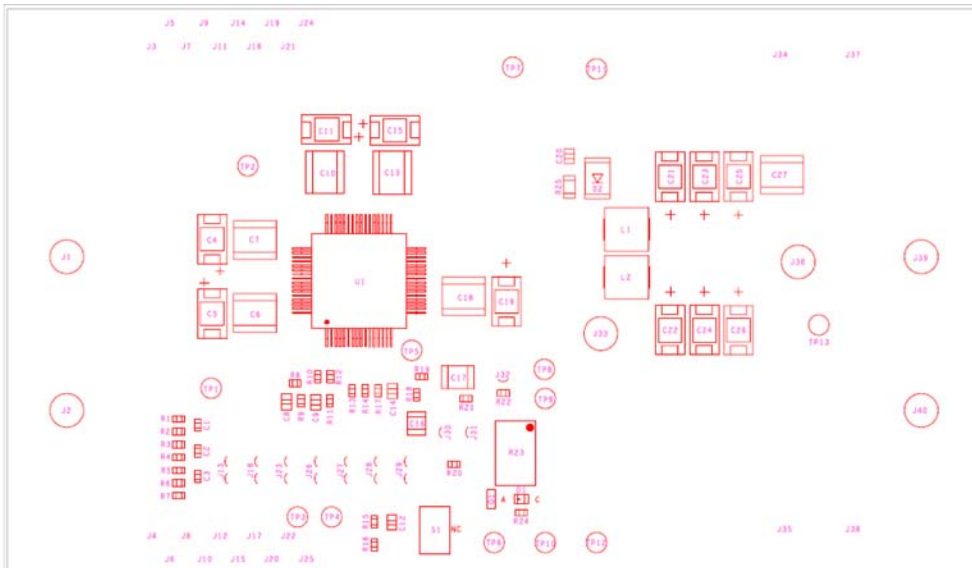

FIGURE 21. TOP SIDE ASSEMBLY DRAWING

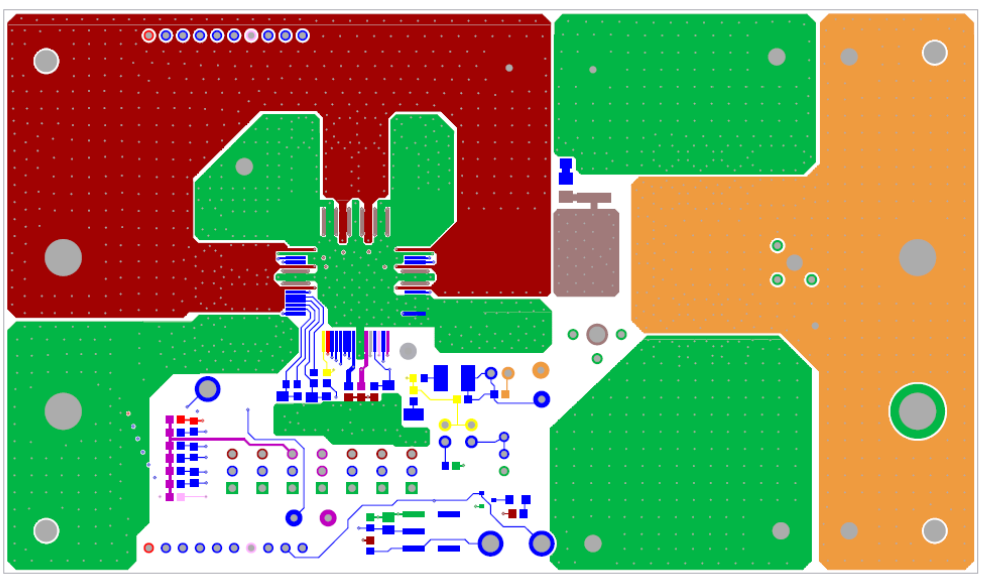

FIGURE 22. TOP LAYER

Board Layout (Continued)

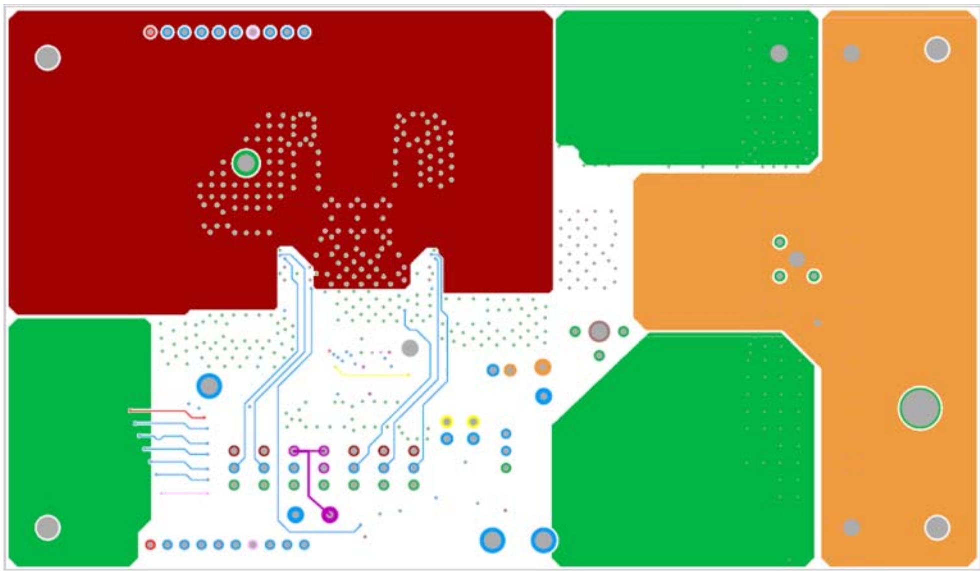

FIGURE 23. LAYER 2

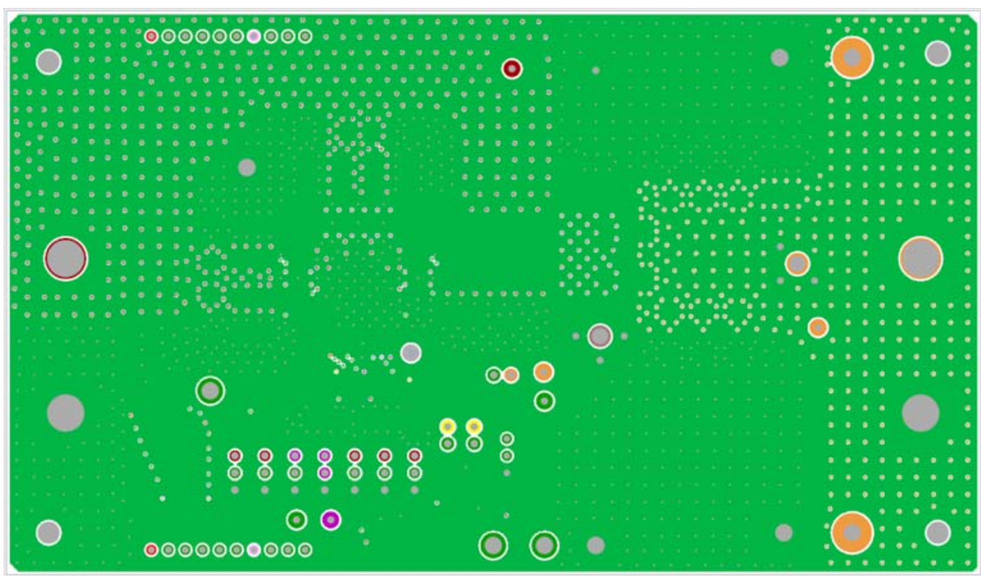

FIGURE 24. LAYER 3

Board Layout (Continued)

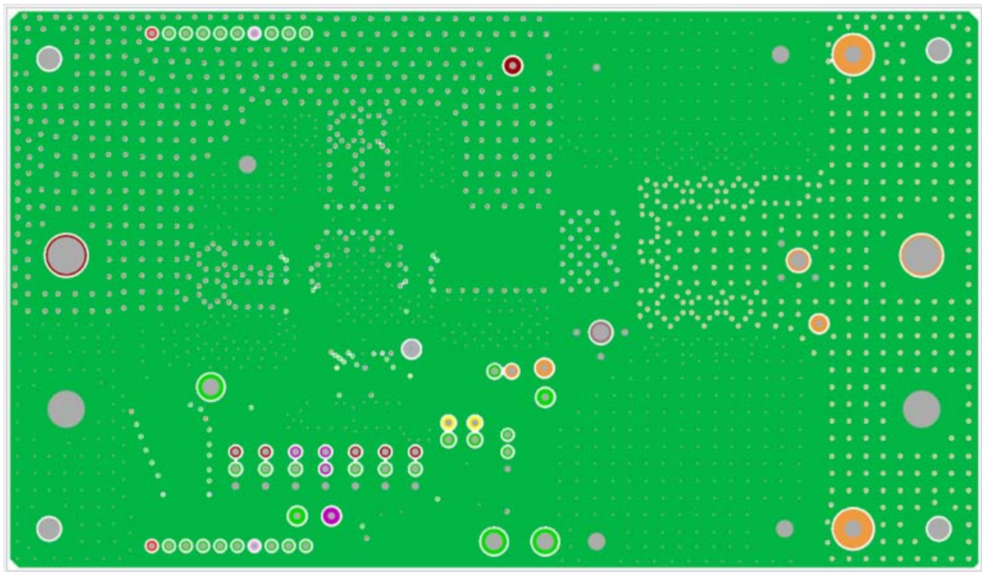

FIGURE 25. LAYER 4

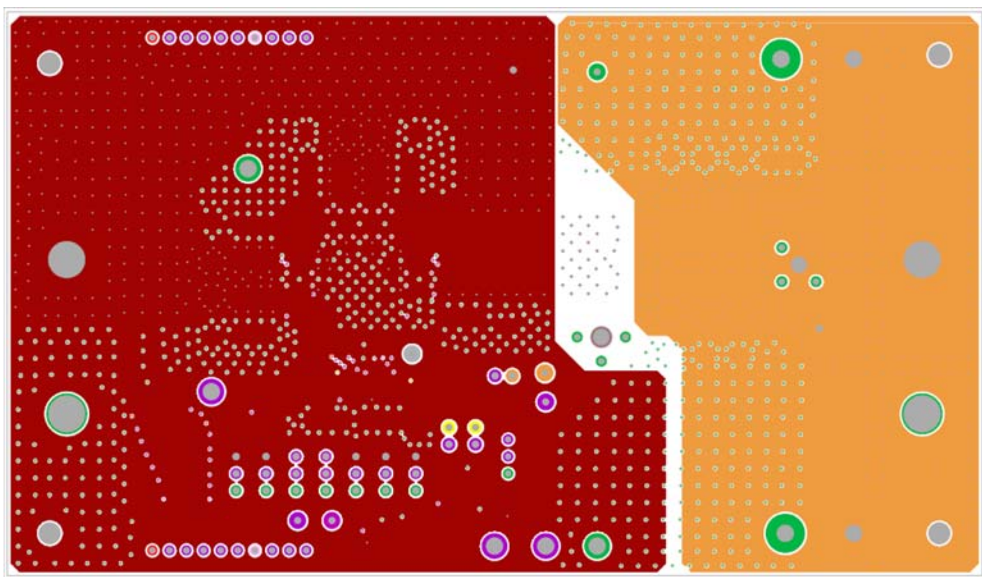

FIGURE 26. LAYER 5

Board Layout (Continued)

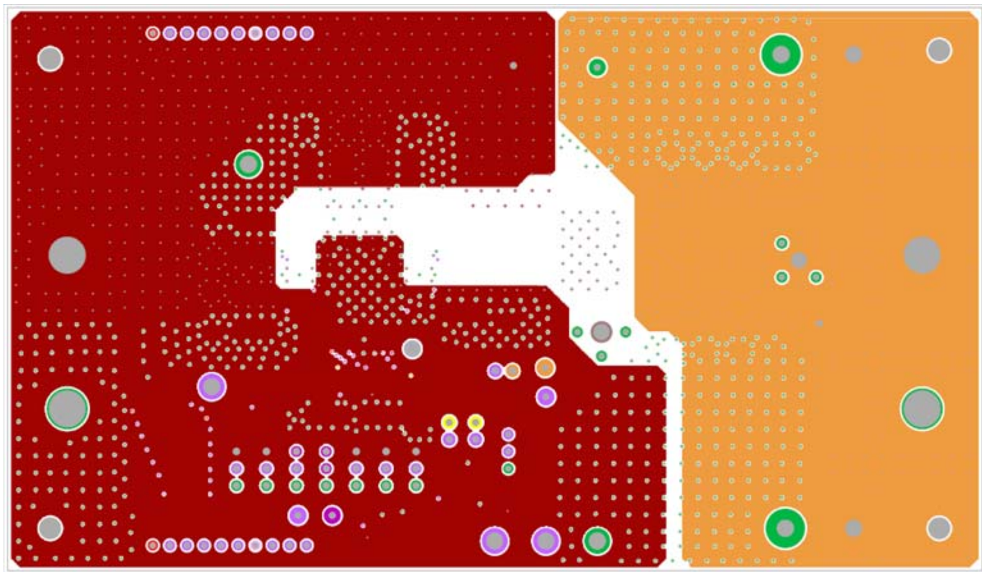

FIGURE 27. LAYER 6

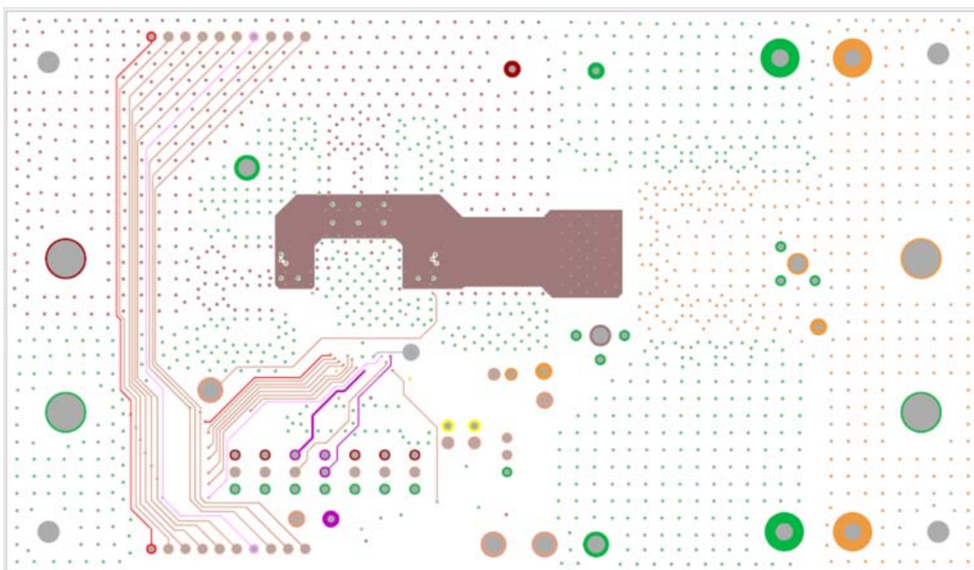

FIGURE 28. LAYER 7

Board Layout (Continued)

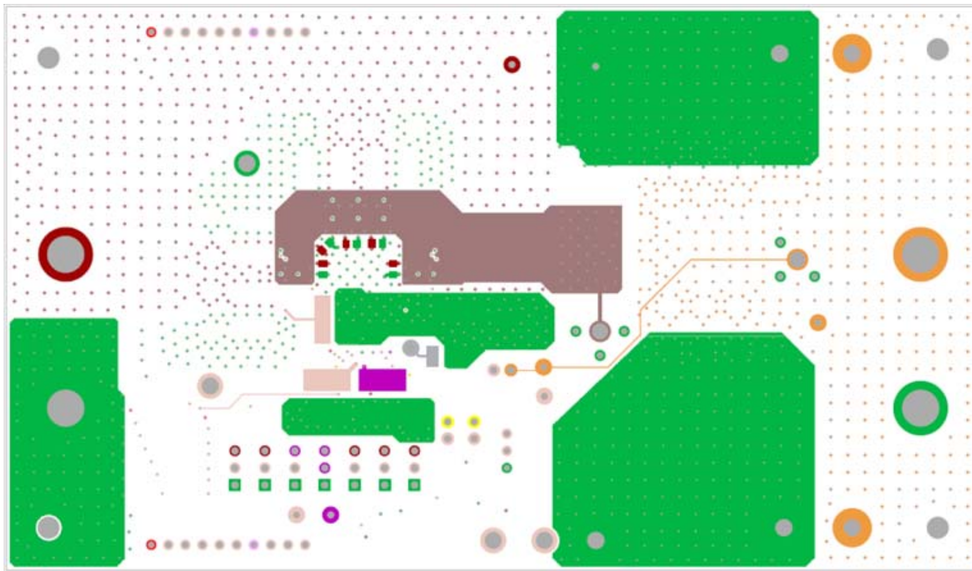

FIGURE 29. BOTTOM LAYER

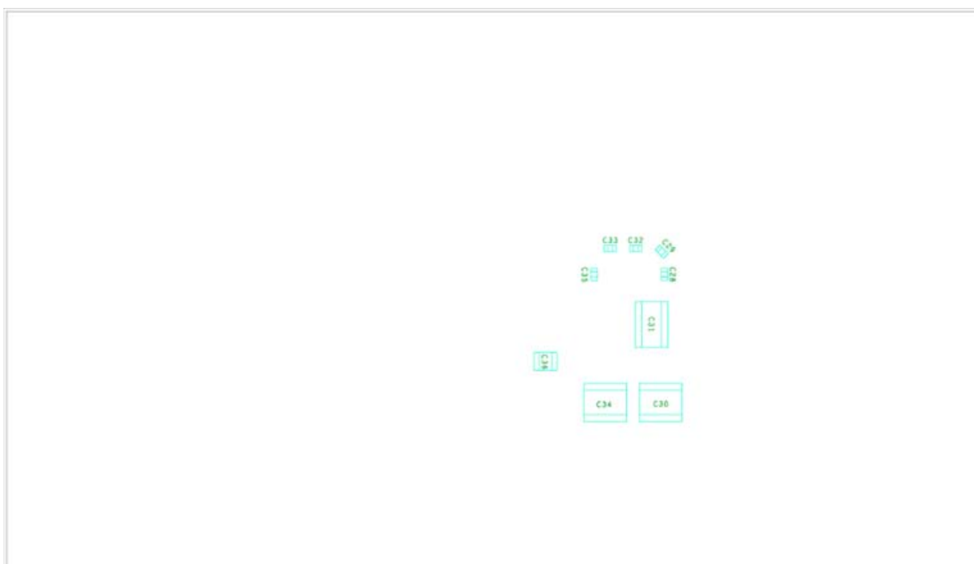

FIGURE 30. BOTTOM SIDE ASSEMBLY DRAWING

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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