User's Manual

ISL70321SEHEVxZ

User's Manual: Evaluation Board

High Reliability

Rev 0.00 Sep 2017

ISL70321SEHEVxZ

Evaluation Board

UG122
Rev.0.00
Sep 18, 2017

1. Overview

The ISL70321SEH evaluation boards highlight an innovative turn-on and turn-off sequencer solution for multi-voltage space-based applications using Point-of-Load (POL) DC/DC voltage converters. The ISL70321SEHEV1Z platform provides a single IC 4-event evaluation platform, whereas the ISL70321SEHEV2Z provides a dual cascaded IC 8-event evaluation platform. Both evaluation boards are provided on the same PCB design, and are both available from inventory in the desired configuration.

1.1 Key Features

- Jumper enabled for stand alone or POL evaluation
- Convenient power connection
- Done indicator
- Easy interconnectivity with other Intersil boards

1.2 Specifications

This board has been configured for the following default operating conditions:

- ISL70321SEHEV1Z for four sequenced outputs
- ISL70321SEHEV2Z for eight sequenced outputs
- V_{IN} = 3V to 13.2V
- Delay timer set for 2ms
- Power-good timer set for 4ms
- Jumper configured for stand-alone evaluation

1.3 Ordering Information

Part Numbers	Description
ISL70321SEHEV1Z	Single sequencer configuration
ISL70321SEHEV2Z	Dual cascaded sequencer configuration

1.4 Related Literature

- For a full list of related documents please visit our website
  - ISL70321SEH product page

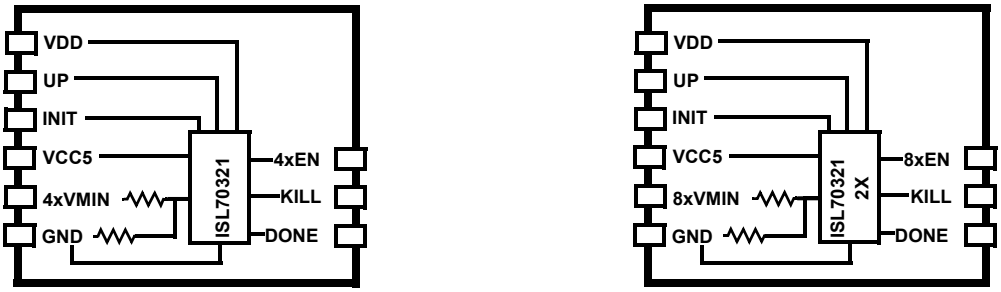


Figure 1. Block Diagrams

2. Functional Description

The ISL70321SEHEV1Z evaluation board provides a simple platform to demonstrate the functionality and features of the ISL70321SEH sequencer IC. The default configuration is a standalone mode wherein the ENx outputs are fed back to the VMx inputs so that the sequencing operation can be demonstrated. Using a combination of jumper settings, the ISL70321SEHEV1Z can be used to address the enable inputs of multiple Intersil POL or LDO evaluation boards using the ENx outputs to create a sequenced on and off multi-voltage rail power supply block.

A common delay timing between the sequenced ENx outputs can be adjusted by changing the TDLY resistor values. Likewise, the power-good timer can be adjusted so that various ramp times of the enabled power supplies can be predetermined.

2.1 Operating Range

By default, the ISL70321SEHEV1Z is configured for the operating V_{IN} range of 3V to 13.2V. The ENx, DONE, and $\overline{KILL}$ outputs are pulled up resistively to the VCC5 output. These outputs can be pulled to another voltage once jumpers are removed. The sequence delay and power-good timers are set to 2ms and 4ms, respectively.

2.2 Quick Start Guide

2.2.1 Single IC Stand-Alone Operation (ISL70321SEHEV1Z)

(1) Ensure that the board is properly connected to the supply and loads prior to applying any power.
(2) Connect the input supply to VIN and GND.
(3) Signal UP high, monitor the four ENABLE outputs with an oscilloscope to see them go high in order.
(4) Signal UP low, monitor the four ENABLE outputs with an oscilloscope to see them go low in reverse order.

2.2.2 Dual IC Cascaded Stand-Alone Operation (ISL70321SEHEV2Z)

(1) Ensure that the board is properly connected to the supply and loads prior to applying any power.
(2) Connect the input supply to VIN and GND.
(3) Signal UP high, monitor the eight ENABLE outputs with oscilloscopes to see them go high in order.
(4) Signal UP low, monitor the eight ENABLE outputs with oscilloscopes to see them go low in reverse order.

2.2.3 Sequence Power Supplies

(1) Change the delay and power-good timer resistors on the board as necessary to achieve the desired timing of sequenced events through the provided resistor positions. Take into account the rise times of the power supplies and the VM input threshold voltage.
(2) Connect the appropriate bias supply to VDD and GND.
(3) Connect the enabling input of the POL or LDO power supplies to be sequenced to the appropriate ISL70321SEH ENx outputs in the order of desired turn-on sequence.
(4) Connect the power supply outputs to the appropriate ISL70321SEH VMx inputs.
(5) Connect UP to the appropriate signaling input.
(6) Use oscilloscopes and DVMs to monitor signals and voltages.
(7) Turn system input power supply ON.
(8) Signal the UP input.
(9) Observe sequencing function and adjust timing and threshold voltages as desired.

3. PCB Layout Guidelines

The ISL70321SEH PCB layout requires no special treatment other than the good design practice of placing the VDD, VCC5, and VREF caps close to the IC body.

3.1 ISL70321SEHEV1Z Evaluation Board

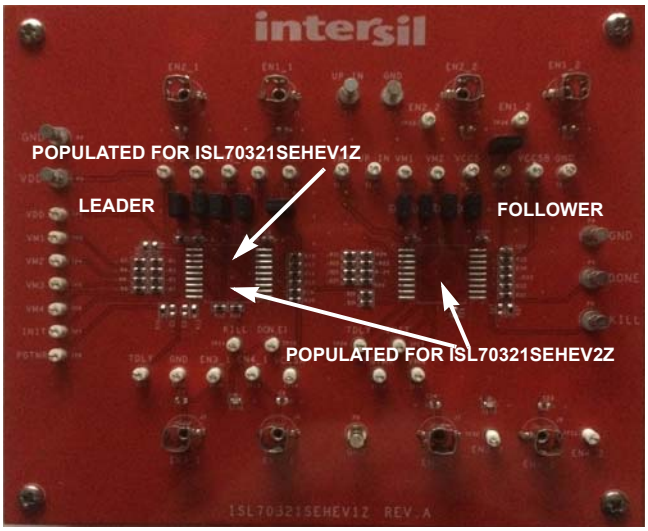


Figure 2. Top Side

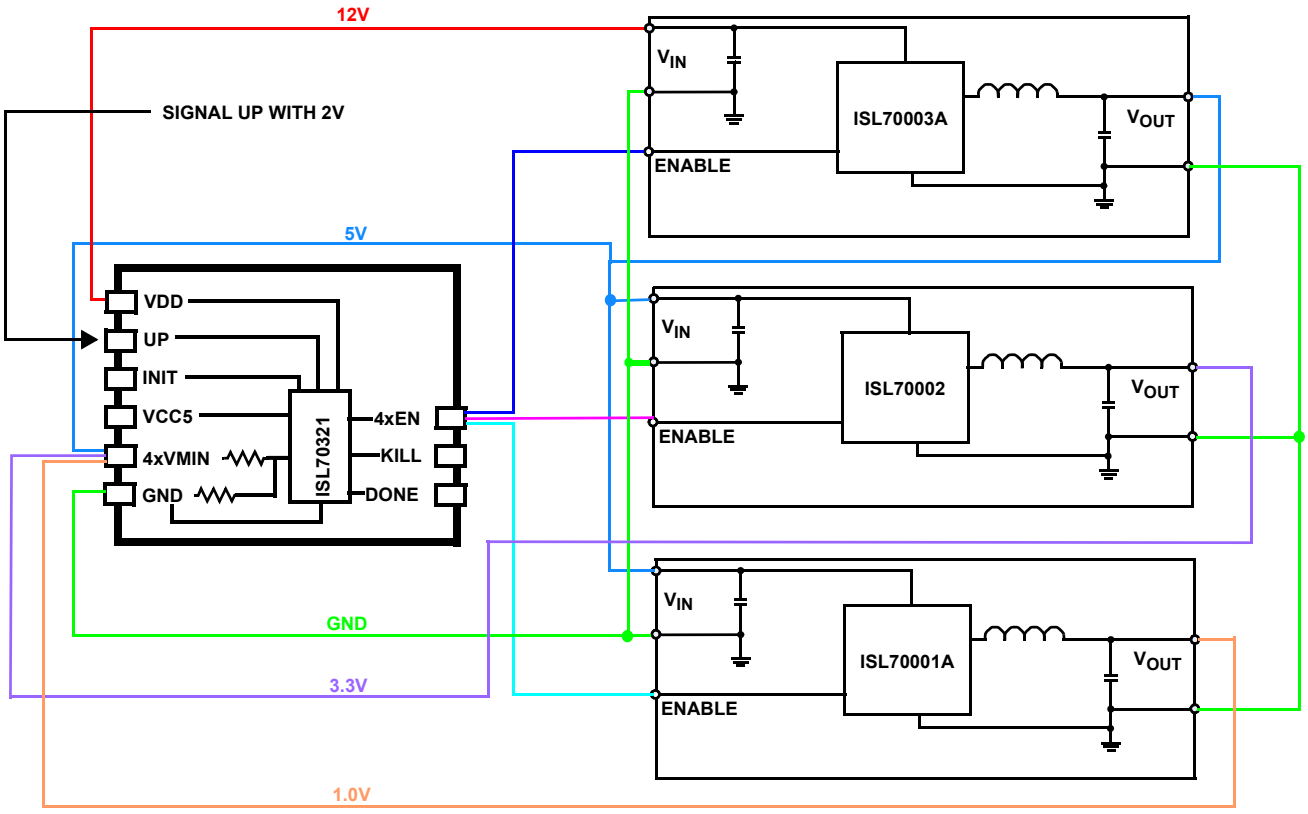


Figure 3. Block Diagram Showing ISL70321SEHEV1Z Enabling Three ISL7000X Regulator Evaluation Boards (See Figures 12, 13)

3.2 ISL70321SEHEVxZ Circuit Schematics

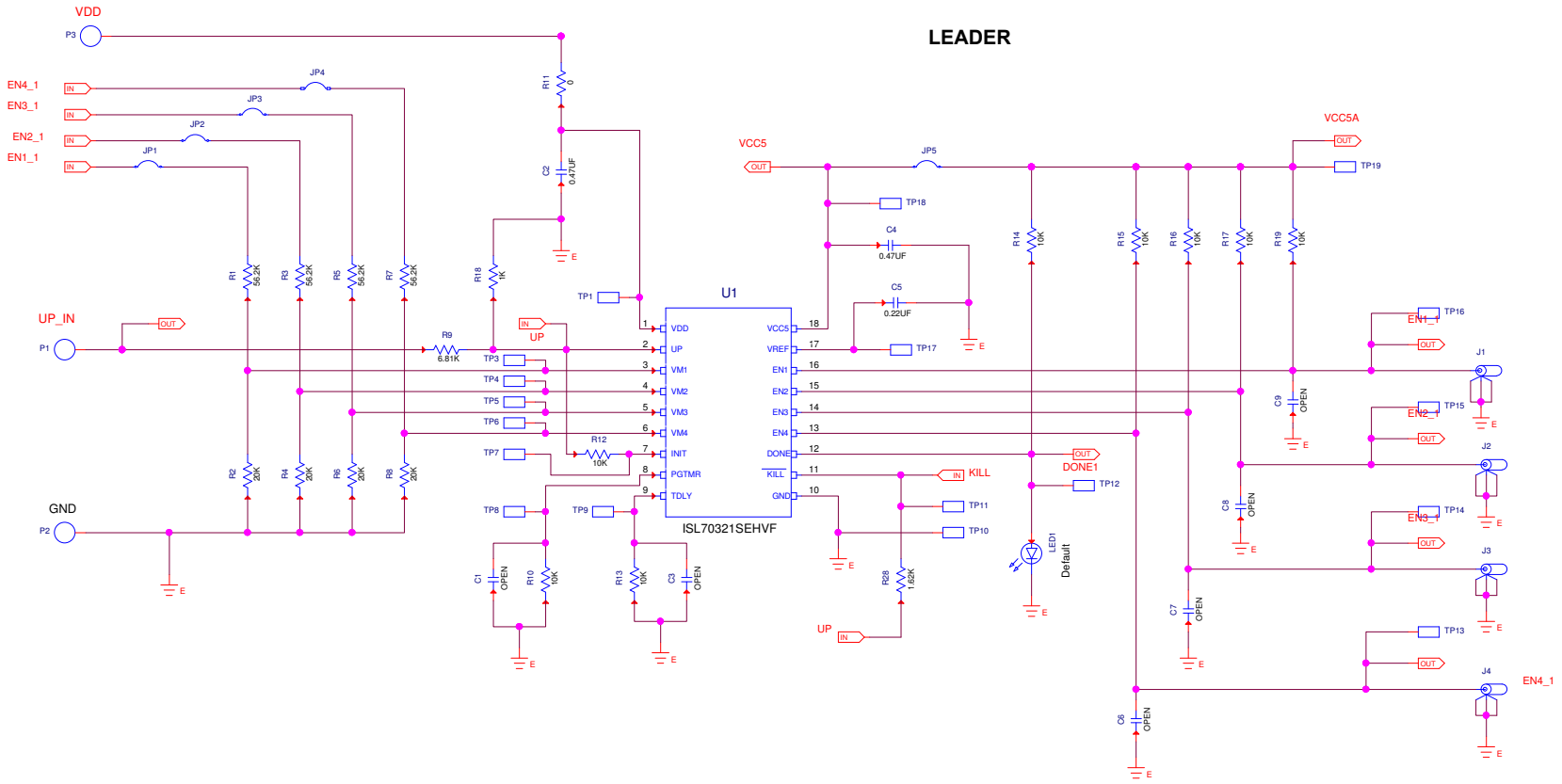


Figure 4. ISL70321SEHEVxZ Schematic - Leader

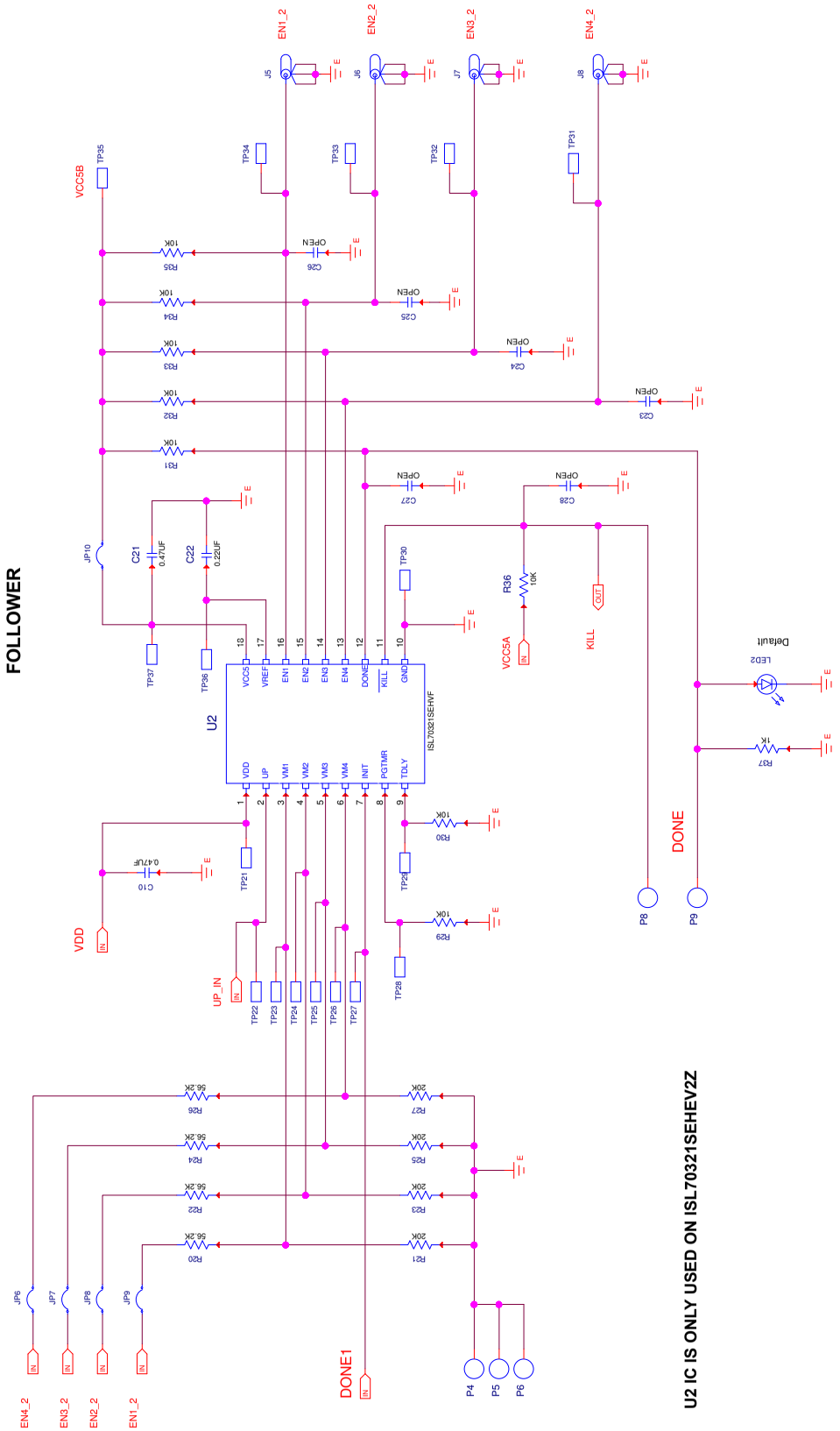


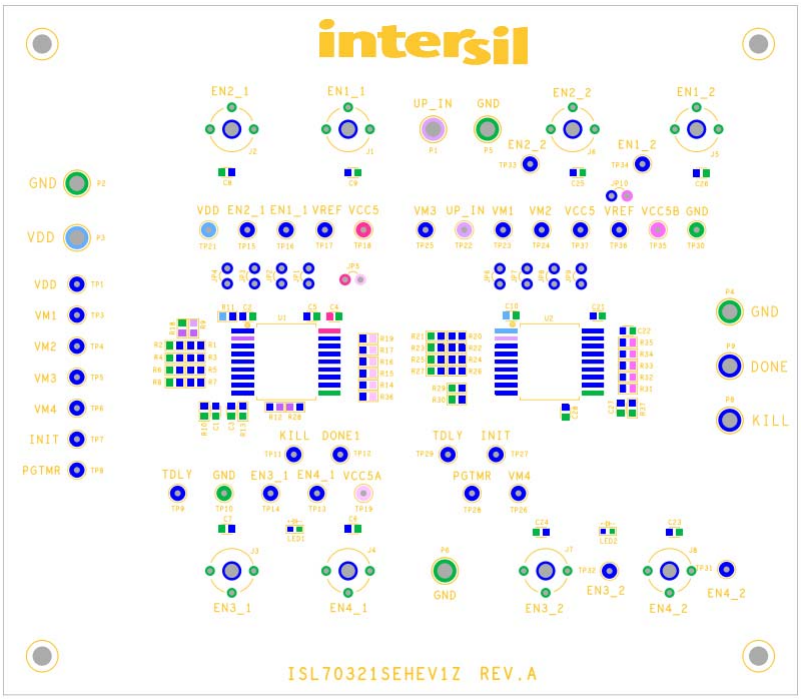
Figure 5. ISL70321SEHEV2Z Schematic - Follower

3.3 Bill of Materials

Item	Qty	Reference Designator	Value	Tol (%)	Rating	PCB Footprint	Manufacturer	Manufacturer Part Number
1	2*	U1, U2*	-	-	-	18 ld Flat Pack	Intersil	ISL70321/PROTO
2	1	R11	0Ω	-	1/10W	0603	GENERIC	GENERIC
3	2	R18, R28, R37	DNP	1	1/10W	0603	GENERIC	GENERIC
4	4	C2, C4, C10, C21	0.47µF	10	16V	0603	TDK	C1608X7R1C474K
5	2	C5, C22	0.22µF	10	10V	0603	GENERIC	GENERIC
6	12	C1, C3, C6-C9, C23-C28	DNP		-	0603	GENERIC	DNP
7	8	R1, R3, R5, R7, R20, R22, R24, R26	27.4kΩ	1	1/10W	0603	GENERIC	GENERIC
8	1	R9	6.81kΩ	1	1/10W	0603	GENERIC	GENERIC
9	16	R10, R12-R17, R19, R29-R36	10kΩ	1	1/10W	0603	GENERIC	GENERIC
10	8	R2, R4, R6, R8, R21, R23, R25, R27	20kΩ	1	1/10W	0603	GENERIC	GENERIC

Note:* U2 only in ISL70321SEHEV2Z Dual Cascaded Evaluation Board

3.4 Board Layout - Two Layers



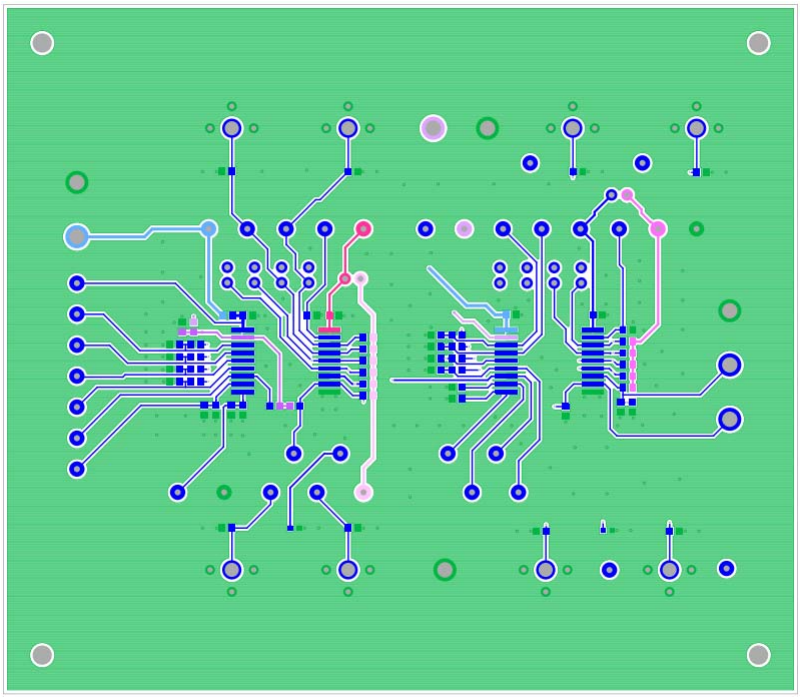


Figure 6. Top Layer (Silkscreen with Top Layer)

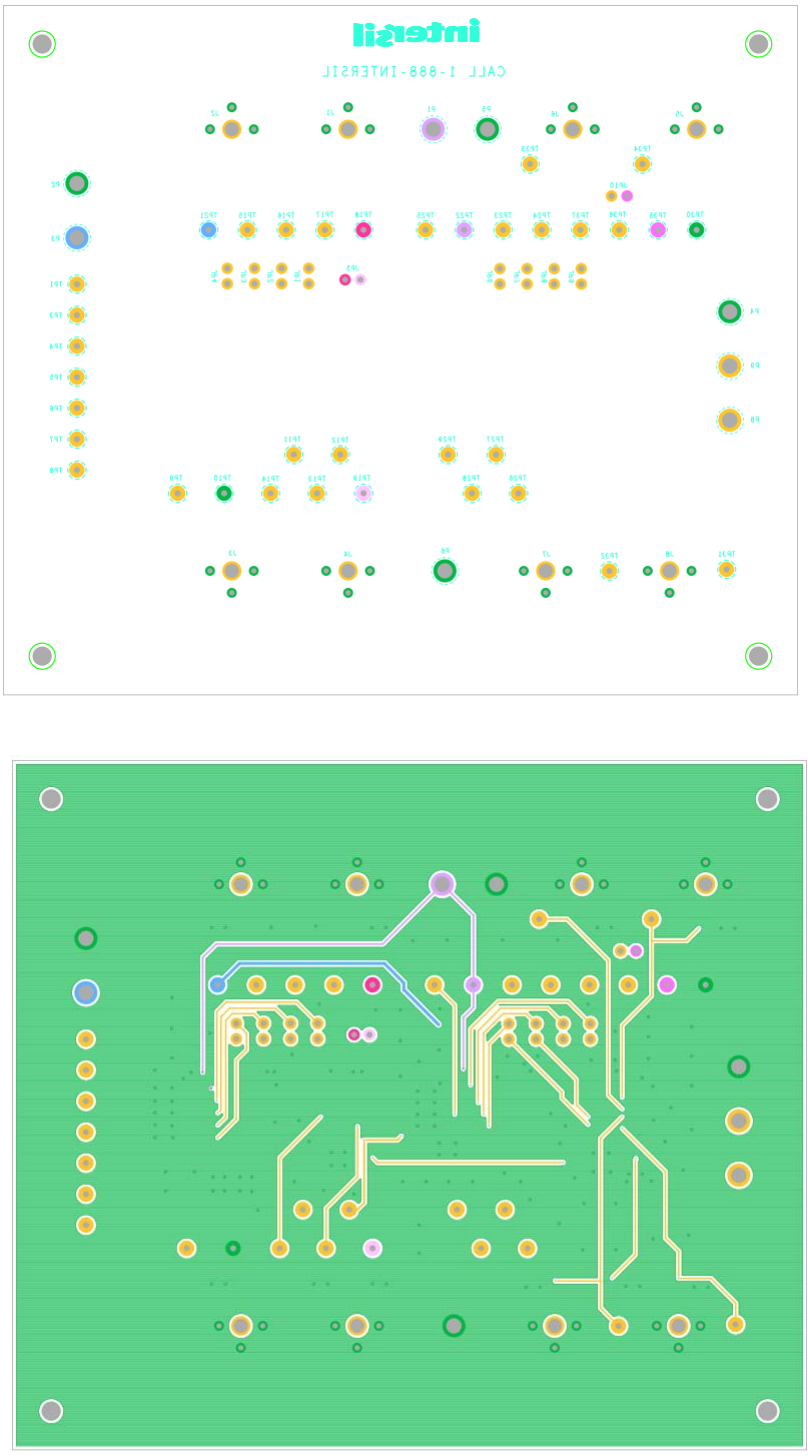


Figure 7. PCB – Bottom Layer (Viewed from Top)

3.5 Typical Performance Curves

Unless noted: V_{IN} = 12V, T_A = +25°C

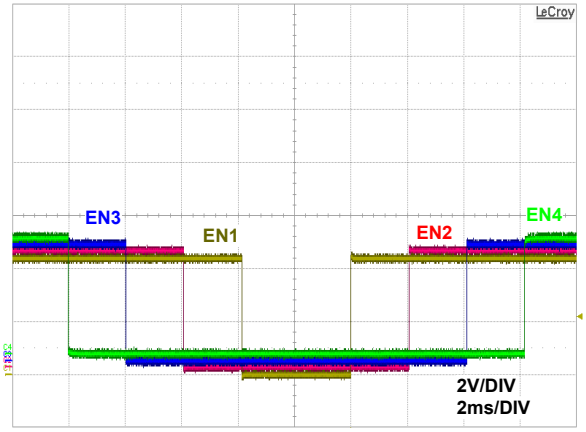


Figure 8. Off and On EN1 - EN4 Sequencing

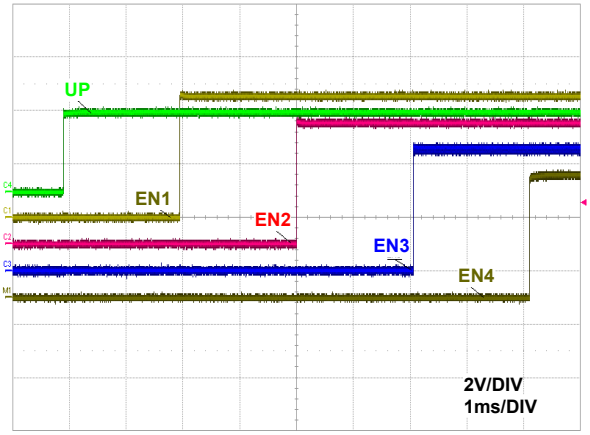


Figure 9. Up to EN1 through EN4, RTDLY = 10kΩ = 2ms

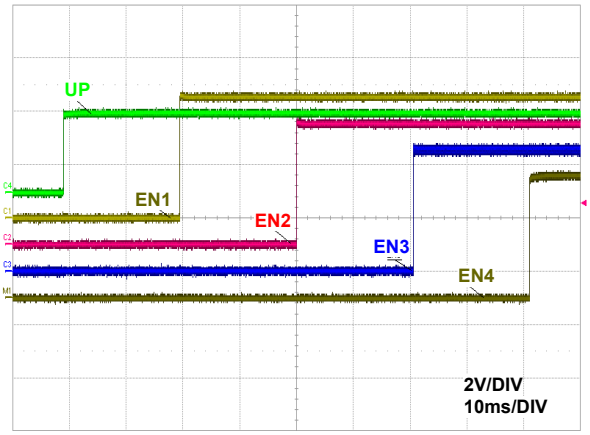


Figure 10. Up to EN1 through EN4, RTDLY = 100kΩ = 20ms

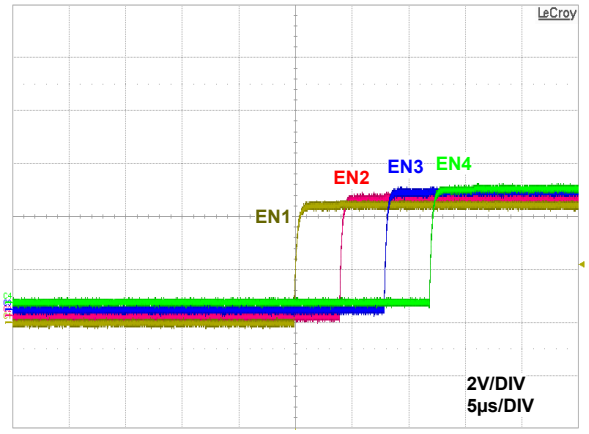


Figure 11. EN1 through EN4, Disabled Delay, TDLY = VCC5

Unless noted: V_{IN} = 12V, T_A = +25°C **(Continued)**

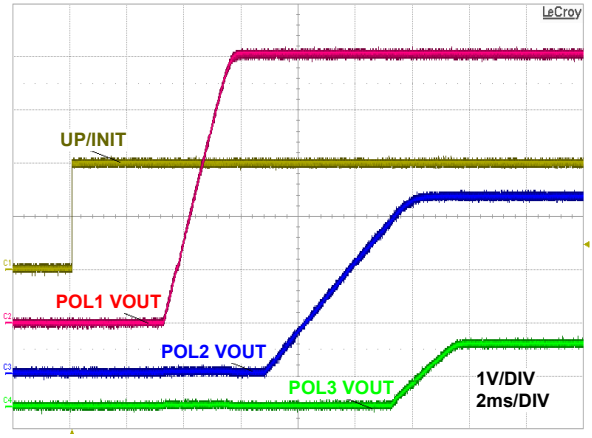


Figure 12. Sequencing On Three POLs, RTDLY = 2ms

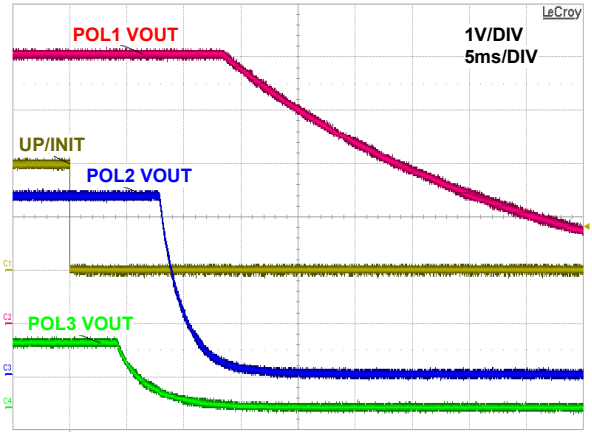


Figure 13. Sequencing Off Three POLs, RTDLY = 2ms

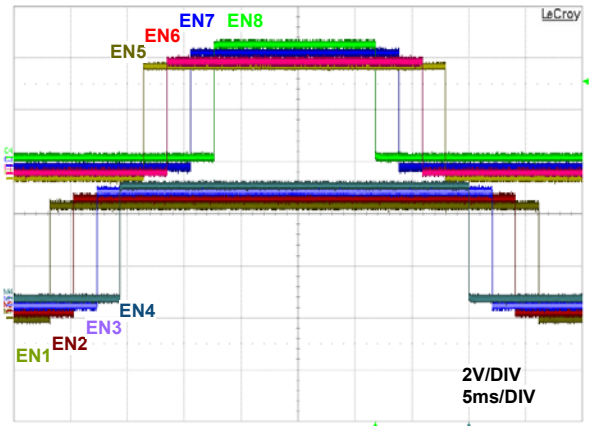


Figure 14. Dual Sequencer On and Off Sequence

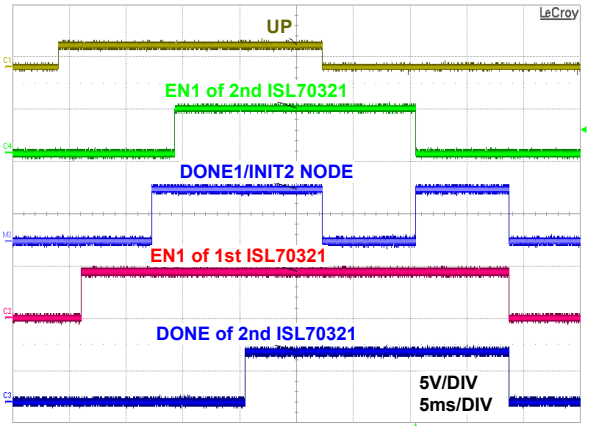


Figure 15. Dual Sequencer Handshake Signals

4. Revision History

Rev.	Date	Description
0.00	Sep 18, 2017	Initial release

ISL70321SEHEVxZ

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