ISL71934MEVAL1Z

Evaluation Board

The ISL71934MEVAL1Z evaluation board provides a quick and easy method for evaluating the ISL71934M, RF SPDT Switch. All aspects of the switch can be exercised on the evaluation board.

Key Features

- Low Insertion Loss: 0.79dB (at 2 GHz)
- High Isolation: 67dB (at 2 GHz)
- Constant Impedance during switching

Specifications

The ISL71934MEVAL1Z is intended to easily test the ISL71934M over all operating parameters.

- Frequency range from 50MHz to 6000MHz
- Supply voltage range: 2.75V to 5.25V
- Control logic range: 1.8V to 3.3V

Ordering Information

Part Number	Description
ISL71934MEVAL1Z	Radiation tolerant SPDT RF switch, ISL71934M, evaluation board

Related Literature

For a full list of related documents, visit our website:

- ISL71934M device page

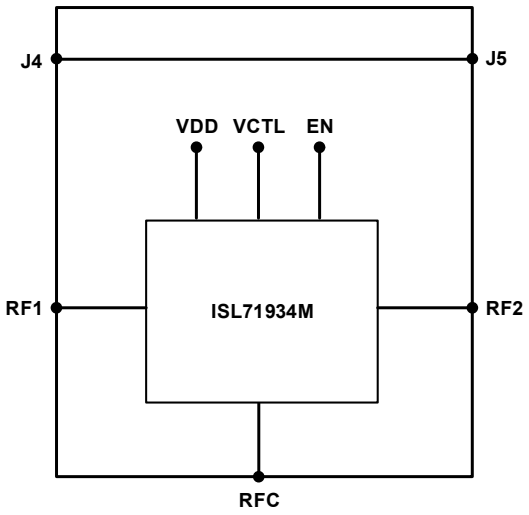

Figure 1. ISL71934MEVAL1Z Block Diagram

1. Functional Description

The ISL71934MEVAL1Z consists of three RF SMA connectors for the RF1, RF2, and RFC signals. The board contains a header for supplying V_{CC}, GND, V_{CTL}, and EN. A through path between J4 and J5 allows for calibration of the PCB board loss. The board does not contain DC blocking capacitors on the RF paths. External blocking capacitors are required if a DC voltage is present on the RF lines. Jumpers allow the V_{CTL} and EN signals to be set to GND or to V_{CC}. If the jumper is inserted, the signal is GND. If the jumper is removed, the signal is pulled high to V_{CC}.

1.1 Operating Range

The ISL71934MEVAL1Z can operate across the ranges listed in Table 1.

Table 1. Operating Range

Parameter	Minimum	Maximum	Unit
Frequency	50	6000	MHz
V_{CC}	2.75[1]	5.25	V
V_{CTL}	1.8	3.3	V
EN	1.8	3.3	V
RF Power		27[2]	dBm

1. When using the on-board voltage divider for the control logic, the minimum V_{CC} is 3.03V.
2. Any State

1.2 Quick Start Guide

1.2.1 External Supply Setup

Set the V_{CC} power supply in a range of 2.75V to 5.25V. Before turning on the supply, ensure that each port is properly terminated.

1.2.2 Logic Control Setup

1.2.2.1 Using the Evaluation Board to Manually Set the Control Logic

1. On connector J6, connect a 2-pin shunt from Pin 3 (V_{CC}) to Pin 4 (V_{LOGIC}). This connection provides the V_{CC} voltage supply to the evaluation board logic control pull-up network. Resistors R5 and R6 form a voltage divider to set the V_{HIGH} level across the 2.7V to 5.25V V_{CC} range for manual logic control.
2. Connector J6 has two logic input pins: EN (Pin 5) and V_{CTL} (Pin 7). See Table 2 for the switch control truth table settings. With the pull-up network enabled (as previously noted) these pins can be left open to provide a logic high through pull-up resistors R3 and R4. To set a logic low for EN and V_{CTL}, connect 2-pin shunts on J6 from Pin 5 (EN) to Pin 6 (GND) and from Pin 7 (V_{CTL}) to Pin 8 (GND).

Table 2. Switch Control Truth Table

VCTL	EN	RFC to RF1	RFC to RF2
0	0	Off	On
1	0	On	Off
0	1	Off	Off
1	1	Off	Off

Note: When using the on-board R5/R6 voltage divider, the current drawn from the V_{CC} supply is higher by approximately V_{CC} /37kΩ.

1.2.2.2 Using External Control Logic

External logic controls are applied to J6 Pin 5 (EN) and Pin 7 (V_{CTL}). See Table 2 for the switch control truth table settings.

1.2.3 Turn-On Procedure

1. Setup the supplies and evaluation board as noted in the External Supply Setup and Logic Control Setup sections.
2. Connect the preset disabled V_{CC} power supply to the red V_{CC} loop and the ground to the GND1 or GND2 point.
3. Enable the V_{CC} supply.
4. Set the required logic setting using J6 Pin 5 (EN) and Pin 7 (V_{CTL}) to achieve the required Table 2 settings.
   Note: The external control logic should not be applied without V_{CC} being present.

1.2.4 Turn-Off Procedure

1. If using an external control logic for EN and V_{CTL}, set them to a logic low.
2. Disable the V_{CC} supply.

1.2.5 De-Embed Insertion Loss

When measuring the s-parameters of the unit, J4 and J5 can be used to de-embed the PCB insertion loss from the measurement.

2. Board Design

2.1 PCB Layout Guidelines

The ISL71934MEVAL1Z follows RF best practices for the layout of the PCB. The RF traces are 50Ω striplines with via transitions to the top of the PCB. The layer below the stripline and the bottom layers are continuous ground planes. An array of vias below the part provide proper RF grounding and a thermal path for heat dissipation.

2.2 ISL71934MEVAL1Z Evaluation Board

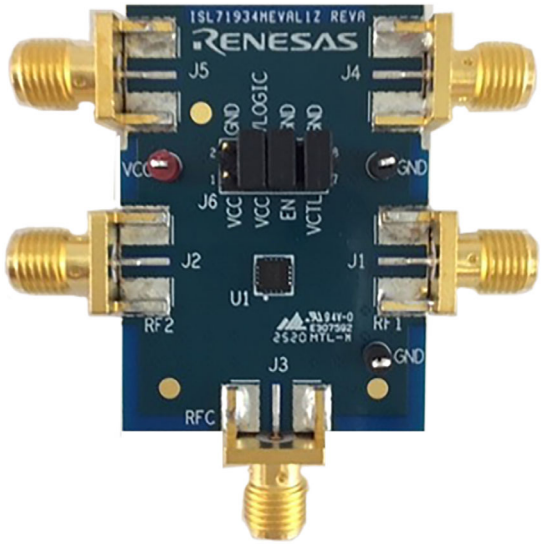

Figure 2. ISL71934MEVAL1Z Evaluation Board (Top)

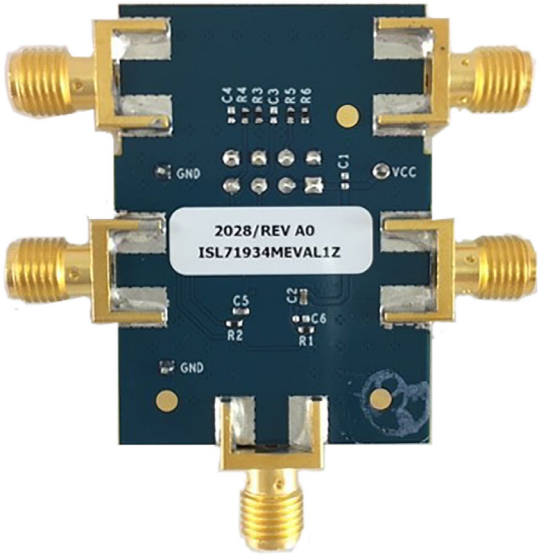

Figure 3. ISL71934MEVAL1Z Evaluation Board (Bottom)

2.3 ISL71934MEVAL1Z Circuit Schematic

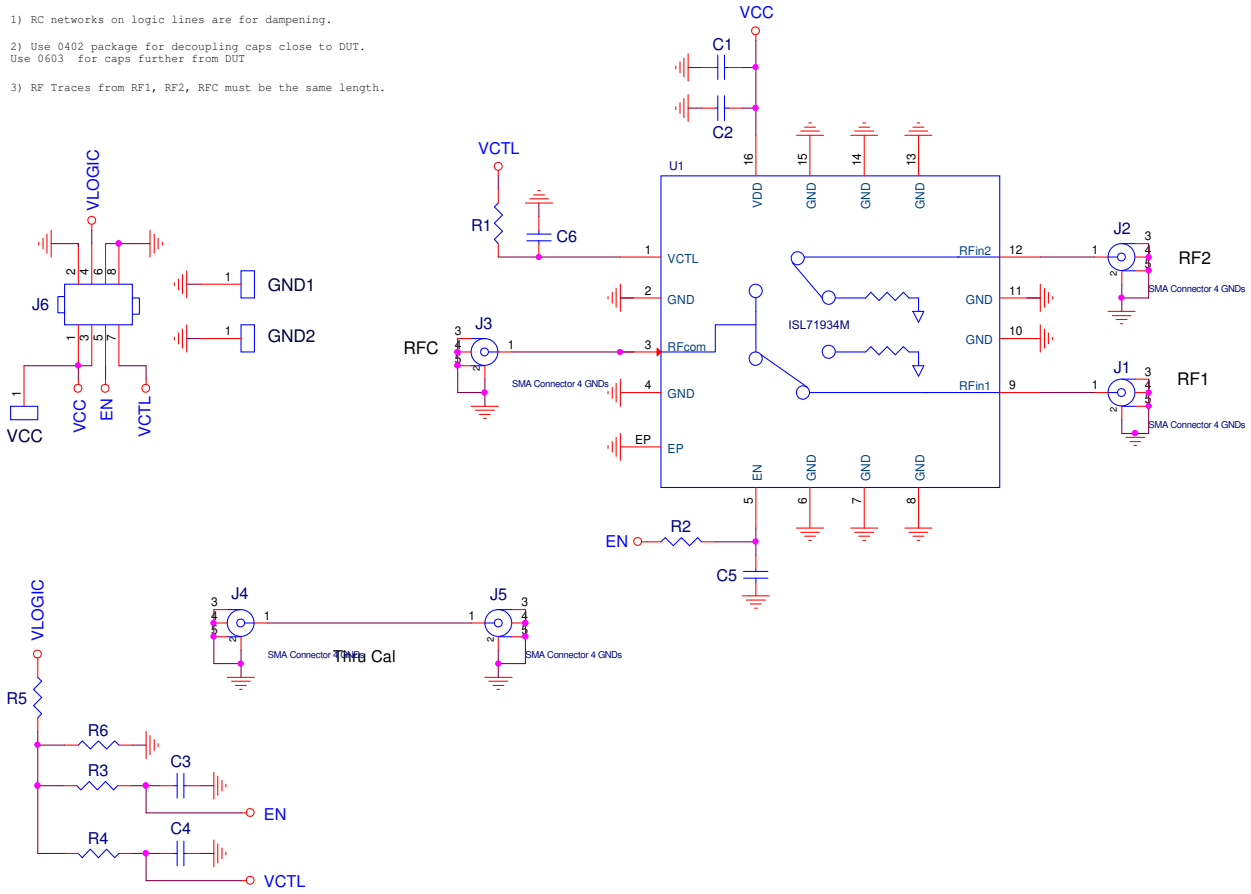

Figure 4. Schematic

2.4 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1		PWB-PCB, ISL71934MEVAL1Z, Rev A, ROHS	Renesas	ISL71934MEVAL1Z
0	C1, C3, C4, C6	Not Installed (0402)		
1	C2	0.1µF ±10%, 16 V, X7R, Ceramic Capacitor (0402)	Murata	GRM155R71C104K
1	C5	100pF ±5%, 50 V, C0G, Ceramic Capacitor (0402)	Murata	GRM1555C1H101J
5	J1, J2, J3, J4, J5	SMA Edge Launch (0.375 inch pitch ground tabs)	Cinch Connectivity	142-0701-851
2	R1, R2	100Ω ±1%, 1/10 W, Resistor (0402)	Panasonic	ERJ-2RKF1000X
2	R3, R4	100kΩ ±1%, 1/10 W, Resistor (0402)	Panasonic	ERJ-2RKF1003X
2	R5	15kΩ ±1%, 1/10 W, Resistor (0402)	Panasonic	ERJ-2RKF1502X
2	R6	22kΩ ±1%, 1/10 W, Resistor (0402)	Panasonic	ERJ-2RKF2202X
2	U1	Radiant Tolerant SPDT RF Switch	Renesas	ISL71934M

2.5 Board Layout

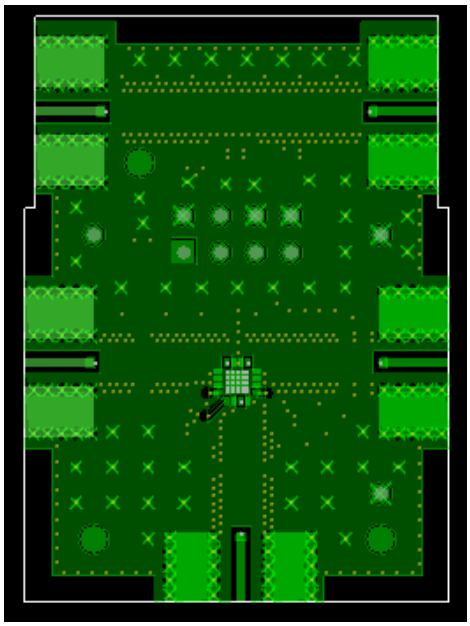

Figure 5. Top Layer

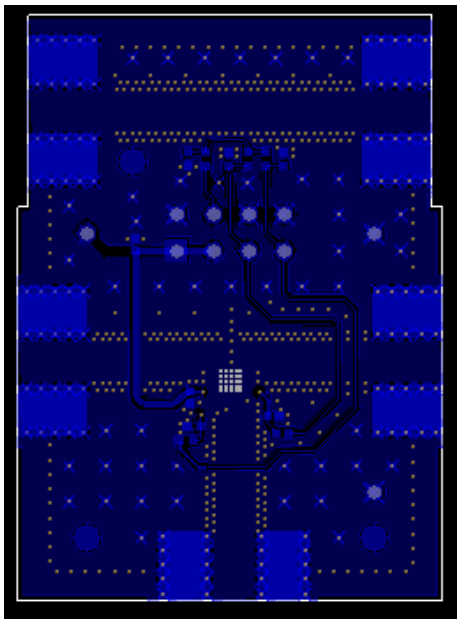

Figure 6. Bottom Layer

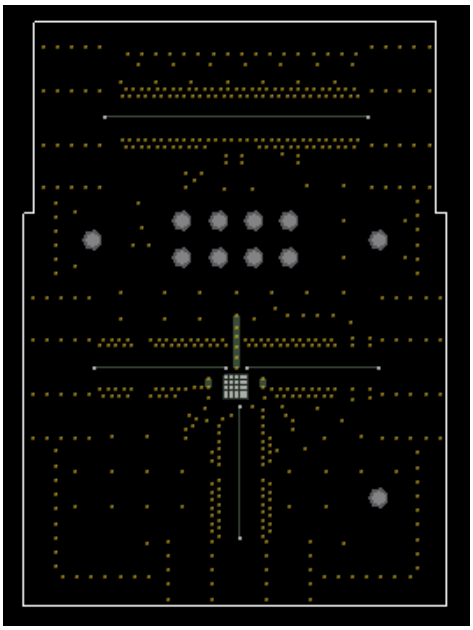

Figure 7. Internal Layer 1

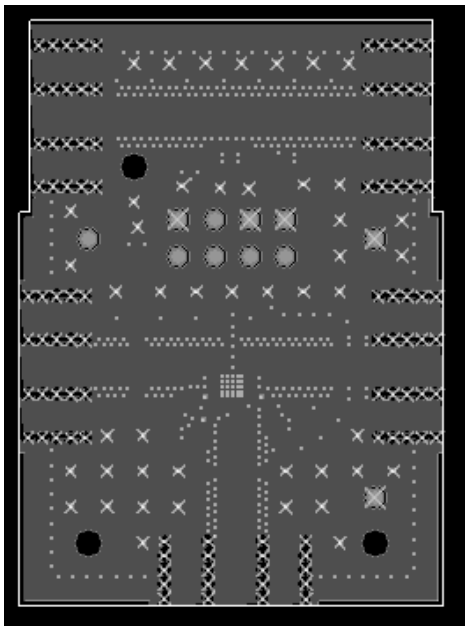

Figure 8. Internal Layer 2

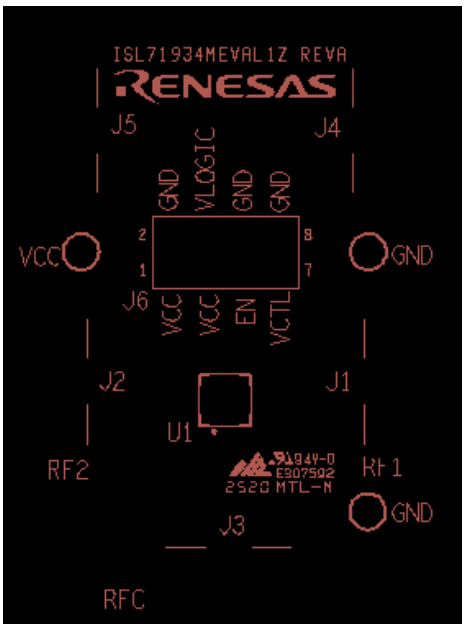

Figure 9. Top Silkscreen

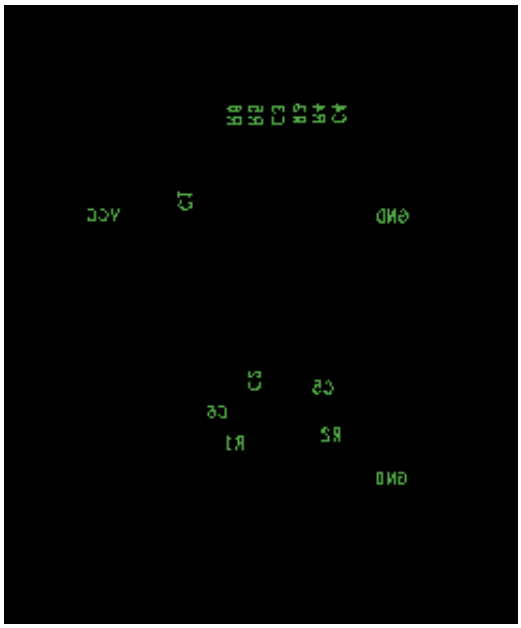

Figure 10. Bottom Silkscreen

3. Typical Performance Curves

Typical: V_{CC} = 5 V, RF1 enabled, T = 25 °C, no de-embedding

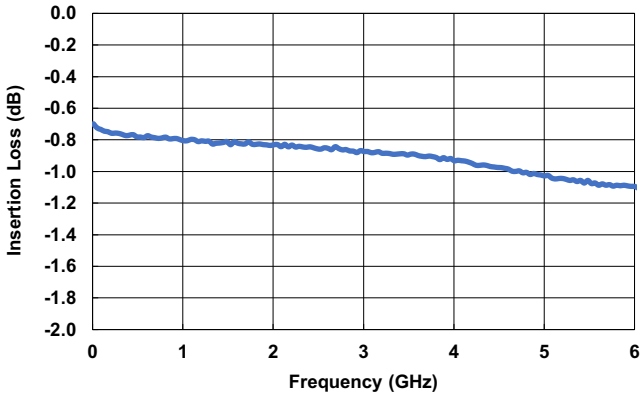

Figure 11. Insertion Loss (typical)

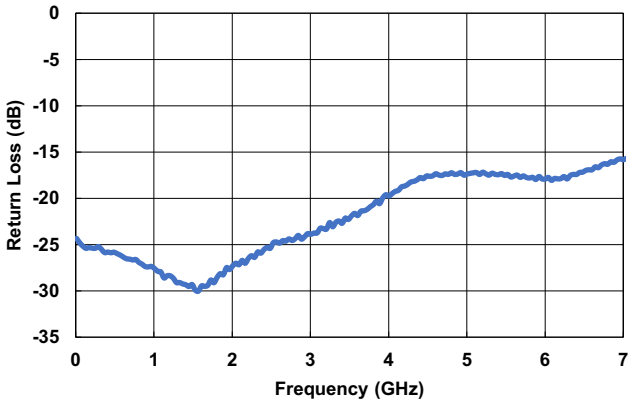

Figure 12. Return Loss RFC (typical)

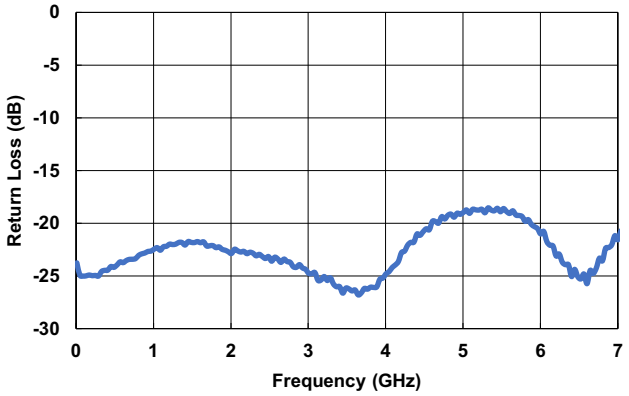

Figure 13. Return Loss RF1 (typical)

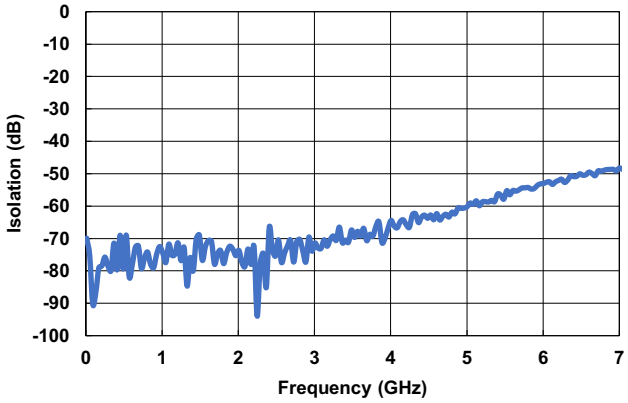

Figure 14. Isolation - RF2 to RFC (typical)

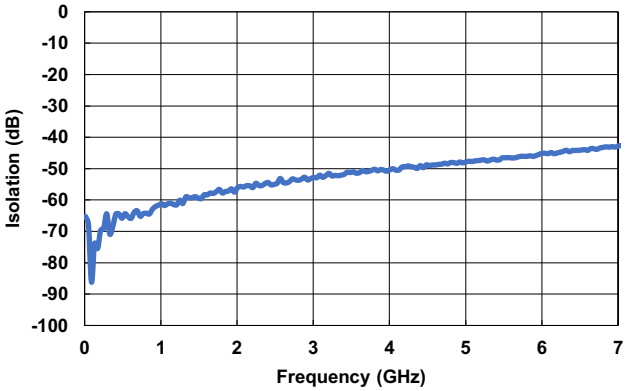

Figure 15. Isolation - RF2 to RF1(typical)

4. Revision History

Rev.	Date	Description
1.0	Feb 11, 2021	Initial release

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(Rev.1.0 Mar 2020)

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