ISL73033SLHEV1Z

Evaluation Board

The ISL73033SLHEV1Z evaluation board evaluates the performance of the ISL73033SLH. The ISL73033SLH is a radiation hardened Driver-GaN Power Stage that integrates a 4.5V gate driver and a 100V, 7.5mΩ enhancement-mode Gallium Nitrade FET (eGaN FET) in a single 8mm x 8mm BGA package. The device simplifies the Printed Circuit Board (PCB) layout by integrating a driver plus GaN FET in one package and is designed for boost and isolated DC/DC converter topologies. The driver operates with a supply voltage from 4.5V to 13.2V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting logic drives with a single device.

The ISL73003SLHEV1Z evaluation board is configured as a common-source open drain 100V current sense load switch with three on board 2512 sized 220mΩ resistors in parallel (73.3mΩ).

Specifications

- Gate Driver Supply Voltage Range: 4.5V to 13.2V
- GaN FET Drain-to-Source Voltage: 100V ($80V_{DC}$ maximum recommended operation)
- Recommended Operating Frequency: Up to 5MHz (limited by Drain-Source rise and fall times)
- Board Dimension: 4cm x 4.5cm
- Board Layers: 4
- Board PCB Copper Weight: 2oz outer; 1oz inner
- Board Revision: A

Ordering Information

Part Number	Description
ISL73033SLHEV1Z	ISL73033SLH evaluation board

Related Literature

For a full list of related documents, visit our website:

- ISL73033SLH device page

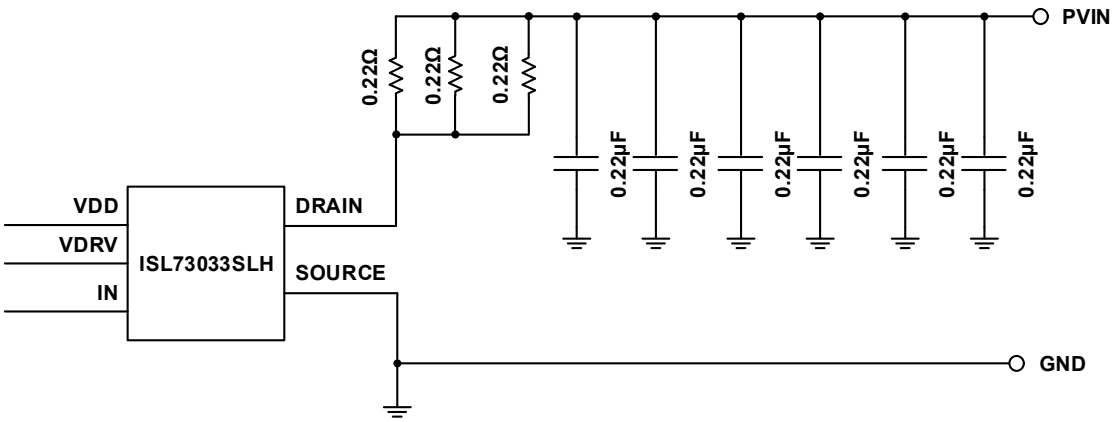

Figure 1. ISL73033SLHEV1Z Block Diagram

Contents

1. Functional Description

The ISL73033SLHEV1Z evaluation board evaluates the performance of the ISL73033SLH. The driver operates with a supply voltage from 4.5V to 13.2V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting logic drives with a single device.

The ISL73003SLHEV1Z evaluation board is configured as a common-source open drain 100V current sense load switch with three on board 2512 sized 220mΩ resistors in parallel (73.3mΩ).

1.1 Quick Start Guide

1. Apply 4.5V to 13.2V across VDD (TP1) and SOURCE (TP2). Check for 4.5V on VDRV (P1).
2. Apply up to 80V across PVIN (BA1) and SOURCE (BA2).
3. Apply a 0V to 5V logic signal on IN (TP3) or INB (TP5). With 0V on IN, the drain of GaN FET is open; with 0V on INB, the drain of GaN FET is shorted to source. With 5V on IN, the drain of GaN FET is shorted to source; with 5V on INB, the drain of GaN FET is open.
   Note: Normally only IN input is used. There is a 0Ω resistor on R_2 that shorts INB to VSS. To use the INB input, depopulate R_2 and place a 0Ω resistor on R_1 to short IN to VDD.
4. When the drain is shorted to source, the only current limiting established from PVIN to SOURCE are the three 0.22Ω 2512 SMD resistors in parallel on R_3 through R_5. Further current limiting may be necessary external to the board.

2. ISL73033SLHEV1Z PCB Guidelines

The ISL73033SLH BGA package ball assignment is placed to allow for a simplified layout and optimizing performance. The following are the layout guidelines for external component placement and Printed Circuit Board (PCB) routing.

- Place a 4.7µF or larger X7R rated ceramic capacitor near the VDD and VSS balls.
- Place a 4.7µF or larger X7R rated ceramic capacitor near the VDRV and SOURCE balls.
- If using a non-inverting configuration, the INB ball is co-located next to the VSS balls for connecting INB to VSS. If using an inverting configuration, the IN ball is co-located next to the VDD ball for connecting IN to VDD.
- For the 100V GaN FET, connect the DRAIN close to the rectifier path to minimize parasitic inductance that may cause ringing or overshoot during switching and potentially exceed the drain-to-source voltage of the GaN FET.

The DRAIN and SOURCE balls are the thermal dissipation path. Allow adequate areas of PCB copper to these balls on the top layer to carry away heat. Renesas also recommends using a conductively filled via underneath the balls to additional PCB layers to help carry heat away from the package.

2.1 Evaluation Board

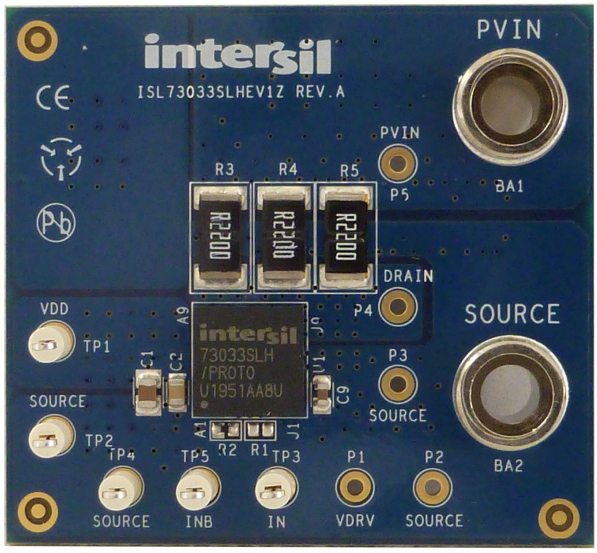

Figure 2. ISL73033SLHEV1Z Evaluation Board (Top)

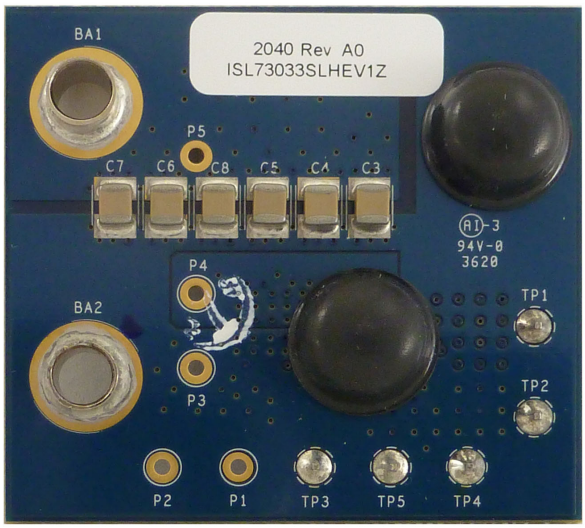

Figure 3. ISL73033SLHEV1Z Evaluation Board (Bottom)

2.2 Circuit Schematic

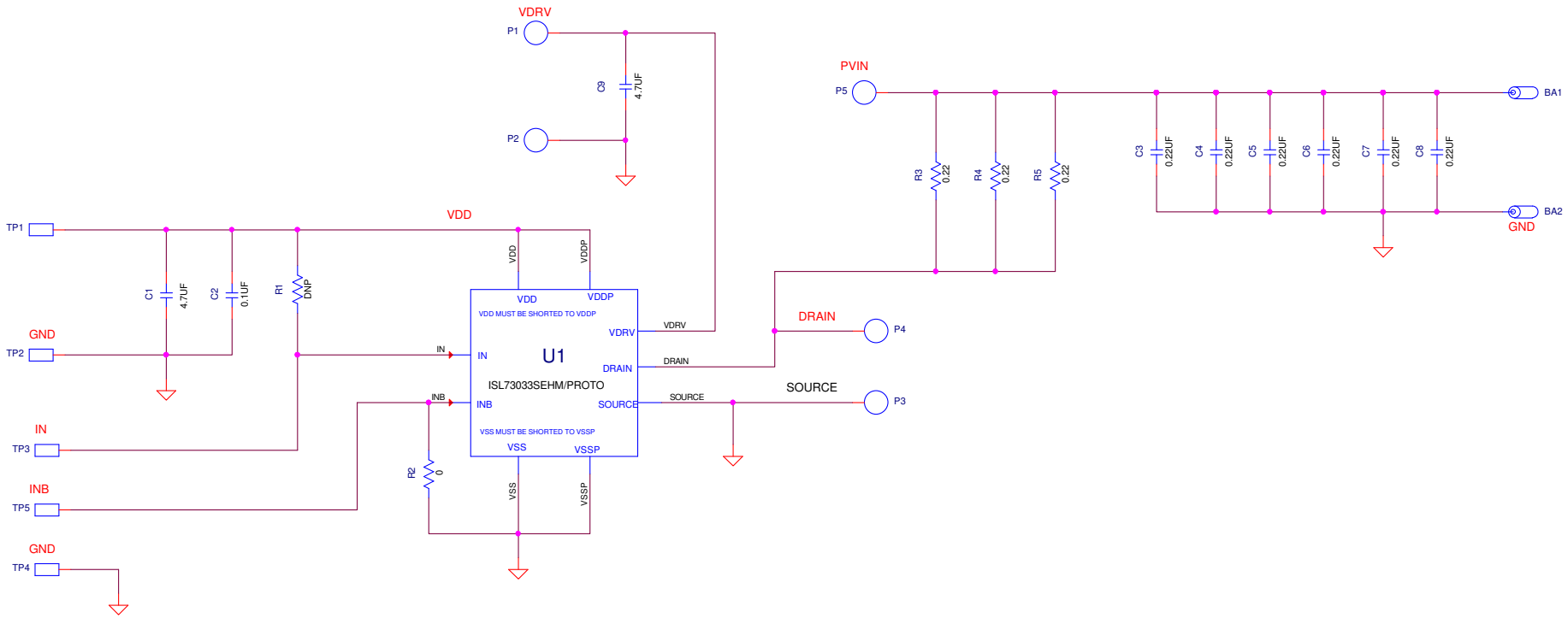

Figure 4. ISL73033SLHEV1Z Circuit Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL73033SLHEV1Z, REVA, ROHS	Imagineering Inc	ISL73033SLHEV1ZREVAPCB
1	C1	CAP-AEC-Q200, SMD, 0805, 4.7µF, 25V, 10%, X7R, ROHS	TDK	CGA4J1X7R1E475K125AC
6	C3, C4, C5, C6, C7, C8	CAP, SMD, 1210, 0.22µF, 250V, 10%, X7R, ROHS	Murata	GRM32DR72E224KW01L
1	C2	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Yageo	CC0603KRX7R8BB104
1	C9	CAP, SMD, 0603, 4.7µF, 10V, 10%, X5R, ROHS	Venkel	C0603X5R100-475KNE
5	TP1, TP2, TP3, TP4, TP5	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
2	BA1, BA2	CONN-JACK,MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS	Keystone	575-4
1	U1	IC-RAD TOLERANT, GaNFET DRIVER COPACK, 81 BALL, 8X8, ROHS	Renesas Electronics	ISL73033SLHMKZ/PROTO
1	R2	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	Venkel	CR0402-16W-00T
0	R1	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS		
3	R3, R4, R5	RES-AEC-Q200, SMD, 2512, 0.22Ω, 3W, 1%, MF, ROHS	Vishay/Dale	WFMB2512R2200FEA
2	Bottom opposite corner ends	BUMPONS, 0.44inWx0.20inH, CYLINDRICAL DOME, BLK, ROHS	3M	SJ-5003 (BLACK)
0	P1-P5	DO NOT POPULATE OR PURCHASE		

2.4 Board Layout

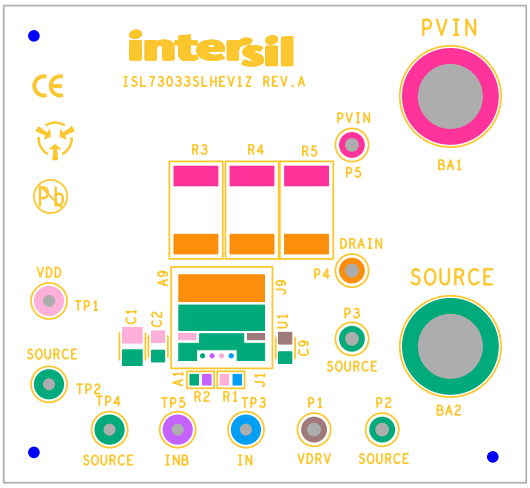

Figure 5. Silkscreen Top

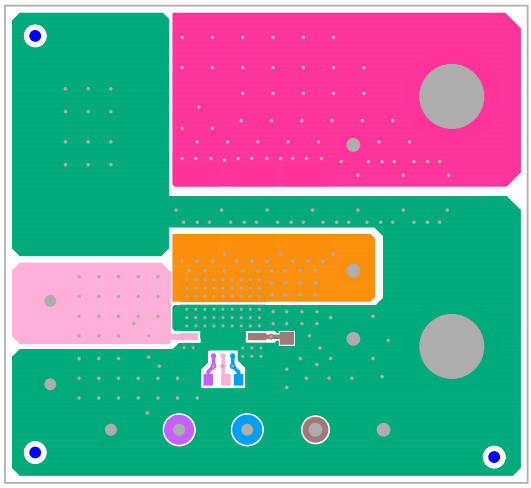

Figure 6. Top Layer

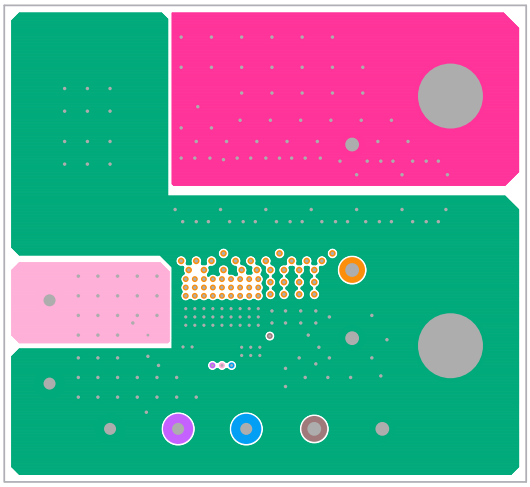

Figure 7. Layer 2

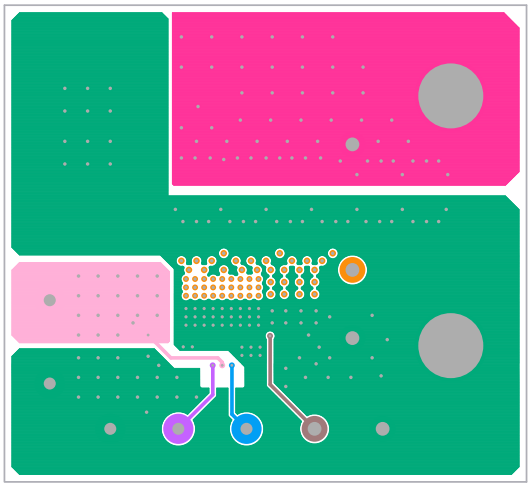

Figure 8. Layer 3

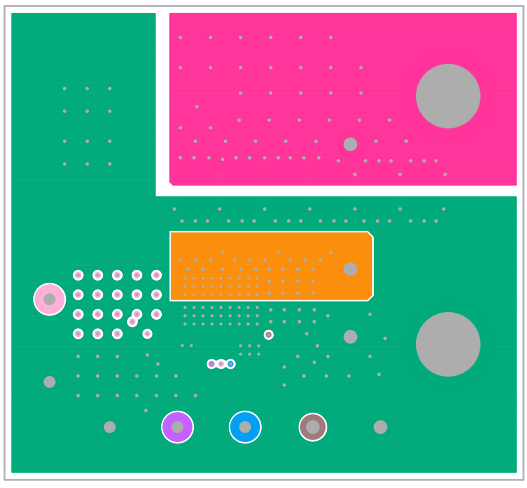

Figure 9. Bottom Layer

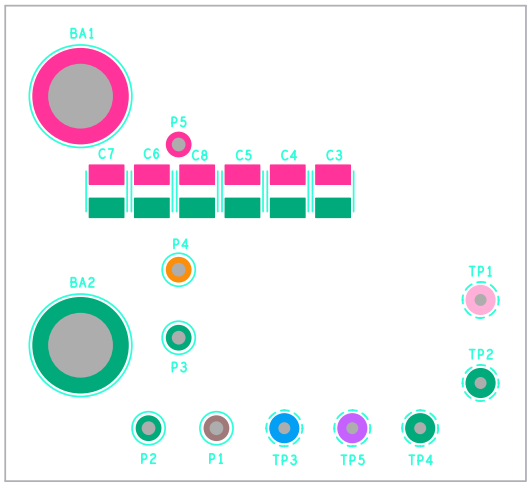

Figure 10. Silkscreen Bottom

3. Typical Performance

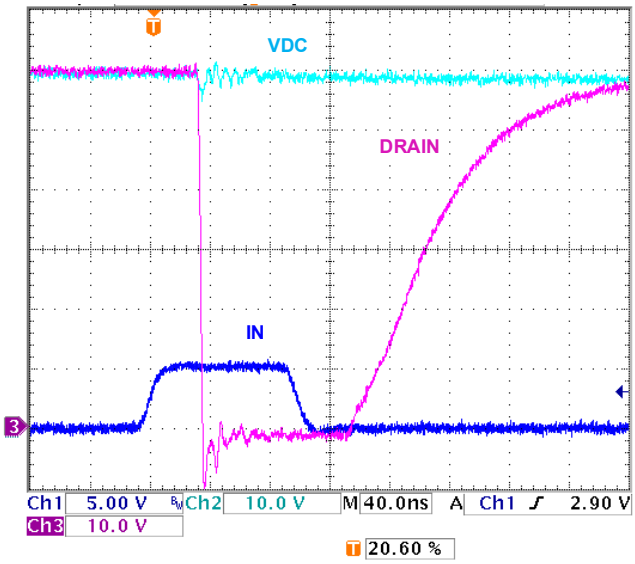

Figure 11. Waveform 1

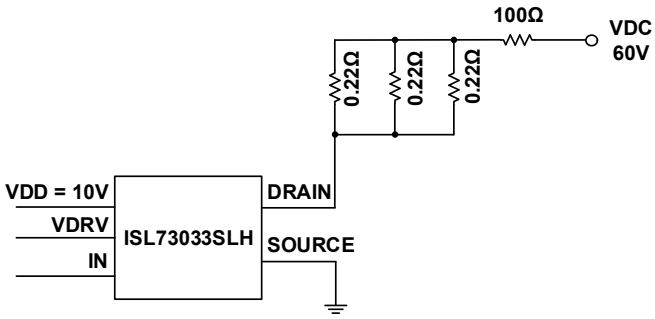

Figure 12. Test Circuit for Waveform 1

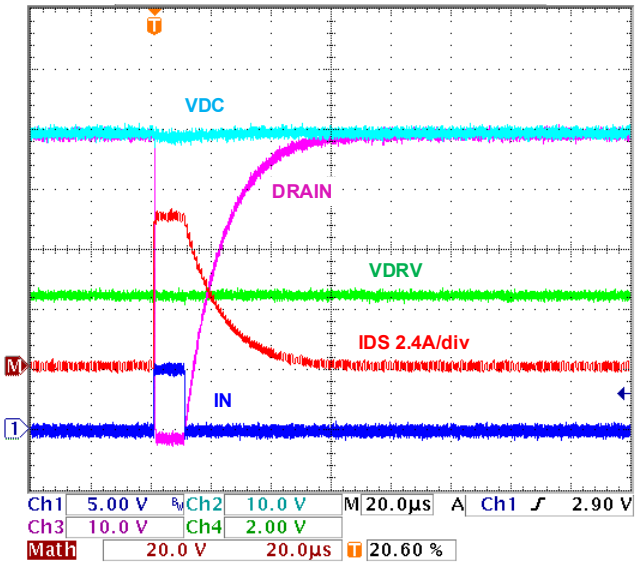

Figure 13. Waveform 2

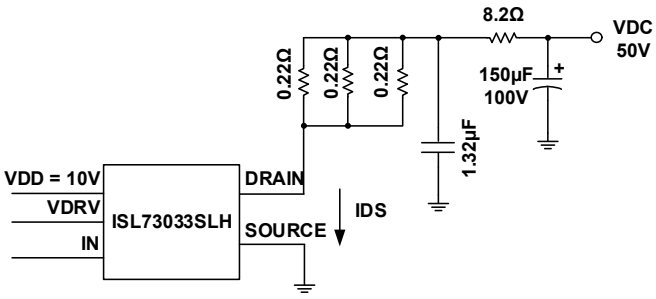

Figure 14. Test Circuit for Waveform 2

4. Revision History

Rev.	Description	Description
1.0	Jan.12.21	Initial release

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