ISL73041SEHEV1Z

The ISL73041SEHEV1Z evaluation board evaluates the performance of the radiation-hardened ISL73041SEH 12V half-bridge GaN FET driver in an open-loop Buck configuration. The ISL73041SEHEV1Z evaluation board includes the GaN FET half-bridge driver, Renesas GaN FETs, and a Buck converter power stage inductor and output capacitors.

For more information about the ISL73041SEH, refer to the *ISL73041SEH Datasheet*.

Features

- 4.75V to 13.2V VDD power supply range
- 300kHz to 1MHz PWM frequency range (external component limited)
- Bridge voltage (V_BUS) range: Up to 13.2V
- 5V max recommended buck output voltage (external component limited)
- Buck output load current up to 25A

Specifications

- Number of layers: 4
- PCB copper weight: 2oz
- Board revision: C

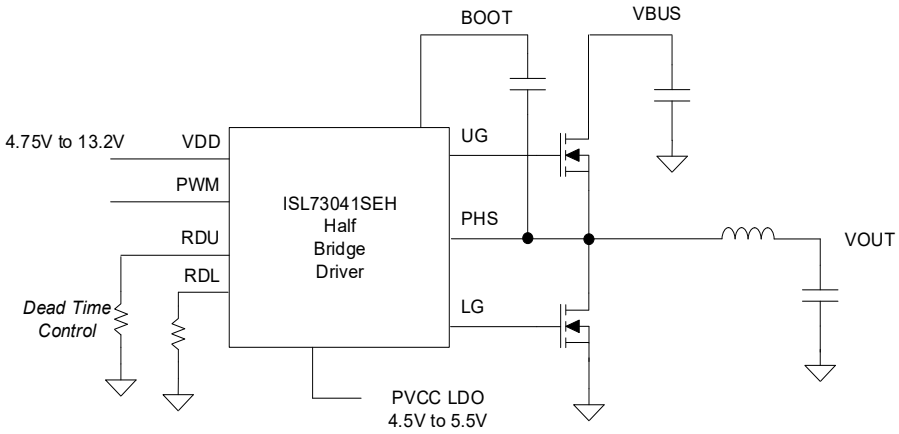

Figure 1. Application Diagram ISL73041SEH Driving GaN FET Half Bridge

Contents

1. Functional Description

1.1 Quick Start Instructions

1. Verify that the following jumpers are installed:
   - JP1 – Install LED indicator for FLTb fault status
   - JP2 – 2-3 position for 2.12kΩ (10ns dead time); DNP for 10kΩ (50ns dead time);
   - JP3 – 2-3 position for 2.12kΩ (10ns dead time); DNP for 10kΩ (50ns dead time)
   - JP4 – Install for FB = PVCC = 4.5V
   - JP5 – 2-3 position for EN = VDD
   - No other jumpers should be populated
2. Apply 4.75V to 13.2V from VDD to GND. Check for voltage on AVCC = 5.0V and PVCC = 4.5V. FLTb LED should be green.
3. Apply 5V to 13.2V from V_BUS to GND.
4. Apply a 0V to 5V, 500kHz signal with a duty cycle of D = ton/Ts to PWM input.
5. Measure voltage at V_OUT. It should be D×V_BUS, where D is the duty cycle of the PWM signal. Renesas recommends keeping V_OUT below 5V.

1.2 Changing Power Inductor

The ISL73041SEHEV1Z is populated with a 0.22µH inductor on the L1 footprint targeted for 500kHz to 1MHz switching frequency. The inductor used is a Coilcraft XAL1010-022. If the user requires using a lower switching frequency and maintaining a similar ripple current, a larger inductance must be used. The L2 footprint is overlaid on L1 and is physically larger to accommodate a larger inductance value with similar saturation current rating.

1.3 Changing Power GaN FETs

The ISL73041SEHEV1Z is configured with a Renesas ISL70020SEH 40V GaN FET for the high side and two ISL70020SEH GaN FET in parallel for the low side, intended for low-duty cycle operation. Renesas also offers 100V and 200V GaN FETs in the same package. The user may change out these GaN FETs depending on their $r_{DS(ON)}$ requirements.

1.4 Changing Programmable Dead Time

The ISL73041SEH driver offers 6.5ns-50ns programmable dead-time for the PWM inputs. Rising edge delays on UG and LG are independently programmable through a resistor on the RDU and RDL pins. See Figure 11 and Figure 12 to help choose the select resistor for the required dead time.

1.5 Changing the GaN FET Gate Drive Voltage

The gate drive voltage for the GaN FETs is set by the PVCC LDO internal to the ISL73041SEH. The PVCC LDO has a programmable range of 4.5V to 5.5V with the option to short the FB pin to PVCC to set PVCC = 4.5V using internal resistor dividers. If the user requires a different PVCC voltage, set the external feedback resistors using Equation 1. For the GaN FETs, Renesas recommends keeping the PVCC gate drive voltage to 4.5V.

(EQ. 1) $$PVCC = 1.2V \times \left(\frac{R12}{R13} + 1\right)$$

2. Board Design

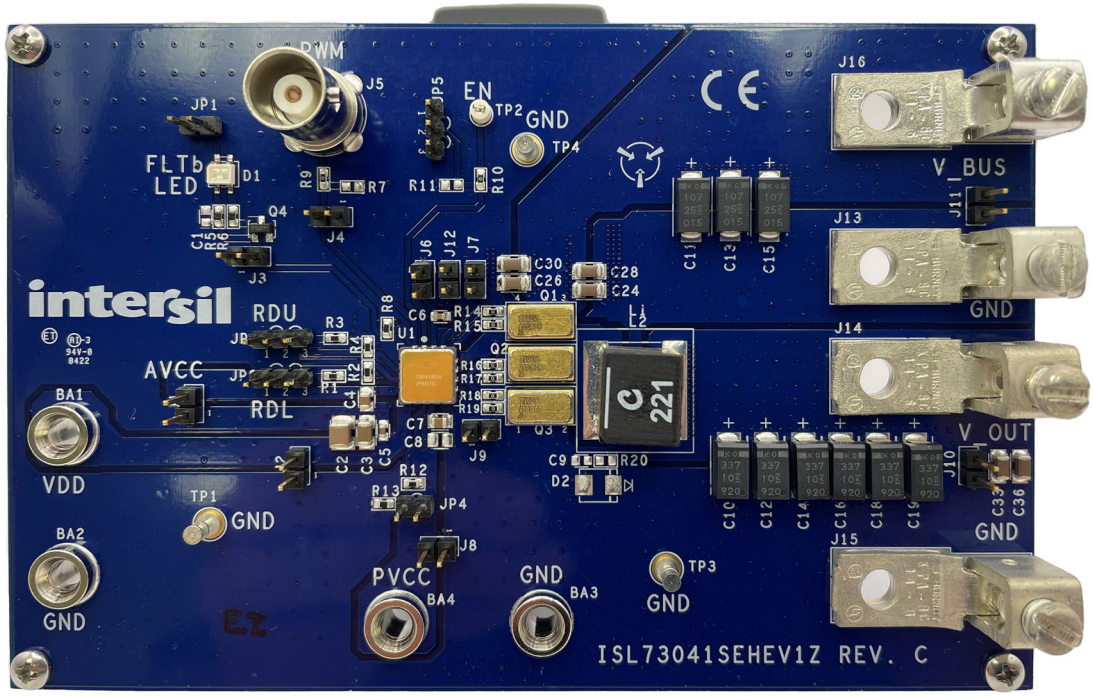

Figure 2. Evaluation Board (Top)

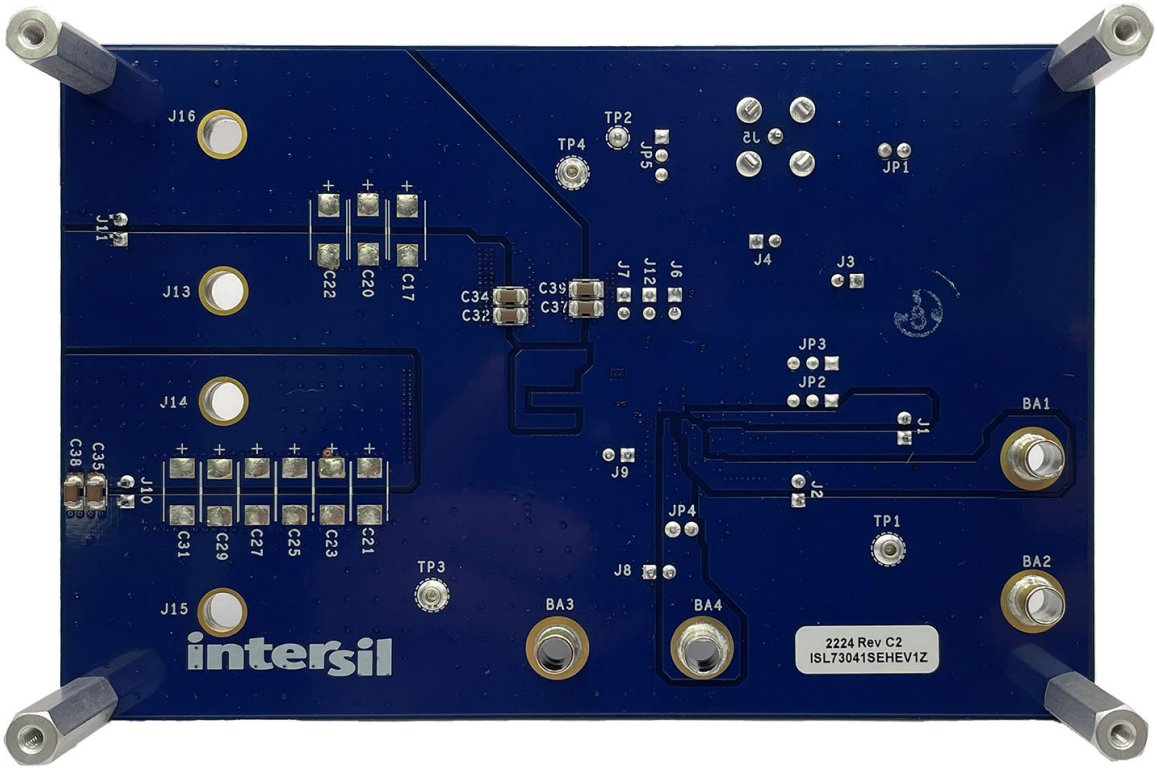

Figure 3. Evaluation Board (Bottom)

2.1 Layout Guidelines

PCB design files are available on the website to study or incorporate into your design.

- Use a multi-layer PCB with 2-ounce (70µm) copper outer layers to maximize PCB current capacitor and thermal handling.
- Place low ESR X7R grade or better ceramic capacitors for high-frequency decoupling as close to the package pins as possible. These include the capacitors between VDD-SGND, AVCC-SGND, PVCC-PGND, and BOOT-PHS.
- Place the RDU and RDL dead-time control resistors close to their respective pins and connect them to SGND through the PCB GND plane.
- Connect the PGND pin and four bottom EPADs of the package to the top layer GND plane of the PCB. To further improve thermal performance, place at least four vias in the GND plane under the package EPAD to another internal GND plane to dissipate heat.
- Place the ISL73041SEH as close as possible to the half-bridge power GaN FET to minimize trace inductance and high current loop area between driver output and GaN FET gate.
- The PGND pin and low-side FET source should be connected commonly through the PCB GND plane. Route the PHS pin to the switch node of the half-bridge power stage with a short and wide trace to minimize inductance and loop area.
- For the low-side drive, the PVCC capacitor, PVCC and PGND pins, low-side driver gate outputs, low-side FET gate, and GND plane form a current loop during FET turn on and turn off. For the high-side drive, the bootstrap capacitor, BOOT and PHS pins, high-side driver gate outputs, high-side FET gate, and switch node form a current loop during FET turn on and turn off. Keep these loops short, wide, and avoid overlapping with other sensitive signals.
- Size the phase node of the half-bridge (high-side FET source and low-side FET drain) area to handle the current and thermal dissipation from the FETs and switching load. The phase node copper area usually ends up being a significantly large shape. In addition, the phase node is where high voltage and high dv/dt switching occurs. In general, there are two layout practices for handling the phase node. One recommendation is to remove any conductors (including ground) that overlap the phase node on the adjacent layer of the PCB. The other recommendation is to repeat the phase node shape on every layer of the PCB. Both methods minimize the capacitive coupling of noise into the GND plane and prevent any sensitive analog signals from being routed underneath the phase node and causing unintentional common mode noise.

2.2 Schematic Diagram

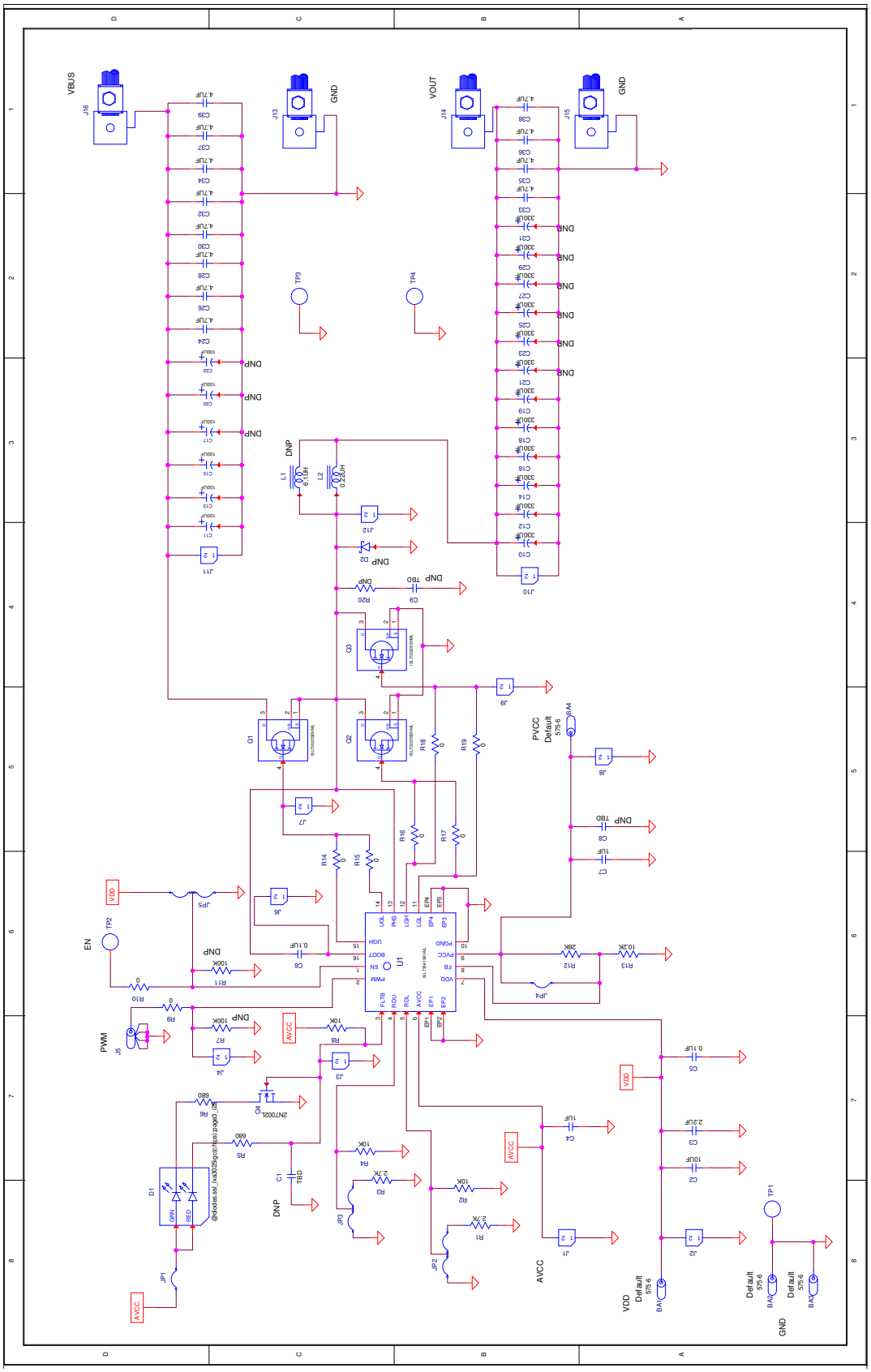

Figure 4. ISL73041SEHEV1Z Board Schematics

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL73041SEHEV1Z, REVC, ROHS	Imagineering Inc	ISL73041SEHEV1ZREVCPCB
2	C4, C7	CAP, SMD, 0805, 1.0µF, 25V, 10%, X7R, ROHS	TDK	C2012X7R1E105K
12	C24, C26, C28, C30, C32-C39	CAP, SMD, 1206, 4.7µF, 25V, 10%, X7R, ROHS	TDK	C3216X7R1E475K
1	C2	CAP, SMD, 1210, 10µF, 25V, 10%, X7R, ROHS	TDK	C3225X7R1E106K
1	C3	CAP, SMD, 1206, 2.2µF, 50V, 10%, X7R, ROHS	Murata	GRM31CR71H225KA88L
1	C6	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	Murata	GCM188R71C104KA37D
1	C5	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Yageo	CC0603KRX7R8BB104
0	C1, C9	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
0	C8	CAP, SMD, 0805, DNP-PLACE HOLDER, ROHS		
3	C11, C13, C15	CAP-TANT, SMD, 7.3×4.3mm, 100µF, 25V, 20%, 40mΩ at 100MHz, ROHS	Kemet	T521D107M025ATE040
6	C10, C12, C14, C16, C18, C19	CAP-TANT, SMD, 7.3×4.3×4, 330µF, 10V, 20%, 5mΩ, TIN, ROHS	Kemet	T530X337M010ATE005
1	L2	COIL-PWR INDUCT, AEC-Q200, SMD, 11.3×10mm, 0.22µH, 20%, 98.8A, ROHS	Coilcraft	XAL1010-221MEB
3	TP1, TP3, TP4	CONN-DBL TURRET, TH, 0.218x0.109 PCB MNT, TIN/BRASS, ROHS	Keystone	1502-2
1	J5	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
1	TP2	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
4	BA1-BA4	CONN-JACK, MINI BANANA, SDRLESS, NICKEL/BRASS, 0.175 PLUG, ROHS	Keystone	575-6
3	JP2, JP3, JP5	CONN-HEADER, 1×3, BREAKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
2	JP1, JP4	CONN-HEADER, 1×2, RETENTIVE, 2.54mm, 0.230×0.120, RoHS	BERG/FCI	69190-202HLF
11	J1, J2, J3, J4, J6, J7, J8, J9, J10, J11, J12	CONN-HEADER, TH, 2×1, BRKAWY, 0.100inCENTER, 0.230×0.200in, ROHS	Samtec	TSW-102-08-F-S
1	D1	LED, SMD, 3×2.5mm, 4P, RED/GREEN, 12/20MCD, 2V	Lumex	SSL-LXA3025IGC-TR
3	Q1-Q3	IC-PROTO, RAD HARD, 40V GAN FET, 4P, CLCC, ROHS	Renesas Electronics America	ISL70020SEHL/PROTO
1	U1	IC-RAD LIGHT GaN FET, HALF BRIDGE DRIVER, 14P, CLCC, ROHS	Renesas Electronics America	ISL73041SEHL/PROTO
1	Q4	TRANSISTOR-MOS, N-CHANNEL, SMD, SOT23, 60V, 115mA, ROHS	On Semiconductor	2N7002LT1G
2	R5, R6	RES-AEC-Q200, SMD, 0603, 680Ω, 1/10W, 1%, TF, ROHS	Vishay/Dale	CRCW0603680RFKEA
0	R20	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		
8	R9, R10, R14-R19	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
3	R2, R4, R8	RES, SMD, 0603, 10K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
1	R13	RES, SMD, 0603, 10.2K, 1/10W, 1%, TF, ROHS	Yageo	9C06031A1022FKHFT
2	R1, R3	RES, SMD, 0603, 2.7K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2701FT
1	R12	RES, SMD, 0603, 28K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2802FT
0	R7, R11	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
4	Four corners	SCREW, 4-40X1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	BUILDING FASTENERS	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
4	J13-J16	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS	BERG/FCI	KPA8CTP
1	Place assy in bag	BAG, STATIC, 6X8, ZIPLOC, ROHS	Uline	S-2262
0	C17, C20, C22 (T521D107M025ATE040)	DO NOT POPULATE OR PURCHASE		

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
0	C21, C23, C25, C27, C29, C31	DO NOT POPULATE OR PURCHASE		
0	D2 (B120B)	DO NOT POPULATE OR PURCHASE		
0	L1 (XAL1580-612MEB)	DO NOT POPULATE OR PURCHASE		

2.4 Board Layout

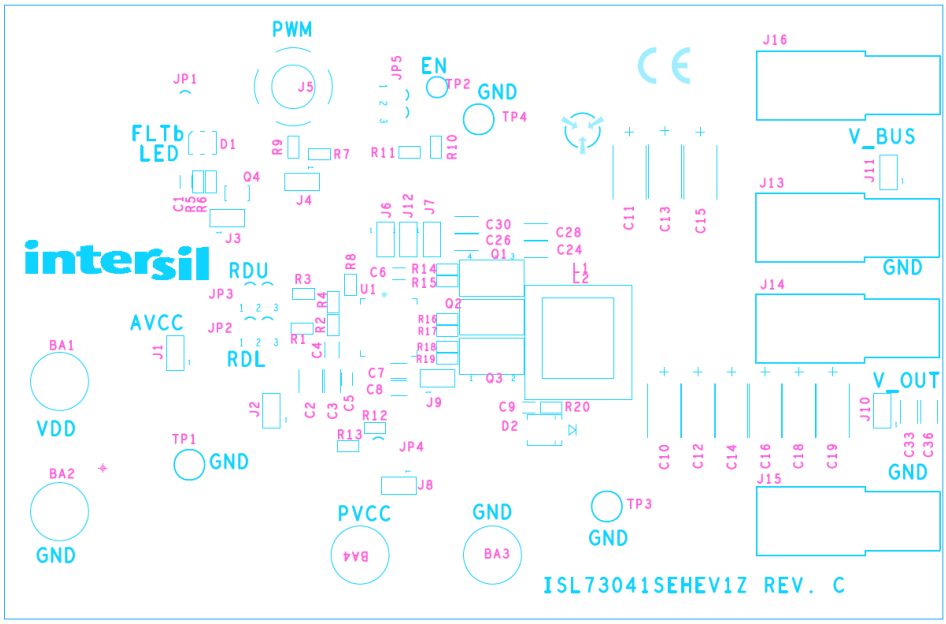

Figure 5. ISL73041SEHEV1Z Top Assembly Layer

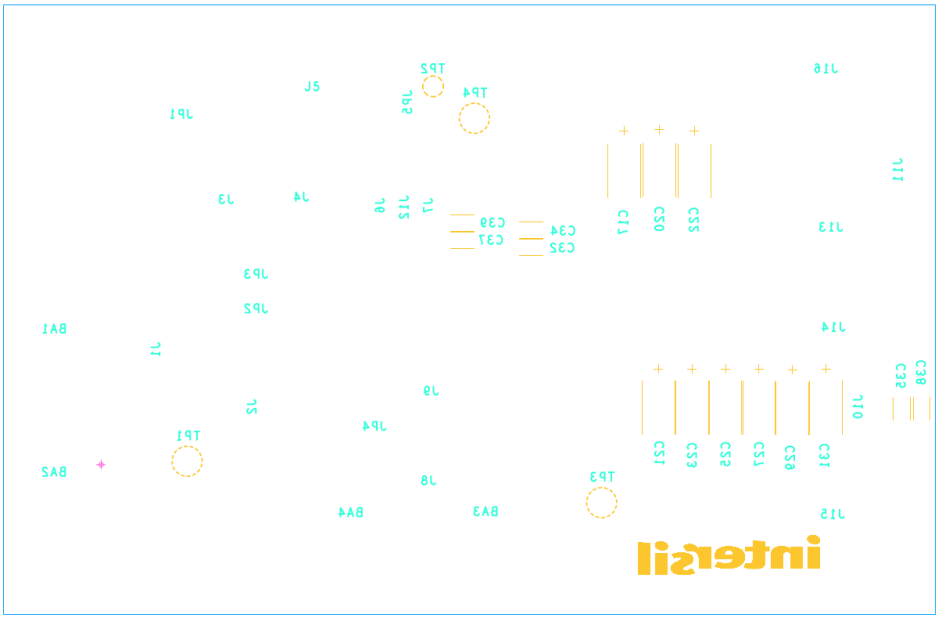

Figure 6. ISL73041SEHEV1Z Bottom Assembly Layer

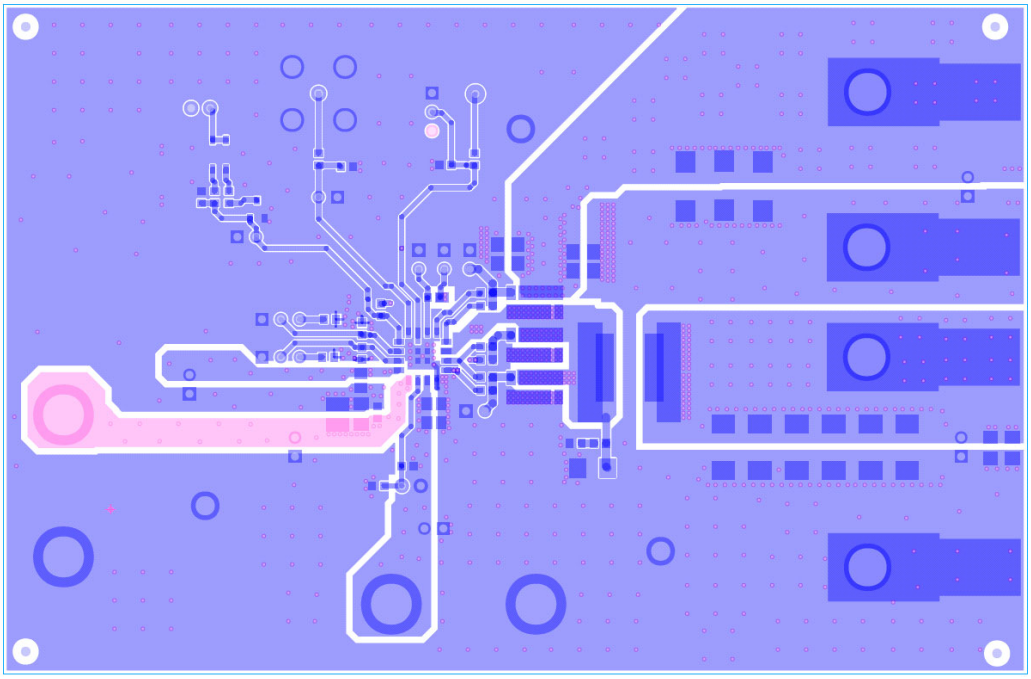

Figure 7. ISL73041SEHEV1Z Layer 1

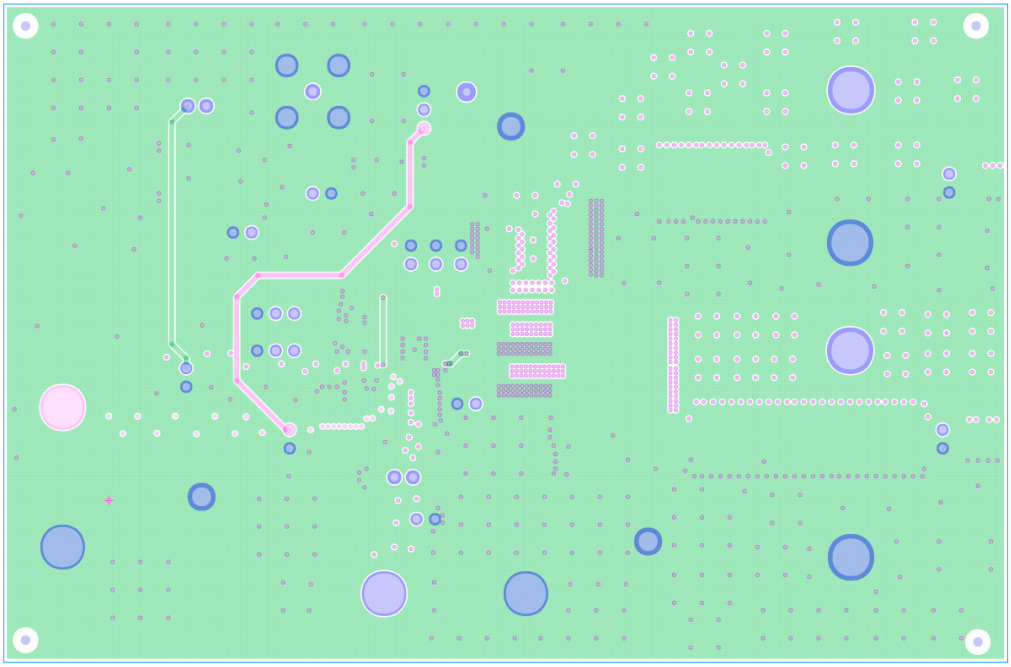

Figure 8. ISL73041SEHEV1Z Layer 2

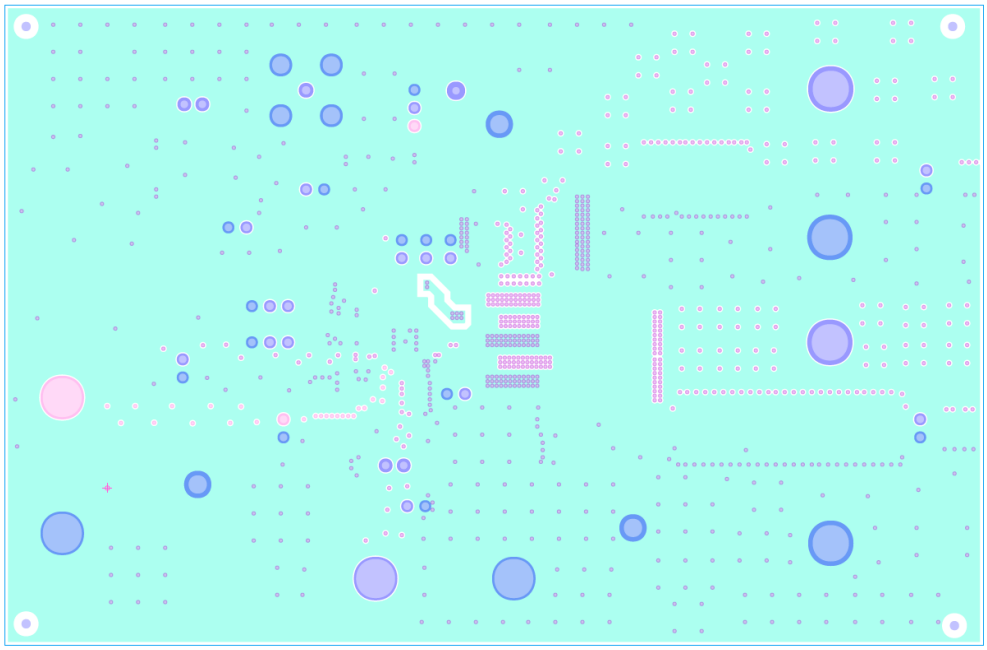

Figure 9. ISL73041SEHEV1Z Layer 3

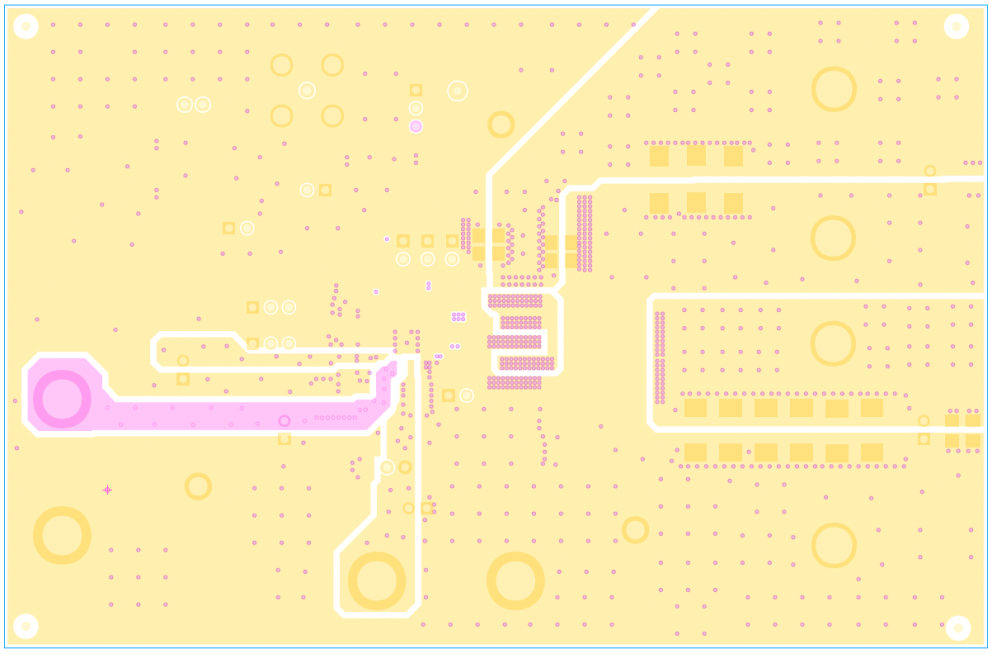

Figure 10. ISL73041SEHEV1Z Layer 4

3. Typical Performance Curves

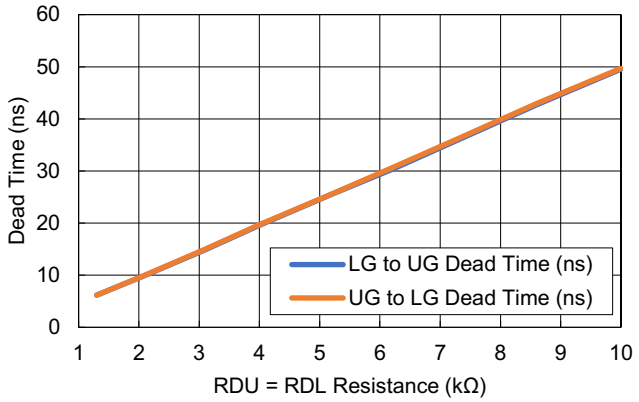

Figure 11. Dead Time vs Resistance; 1.3kΩ-10kΩ

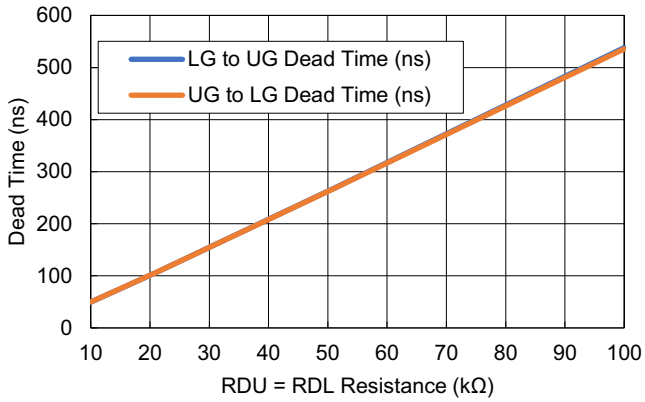

Figure 12. Dead Time vs Resistance; 10kΩ-100kΩ

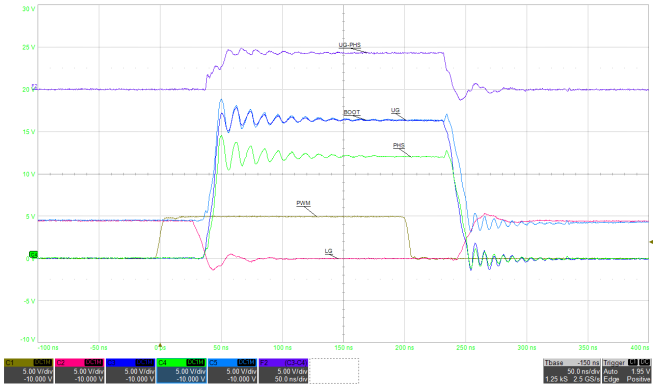

Figure 13. Half Bridge Switching Waveforms; I_LOAD = 0A

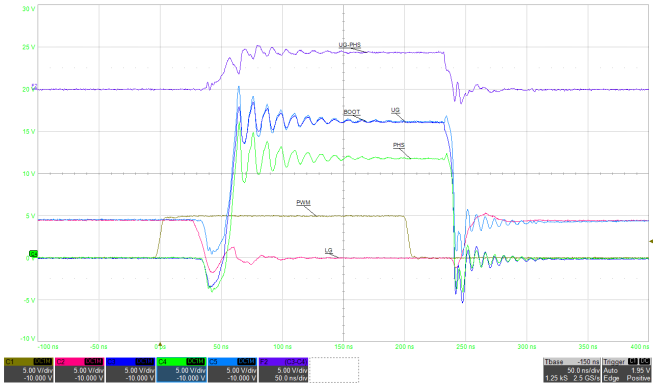

Figure 14. Half Bridge Switching Waveforms; I_LOAD = 20A

4. Ordering Information

Part Number	Description
ISL73041SEHEV1Z	ISL73041SEH 12V GaN Half Bridge Driver Evaluation Board

5. Revision History

Revision	Date	Description
1.01	Jun 21, 2023	Updated the Quick Start Instructions section. Updated the Changing Programmable Dead Time section. Updated Figure 11 title.
1.00	Feb 9, 2023	Initial release

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