ISL74420MEV1Z

The ISL74420MEV1Z Radiation Tolerant Quad Clock Fanout IC evaluation board (shown in Figure 3) features the ISL74420M Plastic version of the device.

The ISL74420MEV1Z provides users with mechanical switches for configuration. This eases user experimentation of frequency and delay selections and other configuration options.

The ISL74420MEV1Z is functionally similar to another evaluation board, the ISL74420MDEMO1Z. ISL74420MDEMO1Z is an example small footprint layout with SMD resistors to provide user-defined power-up configuration.

Both versions of the ISL74420M boards support I^2C interface. The I^2C interface allows overriding the power-up pin-selected configuration.

The *ISL74420M Datasheet* provides further details regarding the I^2C specifications. The datasheet also provides links to software tools and approaches available writing and reading the device registers.

The ISL74420MEV1Z evaluation board and this accompanying manual provide a physical / electrical method to evaluate the stand-alone operation of the ISL74420M. However, before starting an evaluation the reader should review the *ISL74420M Datasheet* for more detailed information about the operation, function, and performance of the device.

Features

- User settable switches for easy selection of frequency and phase configuration.
- Banana Plugs for bench supply connection to PVIN and VCCEXT inputs.
- SW3 (PVIN) for power cycling to enable strapping sense connection updates.
- Dual Pin 0.1 spacing connectors or coaxial routing of clock outputs.
- Enables I^2C access for software control on internal device registers and associated operation.

Specifications

The ISL74420MEV1Z evaluation board is configured using switch settings for immediate evaluation of board operation / functionality.

The board allows for other conditions to be evaluated with user switches strapping connections or I^2C software control of the internal device registers.

The electrical ratings of the ISL74420MEV1Z evaluation board are shown in Table 1.

Table 1. Electrical Ratings

Parameter	Rating
PVIN Supply Voltage	3V to 18V
CLOCKOUT 0-3 VCCEXT Range	3V to 5.5V
Operating Frequency Range	25kHz to 50MHz
Output Phase / (Delay) Selection	15° Increments
Temperature	-55°C to +125°C

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Contents

1. Functional Description

ISL74420MEV1Z as shipped is tested and configured for:

- Core Oscillator: 48MHz (Master Mode Enabled)
- PRESCALE: Divide-by-2
- CLKOUT0: 2MHz, 0° phase delay
- CLKOUT1: 2MHz, 180° phase delay
- CLKOUT2: 2MHz, 90° phase delay
- CLKOUT3: 2MHz, 270° phase delay

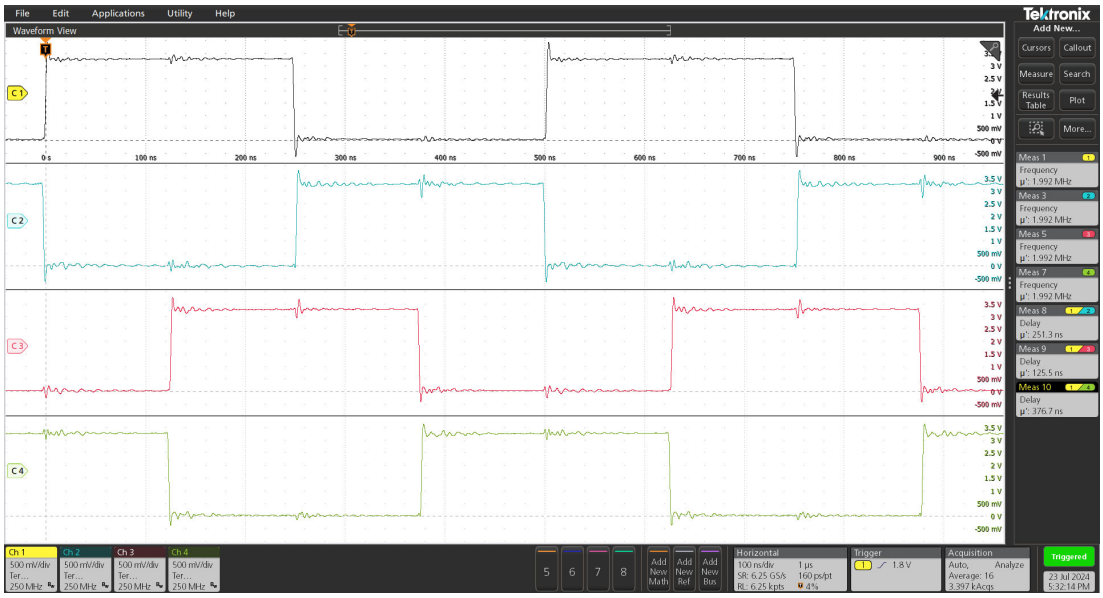

Figure 1. ISL74420MEV1Z as Shipped, Tested and Configured

This setup provides an example for ideal SYNC signals for a ISL73847 4-phase design such as the ISL73847SEHEV3Z. Contact Renesas regarding your customer specific sync outputs configuration options and discussion.

Photographs of the ISL74420MEV1Z are shown in Figure 3 and Figure 4.

The ISL74420MEV1Z evaluation board provides access to the pins of the IC device and convenient pads for connecting test equipment. For more information, see the schematic (Figure 5), PCB layers (Figure 6 through Figure 11), and Bill of Materials. Performance data taken using the ISL74420MEV1Z and basic lab equipment is shown in Figure 12 through Figure 25.

1.1 Operational Characteristics

The ISL74420MEV1Z only requires a single voltage supply 3.0V<PVIN<18V connected to the PVIN banana plug. The internal regulator creates a $3.3V_{CC}$ (50mA) supply for the ISL74420M. It is best to keep PVIN > 3.6V when using the internal regulator. This is the default condition of the board. Applying the PVIN voltage results in the device outputting four continuous clocks as previously described.

The board contains resistors to modify the board's operation. Removing R4 disconnects VCCEXT from VCC so it can be connected to an external DC supply. Installing R6 enables the connection of VCCEXT to J1.3.

J3 is a two pin connector that provides access to the CLKIN of the device. This enables the use of an external signal source. R1's value should be evaluated based on the signal source used.

The datasheet should also be reviewed regarding operational characteristics regarding OSCTUNE, MASTER, PRESCL, and OUTEN options.

1.2 Setup and Configuration

The following equipment is recommended for testing the board:

- 3V to 18V DC power supply (Set to 5.0 volts for initial evaluation)
- 4-channel 200MHz to 500MHz oscilloscope
- As noted in the Functional Description, the board comes shipped configured as an example for ideal SYNC signals for a 4-phase 90° shifted design
- To review detailed options regarding Setup and Configuration, review the Frequency and I2C Address Selection and Phase Selection tables in the datasheet.

Complete the following steps to configure and use the board:

1. Connect and turn on a 5V power supply to the PVIN pin.
2. Use the oscilloscope to look at CLOCKOUT(0-3) waveforms. Proper probe grounding must be practiced when observing clean waveforms.
3. Advanced: When CLOCKOUT waveforms are observed, the user may wish to experiment with the results of switching between Controller and Target modes. *Note*: The ISL74420MEV1Z board provides user-settable switches to ease experimentation with the ISL74420M. Review the Controller and Target Configuration section in the data sheet to explore the effect on the four clock outputs of these modes and the external CLKIN capability.

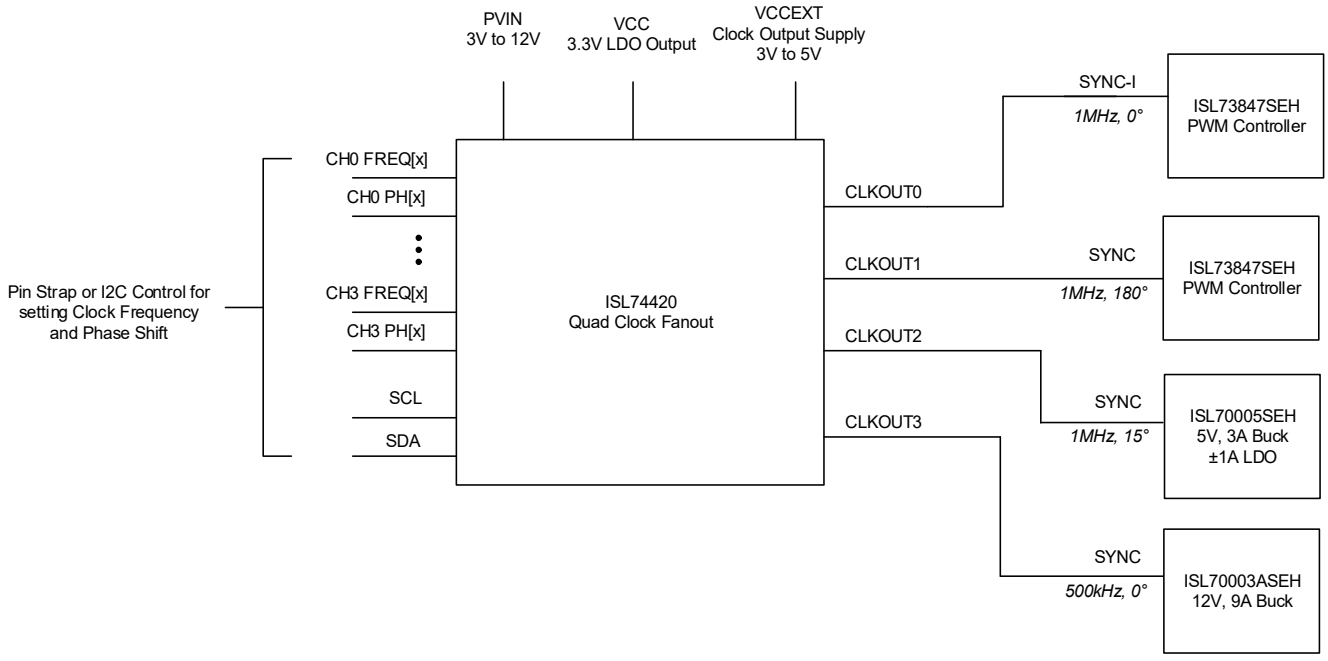

Figure 2. Example Evaluation Test Setup Block Diagram

2. Board Design

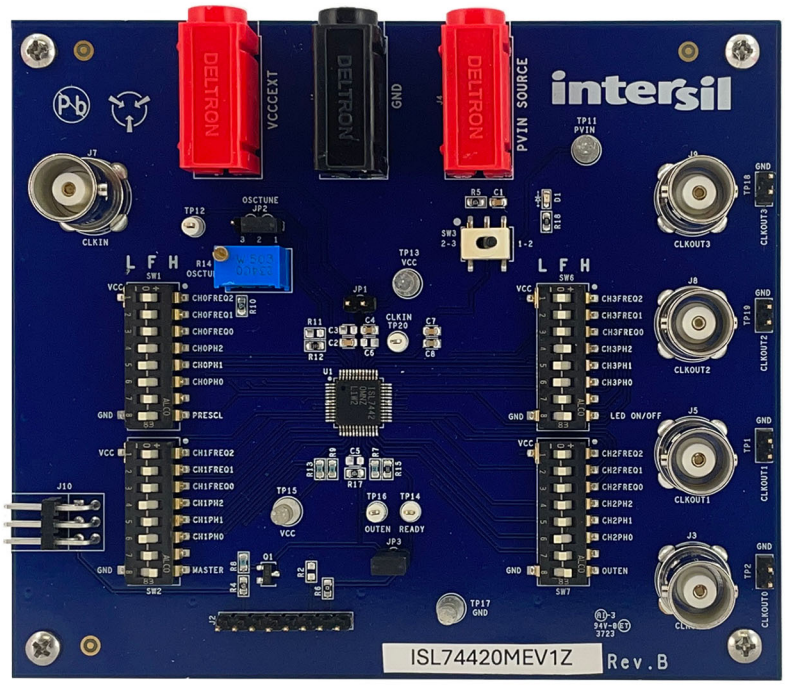

Figure 3. Evaluation Board (Top)

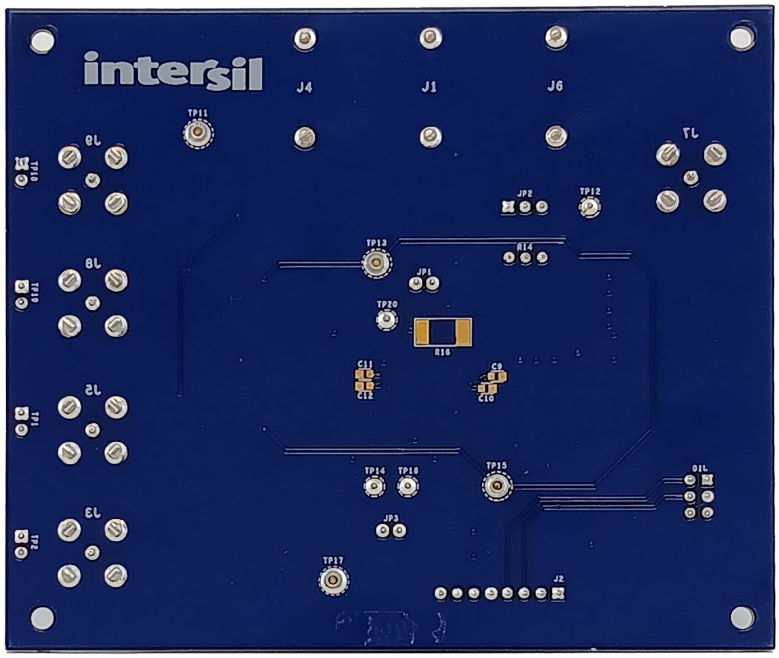

Figure 4. Evaluation Board (Bottom)

2.1 Basic Layout

The ISL74420M is located in the center of the board and is labeled U1. Connect the input power across the PVIN and GND banana receptacles. After a short Power-on Reset (POR) time, the four CLOCKOUTS(0-3) appear across four dual pin 0.1 spaced headers. The other passive components on the top side of board can be changed to vary the internal 48MHz oscillator. These are connected to the OSCTUNE Pin 45 of the ISL74420M. Refer to the *ISL74420M Datasheet* (Core oscillator Tuning section) for detailed information regarding range and effect of the OSCTUNE control. Consult the schematic in (Figure 5) for more details.

2.2 Layout Guidelines

The ISL74420MEV1Z PCB layout has been optimized for ease of testing. This PCB clock outputs can connect specifically to external devices using two pin 0.1 pin connection or coaxial connections.

When incorporating the ISL74420M into a system there are a few guidelines that can ensure optimal electrical and noise performance. Analog circuits can conduct noise through paths that connect it to the outside world. These paths include the PVIN, VCC, VCCEXT, input to any device pin and the outputs. ***Important***: Ensure these paths are kept away from known system noise sources.

When doing a new design, Renesas recommends decoupling the power supply pins (PVIN, VCC and VCCEXT) for power supply filtering. If the traces to the supply lines are long, Renesas recommends using a larger 1µF capacitor at the point of entry for the supply and a smaller capacitor, like a 0.1µF, close to the part to reduce high-frequency perturbations.

CLOCKOUTS(0-3) routing is especially important. Consider placing series termination resistors on the four clock outputs. Renesas recommends reviewing best practice documentation related to clock routing and termination options, see *Renesas Output Terminations Quick Guide*. Locate series Termination placeholders as close as possible to the driving device pin.

PCB design is critical to reduce parasitic inductances with critical components being closely placed to the IC. The critical components are the decoupling capacitor locations and parasitics on the load connection of the four CLOCKOUT pins. Also, refer to the Termination CLKOUT and CLKIN signals discussion of the datasheet.

Important: Refer to the *ISL74420M Datasheet* when reconfiguring the evaluation board. Reference the details of Frequency and I^2C Address Selection sections and the Phase Selection tables in the *ISL74420M Datasheet*. These tables detail configuration options that are set by the four 8-position switch assemblies for user strapping as shown in User Switches Frequency and Phase Selection.

2.3 User Switches Frequency and Phase Selection

Pin Number	Pin Name	L F H (TOP)	Description
1	CH0 FREQ[2]	SW1-1	3-level (tri-level) logic frequency division selection for Channel 0.
2	CH0 FREQ[1]	SW1-2	
3	CH0 FREQ[0]	SW1-3	
48	CH0 PH[2]	SW1-4	3-level (tri-level) logic phase delay selection for Channel 0.
47	CH0 PH[1]	SW1-5	
46	CH0 PH[0]	SW1-6	
-	-	SW1-7	Not used
4	PRESCL	SW1-8	3-level (tri-level) logic pre-scaler selection for all channels.

Pin Number	Pin Name	L F H (TOP)	Description
12	CH1 FREQ[2]	SW2-1	3-level (tri-level) logic frequency division selection for Channel 1.
11	CH1 FREQ[1]	SW2-2	
10	CH1 FREQ[0]	SW2-3	
13	CH1 PH[2]	SW2-4	3-level (tri-level) logic phase delay selection for Channel 1.
14	CH1 PH[1]	SW2-5	
15	CH1 PH[0]	SW2-6	
-	-	SW2-7	Not used
20	MASTER	SW2-8	Logic level input to select if the part should use its internal oscillator when no external clock is present.
25	CH2 FREQ[2]	SW7-1	3-level (tri-level) logic frequency division selection for Channel 2.
26	CH2 FREQ[1]	SW7-2	
27	CH2 FREQ[0]	SW7-3	
22	CH2 PH[0]	SW7-4	3-level (tri-level) logic phase delay selection for Channel 2.
23	CH2 PH[1]	SW7-5	
24	CH2 PH[2]	SW7-6	
-	-	SW7-7	Not Used
19	OUTEN	SW7-8	Logic level input to enable the CLKOUTx pins. (1K to Ready)
36	CH3 FREQ[2]	SW6-1	3-level (tri-level) logic frequency division selection for Channel 3.
35	CH3 FREQ[1]	SW6-2	
34	CH3 FREQ[0]	SW6-3	
37	CH3 PH[2]	SW6-4	3-level (tri-level) logic phase delay selection for Channel 3.
38	CH3 PH[1]	SW6-5	
39	CH3 PH[0]	SW6-6	
-	-	SW6-7	Not Used
-	LED	SW6-8	Test LED

2.4 Schematic Diagram

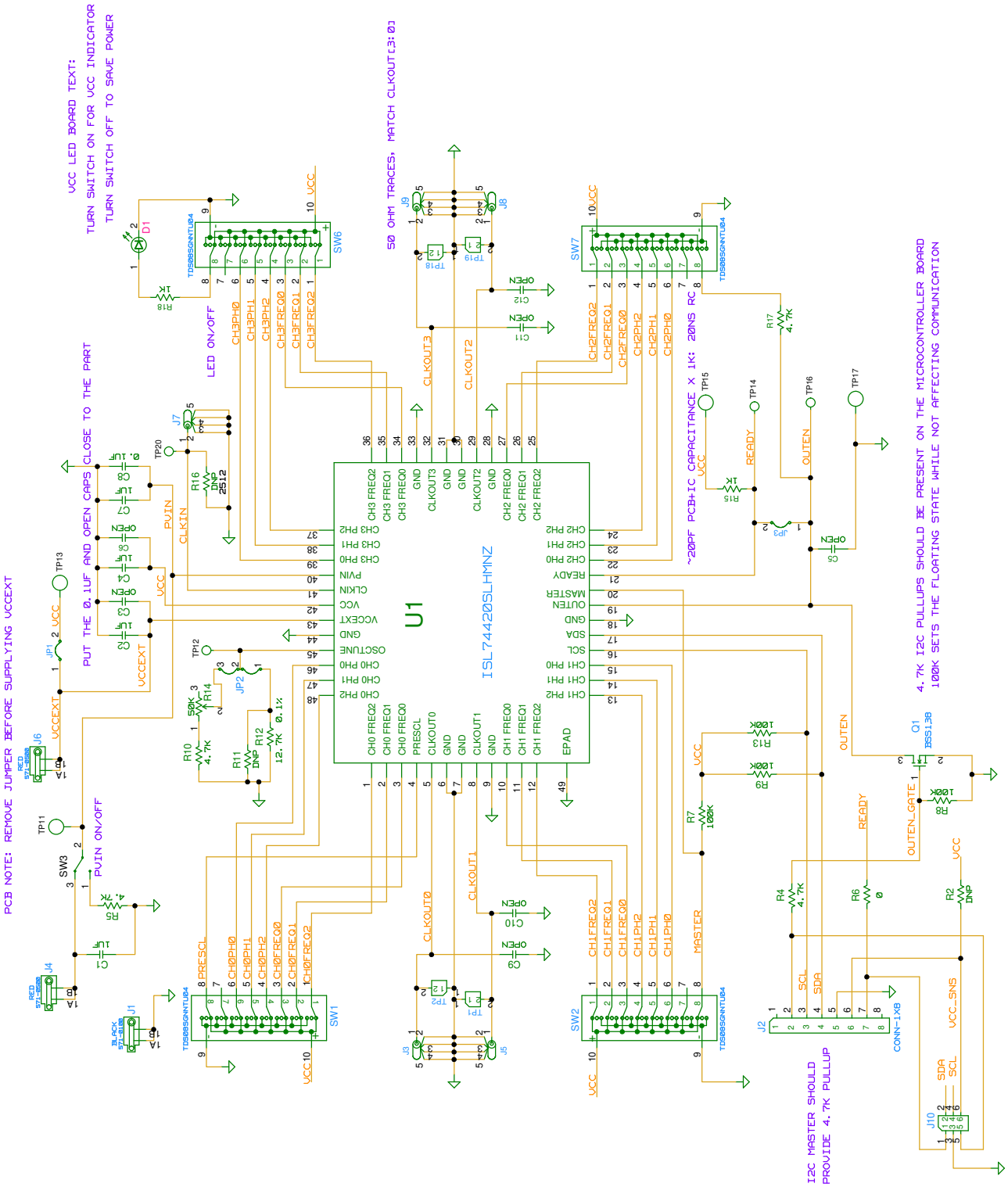

Figure 5. Schematic

2.5 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
4	TP11,TP13,TP15,TP17	Test Point Turret 0.150 Pad 0.100 Thole	Keystone	1514-2
5	J3,J5,J7-J9	Silver Plated 50Ω PCB Mount Receptacle	Amphenol	31-5329-51RFX
1	R14	Trimmer Potentiometer (RoHS Compliant)	Bourns	3299W-1-503-LF
4	TP12,TP14,TP16,TP20	Miniature White Test Point 0.100 Pad 0.040 Thole	Keystone	5002
1	J1	10A BLACK Banana Jack Socket Terminal - Female - Horizontal - 4mm Plug	Deltron	571-0100
2	J4,J6	10A RED Banana Jack Socket Terminal - Female - Horizontal - 4mm Plug	Deltron	571-0500
4	TP1,TP2,TP18,TP19	TEST POINT 2 Pin Header 2.54mm (0.100) Pitch	FCI	68000-236 TESTPOINT
1	Q1	200mA 50V N-Channel Transistor	Diodes-inc	BSS138
1	J2	Male In-line 8 pins × 0.1 inch Connector Strip	Generic	CONN-1X8
1	C8	Multilayer Cap (Automotive AEC-Q200)	Murata	GCJ188R71H104KA12D
4	C1,C2,C4,C7	Ceramic Chip Cap	Murata	GCM188R71E105KA64D
1	SW3	SPDT On-None-On (2 Switch Positions) SM Ultra miniature Toggle Switch	C&K	GT11MSCBE
7	C3,C5,C6,C9-C12	Multilayer Cap	Generic	H1045-OPEN
2	R2,R11	Metal Film Chip Resistor (Do Not Populate)	Generic	H2505-DNP-DNP-1
1	R16	Thick Film Chip Resistor (Do Not Populate)	Generic	H2515-DNP-DNP-1
1	U1	Radiation Hardened LDR to 75Krad(Si) Quad Output Clock Fanout Buffers	Renesas	ISL74420SLHMNZ
1	JP2	Three Pin Jumper	Generic	JUMPER-3-100
2	JP1,JP3	100 mil Spacing Two Pin Jumper	Generic	JUMPER2_100
1	D1	AlInGaP Green	Liteon	LTST-C190KGKT
2	R15,R18	Metal Film Chip Resistor	Rohm	MCR03EZPFX1001
4	R4,R5,R10,R17	Metal Film Chip Resistor	Rohm	MCR03EZPFX4701
1	R6	Thick Film Chip Resistor	Vishay	RCS06030000Z0EA
4	R7-R9,R13	Thick Film Chip Resistor (AEC-Q200)	KOA	RK73H1JTTD1003F
1	R12	Thin Film Resistor	Yageo	RT0603BRD0712K7L
4	SW1,SW2,SW6,SW7	TDS Series Low Profile Tri-State 8-Pos Switch	TE	TDS08SGNNTU04
1	J10	Male 6 Pin Right Angle Header 2.54mm×2.54mm (0.100)	Samtec	TSW-103-08-T-D-RA

2.6 Board Layout

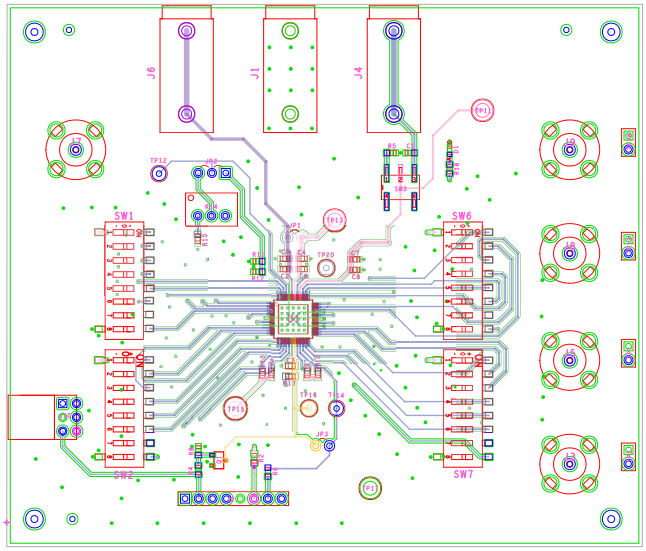

Figure 6. Top Layer

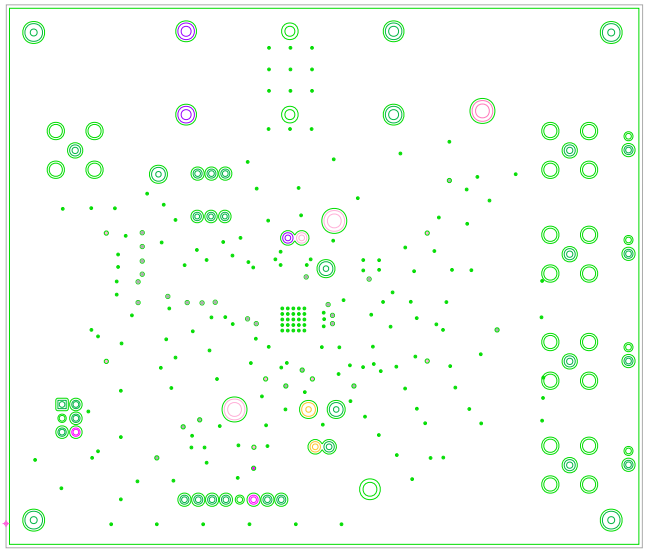

Figure 7. Layer 2

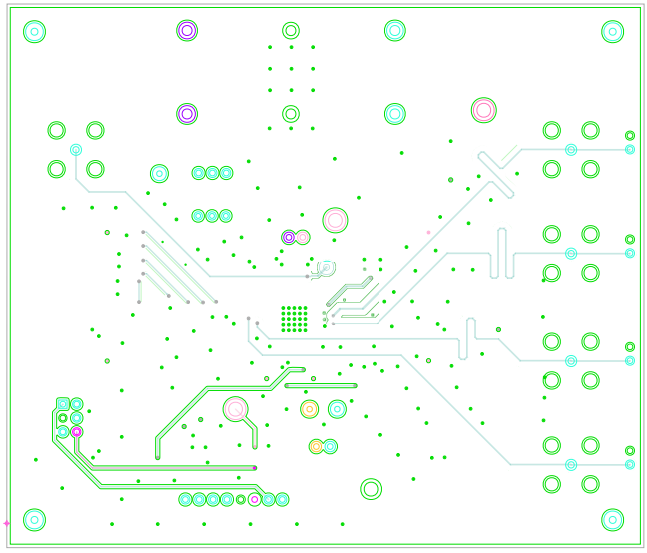

Figure 8. Layer 3

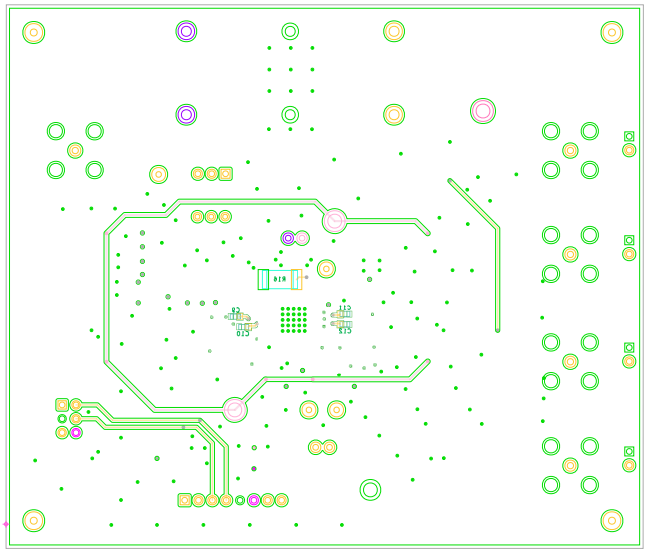

Figure 9. Bottom Layer

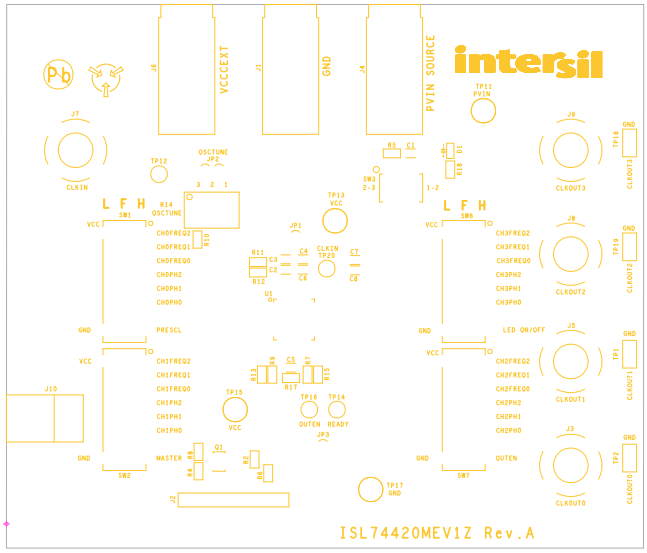

Figure 10. Top Silk Layer

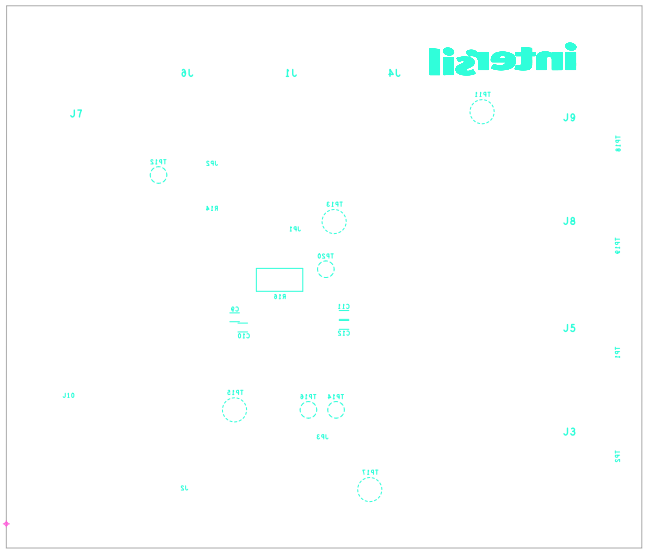

Figure 11. Bottom Silk Layer

2.7 Configuration Scenarios: Selecting Clockout Frequency and Phase (Delay) Options

The ISL74420M design targets low skew and propagation delays regarding the four clockout signal sources. As such, the application requirements must be addressed before selecting the device configuration.

Note: The typical performance graphs provide scope shots for the five configuration scenarios described in the following text and in the datasheet.

The ISL74420M supports a wide variety of frequency configurations, but there are certain rules that must be followed. When the required output frequencies are selected, consider which of the following Scenarios matches the configuration. Next, ensure that the rules are followed for that scenario.

- Scenario 1 (Figure 16 and Figure 17) – All four outputs are at the same frequency
  - All four phase configurations are engaged.
- Scenario 2 (Figure 18 and Figure 19) – Three outputs have the same frequency, one output at a different frequency
  - The three outputs with the same frequency (4MHz) must be on outputs CLKOUT0, CLKOUT1, and CLKOUT2.
  - The phase configurations for CLKOUT0, 1, and 2 are engaged.
  - The different frequency (12MHz) must be on CLKOUT3.
  - The phase configuration for CLKOUT3 is ignored and defaults to 0°.
- Scenario 3 (Figure 20 and Figure 21) – Two outputs have the same frequency, the other two outputs are at a different same frequency (such as, two outputs at 500kHz, two other outputs at 333kHz)
  - One pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The other pair of frequencies must be on CLKOUT2 and CLKOUT3.
  - The phase relationship of CLKOUT0 and CLKOUT1 is controlled.
  - The phase relationship of CLKOUT2 and CLKOUT3 is controlled.
  - The phase relationship between outputs of different frequencies (such as, CLKOUT0 and CLKOUT3) cannot be controlled.
- Scenario 4 (Figure 22 and Figure 23) – Two outputs have the same frequency, the other two outputs are at two different frequencies (there are three total different frequencies output)
  - The pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The phase configurations for CLKOUT0 and CLKOUT1 are engaged.
  - The two different frequencies must be on CLKOUT2 and CLKOUT3
  - The phase configuration for CLKOUT2 and CLKOUT3 are ignored and default to 0°.
- ▪ Scenario 5 (Figure 24 and Figure 25) – All four outputs are at different frequencies
  - The frequencies can be in any order on any CLKOUTx channel.
  - The phase configuration for all CLKOUTx is ignored and defaults to 0°.

3. Typical Performance Graphs

Unless otherwise noted, PVIN = 5V Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays

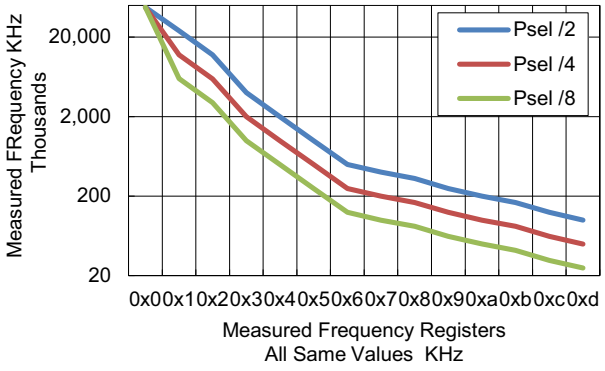

Figure 12. Clockout (0-3) Freq. Options 48MHz Int Clk

Freq Hex	Psel /2	Psel /4	Psel /8
0x0	RSVD	RSVD	RSVD
0x1	23,996,650	11,942,687	5,984,147
0x2	11,962,595	5,978,623	2,990,954
0x3	3,988,690	1,993,907	996,681
0x4	1,995,292	996,619	498,323
0x5	997,471	498,231	249,189
0x6	498,754	249,128	124,589
0x7	398,980	199,298	99,672
0x8	332,497	166,073	83,063
0x9	249,367	124,553	62,293
0xa	199,498	99,640	49,835
0xb	166,231	83,036	41,527
0xc	124,634	62,275	31,146
0xd	99,710	49,818	24,915

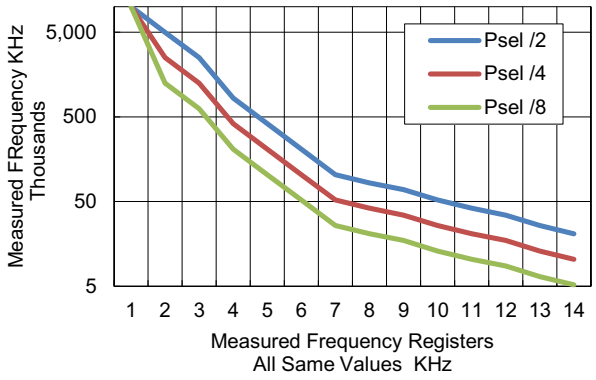

Figure 13. Clockout (0-3) Freq. Options 10MHz Ext Clk

Freq Dec	Psel /2	Psel /4	Psel /8
0	9999492	9997717	9987585
1	4999425	2500473	1250020
2	2500437	1250059	624977
3	833255	416667	208330
4	416645	208332	104167
5	208334	104167	52083
6	104167	52083	26042
7	83333	41667	20833
8	69444	34722	17361
9	52083	26042	13021
10	41667	20833	10417
11	34722	17361	8681
12	26042	13021	6510
13	20833	10417	5208

Unless otherwise noted, PVIN = 5V Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays (Cont.)

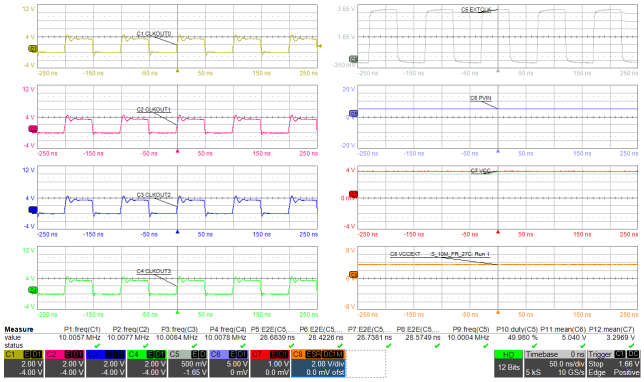

Figure 14. Frequency & Delay External CLKIN 10MHz Pre-Selector /2

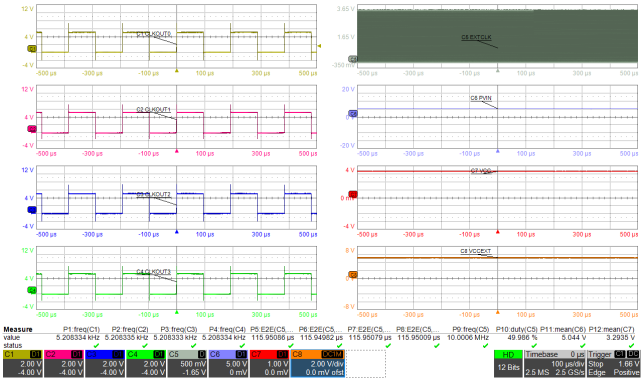

Figure 15. Frequency & Delay External CLKIN 10MHz Pre-Selector /8

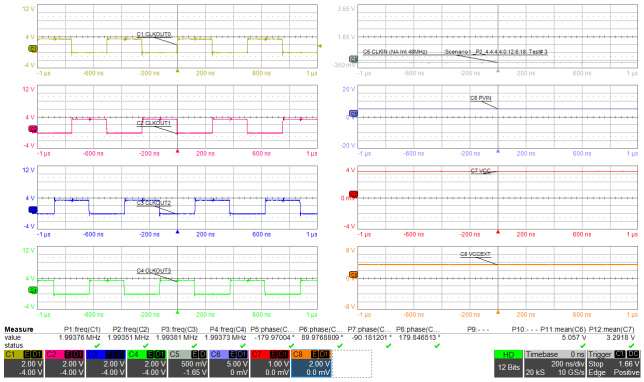

Figure 16. Example Scenario 1: Frequency and Phase

(Four 2MHz frequency and four 90 phase measurements)

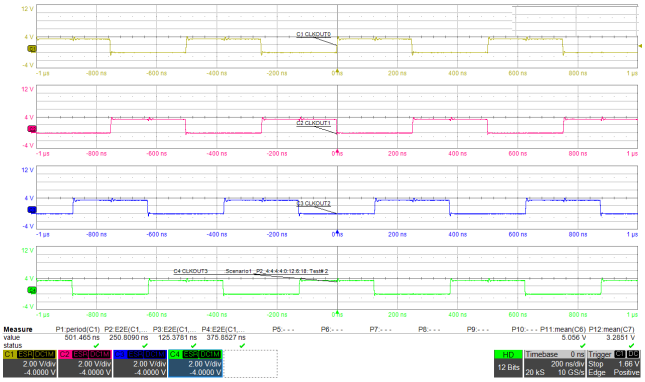

Figure 17. Example Scenario 1: Period and Delay

(Four 500ns Period with Four delays (125ns))

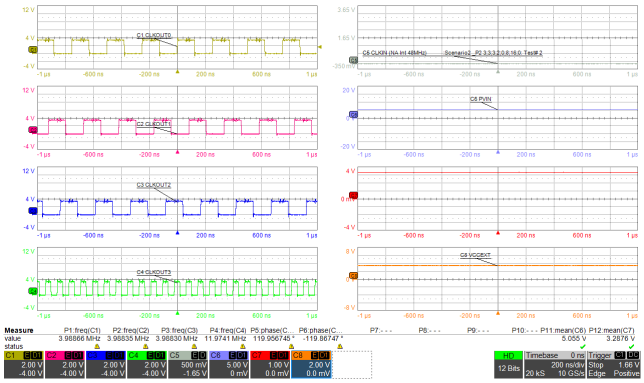

Figure 18. Example Scenario 2: Frequency and Phase

Three outputs have the same frequency (4MHz), one output at a different frequency (12MHz)

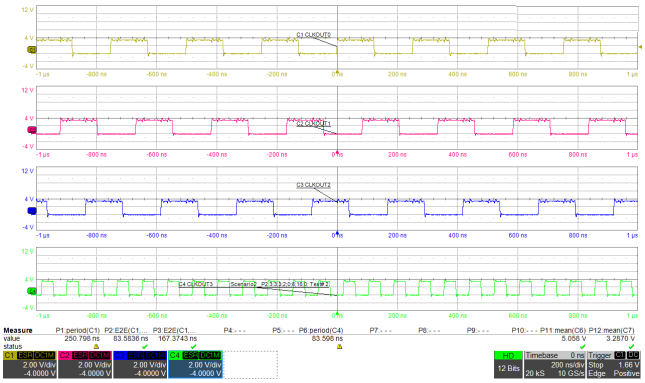

Figure 19. Example Scenario 2: Period and Delay

Three outputs have the same period (250ns), one output at a different period (83.5ns) C1-C2 delay (83ns) C1-C3 delay (167ns)

Unless otherwise noted, PVIN = 5V Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays (Cont.)

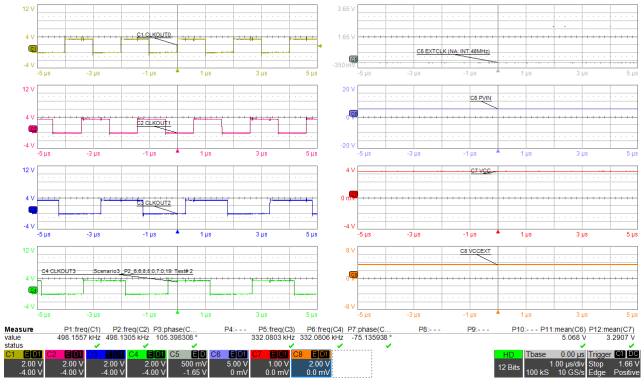

Figure 20. Example Scenario 3: Frequency and Phase

Two outputs have the same frequency (500kHz), the other two outputs are at a different same frequency (333kHz) C1-C2 Phase (105), C3-C4 Phase (-75)

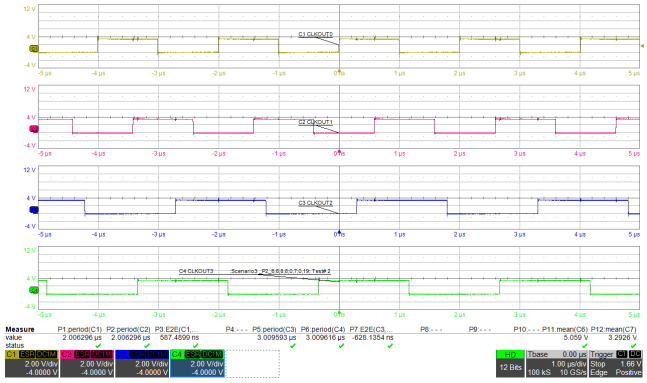

Figure 21. Example Scenario 3: Period and Delay

Two outputs have the same period (2µs), the other two outputs are at a different same period (3µs) C1-C2 delay(587ns) C3-C4 delay (-628NS)

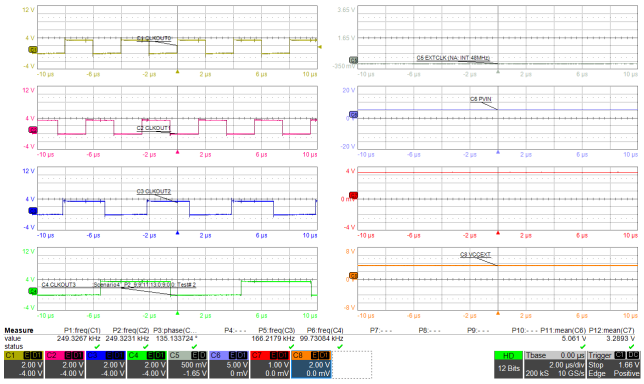

Figure 22. Example Scenario 4: Frequency and Phase

Two outputs have the same frequency (250kHz), the other two outputs are at two different frequencies (166kHz and 99.73kHz)

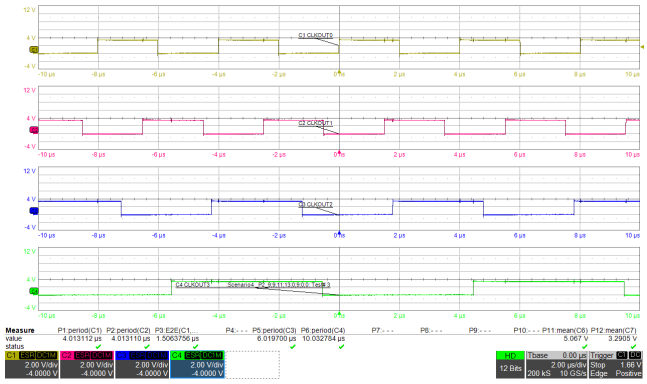

Figure 23. Example Scenario 4: Period and Delay

Two outputs have the same periods (4µs), C1-C2 delay(1.5µs) the other two outputs are at two different periods (6µs and 10µs) (there are three total different periods output)

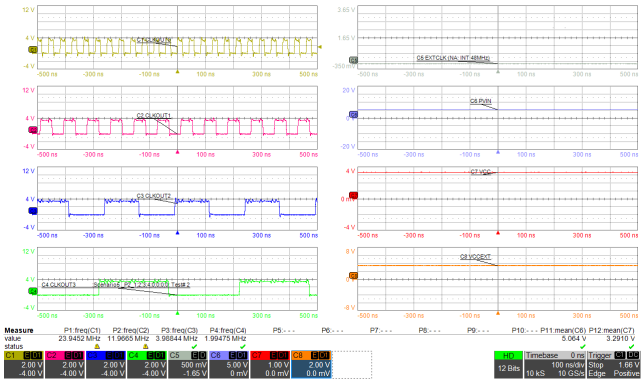

Figure 24. Example Scenario 5: Frequency

Four frequencies that can be in any order on any CLKOUTx channel (24MHz,12MHz, 4MHz, 2MHz).

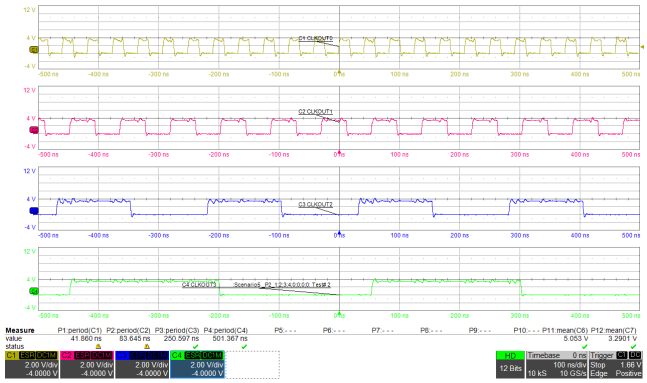

Figure 25. Example Scenario 5: Period

Four unique periods 41ns, 83ns, 250ns, 501ns. No programmable delay options.

4. Ordering Information

Part Number	Description
ISL74420MEV1Z	Radiation Hardened ISL74420M Radiation Hardened Quad Clock Fanout IC evaluation board (Full size Evaluation board: User settable mechanical Switches to select frequency and phase options)

5. Revision History

Revision	Date	Description
1.00	Aug 15, 2024	Initial release

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