ISL74420SLHDEMO1Z

Radiation Hardened Quad Clock Output Demonstration Board

Description

The ISL74420SLHDEMO1Z radiation hardened quad clock fanout IC demonstration board (shown in Figure 3) features the ISL74420SLH ceramic version of the device.

The ISL74420SLHDEMO1Z has a small footprint layout with SMD resistors that provides user-defined power-up configuration.

The ISL74420SLHDEMO1Z is functionally similar to the ISL74420SLHEV1Z evaluation board. The ISL74420SLHDEMO1Z provides mechanical switches for configuration. This eases user experimentation of frequency and delay selections and other configuration options.

Both versions of the ISL74420SLH boards support I^2C interface. The I^2C interface allows overriding the power-up pin-selected configuration.

The *ISL74420SLH Datasheet* provides further details regarding the I^2C specifications. The datasheet also provides links to software tools and approaches available for writing and reading the device registers.

The ISL74420SLHDEMO1Z demonstration board and this accompanying manual provide a physical/electrical method to evaluate the stand-alone operation of the ISL74420SLH. However before starting an evaluation, review the *ISL74420SLH Datasheet* for more detailed information about the operation, function, and performance of the device.

Features

- 0Ω resistors on the underside to select frequency and phase options
- Top of PCB shows how few components are needed for a complete implementation
- Perfect to plug into an existing design and provide clocks
- Provides the ideal clock signals for other boards such as the ISL73847SEHEV3Z
- Enables I^2C access for software control on internal device registers and associated operation.

Specifications

The ISL74420SLHDEMO1Z demonstration board is configured by default using pin strapping for immediate evaluation with minimum components and connections.

The board allows for other conditions to be evaluated with user-modification of SMD resistor pin strapping connections or I^2C software control of the internal device registers.

The electrical ratings of the ISL74420SLHDEMO1Z demonstration board are shown in Table 1.

Table 1. Electrical Ratings

Parameter	Rating
PVIN Supply Voltage	3.0V to 18V
CLOCKOUT 0-3 VCCEXT Range	3.0V to 5.5V
Operating Frequency Range	25kHz to 50MHz
Output Phase / (Delay) Selection	15° Increments
Temperature	-55°C to +125°C

Contents

1. Functional Description

ISL74420SLHDEMO1Z as shipped is tested and configured for the following:

- Core Oscillator: 48MHz (Master Mode Enabled)
- PRESCALE: divide-by-2
- CLKOUT0: 2MHz, 0° phase delay
- CLKOUT1: 2MHz, 180° phase delay
- CLKOUT2: 2MHz, 90° phase delay
- CLKOUT3: 2MHz, 270° phase delay

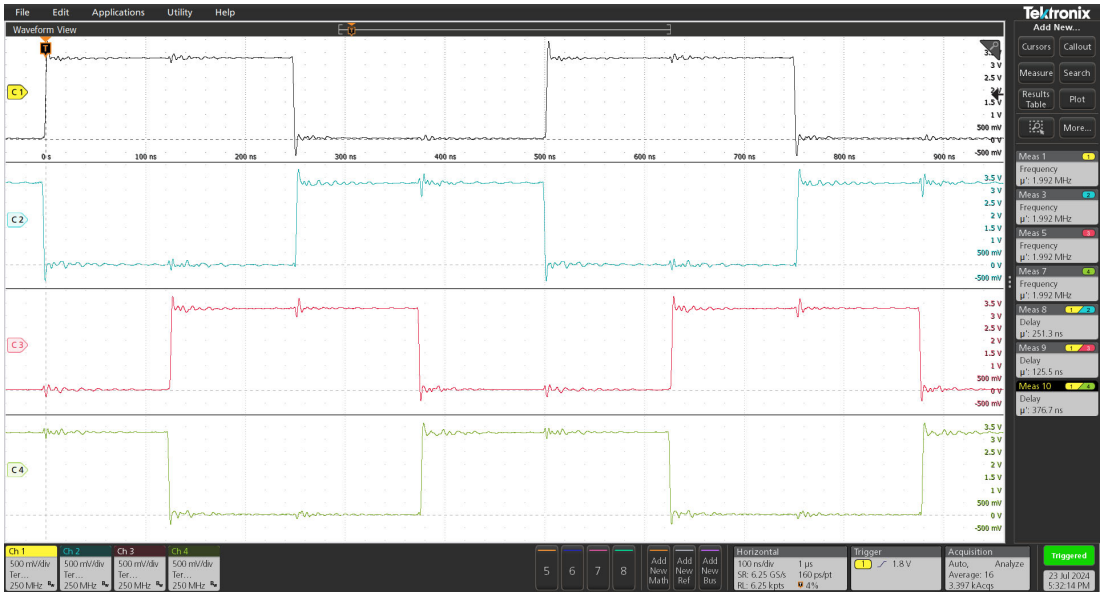

Figure 1. ISL74420SLHDEMO1Z as Shipped, Tested, and Configured

This setup provides an example of ideal SYNC signals for an ISL73847 4-phase design, such as the ISL73847SEHEV3Z. Contact Renesas regarding the customer-specific sync output configuration options and discussion.

Photographs of the ISL74420SLHDEMO1Z are shown in Figure 3 and Figure 4.

The ISL74420SLHDEMO1Z demonstration board provides access to the device pins and convenient pads for connecting test equipment. For more information, see the schematic (Figure 5), PCB layers (Figure 7 through Figure 11), and Bill of Materials. Performance data taken using the ISL74420SLHDEMO1Z and basic lab equipment is shown in Figure 12 through Figure 25.

1.1 Operational Characteristics

The ISL74420SLHDEMO1Z only requires a single voltage supply, 3.0V<PVIN<18V, connected to the PVIN J1.2. The internal regulator creates a $3.3V_{CC}$ (50mA) supply for the ISL74420SLH. It is best to keep PVIN > 3.6V when using the internal regulator, which is the default condition of the board. Applying the PVIN voltage results in the device outputting four continuous clocks as previously described.

The board contains resistors to modify the board's operation. Removing R4 disconnects VCCEXT from VCC so it can be connected to an external DC supply. Installing R6 enables the connection of VCCEXT to J1.3.

J3 is a 2-pin connector that provides access to the CLKIN of the device, which enables the use of an external signal source. Therefore, evaluate the R1 value based on the signal source used.

Review the datasheet regarding operational characteristics regarding OSCTUNE, MASTER, PRESCL, and OUTEN options.

1.2 Setup and Configuration

The following equipment is recommended for testing the board.

- 3V to 18V DC power supply (Set to 5V for initial evaluation)
- 4-channel 200MHz to 500MHz oscilloscope
- As noted in the Functional Description, the board is configured as an example for ideal SYNC signals for a 4-phase 90° shifted design.
- To review detailed options regarding setup and configuration, review the Frequency and I2C Address Selection, and Phase Selection tables in the datasheet.

Complete the following steps to configure and use the board.

1. Connect and turn on a 5V power supply to the PVIN pad.
2. Use the oscilloscope to look at CLOCKOUT(0-3) waveforms. Proper probe grounding must be practiced when observing clean waveforms.
3. Advanced: When CLOCKOUT waveforms are observed, the user might wish to experiment with the results of switching between Controller and Target modes. *Note*: The ISL74420SLHDEMO1Z board provides user-settable switches to ease experimentation with the ISL74420SLH. Review the Controller and Target Configuration section in the datasheet to explore the effect on the four clock outputs of these modes and the external CLKIN capability.

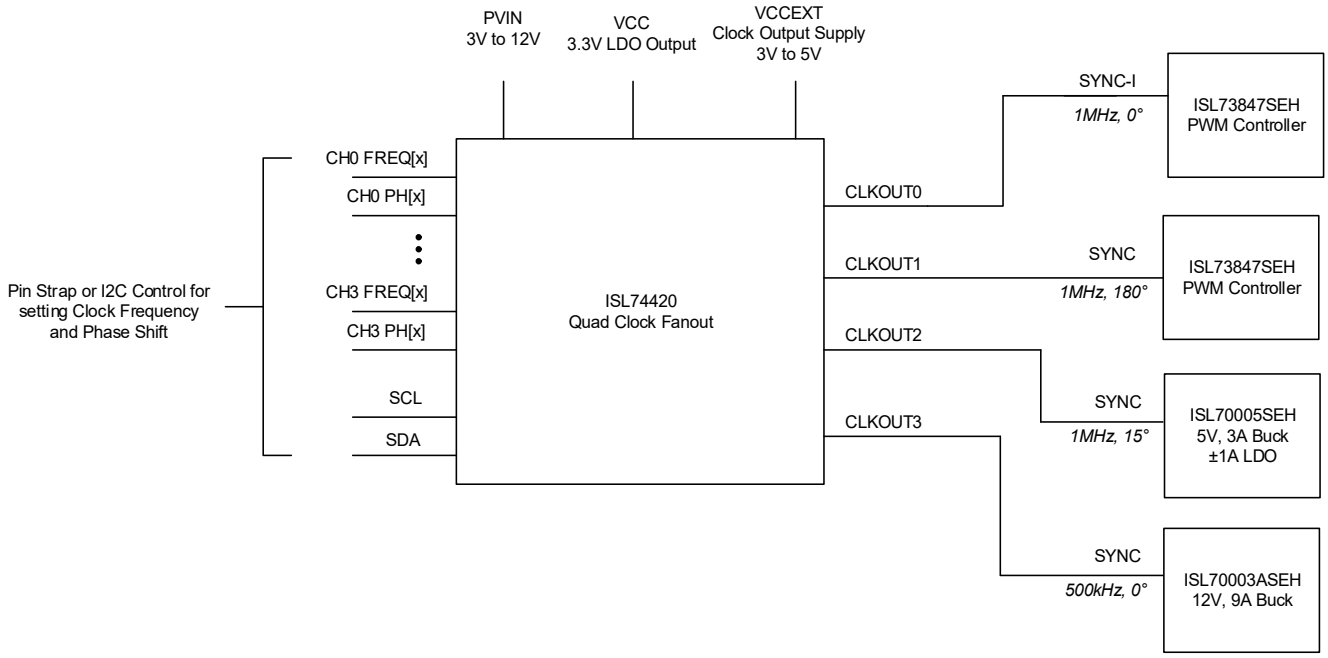

Figure 2. Example Evaluation Test Setup Block Diagram

2. Board Design

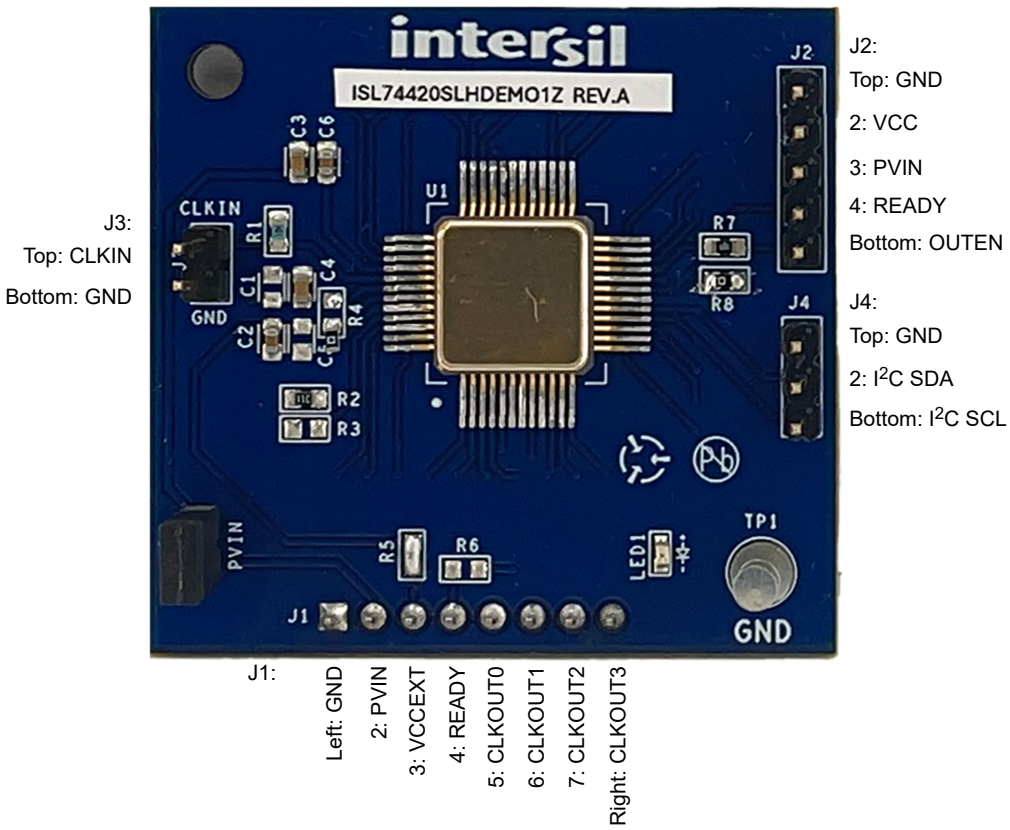

Figure 3. Evaluation Board (Top)

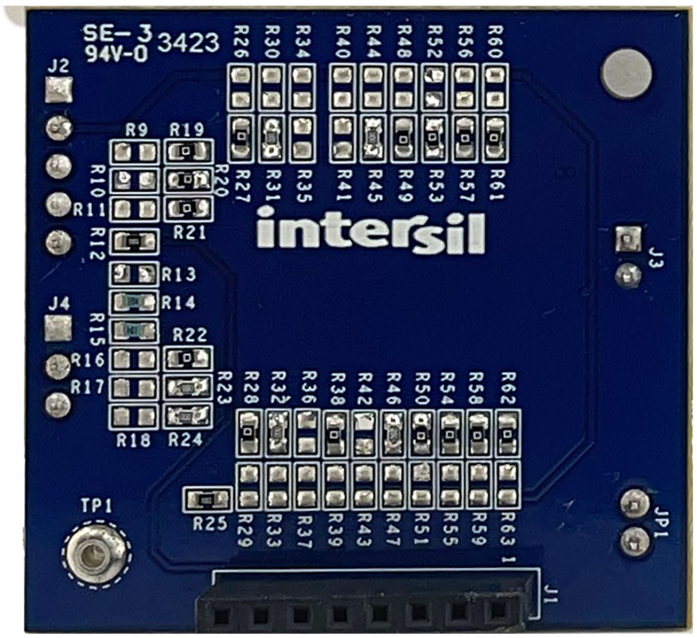

Figure 4. Evaluation Board (Bottom)

2.1 Basic Layout

The ISL74420SLH is located in the center of the board and is labeled U1. Connect the input power across the PVIN J1.2 and J1.1 GND pads. After a short power-on reset (POR) time, the four CLOCKOUTS(0-3) appear across the J1.5, 6, 7, 8, and GND J1.1 pads along the center bottom of the board. The other passive components, R2/R3 (top side of board, center left), can be changed to adjust the internal 48MHz oscillator. These are connected to the OSCTUNE Pin 45 of the ISL74420SLH. Refer to the *ISL74420SLH Datasheet* (Core oscillator Tuning section) for detailed information regarding range and effect of the OSCTUNE control. Consult the schematic in Figure 5 for more details.

2.2 Layout Guidelines

The ISL74420SLHDEMO1Z PCB layout has been optimized for ease of testing. Its clock outputs can be connected to the ISL73847 4-phase DEMO board and provide ideal clock signals in similar applications.

When incorporating the ISL74420SLH into a system, a few guidelines can ensure optimal electrical and noise performance. Analog circuits can conduct noise through paths that connect them to the outside world. These paths include the PVIN, VCC, VCCEXT, input to any device pin, and outputs. ***Important***: Ensure these paths are kept away from known system noise sources.

When designing a new system, Renesas recommends decoupling the power supply pins (PVIN, VCC, and VCCEXT) for power supply filtering. If the traces to the supply lines are long, Renesas recommends using a larger 1µF capacitor at the point of entry for the supply and a smaller capacitor, such as a 0.1µF, close to the part to reduce high-frequency perturbations.

CLOCKOUTS(0-3) routing is critical. Consider placing series termination resistors on the four clock outputs. Renesas recommends reviewing the best practice documentation related to clock routing and termination options, see the *Renesas Output Terminations Quick Guide*. Locate series Termination placeholders as close as possible to the driving device pin.

PCB design is critical to reducing parasitic inductances, closely placing crucial components near the IC. The critical components are the decoupling capacitor locations and parasitics on the load connection of the four CLOCKOUT pins. Also, refer to the datasheet discussion of the Termination CLKOUT and CLKIN signals.

Important: Refer to the *ISL74420SLH Datasheet* when reconfiguring the demonstration board. Reference the details of Frequency and I2C Address Selection sections and the Phase Selection tables. These tables detail configuration options that are set by the resistor strapping on the bottom of the board.

2.3 Pin Strapping Frequency and Phase Selection

Pin Number	Pin Name	Low	High	Description
1	CH0 FREQ[2]	R50	R51	3-level (tri-level) logic frequency division selection for Channel 0.
2	CH0 FREQ[1]	R46	R47	
3	CH0 FREQ[0]	R42	R43	
4	PRESCL	R38	R39	3-level (tri-level) logic pre-scaler selection for all channels.
10	CH1 FREQ[0]	R36	R37	3-level (tri-level) logic frequency division selection for Channel 1.
11	CH1 FREQ[1]	R32	R33	
12	CH1 FREQ[2]	R28	R29	
13	CH1 PH[2]	R24	R18	3-level (tri-level) logic phase delay selection for Channel 1.
14	CH1 PH[1]	R23	R17	
15	CH1 PH[0]	R22	R16	
19	OUTEN	(1k to Ready)		Logic level input to enable the CLKOUTx pins. (1K to Ready)

Pin Number	Pin Name	Low	High	Description
20	MASTER	R8	R13	Logic level input to select if the part should use its internal oscillator when no external clock is present.
22	CH2 PH[0]	R21	R11	3-level (tri-level) logic phase delay selection for Channel 2.
23	CH2 PH[1]	R20	R10	
24	CH2 PH[2]	R19	R9	
25	CH2 FREQ[2]	R27	R26	3-level (tri-level) logic frequency division selection for Channel 2.
26	CH2 FREQ[1]	R31	R30	
27	CH2 FREQ[0]	R35	R34	
34	CH3 FREQ[0]	R41	R40	3-level (tri-level) logic frequency division selection for Channel 3.
35	CH3 FREQ[1]	R45	R44	
36	CH3 FREQ[2]	R49	R48	
37	CH3 PH[2]	R53	R52	3-level (tri-level) logic phase delay selection for Channel 3.
38	CH3 PH[1]	R57	R56	
39	CH3 PH[0]	R61	R60	
46	CH0 PH[0]	R62	R63	3-evel (tri-level) logic phase delay selection for Channel 0.
47	CH0 PH[1]	R58	R59	
48	CH0 PH[2]	R54	R55	

2.4 Schematic Diagram

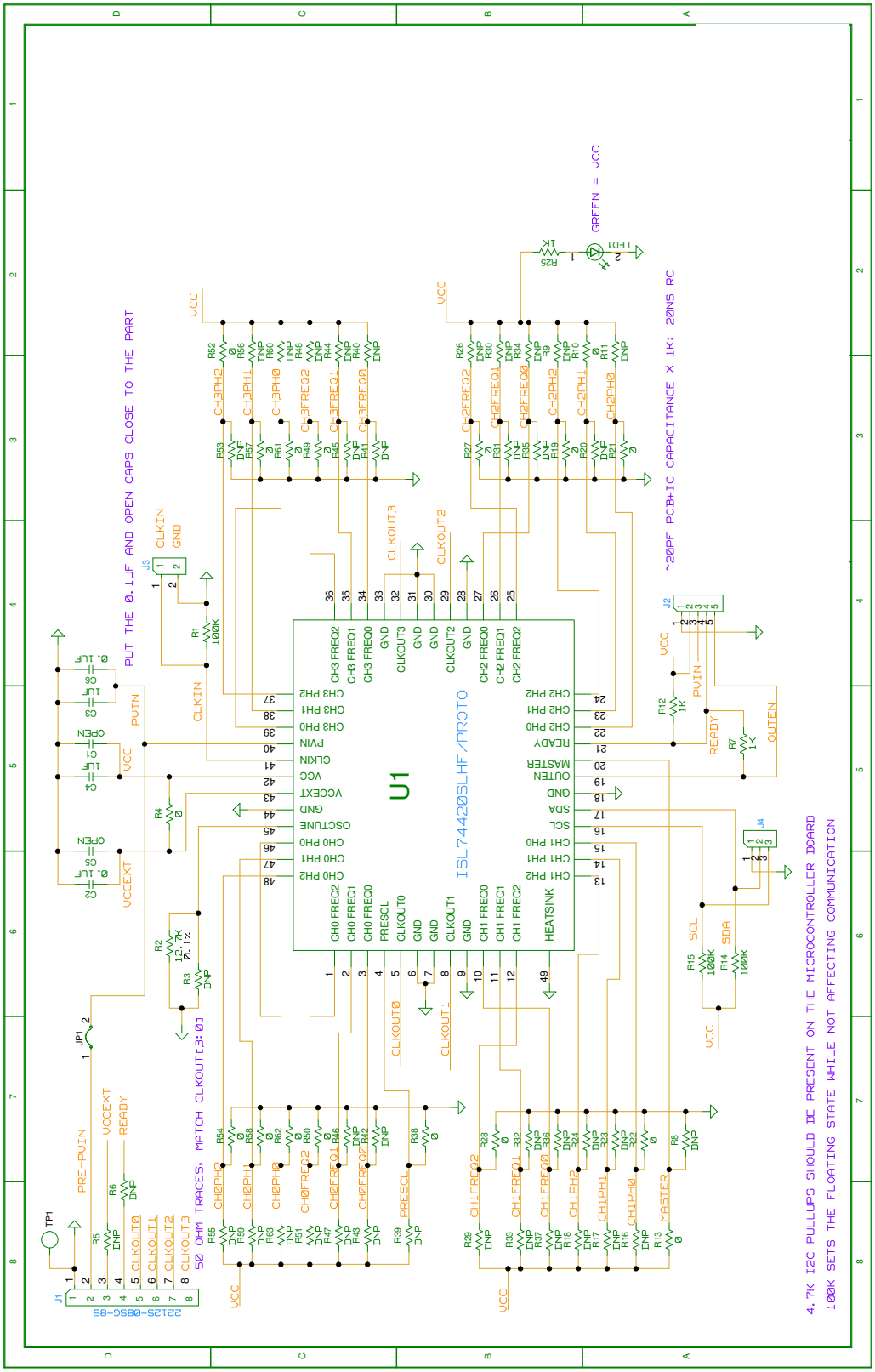

Figure 5. Schematic

2.5 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	TP1	Test Point Turret.150 Pad.100 Thole	Keystone	1514-2
1	J1	Female Incline 8 pins ×0.1 inch Connector	Multicomp	2212S-08SG-85
1	J3	Male 2 Pin Header 2.54mm (.100) Pitch	FCI	68000-236
1	J4	Male In-line 3 pins ×0.1 inch Connector Strip	Various	CONN-1X3
1	J2	Male In-line 5 pins ×0.1 inch Connector Strip	Various	CONN-1X5
2	C2, C6	Multilayer Cap (Automotive AEC-Q200)	Murata	GCJ188R71H104KA12D
2	C3, C4	Ceramic Chip Cap	Murata	GCM188R71E105KA64D
2	C1, C5	Multilayer Cap	Various	Generic
36	R3, R5, R6, R8, R9, R11, R16-R18, R20, R23, R24, R26, R29-R34, R37-R40, R43-R48, R51, R53, R55, R56, R59, R60, R63	Metal Film Chip Resistor (Do Not Populate)	Various	Generic
1	U1	Radiation Hardened LDR to 75Krad(Si) Quad Output Clock Fanout Buffers	Renesas	ISL74420SLHF/PROTO
1	JP1	100 mil Spacing Two Pin Jumper	Various	JUMPER2_100
1	LED1	LED Green Clear Chip SMD	LITEON	LTST-C190KGKT
3	R1,R14,R15	Thick Film Chip Resistor (AEC-Q200)	KOA	RK73H1JTTD1003F
1	R2	Thick Film Chip Resistor (Automotive AEC-Q200)	KOA Speer	RK73H1JTTD1272F
20	R4, R10, R13, R19, R21, R22, R27, R28, R35, R36, R41, R42, R49, R50, R52, R54, R57, R58, R61, R62	Film Chip Resistor	Yageo	RMCF0603ZT0R00
3	R7, R12, R25	Thick Film Chip Resistor	State of the Art	S0603CPX1001F10

2.6 Board Layout

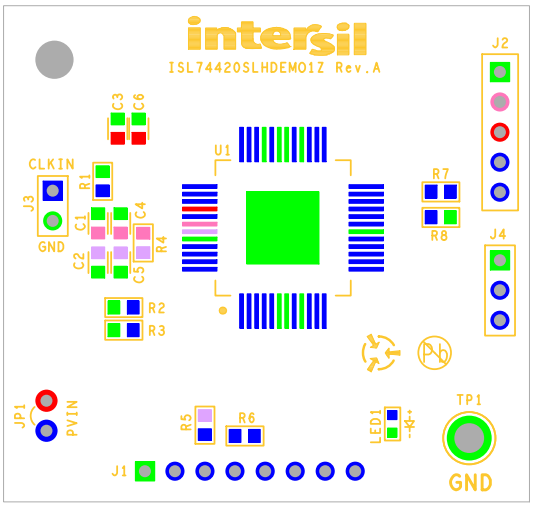

Figure 6. Top Silk Layer

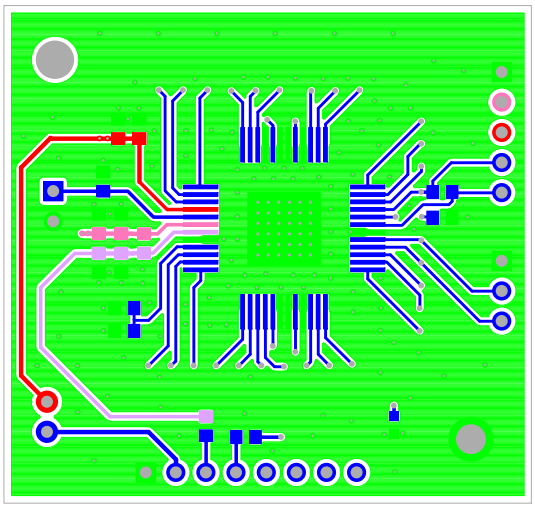

Figure 7. Top Layer

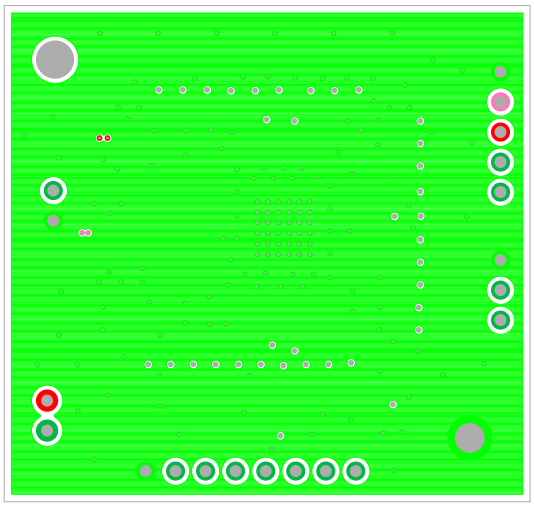

Figure 8. Layer 2

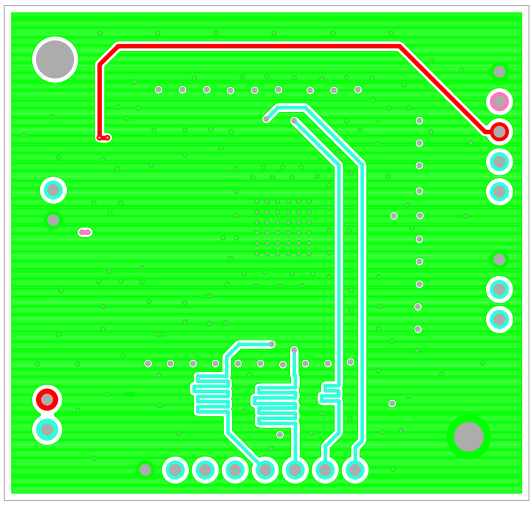

Figure 9. Layer 3

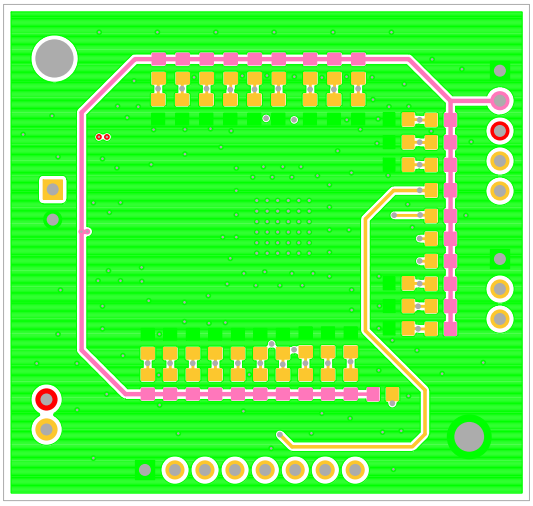

Figure 10. Bottom Layer

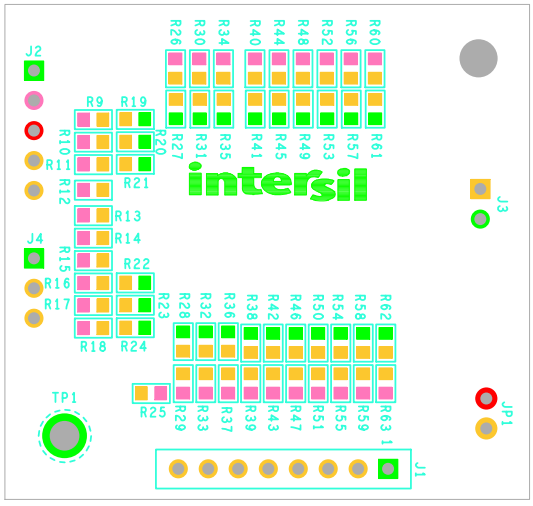

Figure 11. Bottom Silk Layer

2.7 Configuration Scenarios: Selecting Clockout Frequency and Phase (Delay) Options

The ISL74420SLH design targets low skew and propagation delays regarding the four clockout signal sources. As such, the application requirements need to be addressed before selecting the device configuration.

Note: The Typical Performance Graphs provide scope shots for the five configuration scenarios described in the following text and in the datasheet.

The ISL74420SLH supports a wide variety of frequency configurations, but there are certain rules that must be followed. When the required output frequencies are selected, consider which of the following scenarios matches the configuration. Next, ensure that the rules are followed for that scenario.

- Scenario 1 (Figure 16 and Figure 17) – All four outputs are at the same frequency
  - All four phase configurations are engaged.
- Scenario 2 (Figure 18 and Figure 19) – Three outputs have the same frequency, one output at a different frequency
  - The three outputs with the same frequency (4MHz) must be on outputs CLKOUT0, CLKOUT1, and CLKOUT2.
  - The phase configurations for CLKOUT0, 1, and 2 are engaged.
  - The different frequency (12MHz) must be on CLKOUT3.
  - The phase configuration for CLKOUT3 is ignored and defaults to 0°.
- Scenario 3 (Figure 20 and Figure 21) – Two outputs have the same frequency, the other two outputs are at a different same frequency (such as, two outputs at 500kHz, two other outputs at 333kHz)
  - One pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The other pair of frequencies must be on CLKOUT2 and CLKOUT3.
  - The phase relationship of CLKOUT0 and CLKOUT1 is controlled.
  - The phase relationship of CLKOUT2 and CLKOUT3 is controlled.
  - The phase relationship between outputs of different frequencies (such as, CLKOUT0 and CLKOUT3) cannot be controlled.
- Scenario 4 (Figure 22 and Figure 23) – Two outputs have the same frequency, the other two outputs are at two different frequencies (there are three total different frequencies output)
  - The pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The phase configurations for CLKOUT0 and CLKOUT1 are engaged.
  - The two different frequencies must be on CLKOUT2 and CLKOUT3
  - The phase configuration for CLKOUT2 and CLKOUT3 are ignored and default to 0°.
- ▪ Scenario 5 (Figure 24 and Figure 25) – All four outputs are at different frequencies
  - The frequencies can be in any order on any CLKOUTx channel.
  - The phase configuration for all CLKOUTx is ignored and defaults to 0°.

3. Typical Performance Graphs

Unless otherwise noted, PVIN = 5.0 Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays

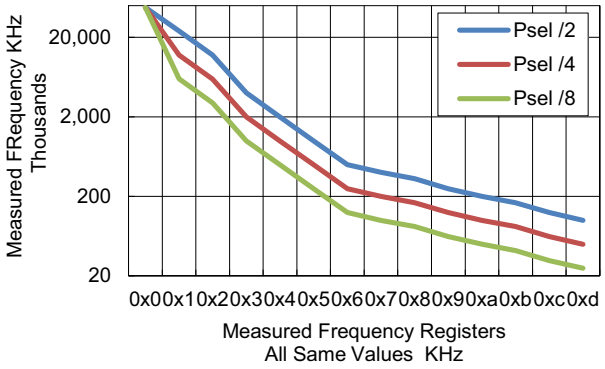

Figure 12. Clockout (0-3) Freq. Options 48MHz Int Clk

Freq Hex	Psel /2	Psel /4	Psel /8
0x0	RSVD	RSVD	RSVD
0x1	23,996,650	11,942,687	5,984,147
0x2	11,962,595	5,978,623	2,990,954
0x3	3,988,690	1,993,907	996,681
0x4	1,995,292	996,619	498,323
0x5	997,471	498,231	249,189
0x6	498,754	249,128	124,589
0x7	398,980	199,298	99,672
0x8	332,497	166,073	83,063
0x9	249,367	124,553	62,293
0xa	199,498	99,640	49,835
0xb	166,231	83,036	41,527
0xc	124,634	62,275	31,146
0xd	99,710	49,818	24,915

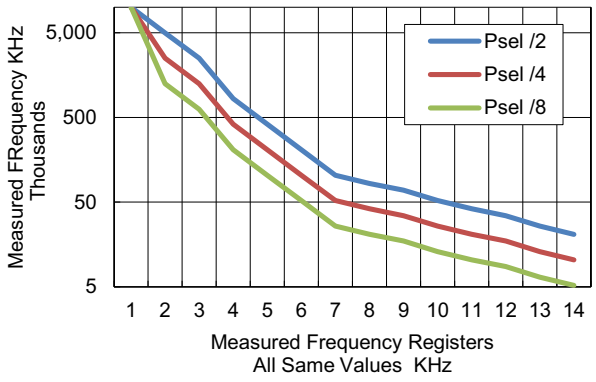

Figure 13. Clockout (0-3) Freq. Options 10MHz Ext Clk

Freq Dec	Psel /2	Psel /4	Psel /8
0	9999492	9997717	9987585
1	4999425	2500473	1250020
2	2500437	1250059	624977
3	833255	416667	208330
4	416645	208332	104167
5	208334	104167	52083
6	104167	52083	26042
7	83333	41667	20833
8	69444	34722	17361
9	52083	26042	13021
10	41667	20833	10417
11	34722	17361	8681
12	26042	13021	6510
13	20833	10417	5208

Unless otherwise noted, PVIN = 5.0 Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays (Cont.)

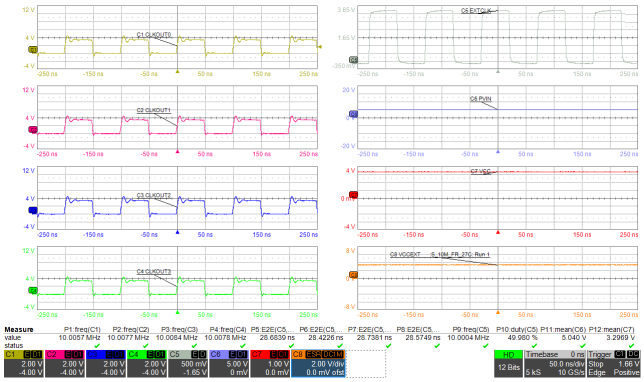

Figure 14. Frequency & Delay External CLKIN 10MHz Pre-Selector /2

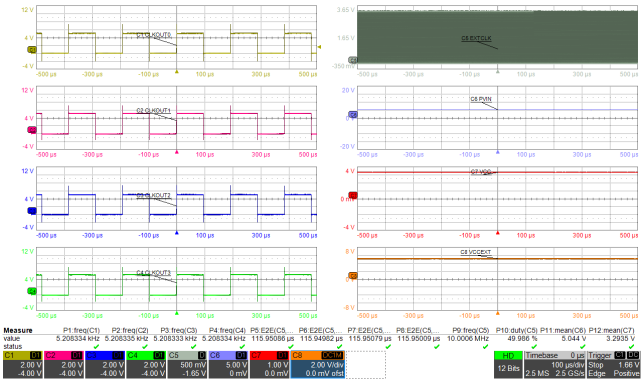

Figure 15. Frequency & Delay External CLKIN 10MHz Pre-Selector /8

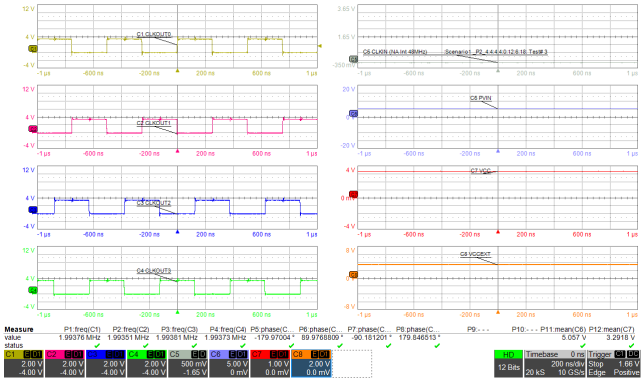

Figure 16. Example Scenario 1: Frequency and Phase

(Four 2MHz frequency and four 90 phase measurements)

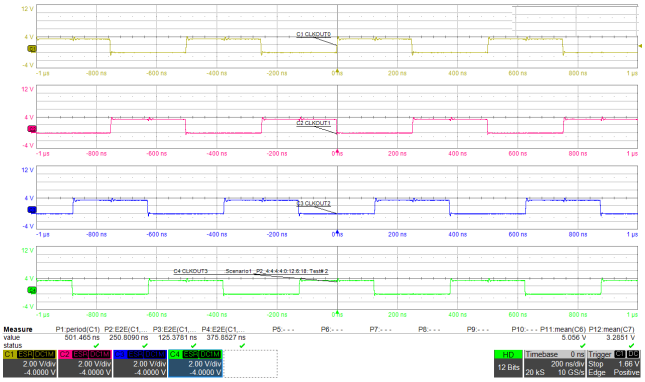

Figure 17. Example Scenario 1: Period and Delay

(Four 500ns Period with Four delays (125ns))

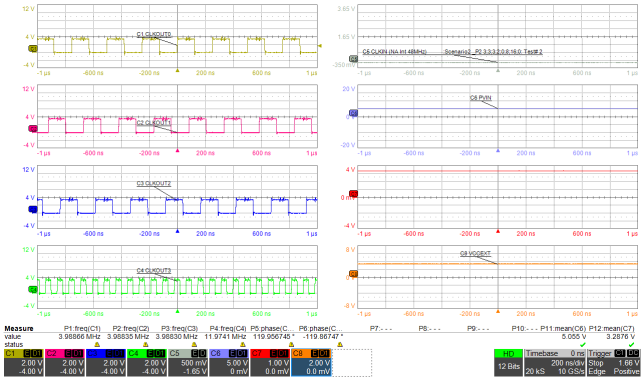

Figure 18. Example Scenario 2: Frequency and Phase

Three outputs have the same frequency (4MHz), one output at a different frequency (12MHz)

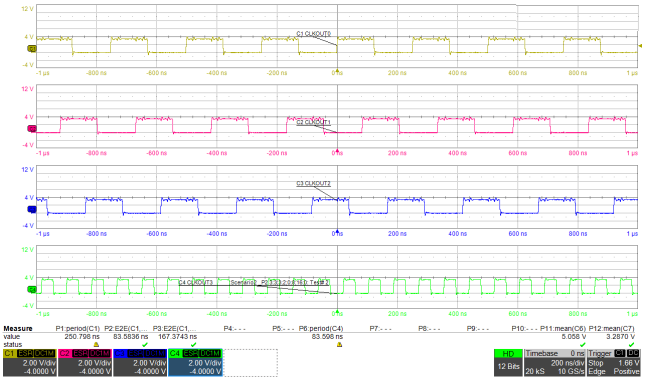

Figure 19. Example Scenario 2: Period and Delay

Three outputs have the same period (250ns), one output at a different period (83.5ns) C1-C2 delay (83ns) C1-C3 delay (167ns)

Unless otherwise noted, PVIN = 5.0 Example Configurations Scenarios 1 to 5 Frequency & Phase / Period and Delays (Cont.)

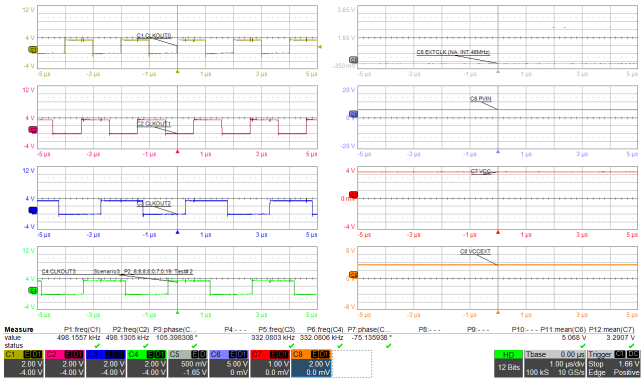

Figure 20. Example Scenario 3: Frequency and Phase

Two outputs have the same frequency (500kHz), the other two outputs are at a different same frequency (333kHz) C1-C2 Phase (105), C3-C4 Phase (-75)

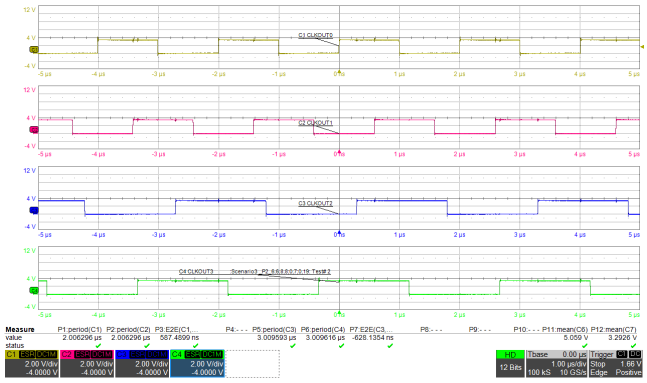

Figure 21. Example Scenario 3: Period and Delay

Two outputs have the same period (2µs), the other two outputs are at a different same period (3µs) C1-C2 delay(587ns) C3-C4 delay (-628NS)

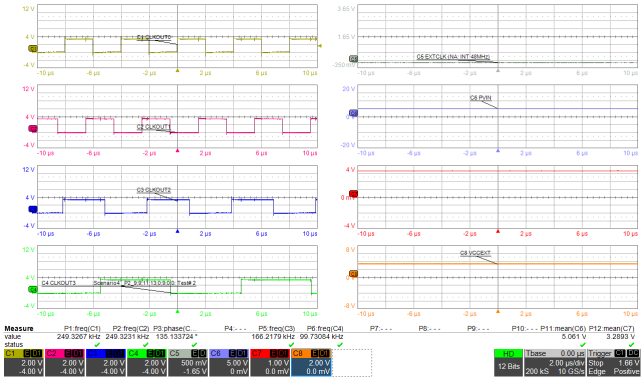

Figure 22. Example Scenario 4: Frequency and Phase

Two outputs have the same frequency (250kHz), the other two outputs are at two different frequencies (166kHz and 99.73kHz)

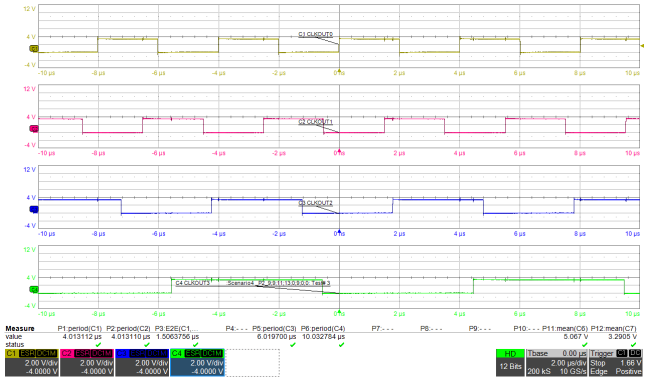

Figure 23. Example Scenario 4: Period and Delay

Two outputs have the same periods (4µs), C1-C2 delay(1.5µs) the other two outputs are at two different periods (6µs and 10µs) (there are three total different periods output)

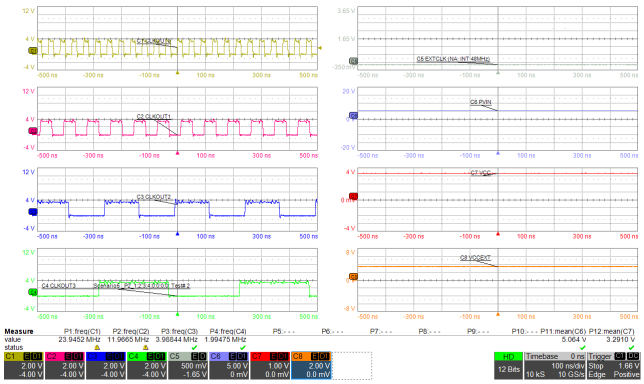

Figure 24. Example Scenario 5: Frequency

Four frequencies that can be in any order on any CLKOUTx channel (24MHz,12MHz, 4MHz, 2MHz).

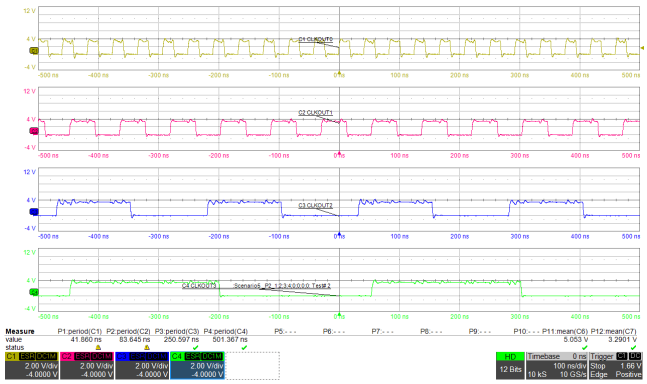

Figure 25. Example Scenario 5: Period

Four unique periods 41ns, 83ns, 250ns, 501ns. No programmable delay options.

4. Ordering Information

Part Number	Description
ISL74420SLHDEMO1Z	Radiation Hardened ISL74420SLH Quad Clock Fanout IC evaluation board (Compact DEMO board: 0Ω resistors on the underside to select frequency and phase options)

5. Revision History

Revision	Date	Description
1.00	Apr 15, 2025	Initial release.

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