ISL75052SEHEVAL1Z

The ISL75052SEH is a high-performance, adjustable, low-voltage, high-current, low-dropout linear regulator specified at 1.5A rated output current for input voltages from 4.0V to 13.2V. The LDO outputs can be adjusted from 0.6V to 12.7V by means of two preset resistors. Salient features of the part include:

- TID, ELDRS, and SEE rated
- Very fast load transient response
- ±2.0% guaranteed V_{OUT} accuracy over line, load and temperature
- Typical dropout of 225mV at 1.5A
- EN feature
- PG feature
- OCP feature
- Short-circuit and over-temperature protection

The ISL75052SEHEVAL1Z evaluation board provides a simple platform to evaluate performance of the ISL75052SEH. The ISL75052SEHEVAL1Z evaluation board provides a simple platform to evaluate performance of the ISL75052SEH. The same board can be used to evaluate the ISL73052SEH which is the same die offered with different radiation assurance screening. The device output voltage is adjustable, and jumpers are provided to easily set popular output voltages.

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Features

- Five preprogrammed output voltages
- Potentiometer to adjust the output voltage
- LED to monitor proper operation
- Test points to easily measure the control loop

Specifications

This board has been configured and optimized for the following operating conditions:

- V_{IN} = 4V to 13.2V
- I_L = 1.5A

What's Inside

Items shipped with board:

- ISL75052SEHEVAL1Z evaluation board
- ISL75052SEH datasheet
- AN1850 application note

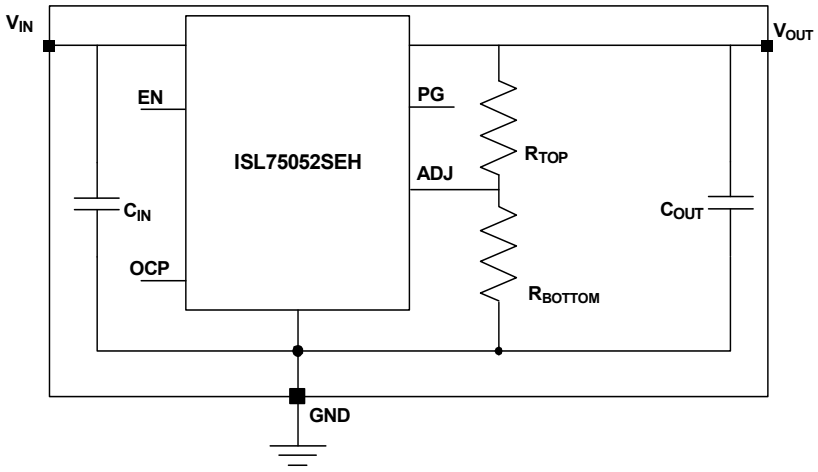

Figure 1. Block Diagram

Contents

1. Functional Description

1.1 Test Steps

1. Select the desired output voltage by shorting one of the jumpers from J1 through J5. The option of JP6 provides for continuous adjustment of V_{OUT} using potentiometer R6.
2. Set the OCP limit by using jumpers JP8 and JP9. JP9 = 0.275A min, and JP8 = 2.75A min.
3. Close JP7. Also closing jumper JP11 (2 and 3) selects R16 = 5.49k as pull-up for PGOOD. Close JP12 (1 and 2).
4. Connect the input supply to V_{IN}/GND and the load to V_{OUT}/GND. Select the V_{IN} to V_{OUT} ratio to keep dissipation within the thermal limits of the device.
5. Use JP10 to enable/disable the IC; Open = Enable, and Close = Disable. (Note: For REVB boards, Close = Enable and Open = Disable.)

2. Optimizing LDO Performance

Performance of the ISL75052SEH can be optimized by following the guidelines provided in this application note.

2.1 Input and Output Capacitor Selection

RH operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 2x100µF, 60mΩ, 25V KEMET T541 series tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor. This is to be connected between VIN to GND pins and VOUT to GND pins of the LDO, with PCB traces no longer than 0.5cm. The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°C. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen on the ISL75052SEHEVAL1Z evaluation board for V_{IN} = 3.3V, V_{OUT} = 1.8V, and I_{OUT} = 3A, with a 220µF, 10V, 25mΩ capacitor, is GM = 16.3dB, and PM = 69.16°C.

2.1.1 Output Voltage Adjustment

The output voltage can be adjusted by means of the resistor divider shown in Figure 1 as R_{TOP} and R_{BOTTOM}.

The resistor values for typical output voltages are given in Table 1. The values listed provide for an evaluation board output voltage that is about 50mV higher than the desired set point to allow for the drop on the line connecting the evaluation board to the desired load.

The resistor divider values can be calculated using the equation:

$V_{OUT} = (0.6X(1+R_{TOP}/R_{BOTTOM})$

Assuming a value R_{TOP} = 15.8k and knowing the required output voltage setting one can calculate the R_{BOTTOM}.

Table 1. Recommended Output Capacitor Values

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	C_{OUT} (µF)
10.0	15.8	1.0	200
9.0	15.8	1.13	200
5.0	15.8	2.15	200
4.0	15.8	2.74	200
2.5[1]	15.8	4.87	47
2.5	15.8	4.87	200

1. Either option could be used depending on cost/performance requirements.

2.2 Output Voltage Soft-Start Adjustment

The output voltage soft-start can be adjusted by means of the capacitor value on the BYP pin, examples are shown in Figure 28 and Figure 29. The BYP cap being 0.2µF and 1.9µF, respectively.

2.3 Output Voltage Start-Up Delay Adjustment

The output voltage start can be adjusted by means of the capacitor value on the VCCX pin examples shown in Figure 28 and Figure 30. The VCCX cap being 0.1µF and 33µF, respectively.

3. Board Design

3.1 Layout Guidelines

Good PCB layout is important to achieving expected performance. When placing components and routing traces, minimize ground impedance and keep parasitic inductance low. Give the input and output capacitors a good ground connection, and place them as close to the IC as possible. Route the traces connecting the ADJ pin away from noisy planes and traces, and keep the board capacitance of the ADJ net to GND as low as possible.

3.2 Thermal Guidelines

If the die temperature exceeds +175°C typical, then the LDO output shuts down to zero until the die temperature cools to +155°C typical. The level of power combined with the thermal impedance of the package (θ_{JC} of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table of the *ISL75052SEH Datasheet*. Mount the device on a high effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between the package base and the PCB copper plane. Select the V_{IN} and V_{OUT} ratios to ensure that dissipation for the selected V_{IN} range keeps T_J within the recommended operating level of 150°C for normal operation.

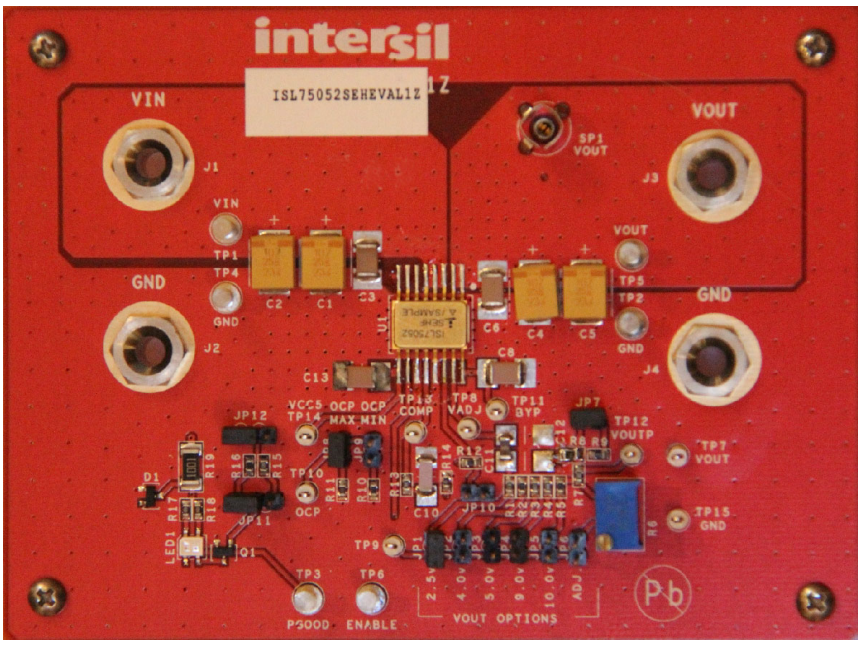

Figure 2. ISL75052SEHEVAL1Z Evaluation Board

3.3 Schematic

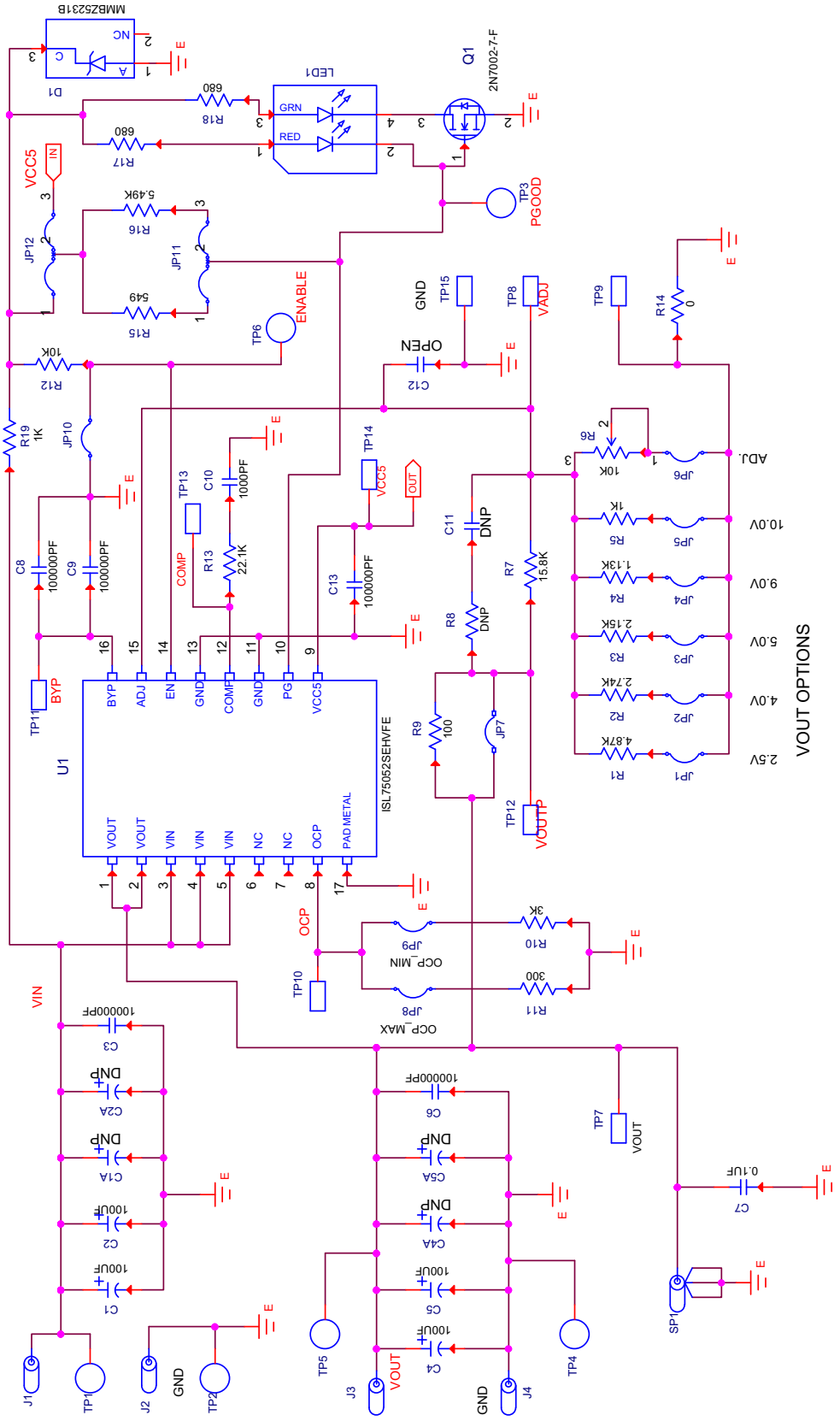

Figure 3. ISL75052SEHEVAL1Z Schematic

3.4 Bill of Materials

Qty	Reference Designator	Description	Mfr	Manufacturer Part
1	SEE LABEL-RENAME BOARD	PWB-PCB, ISL75052SEHEV1Z, REVB, ROHS	TBD	ISL75052SEHEV1ZREVBPCB
1	C10	CAP-MILPRF-55681, SMD, 1808, 0.001µF, 100V, 10%, ROHS	AVX	CDR03BP102BKMR
5	C3, C6, C8, C9, C13	CAP-MILQUAL, SMD, 1812, 0.1µF, 50V, 10%, BX, ROHS	AVX	CDR04BX104AKMR
1	C7	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	MURATA	GRM39X7R104K016AD
4	C1, C2, C4, C5	CAP-TANT, LOW ESR, SMD, E, 100µF, 25V, 10%, 100mΩ, ROHS	KEMET	T495E107K025ATE100
4	J1-J4	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, ROHS	JOHNSON COMPONENTS	108-0740-001
1	SP1	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX	131-4353-00
6	TP1-TP6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
9	TP7-TP15	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
2	JP11, JP12	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
10	JP1-JP10	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	BERG/FCI	69190-202HLF
1	D1	DIODE-ZENER, SMD, SOT-23, 3P, 5.1V, 350mW, ROHS	DIODES INC.	MMBZ5231B-7-F
1	LED1	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 12/20MCD, 2V	LUMEX	SSL-LXA3025IGC-TR
1	Q1	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	DIODES, INC.	2N7002-7-F
1	R6	POT-TRIM, TH, 3P, 10k, 1/2W, 10%, 3/8SQ, 25TURN, TOPADJ, ROHS	BOURNS	3299W-1-103LF
0	R8	RESISTOR, SMD, 0805, DNP, DNP, DNP, TF		
1	R14	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
1	R9	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1000FT
1	R5	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1001V
1	R12	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F
1	R4	RES, SMD, 0603, 1.13k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-071K13L
1	R7	RES, SMD, 0603, 15.8k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1582FT

Qty	Reference Designator	Description	Mfr	Manufacturer Part
1	R3	RES, SMD, 0603, 2.15k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-072K15L
1	R13	RES, SMD, 0603, 22.1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF2212V
1	R2	RES, SMD, 0603, 2.74k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-2741FT
1	R11	RES, SMD, 0603, 300Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX3000
1	R10	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-073KL
1	R1	RES, SMD, 0603, 4.87k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF4871V
1	R15	RES, SMD, 0603, 549Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5490FT
1	R16	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5491FT
2	R17, R18	RES, SMD, 0603, 680Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX6800
1	R19	RES, SMD, 2010, 1k, 1/2W, 1%, TF, ROHS	PANASONIC	ERJ-12SF1001U
4	Four corners	SCREW, 4-40X1/4in, PAN, SS, PHILLIPS		
4	Four corners	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, ROHS	KEYSTONE	2204 (.250 OD)
1	Place assy in bag	BAG, STATIC, 8X8, ZIP LOC, ROHS	ULINE	S-5092
0	U1 (ISL75052SEHQF)	DO NOT POPULATE OR PURCHASE		

3.5 Layout

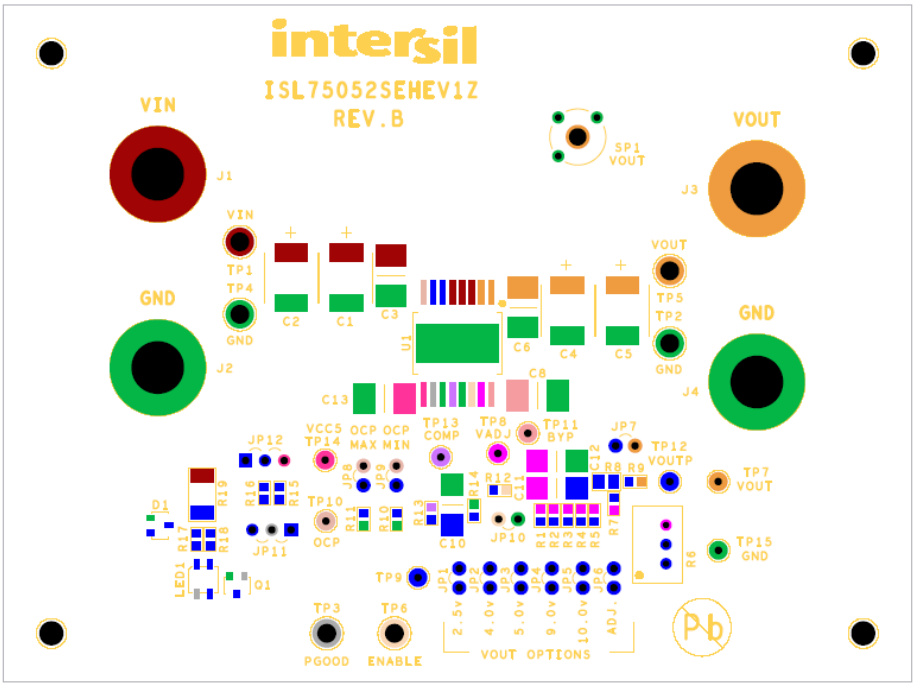

Figure 4. Silkscreen Top

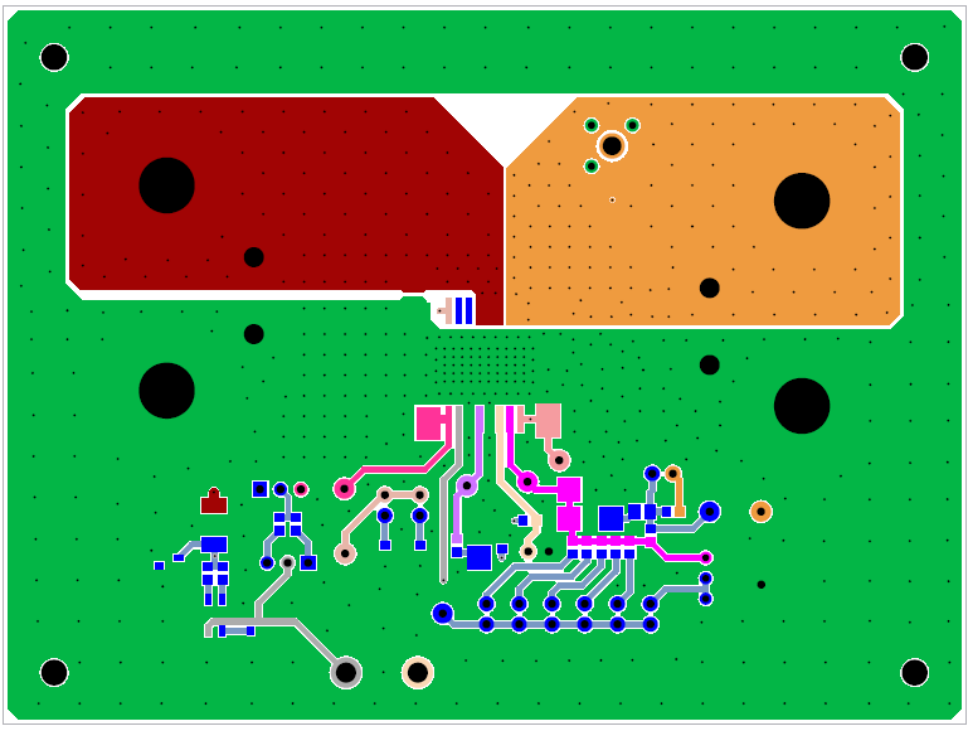

Figure 5. Top Layer Component Side

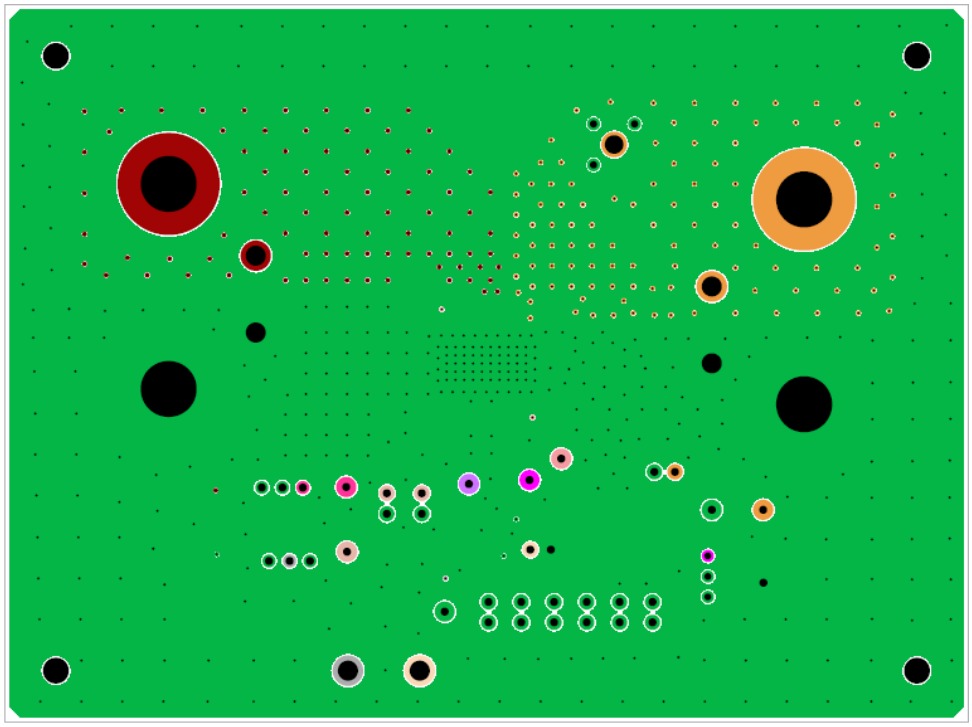

Figure 6. Layer 2

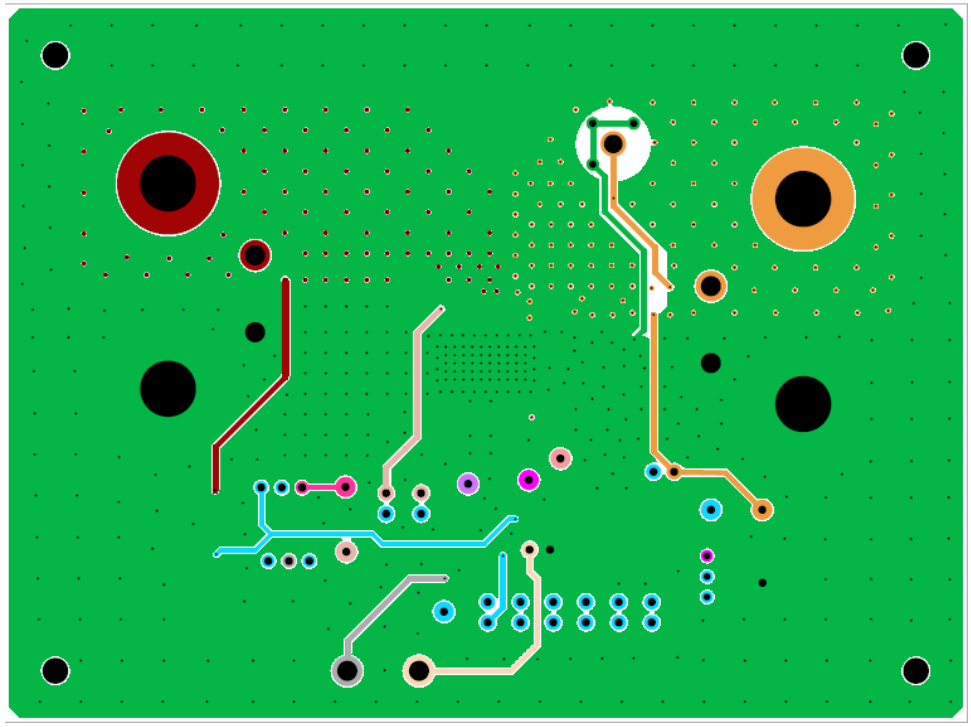

Figure 7. Layer 3

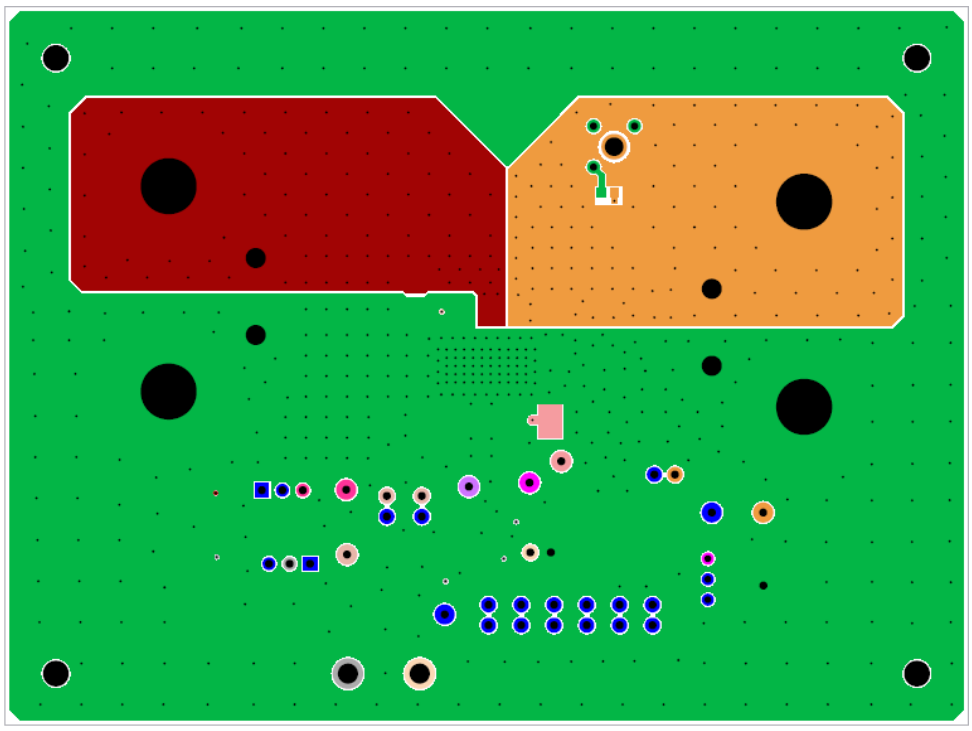

Figure 8. Bottom Layer Solder Side

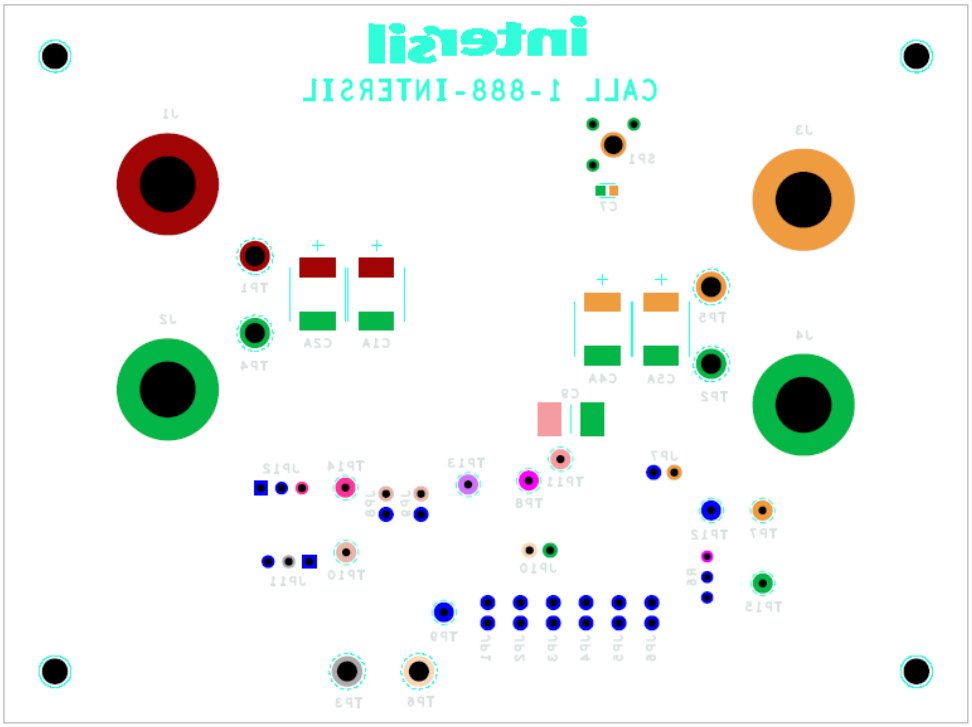

Figure 9. Silkscreen Bottom

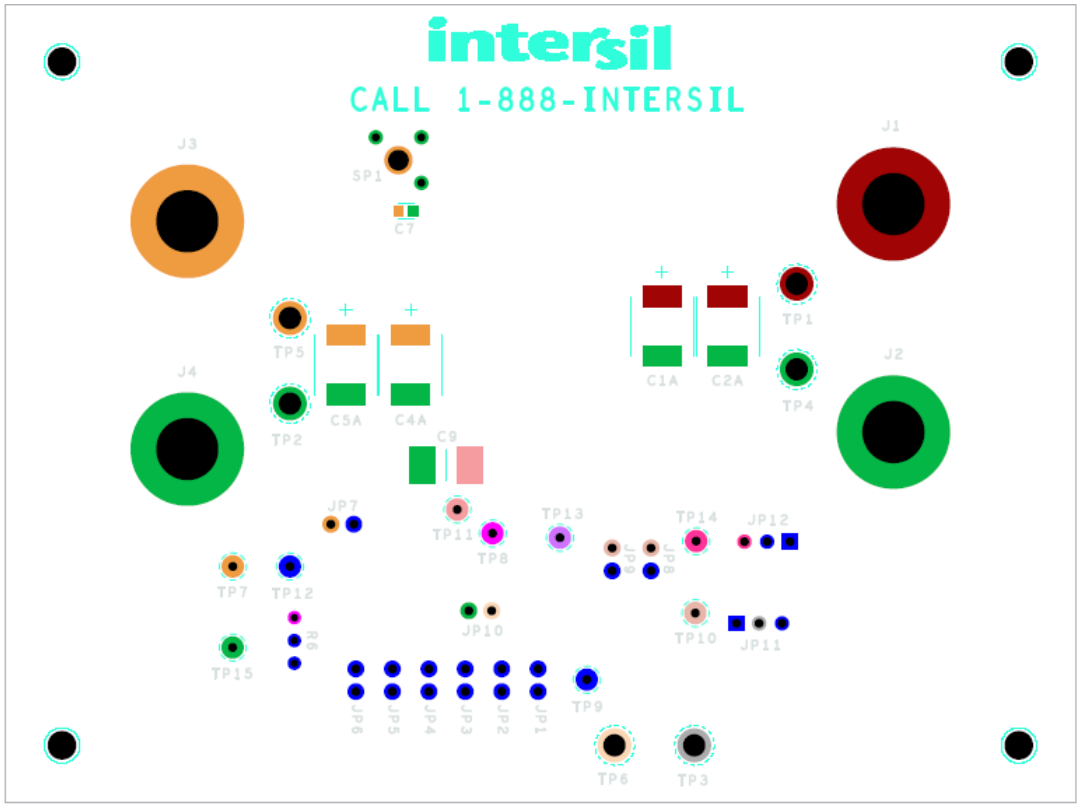

Figure 10. Silkscreen Bottom Mirror

4. Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$.

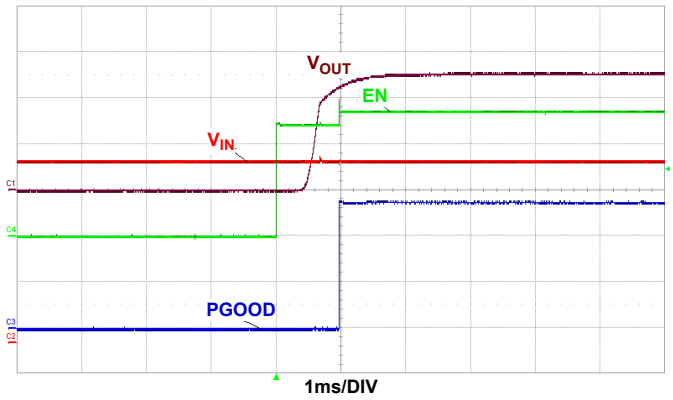

Figure 11. Start-Up Waveforms: V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.1A, EN Low to High

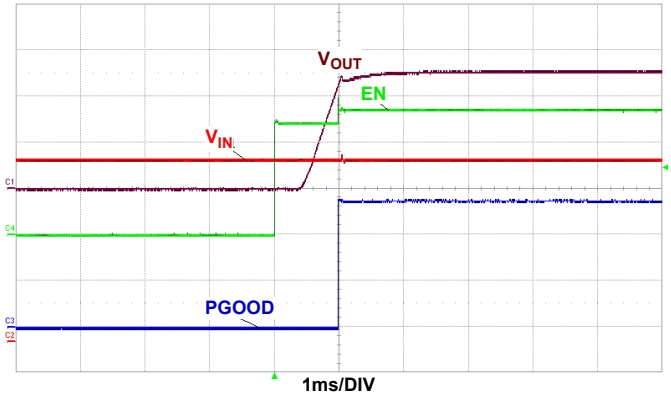

Figure 12. Start-Up Waveforms: V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, EN Low to High

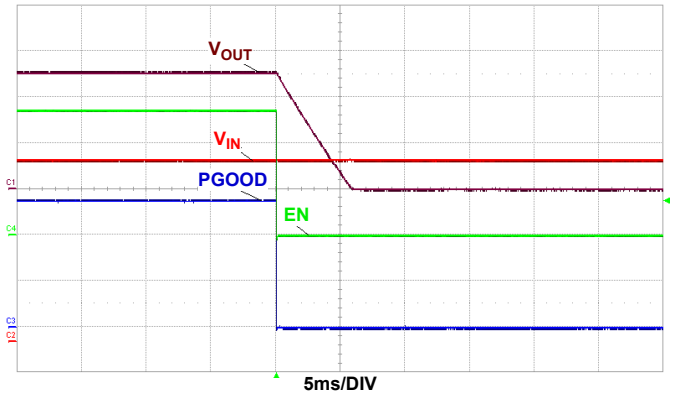

Figure 13. Shutdown Waveform: V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.1A EN High to Low

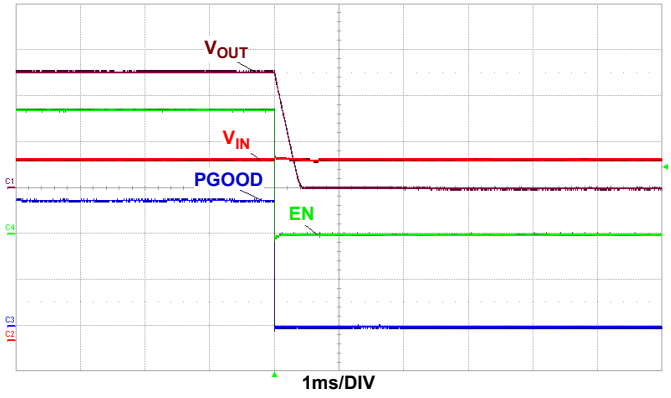

Figure 14. Shutdown Waveform: V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, EN High to Low

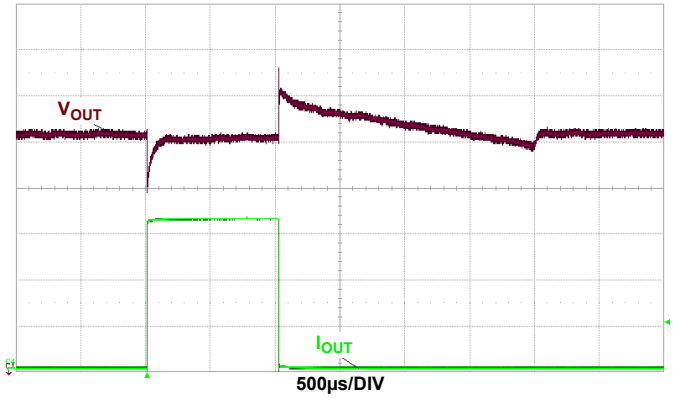

Figure 15. Load Transient, V_{IN} = 13.2.0V, V_{OUT} = 10.0V, I_{OUT} = 0A TO 1.6A, C_{OUT} = 200µF 30mΩ

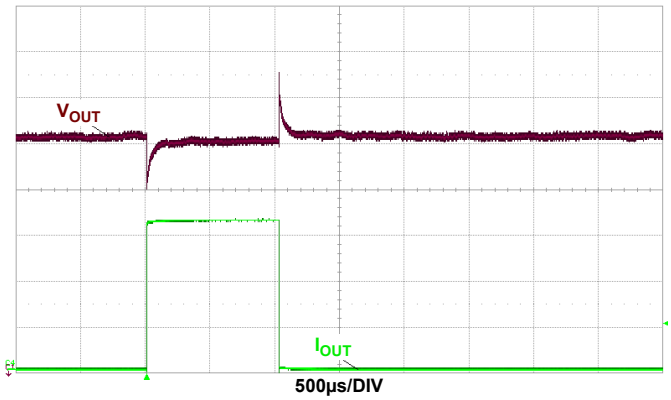

Figure 16. Load Transient, V_{IN} = 13.2V, V_{OUT} = 4.0V, I_{OUT} = 0.15A TO 1.6A, C_{OUT} = 200µF 30mΩ

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. (Cont.)

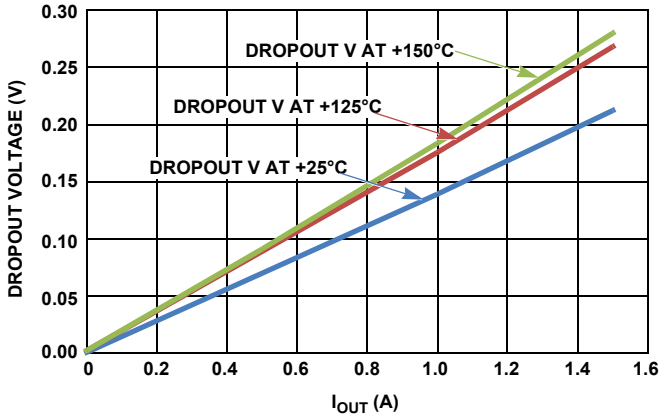

Figure 17. Dropout vs I_{OUT} AT V_{OUT} = 3.6V

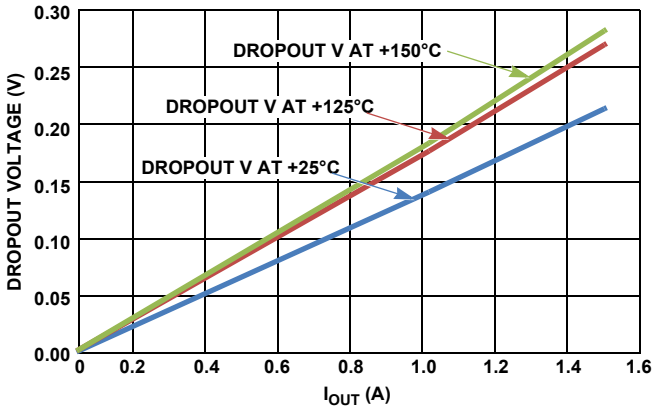

Figure 18. Dropout vs I_{OUT} AT V_{OUT} = 12.7V

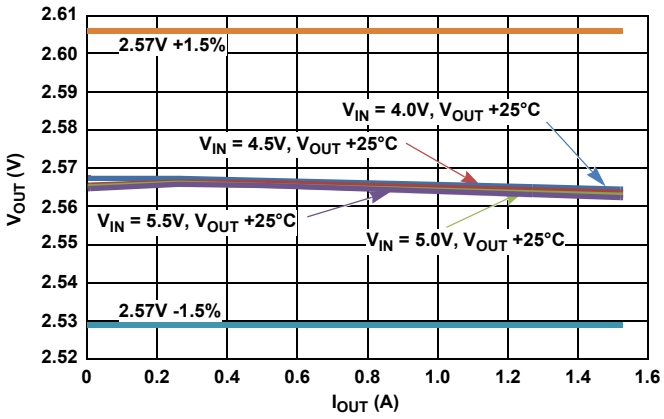

Figure 19. Load Regulation V_{OUT} vs I_{OUT}

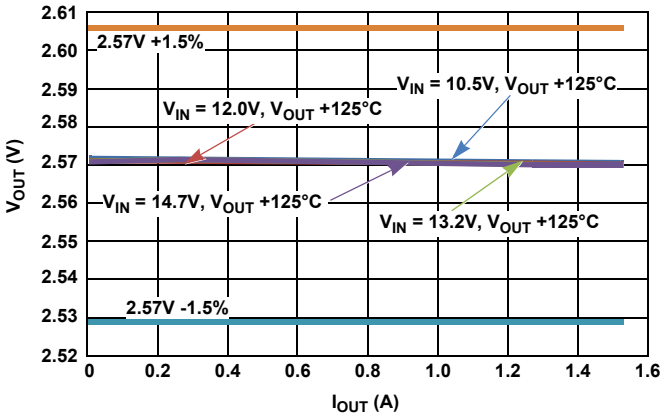

Figure 20. Load Regulation V_{ADJ} vs I_{OUT}

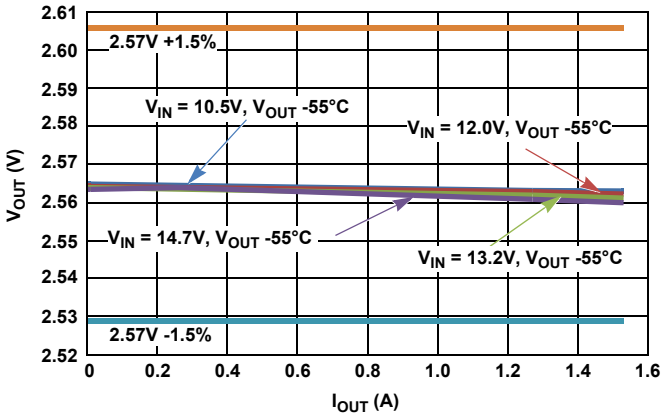

Figure 21. Load Regulation V_{OUT} vs I_{OUT}

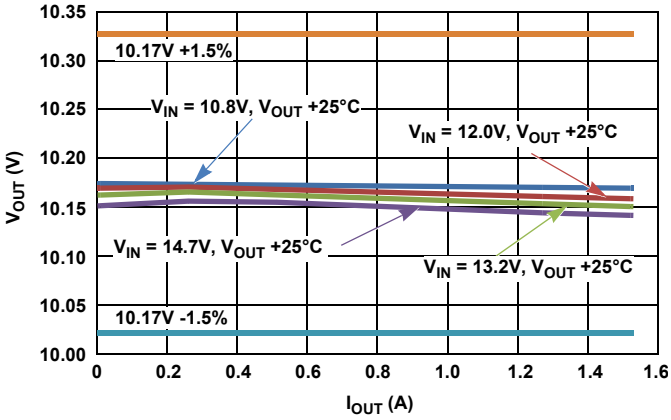

Figure 22. Load Regulation V_{ADJ} vs I_{OUT}

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. (Cont.)

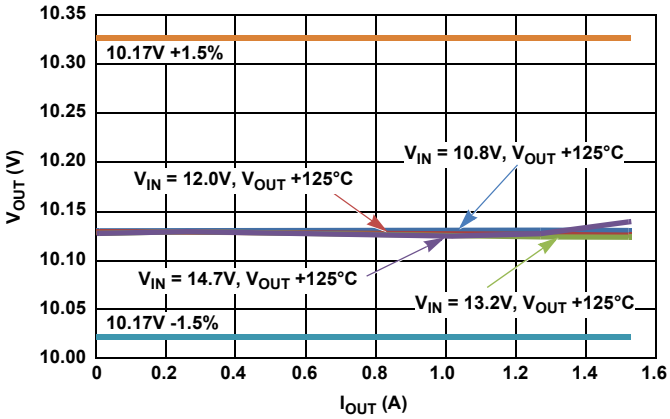

Figure 23. Load Regulation V_{OUT} vs I_{OUT}

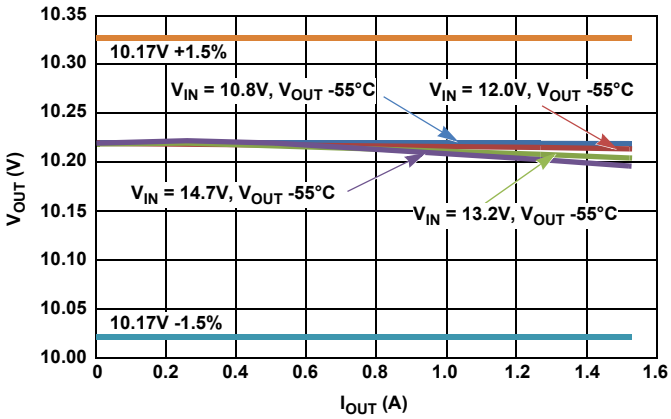

Figure 24. Load Regulation V_{ADJ} vs I_{OUT}

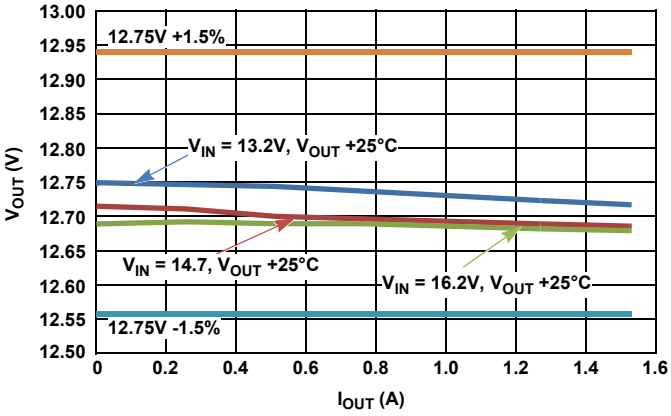

Figure 25. Load Regulation V_{OUT} vs I_{OUT}

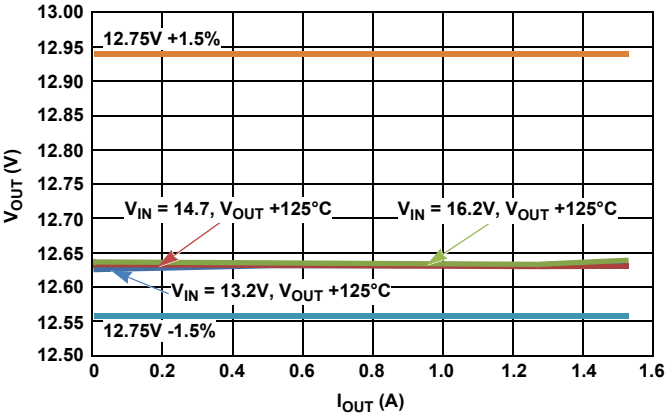

Figure 26. Load Regulation V_{OUT} vs I_{OUT}

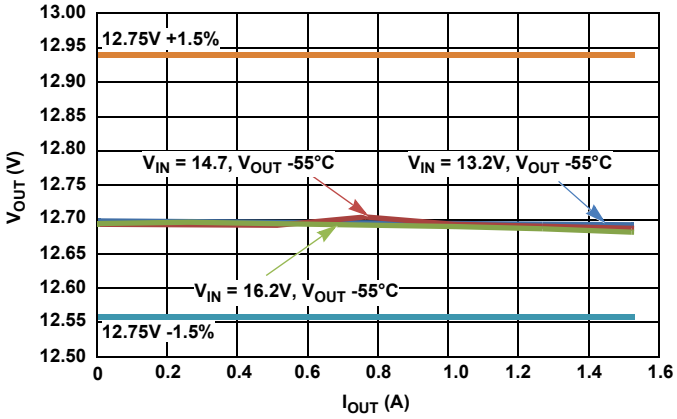

Figure 27. Load Regulation V_{OUT} vs I_{OUT}

Unless otherwise specified, V_{IN} = V_{OUT} + 0.4V, V_{OUT} = 2.5V, C_{IN} = C_{OUT} = 200µF, T_J = +25°C, I_{LOAD} = 0A. (Cont.)

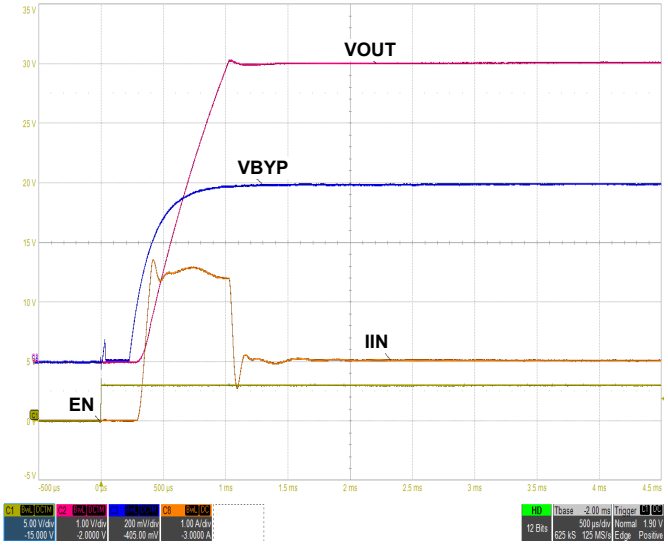

Figure 28. Soft-Start with BYP CAP = 0.2µF and EN to V_{OUT} Delay with VCCX CAP = 0.1µF V_{IN} = 6.5V, V_{OUT} = 5V, R_L = 5Ω, C_{OUT} = 220µF, R_{OCP} = 300Ω

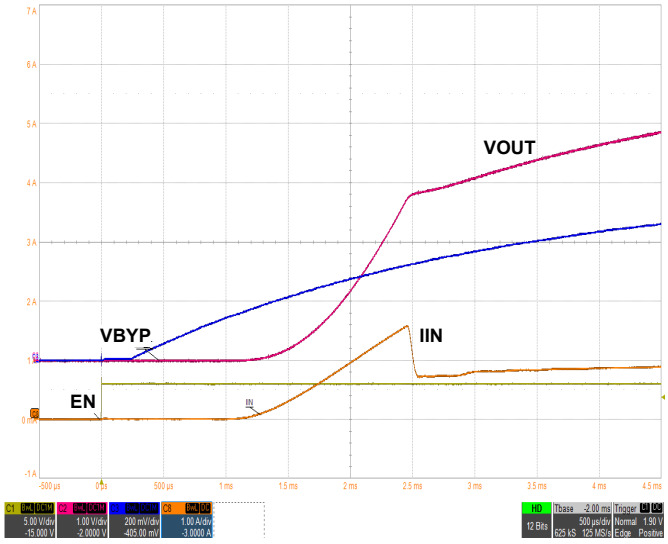

Figure 29. Soft-Start with BYP CAP = 1.9µF and EN to V_{OUT} Delay with VCCX CAP = 0.1µF V_{IN} = 6.5V, V_{OUT} = 5V, R_L = 5Ω, C_{OUT} = 220µF, R_{OCP} = 300Ω

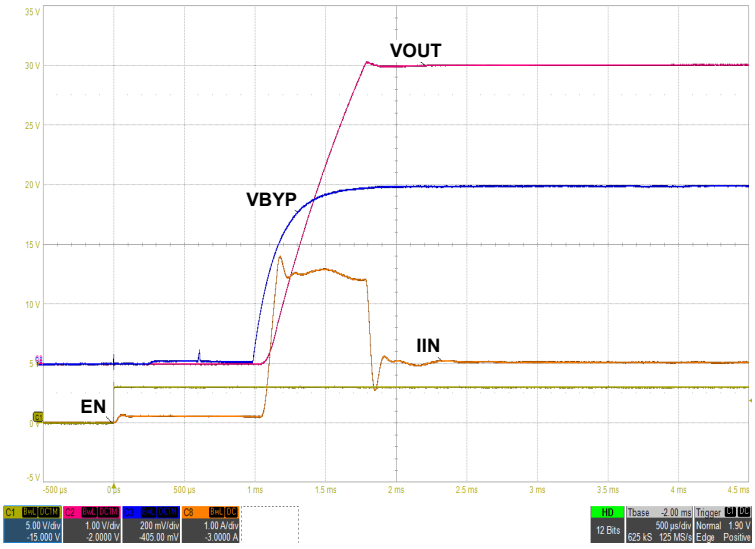

Figure 30. Soft-Start with BYP CAP = 0.2µF and EN to V_{OUT} Delay with VCCX CAP = 33µF V_{IN} = 6.5V, V_{OUT} = 5V, R_L = 5Ω, C_{OUT} = 220µF, R_{OCP} = 300Ω

5. Revision History

Revision	Date	Change
2.00	Jan 9, 2023	Applied new template. Updated Page 1 description.
1.01	Oct 24, 2022	Removed Related Literature section. Added Output Voltage Soft-Start Adjustment and Output Voltage Start-Up Delay Adjustment sections. Added Figures 28 - 30. Added Revision History section.
1.00	Aug 10, 2017	Applied New Header/Footer Updated Title Added Features, Specifications, Ordering Information, and Related Literature sections. Fixed order of user guide. Updated Schematic to new format. Corrected first label on Figures 17 and 18.
0.00	July 2, 2013	Initial release

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