ISL81100EVAL1Z

The ISL81100EVAL1Z evaluation board (Figure 4) features the ISL81100, a 100V high voltage synchronous buck controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 2MHz helps to optimize inductor size while the strong gate driver delivers up to 10A for the buck output.

Specifications

The ISL81100EVAL1Z evaluation board is designed for high-current applications. The current rating of the ISL81100EVAL1Z is limited by the inductor and FETs selected. The ISL81100EVAL1Z electrical ratings are in Table 1.

Table 1. ISL81100EVAL1Z Electrical Ratings

Parameter	Rating
Input Voltage	18V to 100V
Switching Frequency	250kHz
Output Voltage	12V
Output Current	10A
OCP Set Point	Minimum 12A at ambient room temperature

Features

- Wide input range: 18V to 100V
- High light-load efficiency in DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional Standalone CC/HICCUP
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Back biased from output to improve efficiency

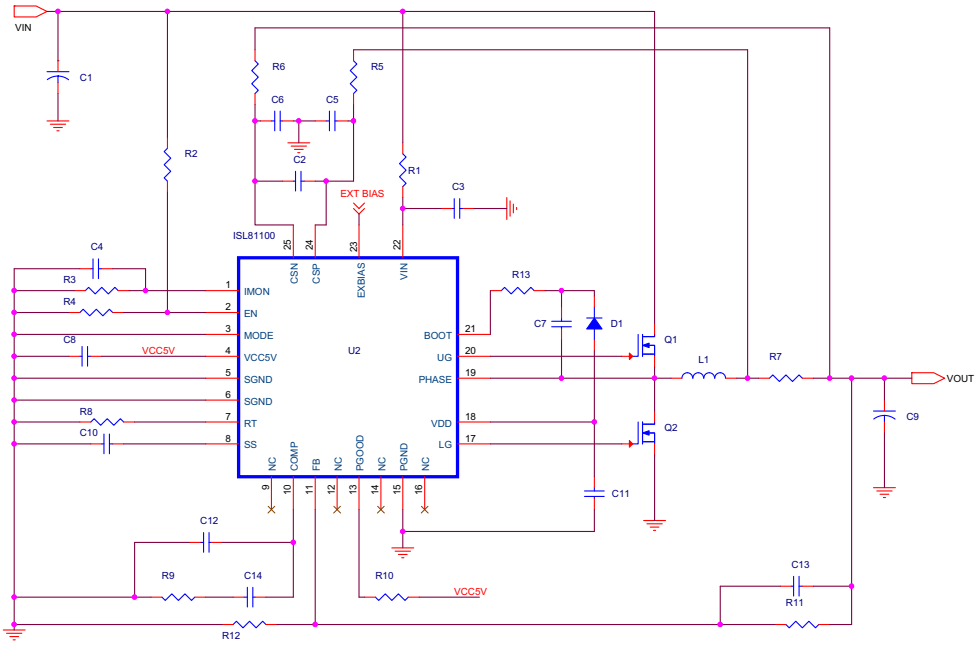


Figure 1. ISL81100EVAL1Z Block Diagram

Contents

1. Functional Description

The ISL81100EVAL1Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81100 TQFN IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3, 18V to 100V V_{IN} is supplied to J17 (+) and J18 (-). The regulated 12V output on J22 (+) and J21 (-) can supply up to 10A to the load. Due to the high power efficiency, the evaluation board can run at 10A continuously without airflow at ambient room temperature conditions.

Test points TP1 through TP23 provide easy access to the IC pin and external signal injection terminals.

Table 2 shows connector J15, which you can use to select either Forced PWM mode (floating) or DEM mode (shorting pins 1 and 2). Use connector J16 to set a constant current limit (shorting pins 1 and 2) or HICCUP OCP (floating). Use connector J3 to power the converter from the output by shorting its pins 1 and 2.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 100V power supply with at least 20A source current capability
- Electronic loads capable of sinking current up to 20A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 18V to 100V for an output voltage of 12V. If you set the output voltage to a lower value, you can reset the minimum V_{IN} to a lower value by changing the ratio of R_{12} and R_{15}. You can set VIN to the minimum EN threshold of 4.5V.

The rated load current is 10A, with the OCP point set at a minimum of 12A at ambient room temperature. The operating temperature range of this board is -40°C to +85°C.

Note: You need Airflow for higher temperature ambient conditions.

1.3 Quick Test Guide

1. Jumper J15 provides the option to select PWM or DEM. Jumper J16 provides the option to select a constant current limit or HICCUP. See Table 2 for the operating options. Ensure that the circuit is connected correctly to the supply and electronic loads before applying any power. See Figure 3 for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see Figure 2 for the proper test setup.

Table 2. Operating Options

Jumper	Position	Function
15	Floating	PWM
	Pin 1-2	DEM
16	Pin 1-2	Stand alone constant current
	Pin 2-3	Current sharing constant current
	Floating	Hiccup

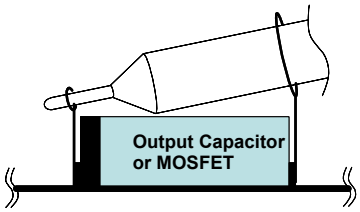


Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

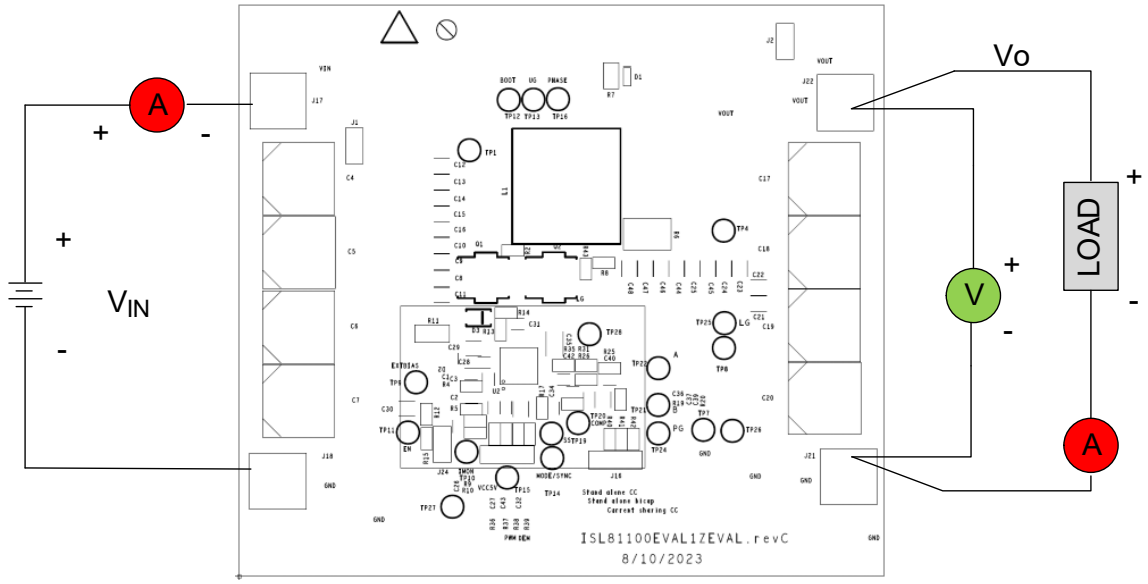


Figure 3. Proper Test Setup

2. Board Design

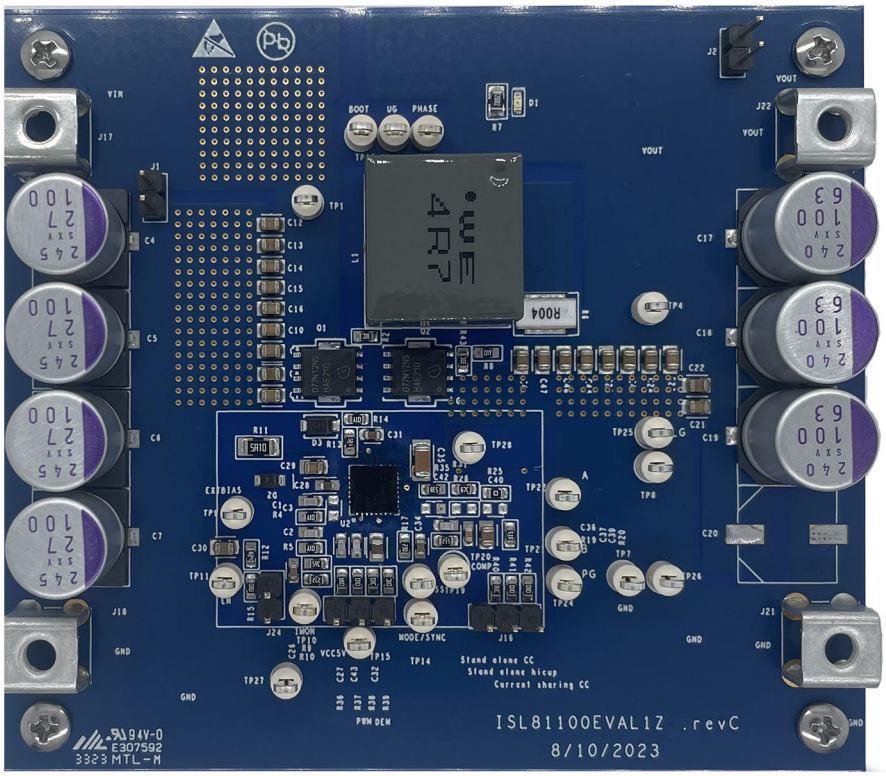


Figure 4. ISL81100EVAL1Z Evaluation Board, Top View

2.1 Layout Guidelines

Attention to Printed Circuit Board (PCB) layout requirements is necessary to implement an ISL81100-based DC/DC converter successfully. The ISL81100 switches at a high frequency; therefore, the switching times are short. Even the shortest trace has significant impedance at these switching frequencies, and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81100 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. Renesas recommends using a multilayer PCB.

Complete the following steps to optimize the PCB layout.

1. Place the input capacitors, FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high-frequency decoupling ceramic capacitors close to the MOSFETs.
2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use

separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. *Note:* **DO NOT** connect them together anywhere else.

3. Keep the loop formed by the input capacitor, the top FET, and the bottom FET as small as possible.
4. Ensure the current paths from the input capacitor to the FETs, the power inductor, and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the lower FETs. The low-side FET gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place the VDD bypass capacitor very close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via.
   Note: **DO NOT** connect the PGND pin directly to the SGND EPAD.
7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
8. Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper-filled polygons or wide, short traces to connect the junction of the upper FET, lower FET, and output inductor. Keep the PHASE node connection to the IC short. *Note:* **DO NOT** unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
10. Route all high-speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths, including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
12. Use a pair of traces with a minimum loop for the output current sensing connection.
13. Ensure the feedback connection to the output capacitor is short and direct.

2.2 Schematic Diagram

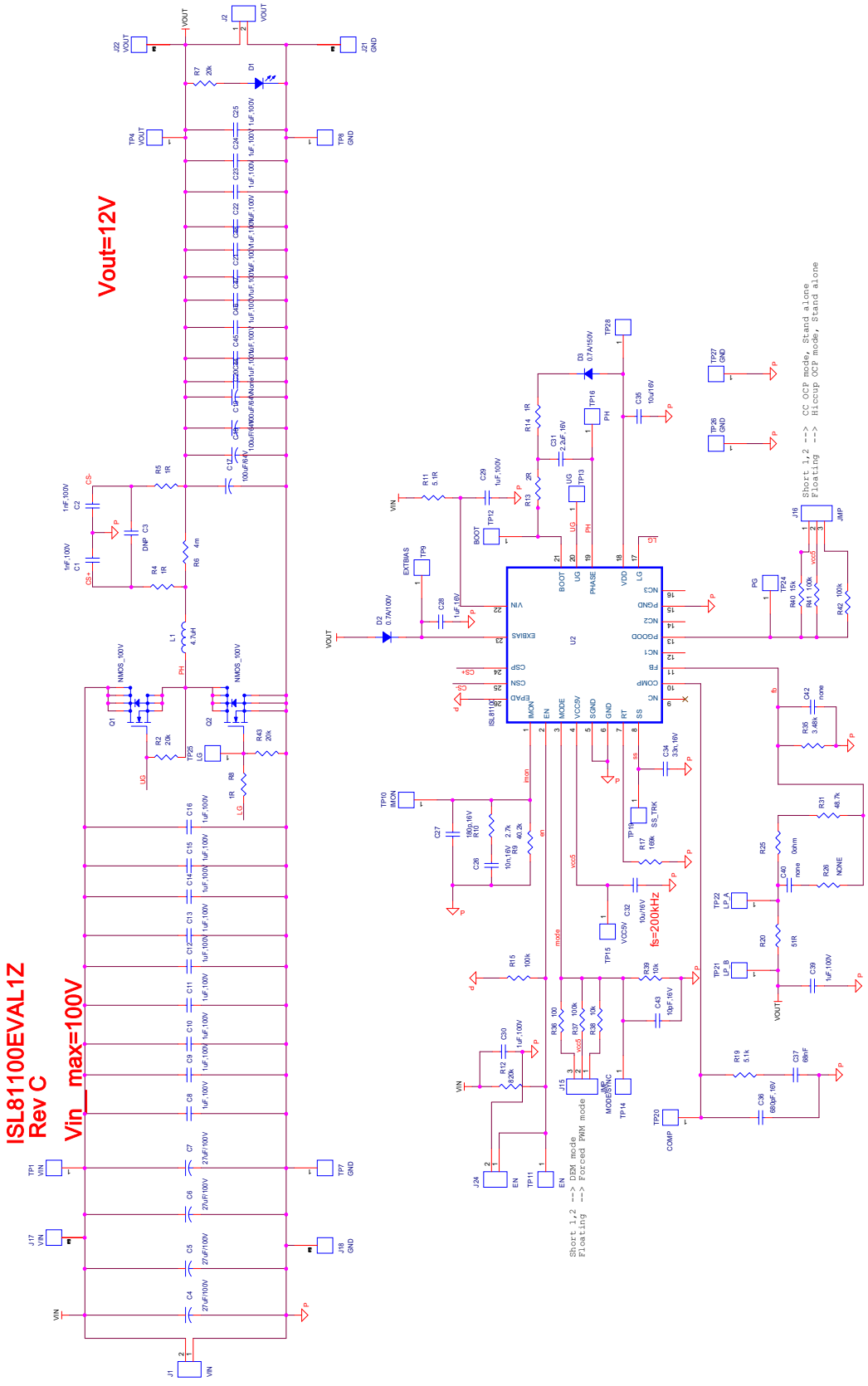


Figure 5. Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL81100EVAL1Z, REVC, ROHS	Multilayer PCB Technology	ISL81100EVAL1ZREVCPCB
2	C1, C2	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1000PF 100V 5% 0603	Murata or TDK	GRM1885C2A102JA01 or C1608C0G2A102J080AA
4	C3, C20, C40, C42	NONE, DNP	-	-
4	C4, C5, C6, C7	Aluminum Organic Polymer Capacitors 100VDC 27µF 20% 30mΩ SMD	Panasonic	100SXV27M
22	C8, C9, C10, C11, C12, C13, C14, C15, C16, C21, C22, C23, C24, C25, C29, C30, C39, C44, C45, C46, C47, C48	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1.0µF 100V 10% 0805	Murata or TDK	GRM21BC72A105KE01 or C2012X7S2A105K125AB
3	C17, C18, C19	Aluminum Organic Polymer Capacitors 63V 100µF ESR 12mΩ	Panasonic	63SXV100M
1	C26	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0.01µF 100V 10% 0603	Murata or TDK	GCM188R72A103KA37 or C1608C0G1H103J080AA
1	C27	Multilayer Ceramic Capacitors MLCC - SMD/SMT 180PF 100V 5% 0603	Murata or TDK	GCM1885C2A181JA16 or CGA3E2C0G1H181J080AA
1	C28	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1.0µF 25V 10% 0805	Murata or TDK	GCJ188R71E105KA01D C1608X7R1C105K080AC
1	C31	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 16V 2.2µF X5R 10% T: 0.8mm	Murata or TDK	GCM188C71C225ME11 or C1608X5R1C225K080AB
1	C32	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10µF 16V 10% 0603	Murata or TDK	GRM188R61C106KAALJ or C2012X6S1C106K125AC
1	C34	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0.033µF 50V 10% 0603	Murata or TDK	GCM188L81H333MA55 or CGA3E2X7R1H333K080AA
1	C35	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 16V 10µF X5R 10% T: 1.6mm	Murata or TDK	GRM31CC81E106MA12 or C3216X5R1C106K160AA
1	C36	Multilayer Ceramic Capacitors MLCC - SMD/SMT 680PF 100V 5% 0603	Murata	GCM1885C2A681JA16D
1	C37	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0.068µF 100V 10% 0603	Murata or TDK	GCM188R72A683KA37 or C1608C0G1V683J080AC
1	C43	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10PF 100V 5% 0603	Murata	GCM1885C2A100JA16D
1	D1	Standard LEDs - SMD Green Clear 571nm	Lite-On	LTST-C191KGKT

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	D2	Schottky Diodes & Rectifiers SCHOTTKY DIODE 100V 0.7A	ROHM Semiconductor	RB578VAM100
1	D3	Schottky Diodes & Rectifiers 150V 1A Schottky Barrier Rectifier	Onsemi	S115FP
4	J17, J18, J21, J22	HDWARE, TERMINAL, M4 METRIC SCREW, TH, 4P, SNAP-FIT, ROHS	Keystone	7795
2	J1, J2	CONN-HEADER, 1x2, BRKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
2	J15, J16	CONN-HEADER, 1x3, BREAKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	L1	Power Inductors - SMD WE-XHMI SMD 1510 4.7uH 17A 3.5mΩ	Wurth	74439370047
1	U2	100V Buck PWM Controller, 25P, TQFN, 5×5, ROHS	Renesas Electronics America	ISL81100FRTZ
2	Q1, Q2	MOSFET N-Ch 100V 90A TDSON-8	Infineon	BSC070N10NS5ATMA1
1	R26	DNP		
2	R2, R43	RES SMD 20kΩ 1% 1/10W 0603	Yageo	RC0603FR-0720KL
4	R4, R5, R8, R14	RES SMD 1Ω 1% 1/10W 0603	Yageo	RC0603FR-071RL
1	R6	RES SMD 0.004Ω 3W 2512 WIDE	Susumu	KRL6432E-M-R004-F-T1
1	R7	RES SMD 20kΩ 1% 1/10W 0805	Yageo	RC0805FR-0720KL
1	R9	RES SMD 40.2Ω 1% 1/10W 0603	Yageo	RC0603FR-0740K2L
1	R10	RES SMD 2.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-072K7L
1	R11	RES SMD 5.1Ω 1% 1/10W 1206	Yageo	RC1206FR-075R1L
1	R12	RES SMD 820kΩ 1% 1/10W 0603	Yageo	RC0603FR-07820KL
1	R13	RES SMD 2Ω 1% 1/10W 0603	Yageo	RC0603FR-072RL
4	R15, R37, R41, R42	RES SMD 100kΩ 1% 1/10W 0603	Yageo	RC0603FR-07100KL
1	R17	RES SMD 169kΩ 1% 1/10W 0603	Yageo	RC0603FR-07169KL
1	R19	RES SMD 5.1kΩ 1% 1/10W 0603	Yageo	RC0603FR-075K1L
1	R20	RES SMD 51Ω 1% 1/10W 0603	Yageo	RC0603FR-0751RL
1	R25	RES SMD 0Ω 1% 1/10W 0603	Yageo	RC0603FR-070RL
1	R31	RES SMD 48.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-0748K7L
1	R35	RES SMD 3.48kΩ 1% 1/10W 0603	Yageo	RC0603FR-073K48L
1	R36	RES SMD 100Ω 1% 1/10W 0603	Yageo	RC0603FR-07100RL
2	R38, R39	RES SMD 10kΩ 1% 1/10W 0603	Yageo	RC0603FR-0710KL
0	R40	RES SMD 15kΩ 1% 1/10W 0603	Yageo	RC0603FR-0715KL
21	TP1, TP4, TP7-TP16, TP19-TP22, TP24-TP28	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	Keystone	5007
2	J15, J16	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	Sullins	SPC02SYAN
4	Four corners	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Keystone	2204

2.4 Board Layout

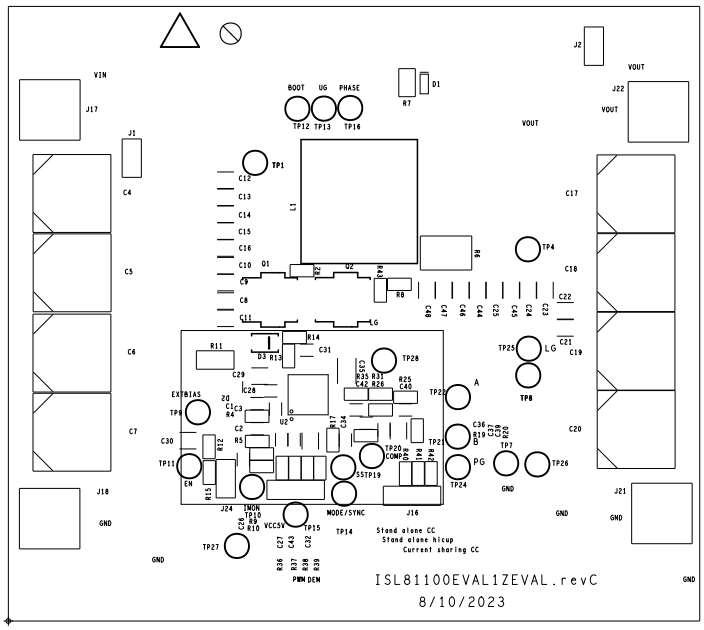


Figure 6. Silkscreen Top

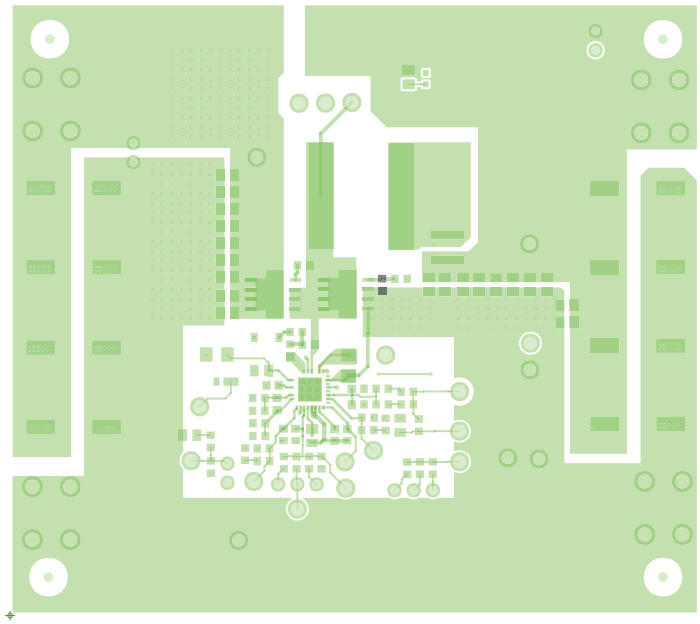


Figure 7. Top Layer

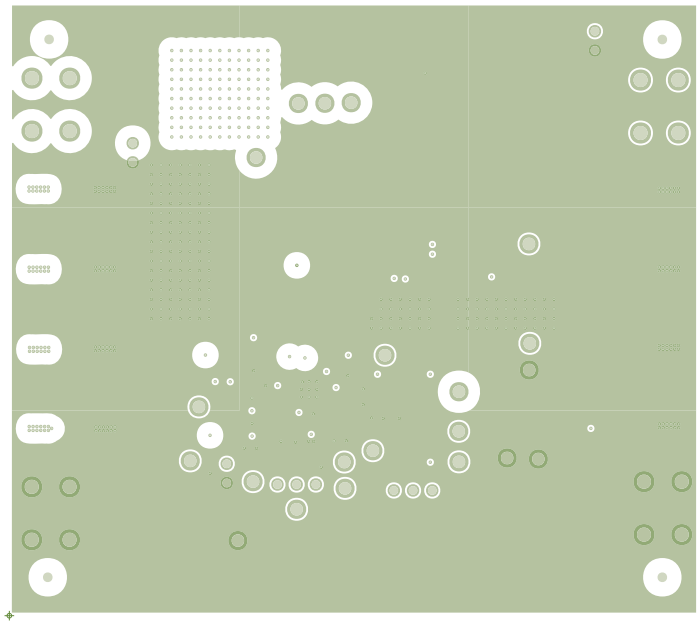


Figure 8. Second Layer (Solid Ground)

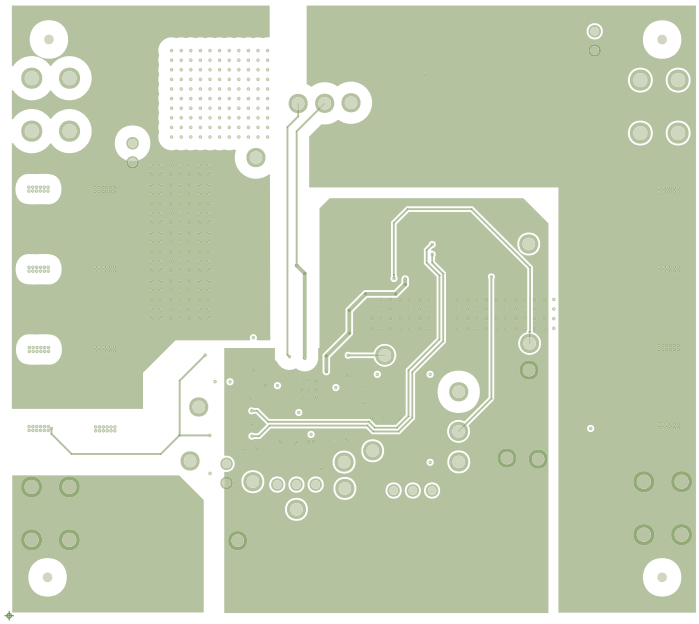


Figure 9. Third Layer

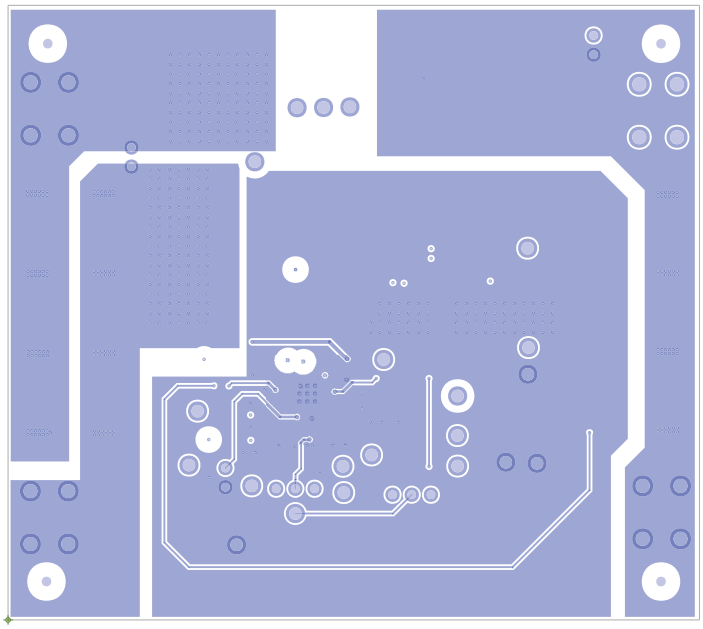


Figure 10. Bottom Layer

3. Design Example

3.1 Design Requirements

Parameter	Rating
Input Voltage	18V to 100V
Switching Frequency	250kHz
Output Voltage	12V
Output Current	10A
OCP Set Point	12.5A
PWM Mode	Forced PWM
OCP Mode	Constant current

3.2 Frequency Setting

The resistor R_T (R_{17}) determines the default switching frequency of the PWM controller. The resistor adjusts the default switching frequency from 100kHz to 2MHz. Calculate the R_T value for f_{SW} = 250kHz using Equation 1, where f_{SW} is the switching frequency in MHz.

(EQ. 1) $$R_T = \left(\frac{44}{f_{SW}} - 7.5\right) = \frac{44}{0.25} - 7.5 = 168.5k\Omega$$

Select a standard value resistor R_T = 169kΩ.

3.3 Output Voltage Setting

You can set the output voltage from 0.8V to a level determined by the feedback voltage divider. A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB_OUT pin. With V_{OUT} = 12V and R_{FBO1} (R_{31}) = 48.7k, use Equation 2 to calculate the R_{FBO2} (R_{35}) value, where R_{FBO1} (R_{31}) is the top resistor of the feedback divider network and R_{FBO2} (R_{35}) is the bottom resistor connected from FB_OUT to ground.

(EQ. 2) $$R_{FBO2} = \frac{0.8V \times R_{FBO1}}{V_{OUT} - 0.8V} = \frac{0.8V \times 48.7k\Omega}{12V - 0.8V} = 3.48k\Omega$$

To avoid an unstable state during a hiccup, the value of R_{FBO1} and R_{FBO2} in parallel should be no less than 3k. Select a standard value resistor R_{FBO2} = 3.48kΩ.

3.4 UVLO Setting

The ISL81100 has input UVLO protection. The PWM modulator is enabled when the EN/UVLO pin voltage reaches 1.8V. You can implement an accurate UVLO feature using a voltage divider by feeding the VIN into the EN/UVLO pin. After selecting the VIN rising and falling thresholds, you can calculate R_{12} using Equation 3.

(EQ. 3) $$R_{12} = \frac{V_{INRISE}V_{UVLO\_THF} - V_{INFALL}V_{UVLO\_THR}}{I_{UVLO\_HYST}V_{UVLO\_THR} - I_{UVLO\_LSC}V_{UVLO\_THF}} = 820k\Omega$$

You can calculate R_{15} using Equation 4, where I_{UVLO_HYST} is the UVLO hysteresis current, typically 4.4µA.

(EQ. 4) $$R_{15} = \frac{V_{INRISE}V_{UVLO\_THF} - V_{INFALL}V_{UVLO\_THR}}{I_{UVLO\_HYST} \times (V_{INRISE} - V_{UVLO\_THR}) + I_{UVLO\_LSC} \times (V_{INFALL} - V_{UVLO\_THF})} = 100k\Omega$$

3.5 Soft-Start Capacitor

The soft-start capacitor C_{SS} (C_{34}) value (connected from SS/TRK1 to GND) sets the soft-start time for dual-phase. You can calculate the soft-start time with C_{34} = 33nF using Equation 5.

(EQ. 5) $$t_{SS} = 0.8V\left(\frac{C_{SS}}{2\mu A}\right) = 0.8V \times \left(\frac{33nF}{2\mu A}\right) = 13.2ms$$

When the soft-start time set by the external C_{34} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

3.6 MOSFET Considerations

The MOSFETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations. The maximum V_{IN} voltage defines the maximum operating voltage of the MOSFETs.

You can calculate the power loss of the upper MOSFET for each phase using Equation 6 and calculate the power loss of the lower MOSFET for each phase using Equation 7. The equations assume linear voltage-current transitions and do not model power loss due to the reverse recovery for the body diode of the lower MOSFET.

The turn-on gate resistance includes the following:

- A boot resistor
- A upper driver pull-up resistor
- The gate resistance of the MOSFET

The turn-off gate resistance includes the following:

- A upper driver pull-down resistor
- The gate resistance of the MOSFET

(EQ. 6)

$$P_{UPPERMAX} = \frac{(I_{OUT}{}^2)(r_{DS(ON)})(V_{OUT})}{V_{INMAX}} + \frac{(I_{OUT})(V_{INMAX})(t_{SW})(f_{SW})}{2}$$

$$= \frac{(10A^2)(6m\Omega)(12V)}{100V} + \frac{(10A)(100V)\left(\frac{6nC}{\left(\frac{8V-4.9V}{8.8\Omega}\right)} + \frac{6nC}{\left(\frac{4.9V}{2.5\Omega}\right)}\right)(250kHz)}{2} = 0.072W + 1.632W = 1.7W$$

(EQ. 7)

$$P_{LOWERMAX} = \frac{(I_{OUT}{}^2)(r_{DS(ON)})(V_{INMAX} - V_{OUT})}{V_{INMAX}}$$

$$= \frac{(10A)^2(6m\Omega)(100V - 12V)}{100V} = 0.53W$$

Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

3.7 Inductor Selection

The inductor value determines the ripple current of the converter. The ripple voltage is a function of the ripple current and the output capacitor(s) ESR. Assume the ripple current ratio is 90% of the average inductor current at the maximum input voltage and the full output load condition. You can calculate the inductor value for each phase using Equation 8.

(EQ. 8)

$$L_{INMIN} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(0.9 \times I_{OUTMAX})(V_{INMAX})} = \frac{(100V - 12V)(12V)}{(250kHz)(0.9 \times 10A)(100V)} = 4.69\mu H$$

The recommended inductor value is 4.7µH. Then the ripple current and peak current are calculated using Equation 9, Equation 10, and Equation 11.

(EQ. 9)

$$\Delta I_{LMAX} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{INMAX})} = \frac{(100V - 12V)(12V)}{(250kHz)(4.7\mu H)(100V)} = 8.98A$$

(EQ. 10)

$$I_{LRMS} = \sqrt{(I_{OUTMAX})^2 + \frac{(\Delta I_{LMAX})^2}{12}} = \sqrt{(10A)^2 + \frac{(8.98A)^2}{12}} = 10.33A$$

(EQ. 11) $$I_{LPEAKMAX} = I_{OUTOCP} + \frac{\Delta I_{LMAX}}{2} = 12A + \frac{8.98A}{2} = 16.49A$$

The saturation current of the inductor should be larger than 16.49A. The heat rating current of the inductor should be larger than 10.33A.

You can calculate the maximum DC power dissipation in the inductor using Equation 12.

(EQ. 12) $$P_{LMAX} = (I_{LRMS})^2(DCR) = (10A)^2 \times (3.5m\Omega) = 0.37W$$

3.8 Output Capacitor Selection

Equation 13 shows the minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor, where C_{OUTMIN} is the minimum output capacitor(s) required, I_{TRAN} is the transient load current step, and ΔV_{OUT} is the drop in output voltage allowed during the load transient.

(EQ. 13) $$C_{OUTMIN} = \frac{L(I_{TRAN})^2}{2(V_{INMIN} - V_{OUT})(\Delta V_{OUT})} = \frac{4.7\mu H \times (10A - 0A)^2}{2(18V - 12V)\left(12V \times \frac{1.5}{100}\right)} = 217.6\mu F$$

Choose a capacitor no less than 217.6µF. 300µF Aluminum Organic Polymer Capacitors and 5µF MLCC in total are used for this board.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 14.

(EQ. 14) $$V_{RIPPLE} = \Delta I_{LMAX} \times ESR = 8.98A \times 10m\Omega = 89.8mV$$

3.9 Input Capacitor Selection

The critical parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage, and 1.5 times is a conservative guideline. The AC RMS input current varies with the load given in Equation 15.

(EQ. 15) $$I_{RMS} = I_{OUT} \times \sqrt{D - D^2}$$

The maximum RMS current for the input capacitance occurs at D = 0.5. Therefore, Equation 16 shows the maximum AC RMS current.

(EQ. 16) $$I_{RMSMAX} = 10 \times \sqrt{0.5 - 0.5^2} = 5A$$

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high-frequency decoupling and bulk capacitors to supply the RMS current. Four 27µF Aluminum Organic Polymer capacitors with 12A rating current and nine 1µF ceramic capacitors are used to share the 5A RMS input current on this board.

3.10 First Level Peak Current Limit and Sense Resistor Selection

The sense resistor R_S (R_6) senses the inductor peak current. When the voltage drop on R_S reaches the set point $V_{OCSET-CS}$ typical 82mV, it triggers the pulse-by-pulse peak current limit. With the current limit set point $I_{OCPP} = I_{OUTMAX} = 10A$, you can calculate the sense resistor value using Equation 17.

(EQ. 17) $$R_6 = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{82mV}{10A} = 8.2m\Omega$$

Select a standard value resistor R_S = 4mΩ. Then, calculate the actual peak current limit using Equation 18.

(EQ. 18) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{82mV}{4m\Omega} = 20.5A$$

Calculate the maximum power dissipation in R_S using Equation 19.

(EQ. 19) $$P_{RSMAX} = (I_{OUT})^2 R_S = (10A)^2(4m\Omega) = 0.4W$$

Therefore, a sense resistor with 1W power rating is sufficient for this application.

3.11 Second Level Hiccup Peak Current Protection

In the output dead short condition, especially at high V_{IN}, the inductor current runs away with the minimum off PWM duty. The ISL81100 integrates a second-level hiccup type of peak current protection. You can calculate the second level peak current protection set point I_{OCPP2} using Equation 20.

(EQ. 20) $$I_{OCPP2} = \frac{V_{OCSET-CS-HIC}}{R_S} = \frac{115mV}{4m\Omega} = 28.75A$$

3.12 Output Average Overcurrent Protection and R_{IM} Selection

The ISL81100 provides either constant current or hiccup type of overcurrent protection for average output current. A resistor connected between the PGOOD pin and VCC5V sets the OCP mode. With the output constant current/hiccup set point I_{OUTOCP} = 12A, calculate the current monitoring resistor R_{IM} (R_9) using Equation 21, where $I_{CSOFFSET}$ is the output current sense op amp internal offset current, typical 20µA.

(EQ. 21) $$R_{IM} = \frac{1.2}{I_{OUTOCP} \times R_S \times Gm_{CS} + I_{CSOFFSET}} = \frac{1.2V}{12Ax4m\Omega x195\mu S + 20\mu A} = 40.87k\Omega$$

Select a standard value resistor R_{IM} = 40.2kΩ.

3.13 PWM Mode Selection

You can set the ISL81100 to either forced PWM or DE. The voltage on the MODE/SYNC pin sets the mode. This design sets a header (J15) with three resistors connected with MODE/SYNC pin and VCC5V. Floating the jumper is PWM mode, connecting pin1 and pin2 of header sets it to DEM mode, for more details see Table 2.

3.14 Overcurrent Protection Mode Selection

Selecting a different value for the resistor R_{OCMODE} (R_{40}, R_{41}, R_{42}) connected between PG_OC_MODE and VCC5V sets the ISL81100 to a constant current or hiccup type of overcurrent protection for average output current. Calculate the boundary resistor values for R_{OCMODE} using Equation 22 and Equation 23.

(EQ. 22) $$R_{OCMODEL} = \frac{5V}{60\mu A} = 83.3k\Omega$$

(EQ. 23) $$R_{OCMODEH} = \frac{5V}{190\mu A} = 26.3k\Omega$$

A resistor less than 26.3kΩ sets the converter to the stand-alone constant current mode. A resistor higher than 26.3kΩ and less than 83.3kΩ sets the converter to current sharing constant current mode. A resistor higher than 83.3kΩ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges, Renesas recommends using 15kΩ to set the stand-alone constant current, 50kΩ to set the current sharing constant current mode, and 100kΩ to select the Hiccup mode.

3.15 SYNC operation

Connect the MODE/SYNC pin to an external clock for synchronization. When the external clock frequency is higher than the internal set frequency, the controller works at the external clock frequency. Make the synchronization signal falling edge far away with the UG falling edge, or use longer rising and falling times of the synchronization signal.

3.16 Feedback Loop Compensation

Due to the current loop feedback, the modulator has a single pole response with a -20dB slope at a frequency determined by the load using Equation 24, where R_O is load resistance and C_O is total load capacitance for each phase. A Type 2 compensation circuit is usually sufficient for this modulator.

(EQ. 24) $$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} = \frac{1}{2\pi \cdot \frac{12V}{10A} \cdot 1081\mu F} = 122Hz$$

Figure 11 shows a Type 2 amplifier and its response, along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole. The R_{COMP}, C_{COMP1}, and C_{COMP2} network connected on the Gm regulator output COMP pin is needed to compensate the loop for stable operation. The loop stability can be affected by many different factors, such as V_{IN}, V_{OUT}, load current, switching frequency, inductor value, output capacitance, and the compensation network on the COMP pin.

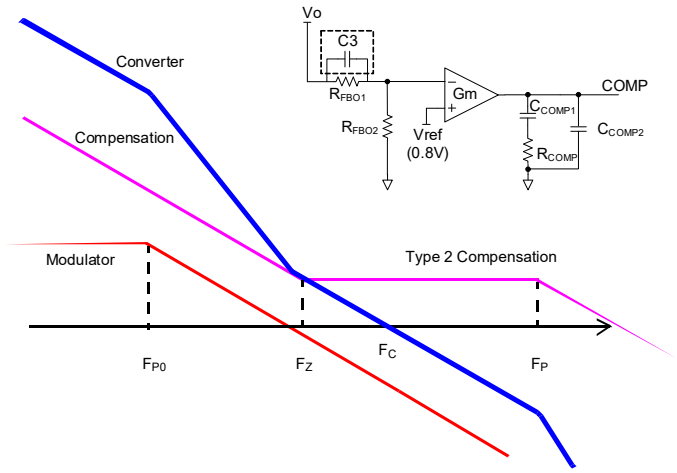


Figure 11. Feedback Loop Compensation

Choose high amplifier zero frequency and modulator gain to satisfy most typical applications. The crossover frequency appears where the modulator attenuation equals the amplifier's high-frequency gain. The crossover frequency F_C is about 1/10 to 1/30 of the switching frequency. Large-value capacitors are used on the output side to fulfill the various applications. Therefore, a reasonable target crossover frequency F_C in this application is 4kHz.

Place the compensation zero F_Z between F_{PO} and F_C. Setting F_Z to 0.5kHz, with C_{COMP1} (C_{37}) = 68nF, calculate the R_{COMP} (R_{19}) using Equation 25.

(EQ. 25) $$R_{COMP} = \frac{1}{2\pi \cdot F_Z \cdot C_{COMP1}} = \frac{1}{2\pi \cdot 0.5kHz \cdot 68nF} = 4.6k\Omega$$

Select a standard value resistor R_{COMP} = 5.1kΩ. A larger C_{COMP1} makes the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. Lower R_{COMP} improves stability but slows the loop response.

Place a high-frequency pole F_P by a capacitor C_{36} parallel to R_{COMP} and C_{COMP1}. Set the frequency of this pole at about 7 to 10 times of crossover frequency F_C to attenuate switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target F_P = 45kHz, calculate the C_{COMP2} using Equation 26.

(EQ. 26) $$C_{COMP2} = \frac{1}{2\pi \cdot R_{COMP1} \cdot F_P} = \frac{1}{2\pi \cdot 5.1k\Omega \cdot 45kHz} = 693pF$$

Select a standard value capacitor C_{COMP2} = 680pF.

Connecting capacitor C_{40} in parallel with the upper resistor R_{31} of the divider can achieve some phase boost. These values provide a good starting point for the compensation design, and you should optimize the final compensation network with a bench test.

4. Typical Performance Curves

V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

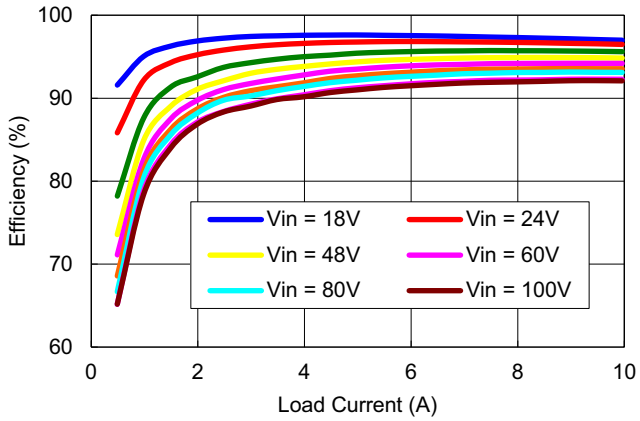


Figure 12. Efficiency, Forced PWM

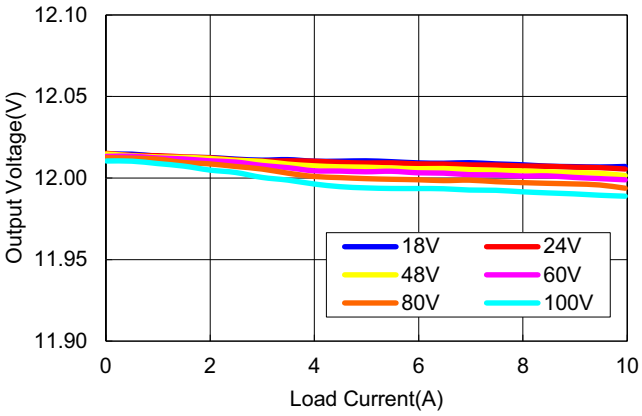


Figure 13. Load Regulation, Forced PWM

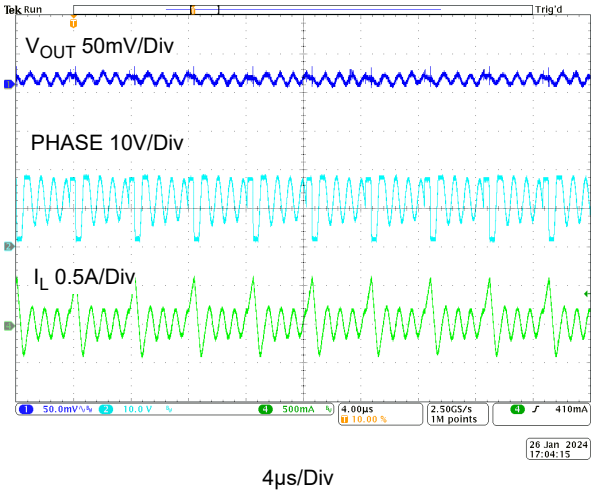


Figure 14. DEM Mode Waveforms, V_{IN} = 18V, I_{OUT} = 0A

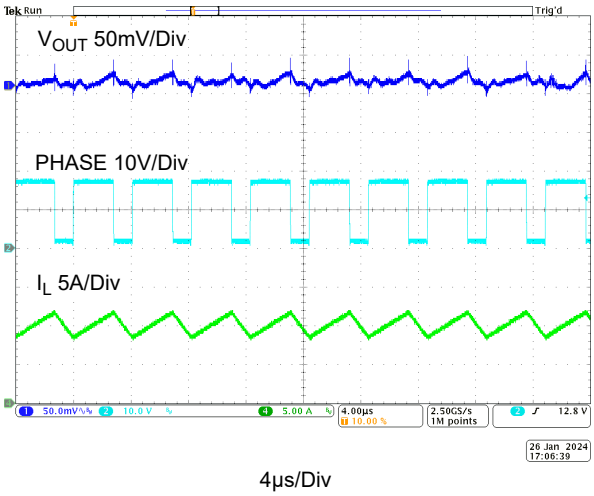
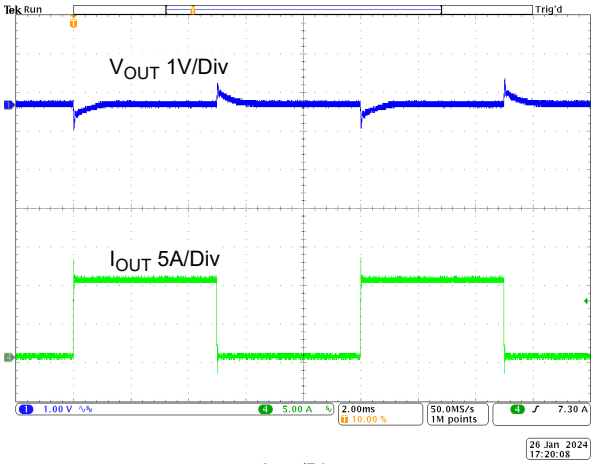


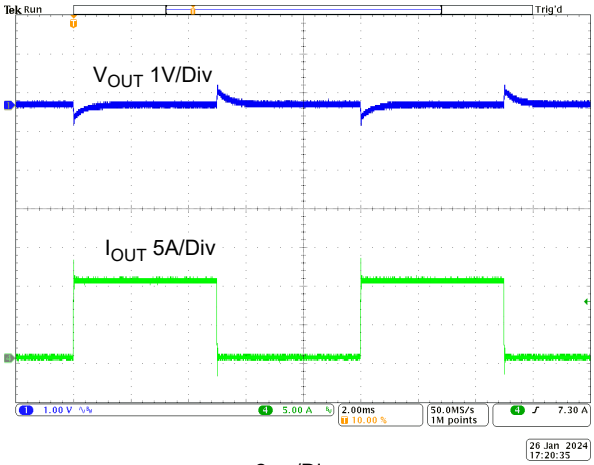
Figure 15. V_{IN} = 18V, I_{OUT} = 10A, Forced PWM Mode

V_{IN} = 48V, T_A = 25°C, unless otherwise noted. (Cont.)



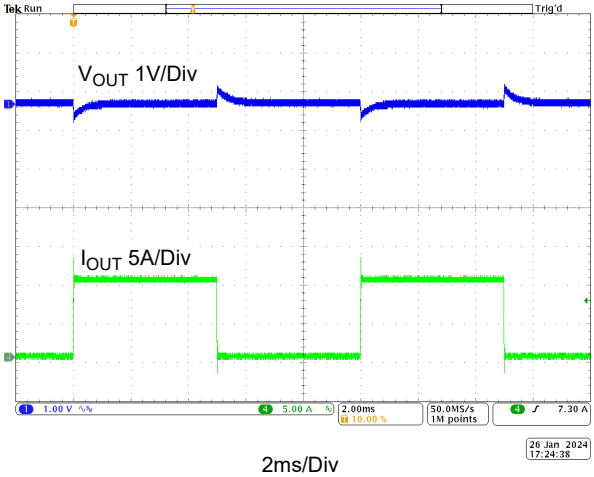
2ms/Div

Figure 16. Load Transient, V_{IN} = 18V, I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM



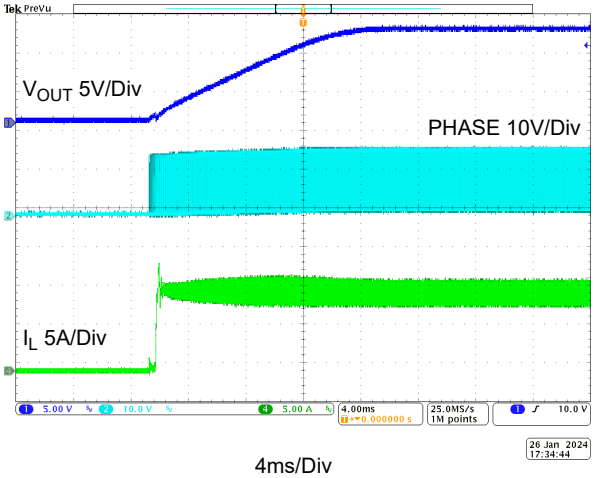
2ms/Div

Figure 17. Load Transient, V_{IN} = 48V, I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM



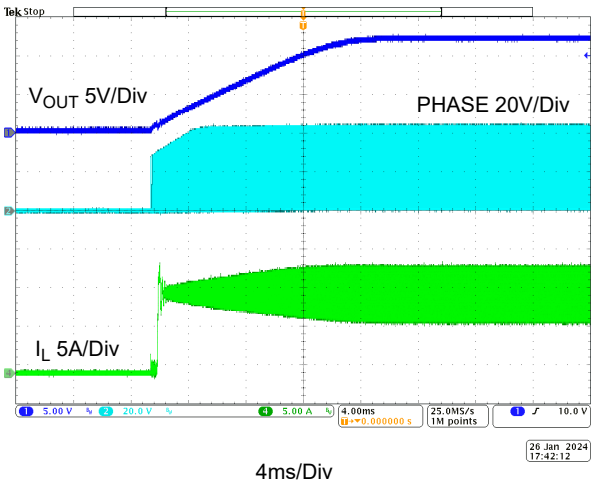
2ms/Div

Figure 18. Load Transient, V_{IN} = 100V, I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM



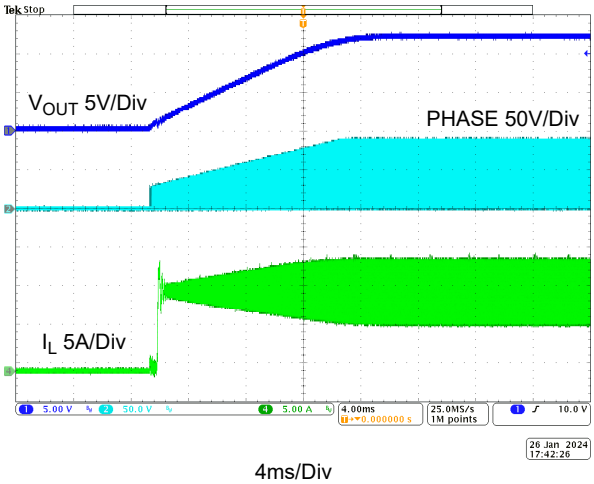
4ms/Div

Figure 19. Start-Up Waveform, V_{IN} = 18V, I_{OUT} = 10A, Forced PWM



4ms/Div

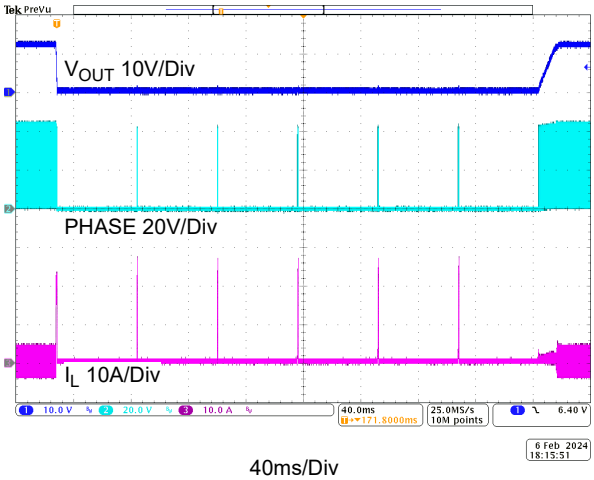
Figure 20. Start-Up Waveform, V_{IN} = 48V, I_{OUT} = 10A, Forced PWM



4ms/Div

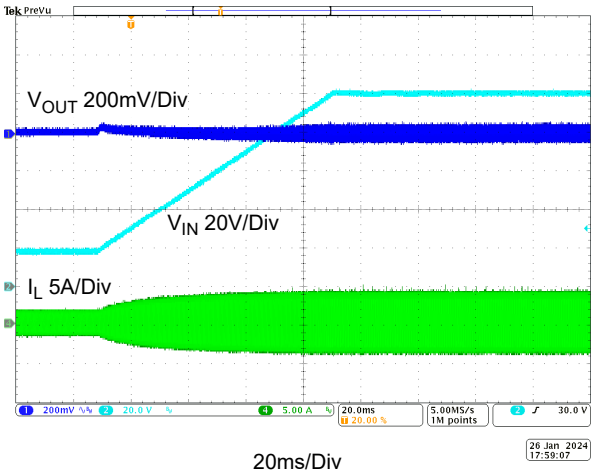
Figure 21. Start-Up Waveform, V_{IN} = 100V, I_{OUT} = 10A, Forced PWM

V_{IN} = 48V, T_A = 25°C, unless otherwise noted. (Cont.)



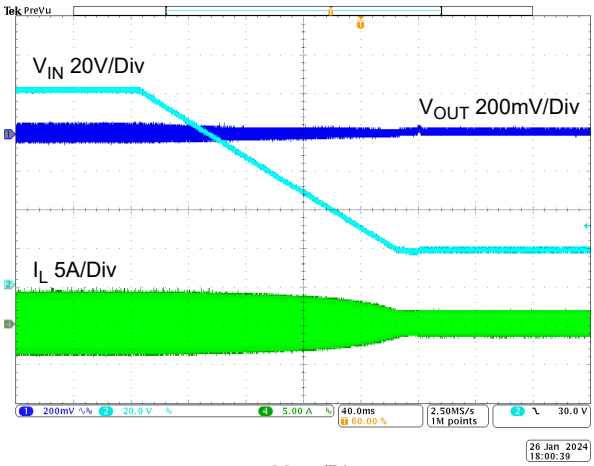
40ms/Div

Figure 22. OCP Response, Output Short-Circuited from No Load to Ground and Released, Forced PWM Mode, V_{IN} = 48V



20ms/Div

Figure 23. Line Transient, V_{IN} = 18V to 100V, 1V/ms, I_{OUT} = 0A



20ms/Div

Figure 24. Line Transient, V_{IN} = 100V to 18V, 1V/ms, I_{OUT} = 0A

5. Ordering Information

Part Number	Description
ISL81100EVAL1Z	High Voltage Buck Controller Evaluation Board

6. Revision History

Rev.	Date	Description
1.02	Feb 27, 2024	Updated the Functional Description section. Updated Figures 1, 3, 4, and 13 - 24.
1.01	Nov 2, 2023	Updated features section. Updated Table 2. Updated Figures 1, 3, 4-10 Updated Layout Guidelines section. Updated BOM. Minor updates to the following sections: ▪ UVLO Setting ▪ Soft-Start Capacitor ▪ Output Capacitor Selection ▪ Output Average Overcurrent Protection and RIM Selection ▪ PWM Mode Selection ▪ SYNC operation ▪ Feedback Loop Compensation ▪ Typical Performance Curves Removed the Parallel Connection section.
1.00	Jun 26, 2023	Initial release

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