ISL81807EVAL1Z

The ISL81807EVAL1Z dual-phase evaluation board (shown in Figure 4) features the ISL81807, an 80V high voltage dual synchronous boost controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 2MHz helps to optimize inductor size while the strong gate driver delivers up to 240W for the boost output.

Specifications

The ISL81807EVAL1Z dual-phase evaluation board is designed for high output voltage applications. The current rating of the ISL81807EVAL1Z is limited by the FETs and inductor selected. The ISL81807EVAL1Z electrical ratings are shown in Table 1.

Table 1. ISL81807EVAL1Z Electrical Ratings

Parameter	Rating
Input Voltage	12V to 36V
Switching Frequency	500kHz
Output Voltage	36V/48V/60V/80V
Output Power	150W(V_{IN} = 12V), 240W(V_{IN} = 24V/36V)
OCP Set Point (pulse by pulse)	20.5A
OCP Set Point (input average)	18A

Features

- Wide input range: 12V to 36V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- External bias to improve efficiency
- Optional input/output average OCP

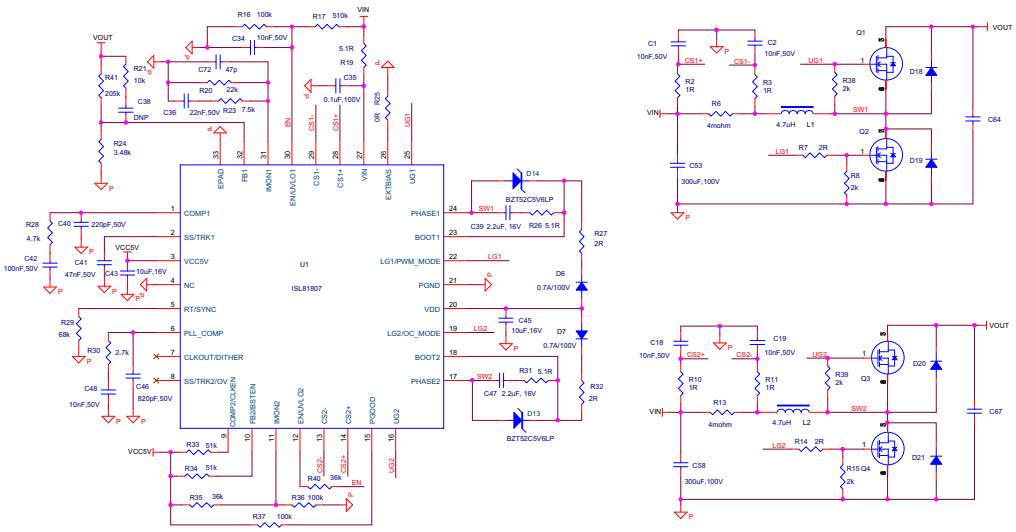

Figure 1. ISL81807EVAL1Z Block Diagram

Contents

1. Functional Description

The ISL81807EVAL1Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81807. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3, 12V to 36V V_{IN} is supplied to TP1(+) and TP2 (-). The regulated output on TP3 (+) and TP8 (-) can supply up to 240W to the load. Because of the high-power efficiency, the evaluation board can run at 240W continuously without airflow at ambient room temperature conditions.

As shown in Table 2, connector J3/J4/J5 provides a selection of either output voltage of 80V/60V/48V/36V. The output voltage is 36V when only J5 is added with a jumper. The output voltage is 48V when only J4 is added with a jumper. The output voltage is 60V when only J3 is added with a jumper. The output voltage is 80V when none of J3, J4, J5 is added with a jumper.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 40V power supply with at least 20A source current capability
- Electronic loads capable of sinking current up to 7A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 12V to 36V.

The rated load current is 240W with the input average OCP point set at a minimum 18A at ambient room temperature conditions. The operating temperature range of this board is -40°C to +85°C.

Note: Airflow is needed for higher temperature ambient conditions.

1.3 Quick Test Guide

1. Add a jumper to J4 and leave the J3, J5 empty. See Table 2 for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads before applying any power. See Figure 3 for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see Figure 2 for the proper test setup.

Note: Renesas recommends adding a minimum 0.1A load current if configured as DEM.

Table 2. Operating Options

Jumper	Function
3	V_{OUT} is set to 60V if only J3 is added
4	V_{OUT} is set to 48V if only J4 is added
5	V_{OUT} is set to 36V if only J5 is added
	V_{OUT} is set to 80V if remove all J3, J4 and J5.

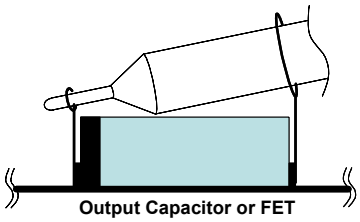

Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

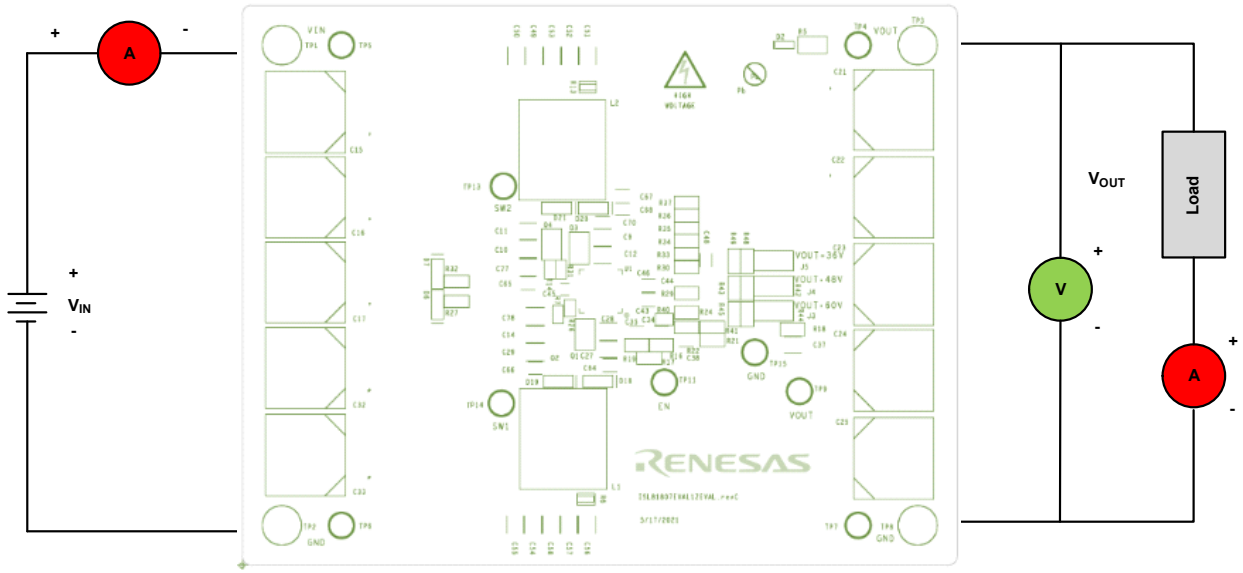

Figure 3. Proper Test Setup

2. Board Design

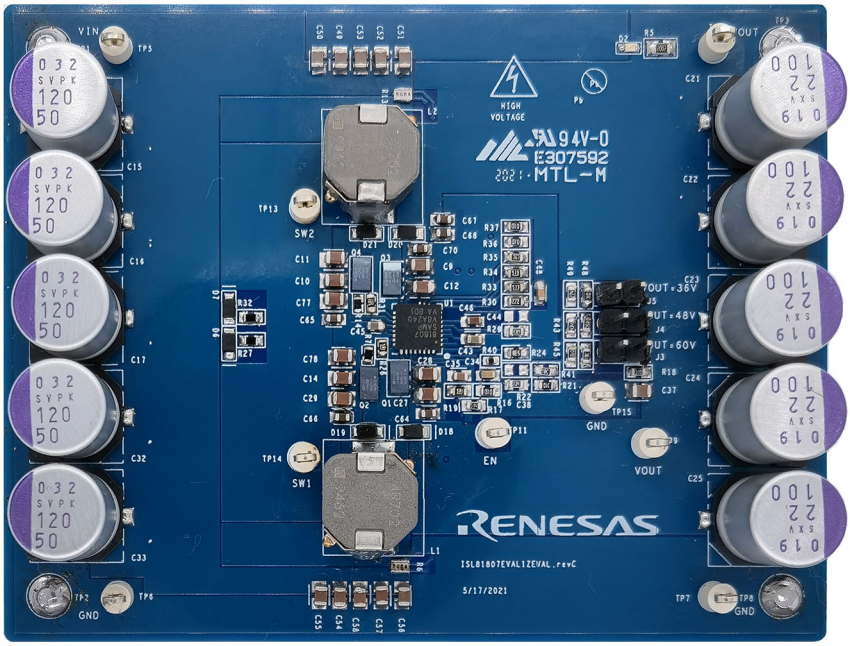

Figure 4. ISL81807EVAL1Z Evaluation Board, Top View

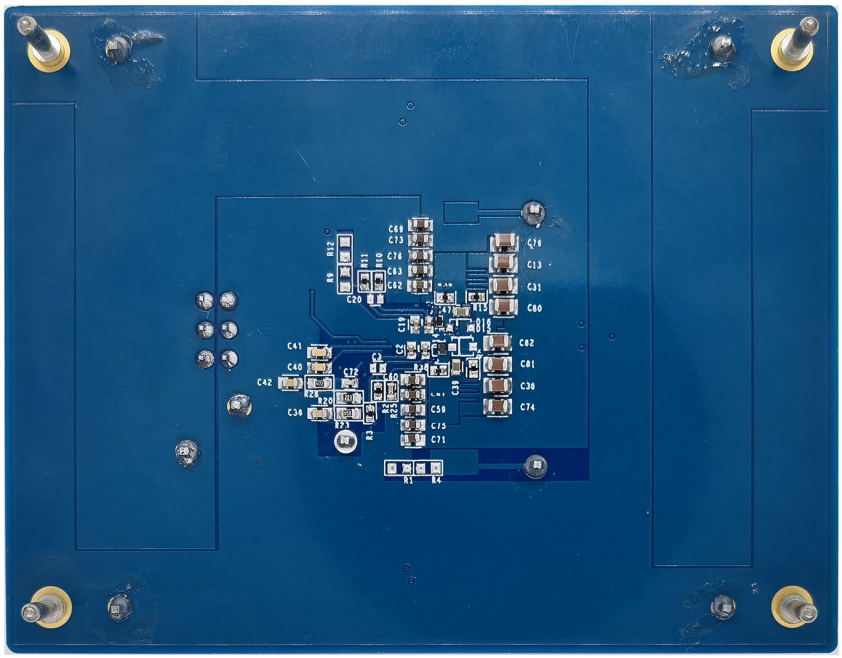

Figure 5. ISL81807EVAL1Z Evaluation Board, Bottom View

2.1 PCB Layout Guidelines

Careful attention to Printed Circuit Board (PCB) layout requirements is necessary for the successful implementation of an ISL81807 based DC/DC converter. The ISL81807 switches at a high frequency, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81807 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout.

1. Place the input capacitors, FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the FETs.
2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. **Note: DO NOT** connect them together anywhere else.
3. Keep the loop formed by the input capacitor, the top FET, and the bottom FET as small as possible.
4. Ensure the current paths from the input capacitor to the FETs, the power inductor, and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane using a via. **Note: DO NOT** connect the PGND pin directly to the SGND EPAD.
7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
8. Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper filled polygons or wide, short traces to connect the junction of the upper FET, lower FET, and output inductor. Keep the PHASE nodes connection to the IC short. **Note: DO NOT** unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
10. Route all high-speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
12. Use a pair of traces with minimum loop for the input or output current sensing connection.
13. Ensure the feedback connection to the output capacitor is short and direct.

2.2 Schematic Drawing

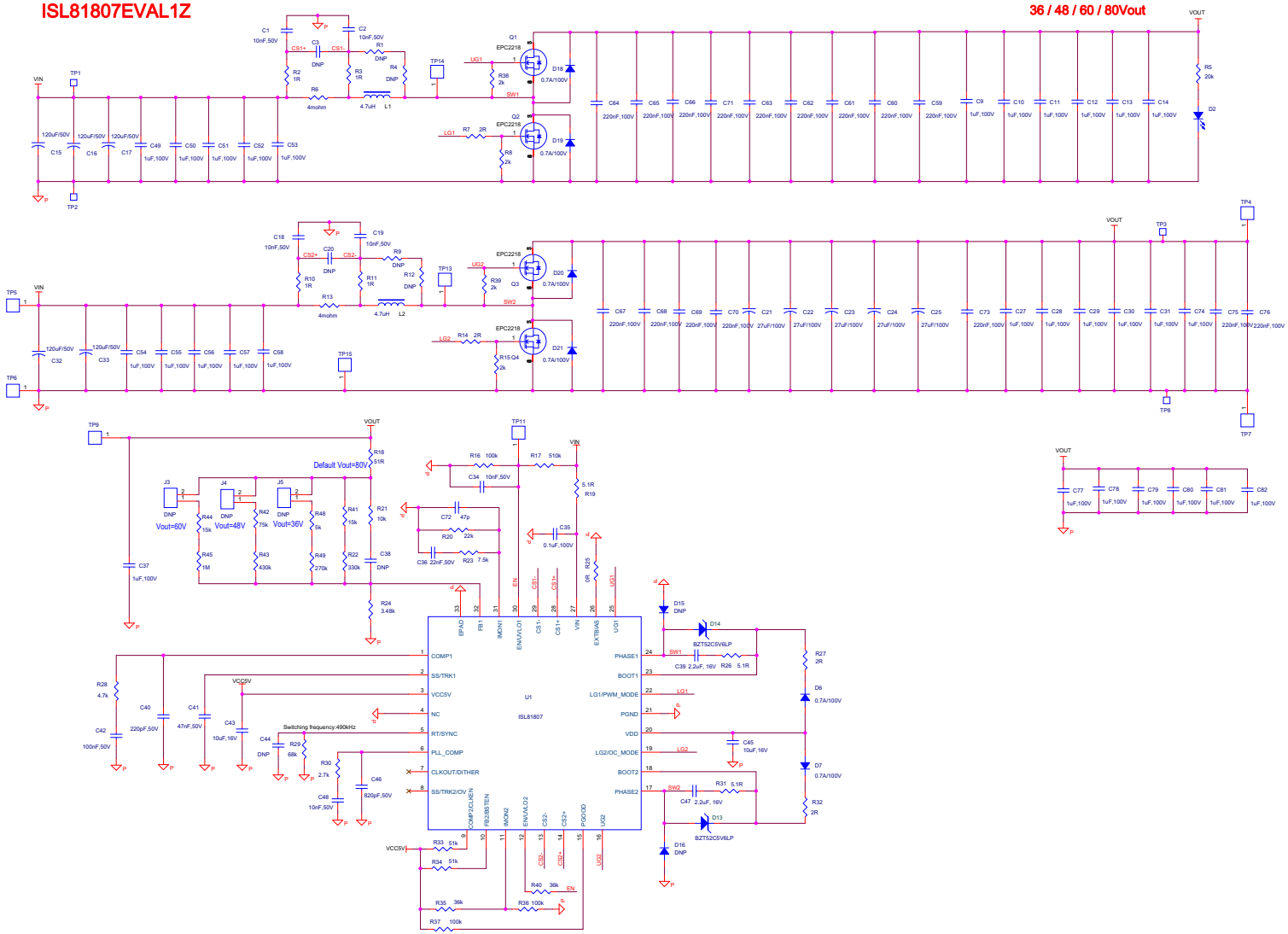

Figure 6. Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL81807EVAL1Z, REVC, ROHS	MTL (Multilayer PCB International (HK) CO.LTD)	ISL81807EVAL1ZREVCPCB
4	C1, C2, C18, C19	CAP, SMD, 0402, 0.01µF, 50V, 10%, X7R, ROHS	Venkel	C0402X7R500-103KNE
1	C45	CAP, SMD, 0402, 10µF, 10V, 20%, X5R, ROHS	Samsung	CL05A106MP8NUB8
2	C39, C47	CAP, SMD, 0402, 2.2µF, 25V, 10%, X5R, ROHS	TDK	C1005X5R1E225K050BC
1	C72	CAP, SMD, 0402, 47pF, 50V, 10%, C0G/NP0, ROHS	AVX	04025A470KAT2A
0	C3, C20	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS		
2	C34, C48	CAP, SMD, 0603, 0.01µF, 50V, 10%, X7R, ROHS	AVX	06035C103KAT2A
1	C35	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	Venkel	C0603X7R101-104KNE
1	C42	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX	06035C104KAT2A
1	C43	CAP, SMD, 0603, 10µF, 16V, 10%, X5R, ROHS	Murata	GRM188R61C106KAALD
1	C40	CAP, SMD, 0603, 220pF, 50V, 10%, X7R, ROHS	Murata	GRM188R71H221KA01D
1	C36	CAP, SMD, 0603, 0.022µF, 50V, 10%, X7R, ROHS	Venkel	C0603X7R500-223KNE
1	C41	CAP, SMD, 0603, 0.047µF, 50V, 10%, X7R, ROHS	Panasonic	ECJ-1VB1H473K
1	C46	CAP, SMD, 0603, 820pF, 50V, 10%, X7R, ROHS	Kemet	C0603C821K5RACTU
0	C38, C44	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
29	C9, C10, C11, C12, C13, C14, C27, C28, C29, C30, C31, C37, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C74, C77, C78, C79, C80, C81, C82	CAP, SMD, 0805, 1.0µF, 100V, 10%, X7S, ROHS	TDK	CGA4J3X7S2A105K125AB
16	C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C73, C75, C76	CAP-AEC-Q200, SMD, 0603, 0.22µF, 100V, 10%, X7S, ROHS	Taiyo Yuden	HMK107C7224KAHTE
5	C21, C22, C23, C24, C25	CAP-OSCON, SMD, 10.3mm, 27µF, 100V, 20%, 30mΩ, POLYMER, ROHS	Panasonic	100SXV27M

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
5	C15, C16, C17, C32, C33	CAP-OSCON, SMD, 12.7×10mm, 120µF, 50V, 20%, 20mΩ, ALUM.POLY, ROHS	Panasonic	50SVPK120M
2	L1, L2	COIL-AEC-Q200, PWR INDUCTOR, SMD, 10.5×10, 4.7µH, 20%, 19.3A, ROHS	TDK	SPM10065VT-4R7M-D
4	TP1, TP2, TP3, TP8	CONN-PC PIN, W/FLANGE, TH, 6.55mmPOST, 2.67mmTAIL, ROHS	Keystone	1377-2
9	TP4, TP5, TP6, TP7, TP9, TP11, TP13, TP14, TP15	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	Keystone	5007
1	J4	CONN-HEADER, 1×2, RETENTIVE, 2.54mm, 0.230×0.120, ROHS	BERG/FCI	69190-202HLF
1	J4	CONN-JUMPER, SHUNT, 2P, 2.54mm PITCH, BLK, 6mm, OPEN, ROHS	Sullins	SPC02SYAN
2	D13, D14	DIODE-ZENER, SMD, 0402, 5.1V, 6%, 250mW, 60Ω, ROHS	Diodes Inc.	BZT52C5V1LP-7
6	D6, D7, D18, D19, D20, D21	DIODE-SCHOTTKY, SMD, 2P, TUMD2M, 100V, 700mA, ROHS	Rohm	RB578VAM100TR
1	D2	LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 574nm, 35mcd, ROHS	Liteon/Vishay	LTST-C191KGKT
1	U1	IC-80V PWM CONTROLLER for GaN, 32P, TQFN, 5×5, ROHS	Renesas Electronics	ISL81807FRTZ
4	Q1, Q2, Q3, Q4	TRANSISTOR-GaNFET, N-CHNL, 100V, 60A, SMD, BUMPED-DIE, ROHS	EPC (Efficient Power Conversion)	EPC2218
4	R2, R3, R10, R11	RES, SMD, 0402, 1Ω, 1/16W, 1%, TF, ROHS	Vishay/Dale	CRCW04021R00FKED
2	R7, R14	RES, SMD, 0402, 2Ω, 1/16W, 1%, TF, ROHS	Venkel	CR0402-16W-02R0FT
2	R26, R31	RES, SMD, 0402, 5.1Ω, 1/16W, 1%, TF, ROHS	Yageo	AC0402FR-075R1L
1	R25	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	Venkel	CR0402-16W-00T
4	R8, R15, R38, R39	RES, SMD, 0402, 2k, 1/16W, 1%, TF, ROHS	Panasonic	ERJ-2RKF2001
1	R40	RES, SMD, 0402, 36k, 1/16W, 1%, TF, ROHS	Yageo	RC0402FR-0736KL
2	R27, R32	RES, SMD, 0603, 2Ω, 1/10W, 1%, TF, ROHS	Yageo	9C06031A2R00FGHFT
1	R18	RES, SMD, 0603, 51Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-51R0FT

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R19	RES, SMD, 0603, 5.1Ω, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-075R1L
1	R21	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
3	R16, R36, R37	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1003FT
1	R45	RES, SMD, 0603, 1M, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1004V
2	R41, R44	RES, SMD, 0603, 15k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1502V
1	R20	RES, SMD, 0603, 22k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2202FT
1	R30	RES, SMD, 0603, 2.7k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2701FT
1	R49	RES, SMD, 0603, 270k, 1/10W, 1%, TF, ROHS	Rohm	MCR03EZPFX2703
1	R22	RES, SMD, 0603, 330k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-07330KL
1	R24	RES, SMD, 0603, 3.48k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF3481V
1	R35	RES, SMD, 0603, 36k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF3602V
1	R43	RES, SMD, 0603, 430k, 1/10W, 1%, TF, ROHS	Stackpole	RMCF0603FT430K
1	R28	RES, SMD, 0603, 4.7k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-074K7L
1	R48	RES, SMD, 0603, 4.99k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF4991V
2	R33, R34	RES, SMD, 0603, 51k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0751KL
1	R17	RES, SMD, 0603, 510k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5103V
1	R29	RES, SMD, 0603, 68k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0768KL
1	R23	RES, SMD, 0603, 7.5k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-7501FT
1	R42	RES, SMD, 0603, 75k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-7502FT
0	R1, R4, R9, R12	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
1	R5	RES, SMD, 0805, 20k, 1/8W, 1%, TF, ROHS	Venkel	CR0805-8W-2002FT
2	R6, R13	RES-AEC-Q200, SMD, 0805-WIDE, 0.004Ω, 1W, 1%, ROHS	Susumu	KRL2012E-M-R004-F-T5

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
4	Four corner	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corner	STANDOFF, 4-40×3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	D15, D16 (NSR02100HT1G)	DO NOT POPULATE OR PURCHASE		
0	J3, J5 (BG301-02-A-0540-L-B)	DO NOT POPULATE OR PURCHASE		

2.4 Board Layout

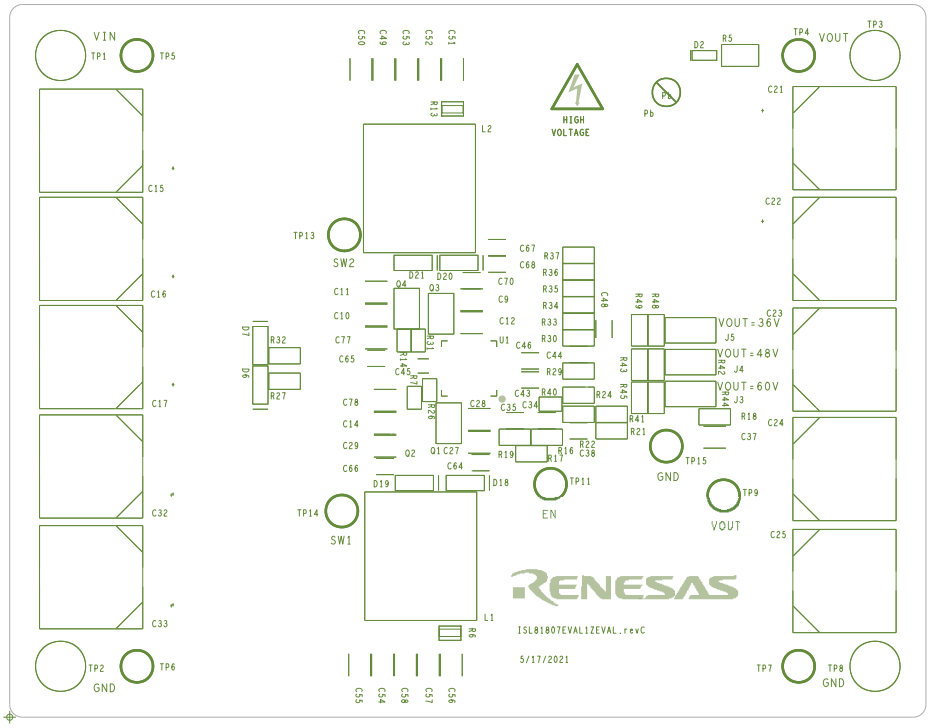

Figure 7. Silkscreen Top

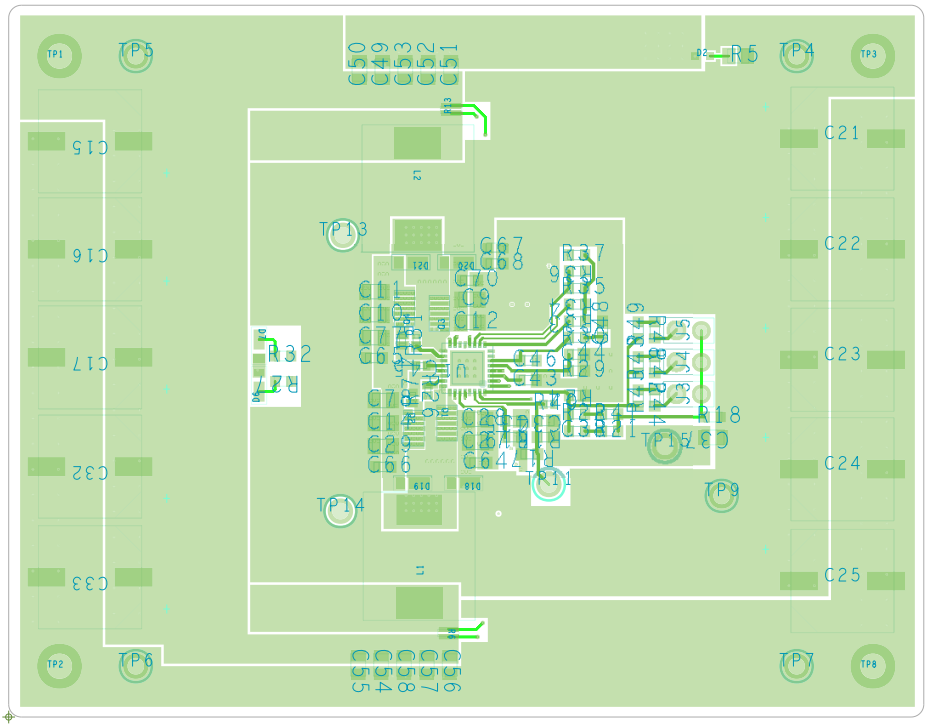

Figure 8. Top Layer

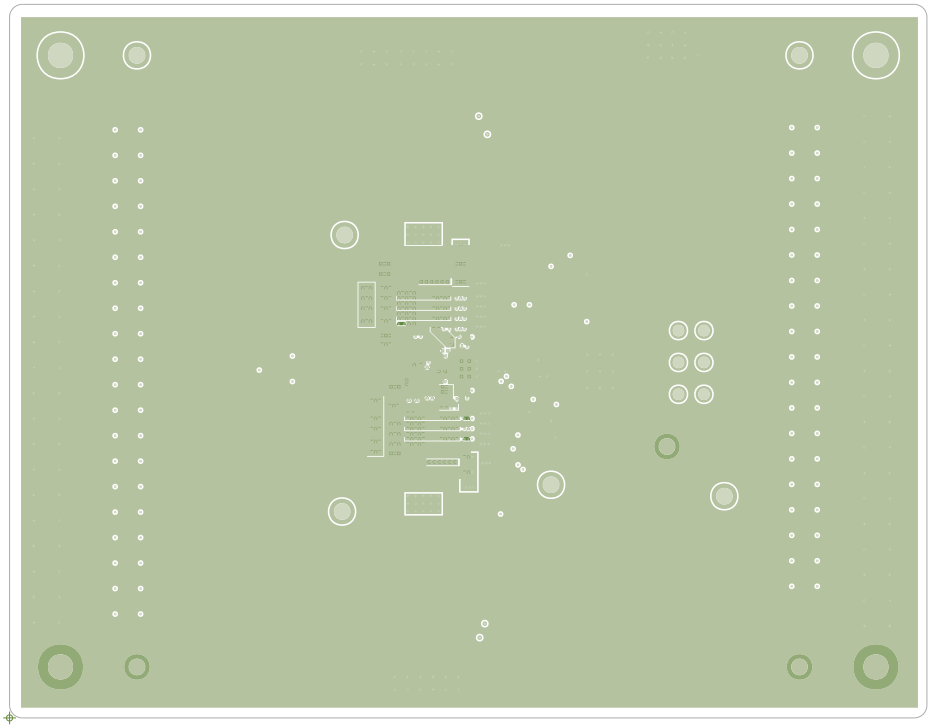

Figure 9. Second Layer (Solid Ground)

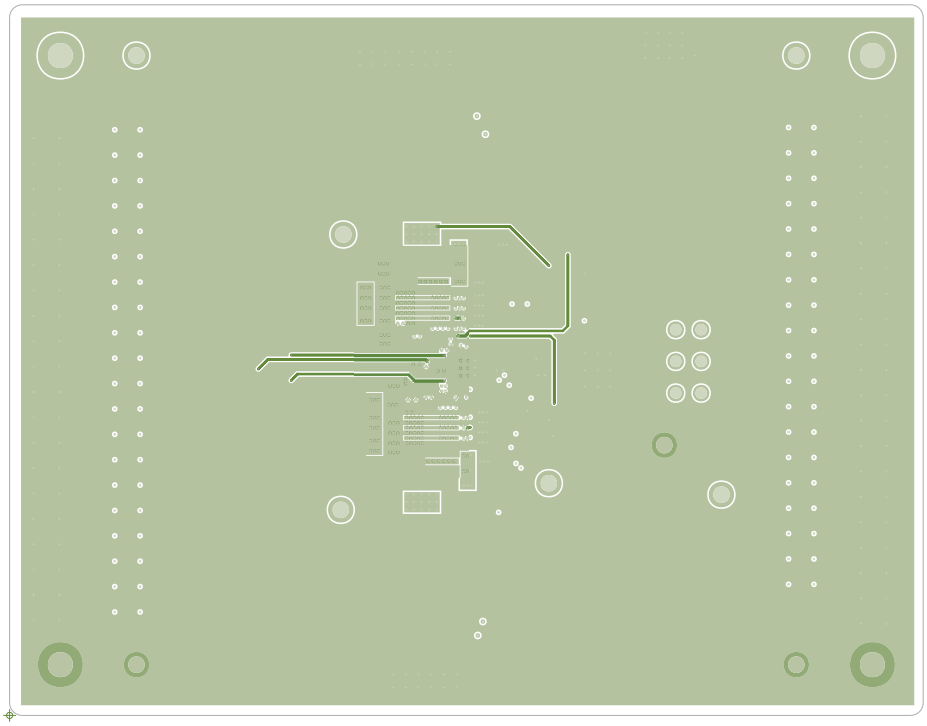

Figure 10. Third Layer

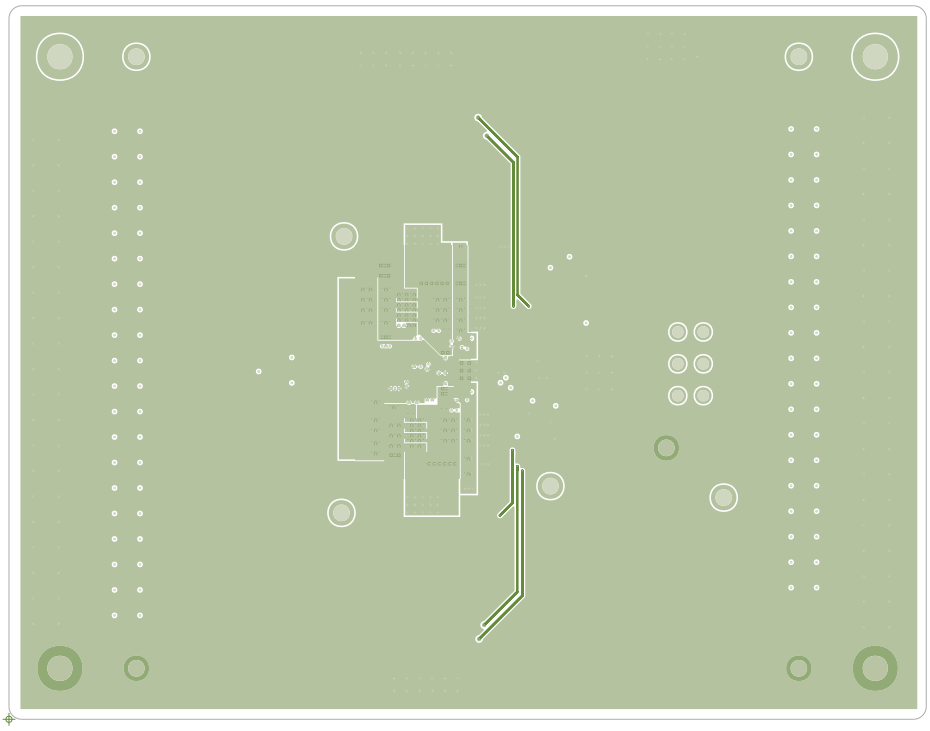

Figure 11. Fourth Layer

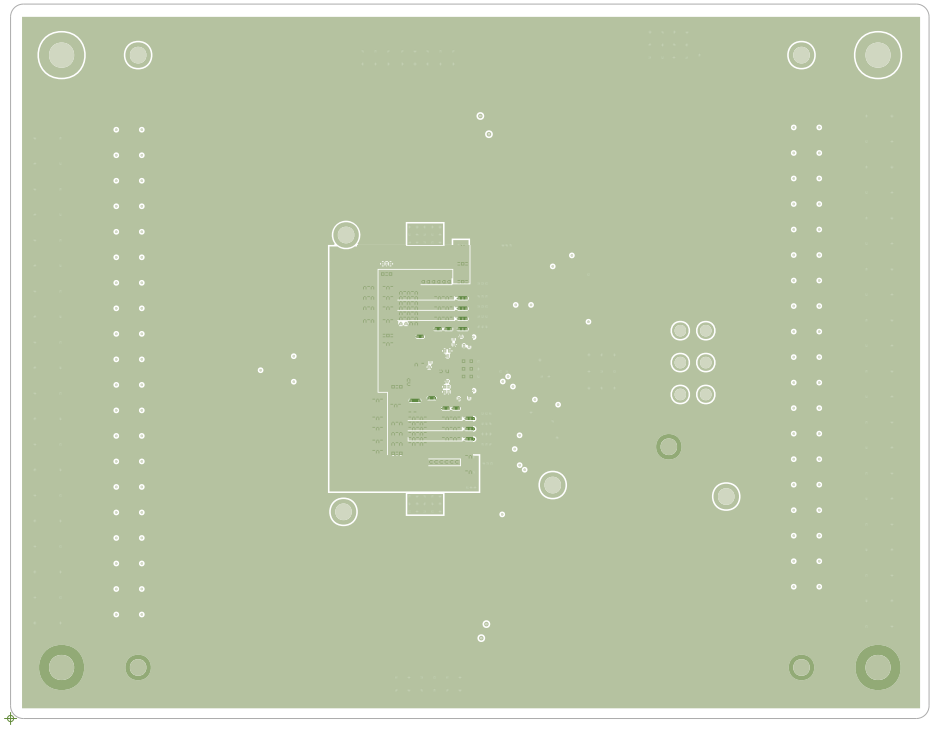

Figure 12. Fifth Layer

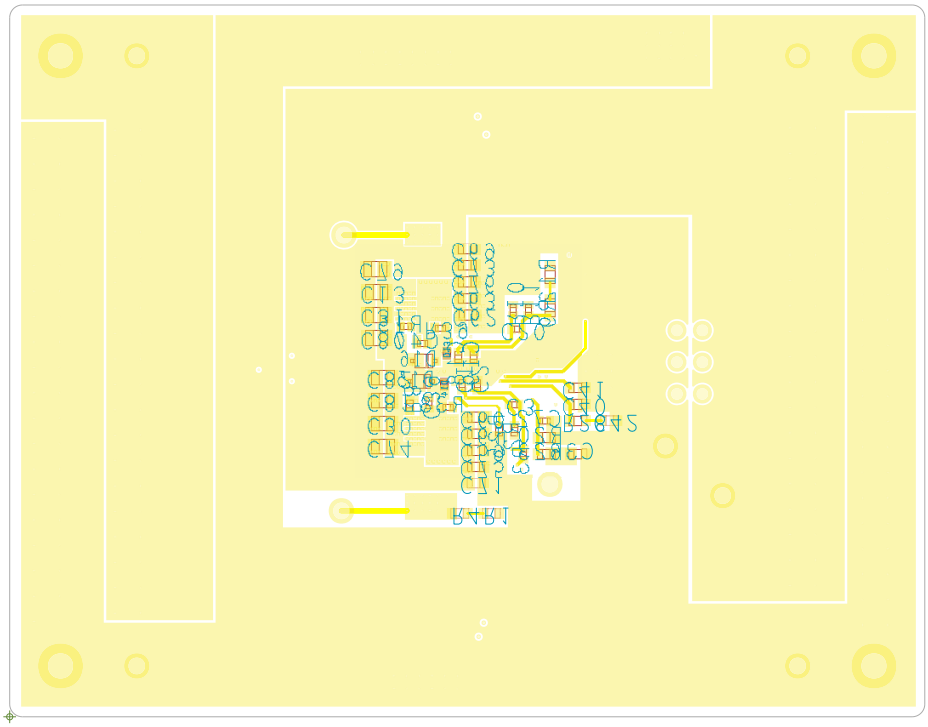

Figure 13. Bottom Layer

Figure 14. Silkscreen Bottom

2.5 Design Procedure

2.5.1 Design Requirements

Parameter	Rating
Input Voltage	12V to 36V
Switching Frequency	500kHz
Output Voltage	36V/48V/60V/80V
Output Power	240W
OCP Set Point (pulse by pulse)	20.5A
OCP Set Point (input average)	18A
Output Mode	Dual phase
PWM Mode	Forced PWM
OCP Mode	Constant current

2.5.2 Frequency Setting

The default switching frequency of the PWM controller is determined by the resistor R_T (R29). It adjusts the default switching frequency from 100kHz to 2MHz. The R_T value for f_{SW} = 500kHz is calculated using Equation 1.

(EQ. 1) $$R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) = \frac{34.7}{0.5} - 4.78 = 64.62k\Omega$$

where f_{SW} is the switching frequency in MHz. Select a standard value resistor R_T = 68kΩ.

2.5.3 Output Voltage Setting

The output voltage can be set from 0.8V up to a level determined by the feedback voltage divider. A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB1 pin. With V_{OUT} = 48V and R_{FBO1} = 205k, the R_{FBO2} (R24) value is calculated using Equation 2.

(EQ. 2) $$R_{FBO2} = \frac{0.8V \times R_{FBO1}}{V_{OUT} - 0.8V} = \frac{0.8V \times 205k\Omega}{48V - 0.8V} = 3.474k\Omega$$

where R_{FBO1} is the top resistor of the feedback divider network and R_{FBO2} (R24) is the bottom resistor connected from FB1 to ground. Select a standard value resistor R_{FBO2} = 3.48kΩ.

2.5.4 UVLO Setting

The ISL81807 has input UVLO protection. When the voltage on the EN/UVLO pin reaches 1.8V, the PWM modulator is enabled. Accurate UVLO feature can be implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} (R17) and R_{UV2} (R16). The V_{IN} UVP rising threshold is calculated using Equation 3.

(EQ. 3) $$V_{UVRISE} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{LEAK}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(510k\Omega + 100k\Omega) - 2.8\mu A(510k\Omega)(100k\Omega)}{100k\Omega} = 9.55V$$

The V_{IN} UVP falling threshold is calculated using Equation 4.

(EQ. 4) $$V_{UVFALL} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{UVLO\_HYST}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(510k\Omega + 100k\Omega) - 6.8\mu A(510k\Omega)(100k\Omega)}{100k\Omega} = 7.5V$$

where V_{UVLO_THR} is the 1.8V UVLO rising threshold and I_{UVLO_HYST} is the 6.8µA UVLO hysteresis current.

2.5.5 Soft-Start Capacitor

The soft-start time for dual-phase is set by the value of the soft-start capacitor C_{SS} (C41) connected from SS/TRK1 to GND. The soft-start time with C_{SS} = 47nF is calculated using Equation 5.

(EQ. 5) $$t_{SS} = 0.8V\left(\frac{C_{SS}}{4\mu A}\right) = 0.8V \times \left(\frac{47nF}{4\mu A}\right) = 9.4ms$$

When the soft-start time is set by an external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

2.5.6 FETs Considerations

The FETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power loss of the upper and lower FETs for each phase is calculated using Equation 6 and Equation 7. The equations assume linear voltage current transitions and ignore the power loss caused by the reverse recovery of the body diode of the lower FET. Take V_{IN} = 12V, V_{OUT} = 48V, and I_{OUT} = 3A as an example.

(EQ. 6) $$P_{LOWERMAX} = \left[\frac{(I_{OUT})^2(V_{OUT})^2}{(V_{INMIN}{}^2)}\right]\frac{(V_{OUT} - V_{INMIN})(r_{DS(ON)})}{V_{OUT}} + \frac{(I_{OUT})(V_{OUT})^2(t_{SW})(f_{SW})}{2(V_{INMIN})}$$

$$= \left[\frac{\left(\frac{3A}{2}\right)^2(48V)^2}{(12V)^2}\right]\frac{(48V - 12V)(3.2m\Omega)}{48V} + \frac{\left(\frac{3A}{2}\right)(48V)^2\left(\frac{1.9nC}{\left(\frac{5.3V - 2V}{2\Omega}\right)} + \frac{1.9nC}{\left(\frac{2V}{2\Omega}\right)}\right)(500kHz)}{2(12V)} = 0.086W + 0.22W = 0.306W$$

(EQ. 7) $$P_{UPPERMAX} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{OUT})}{V_{INMIN}} = \frac{\left(\frac{3A}{2}\right)^2(3.2m\Omega)(48V)}{12V} = 0.03W$$

Ensure that all FETs are within their maximum junction temperature with enough margin at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

2.5.7 Inductor Selection

The inductor value determines the ripple current of the converter. To limit the inductor core loss, the inductor ripple current is usually 40-80% of the rated output current. Assume the ripple current ratio is 80% of the inductor average current at the minimum input voltage and the full output load condition. The inductor value for each phase is calculated using Equation 8.

(EQ. 8) $$L_{INMIN} = \frac{(V_{OUT} - V_{INMIN})(V_{INMIN})}{(f_{SW})(0.8 \times I_{INMAX})(V_{OUT})} = \frac{(48V - 12V)(12V)}{(500kHz)\left(0.8 \times \frac{48Vx3A}{12Vx2}\right)(48V)} = 3.75\mu H$$

The recommended inductor value is 4.7µH. Then the ripple current and peak current are calculated using Equation 9, Equation 10, and Equation 11.

(EQ. 9) $$\Delta I_{LMAX} = \frac{(V_{OUT} - V_{IN})(V_{IN})}{(f_{SW})(L)(V_{OUT})} = \frac{(48V - 12V)(12V)}{(500kHz)(4.7\mu H)(48V)} = 3.83A$$

(EQ. 10) $$I_{LRMS} = \sqrt{(I_{INMAX})^2 + \frac{(\Delta I_{LMAX})^2}{12}} = \sqrt{\left(\frac{48Vx3A}{12Vx2}\right)^2 + \frac{(3.83A)^2}{12}} = 6.1A$$

(EQ. 11) $$I_{LPEAKMAX} = \frac{I_{INOCP}}{2} + \frac{\Delta I_{LMAX}}{2} = \frac{18A}{2} + \frac{3.83A}{2} = 10.92A$$

The saturation current of the inductor should be larger than 10.92A. The heat rating current of the inductor should be larger than 6.1A. Considering the OCP (pulse by pulse) setting point is 20.5A, the inductor saturation current should be higher than 20.5A.

TDK inductor SPM10065VT-4R7M-D is selected as the power inductor, the maximum DC power dissipation in the inductor is approximately calculated using Equation 12.

(EQ. 12) $$P_{LMAX} = (I_{LRMS})^2(DCR) = (6.1A)^2 \times (9.2m\Omega) = 0.34W$$

2.5.8 Output Capacitor Selection

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 13.

(EQ. 13) $$C_{OUTMIN} = \frac{L(V_{OUT})(I_{TRAN})^2}{2(V_{INMIN})^2(\Delta V_{OUT})} = \frac{4.7\mu H \times (48V) \times \left(\frac{3A}{2} - 0A\right)^2}{2(12V)^2\left(48V \times \frac{1}{100}\right)} = 3.67\mu F$$

where C_{OUTMIN} is the minimum output capacitor(s) required, I_{TRAN} is the transient load current step, and ΔV_{OUT} is the drop-in output voltage allowed during the load transient. Choose a capacitor no less than 3.67µF for each phase. 55µF electrolytic capacitor and more than 20µF MLCC in total are used for each phase on this board.

The output voltage ripple is because of the discontinuous ripple current to the output capacitor and the ESR of the output capacitors as defined by Equation 14.

(EQ. 14) $$V_{RIPPLE} = \left(\frac{(I_{OUT})(V_{OUT})}{V_{INMIN}} + \frac{\Delta I_L}{2}\right) \times ESR = \left(\frac{\left(\frac{3A}{2}\right)(48V)}{12V} + \frac{3.83A}{2}\right) \times 5m\Omega = 39.58mV$$

2.5.9 Input Capacitor Selection

The important parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline.

In Boost mode, the input current is continuous. The RMS current supplied by the input capacitance is noticeably small.

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the FETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Five 120µF electrolytic capacitors with 4.3A rating current and ten 1µF ceramic capacitors are used to share the input RMS current on this board.

2.5.10 First Level Peak Current Limit and Sense Resistor Selection

The inductor peak current is sensed by the sense resistor R_S (R6, R13). When the voltage drop on R_S reaches the set point $V_{OCSET-CS}$ typical 82mV, it triggers the pulse-by-pulse peak current limit. With the current limit set point $I_{OCPP1} = 2xI_{INMAX} = 18A$ for each phase, the value of the sense resistor is calculated using Equation 15.

(EQ. 15) $$R_S = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{82mV}{18A} = 4.56m\Omega$$

Select a standard value resistor $R_S = 4m\Omega$. Then the actual peak current limit is calculated using Equation 16.

(EQ. 16) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{82mV}{4m\Omega} = 20.5A$$

The maximum power dissipation in R_S is calculated by Equation 17.

(EQ. 17) $$P_{RSMAX} = (I_{IN})^2 R_S = (6.1A)^2(4m\Omega) = 0.149W$$

Therefore, a sense resistor with 1W power rating is sufficient for this application.

2.5.11 Second Level Hiccup Peak Current Protection

In this condition, V_{IN} is so close to V_{OUT} that the inductor current runs away with the minimum on PWM duty. The ISL81807 integrates a second level hiccup type of peak current protection. The second level peak current protection set point I_{OCPP2} is calculated using Equation 18.

(EQ. 18) $$I_{OCPP2} = \frac{V_{OCSET-CS-HIC}}{R_S} = \frac{98mV}{4m\Omega} = 24.5A$$

2.5.12 Input Average Overcurrent Protection and R_{IM} Selection

The ISL81807 provides either constant current or hiccup type of overcurrent protection for input average current. The OCP mode is set by a resistor connected between the LG2/OC_MODE pin and ground. With input constant current/hiccup set point I_{INOCP} = 18A for two phases in total, the current monitoring resistor R_{IM} (R20) is calculated using Equation 19.

(EQ. 19) $$R_{IM} = \frac{1.2}{I_{INOCP} \times R_S \times Gm_{CS} + 2 \times I_{CSOFFSET}} = \frac{1.2V}{18Ax4m\Omega x195\mu S + 2 \times 20\mu A} = 22k\Omega$$

where $I_{CSOFFSET}$ is the output current sense op amp internal offset current, typical 20µA. Select a standard value resistor R_{IM} = 22kΩ.

2.5.13 Output Mode Selection

When the IMON2 pin voltage is higher than 3V, the IC is set for one output dual-phase application, and the original IMON2 current monitor function pin is disconnected from the IMON2 pin and internally connected to the IMON1 pin. The IMON2 pin is connected to VCC5 using R35 and R36 for dual-phase setting on this board.

2.5.14 PWM Mode Selection

You can set the ISL81807 to either forced PWM mode or DE mode. The mode is set by a resistor $R_{PWMMODE}$ (R8) connected between the LG1/PWM_MODE pin and GND. The boundary resistor value for $R_{PWMMODE}$ is calculated using Equation 20.

(EQ. 20) $$R_{PWMMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to forced PWM mode, while a resistor higher than 30kΩ sets the converter to DE mode. Considering the tolerance in all temperature ranges and GaN FET drain to gate resistance, Renesas recommends using less than 5kΩ to set Forced PWM mode and 39kΩ to set DE mode.

2.5.15 Overcurrent Protection Mode Selection

The ISL81807 is set to either a constant current or hiccup type of overcurrent protection for input average current by selecting a different value of the resistor R_{OCMODE} (R38) connected between LG2/OC_MODE and GND. The boundary resistor value for R_{OCMODE} is calculated using Equation 21.

(EQ. 21) $$R_{OCMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to constant current mode, while a resistor higher than 30kΩ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges and GaN FET drain to gate resistance, Renesas recommends using less than 5kΩ to set constant current and 39kΩ to set the Hiccup mode.

2.5.16 Phase Lock Loop (PLL)

The PLL of the ISL81807 ensures the wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting. The external compensation network of R_{PLL} (R30), C_{PLL1} (C48), and C_{PLL2} (C46) is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}.

2.5.17 Feedback Loop Compensation

To adapt the different applications, the controller is designed with an externally compensation network. Figure 15 shows the peak current mode boost converter circuit.

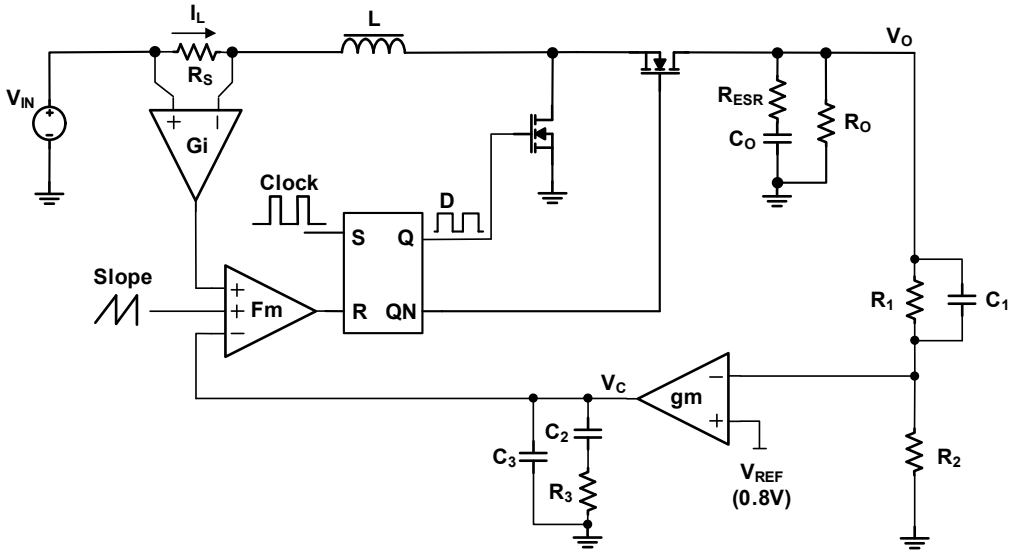

Figure 15. Peak Current Mode Boost Converter Circuit

In the current loop, the control to output simplified transfer function is shown in Equation 22.

(EQ. 22)
$$\frac{\hat{V_O}}{\hat{V_C}} = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1-\frac{s}{\omega_{RHPZ}}\right)\left(1+\frac{s}{\omega_{z(esr)}}\right)}{\left(1+\frac{s}{\omega_{po}}\right)\left(1+\frac{s}{\omega_{pi}}\right)}$$

where:

(EQ. 23)
$$K_d = 2 + \frac{R_O \cdot (1-D)^2}{R_I} \cdot \left(\frac{1}{K_m} + \frac{K}{1-D}\right)$$

(EQ. 24)
$$K_m = \frac{1}{(D-0.5)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_O}}$$

(EQ. 25)
$$K = 0.5R_I \times \frac{T_s}{L} \times D \times (1-D)$$

(EQ. 26)
$$R_I = G_I \times R_S$$

- R_O is the load resistor
- C_O is the output capacitor
- L is the inductor
- R_S is the current sense resistor
- V_O is the output voltage
- T_S is the period of one switching cycle
- D is the duty cycle of lower FET
- V_{SL} = 0.843V, is the slope compensation voltage

- V_{IN} is the input voltage of the boost
- V_C is the output of the error amplifier
- G_I = 5.472, is the gain of the current sensor

The low frequency pole frequency is shown in Equation 27.

(EQ. 27) $$\omega_{p0} = 2\pi f_{p0} = \frac{K_d}{C_o \times R_o}$$

The high frequency pole frequency is shown in Equation 28.

(EQ. 28) $$\omega_{pi} = 2\pi f_{pi} = \frac{K_m \times R_I}{L}$$

The output capacitor ESR (R_{ESR}) zero frequency is shown in Equation 29.

(EQ. 29) $$\omega_{z(esr)} = 2\pi f_{z(esr)} = \frac{1}{C_o \times R_{ESR}}$$

The output voltage is regulated by an error amplifier EA. The EA compensation network parameters can be determined by compensating the current loop poles and zero so as to implement an ideal -20dB/decade close-loop gain with crossover frequency around 1/50~1/20 of f_{sw} crossover frequency.

For boost topology, the maximum crossover frequency is also limited by the RHPZ. Estimate the RHPZ at the minimum input voltage by Equation 30.

(EQ. 30) $$\omega_{RHPZ} = 2\pi f_{RHPZ} = \frac{R}{L} \times (1 - D_{max})^2$$

If the crossover frequency f_c << f_{pi}, a type-2 compensation network is enough to achieve the goal.

The type-2 EA amplifier transfer function is simplified to Equation 31.

(EQ. 31) $$\frac{V_c}{V_o} = \frac{1 + sR_3C_2}{(1 + sR_3C_3)s(C_2 + C_3)}$$

The transfer function has one pole and one zero.

- The pole is at the frequency of $f_{p1} = 1/2\pi R_3C_3$. This is the frequency where the impedance of R_3 is equal to C_3.
- The zero is at the frequency of $f_{z1} = 1/2\pi R_3C_2$. This is the frequency where the impedance of R_3 is equal to C_2.

To achieve ideal compensation, Renesas recommends making f_{z1}= f_{p0} and f_{p1} = $f_{z(esr)}$ as shown in Figure 16.

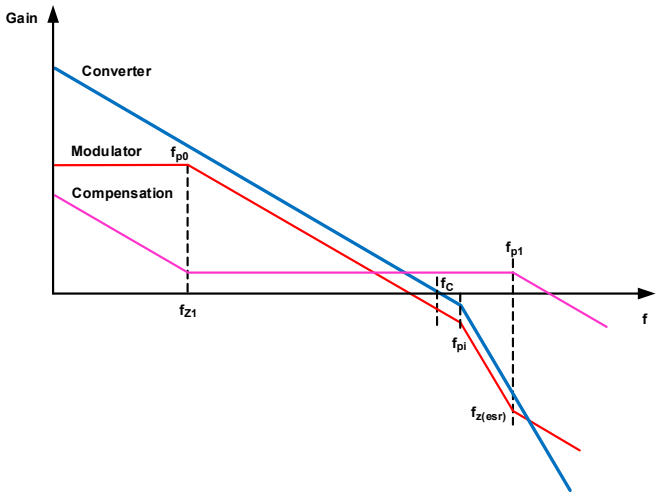

Figure 16. Feedback Loop Compensation

The close-loop transfer function is then simplified to Equation 32.

(EQ. 32) $$G_{loop}(s) = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1-\frac{s}{\omega_{RHPZ}}\right)\left(1+\frac{s}{\omega_{z(esr)}}\right)}{\left(1+\frac{s}{\omega_{p0}}\right)\left(1+\frac{s}{\omega_{pi}}\right)} \times \frac{1+sR_3C_2}{1+sR_3C_3} = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1-\frac{s}{\omega_{RHPZ}}\right)}{\left(1+\frac{s}{\omega_{pi}}\right)}$$

The crossover frequency is shown in Equation 33.

(EQ. 33) $$f_c = \frac{R_O \times (1-D)}{R_I \times K_d}$$

The Loop design example for the 48V output under 20V input voltage is shown in the following:

V_{IN} = 20V, V_{OUT} = 48V, I_{OUT} = 5A, f_{sw} = 500kHz, T_s = 2µs, D = 1-V_{IN} / V_{OUT} = 0.588, L = 4.7µH, C_O = 120µF, R_O = V_{OUT} /I_{OUT} = 9.6Ω, R_s = 5mΩ, R_{esr} = 5mΩ.

(EQ. 34) $$K_m = \frac{1}{(D-0.5)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_O}} = \frac{1}{(0.588-0.5)(4m\Omega \times 5.472) \times \frac{2\mu s}{4.7\mu H} + \frac{0.843V}{48V}} = 54.4$$

(EQ. 35) $$K_d = 2 + \frac{R_O \cdot (1-D)^2}{R_I} \cdot \left(\frac{1}{K_m} + \frac{K}{1-D}\right) = 2 + \frac{9.6 \cdot (1-0.588)^2}{4m\Omega \times 5.472} \cdot \left(\frac{1}{54.4} + 0.5 \times 4m\Omega \times 5.472 \times \frac{2\mu s}{4.7\mu H} \times 0.588\right) = 3.572$$

(EQ. 36) $$G_{dc} = \frac{R_O \times (1-D)}{K_d \times R_I} = \frac{9.6\Omega \times (1-0.588)}{3.572 \times 0.027\Omega} = 50.59$$

(EQ. 37) $$\omega_{p0} = \frac{K_d}{C_O \times R_O} = \frac{3.572}{120\mu F \times 9.6\Omega} = 3.1kHz$$

(EQ. 38) $$f_{p0} = \frac{\omega_{p0}}{2\pi} = 0.494kHz$$

(EQ. 39) $$\omega_{pi} = \frac{K_m \times R_I}{L} = \frac{54.4 \times 0.022\Omega}{4.7\mu H} = 254.6kHz$$

(EQ. 40) $$f_{pi} = \frac{\omega_{pi}}{2\pi} = 40.5kHz$$

(EQ. 41) $$\omega_{z(esr)} = \frac{1}{C_O \times R_{ESR}} = \frac{1}{120\mu F \times 5m\Omega} = 1.67MHz$$

(EQ. 42) $$f_{z(esr)} = \frac{\omega_{z(esr)}}{2\pi} = 265.4kHz$$

The minimum value of RHPZ could be calculate by Equation 43.

(EQ. 43) $$f_{RHPZ} = \frac{R_O}{2\pi \times L} \times (1 - D_{max})^2 = \frac{9.6\Omega}{2\pi \times 4.7\mu H} \times \left(\frac{12V}{48V}\right)^2 = 20.33kHz$$

Therefore make 0.1 x f_{RHPZ} as crossover frequency and make the gain -20dB/decade:

(EQ. 44) $$f_c = 0.1 \times f_{RHPZ} = 2.033kHz$$

If R_3 (R28) = 4.7k, set the frequency of this zero f_{z1}= f_{p0}, then C_2 (C42) is calculated using Equation 45.

(EQ. 45) $$C_2 = \frac{1}{2\pi R_3 f_{p0}} = \frac{1}{2\pi \times 4.7k\Omega \times 0.494kHz} = 68.6nF$$

To increase the stability, Select a standard value capacitor C_2 (C42) = 100nF.

Set the frequency of this pole f_{p1} = $f_{z(esr)}$, and should make sure f_c<< f_{p1} << f_{sw}. Then C_3 (C40) is calculated using Equation 46.

(EQ. 46) $$C_3 = \frac{1}{2\pi R_3 f_{z(esr)}} = \frac{1}{2\pi \times 4.7k\Omega \times 265.4kHz} = 127.7pF$$

To increase the stability, Select a standard value capacitor C_3 (C40) = 220pF.

3. Typical Performance Graphs

V_{IN} = 24V, V_{OUT} = 48V,T_A = 25°C, unless otherwise noted.

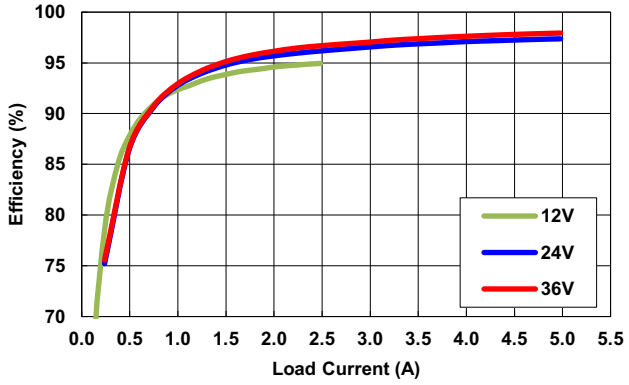

Figure 17. Efficiency, CCM

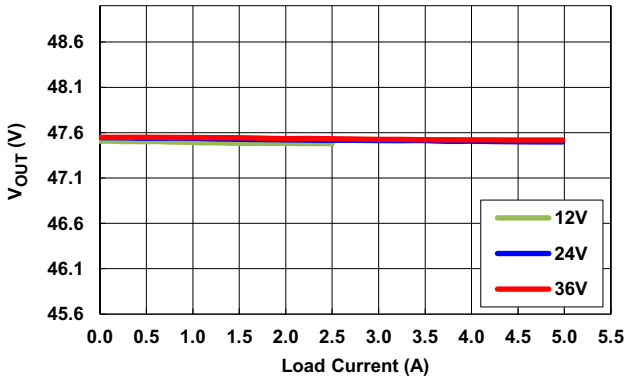

Figure 18. Load Regulation, CCM

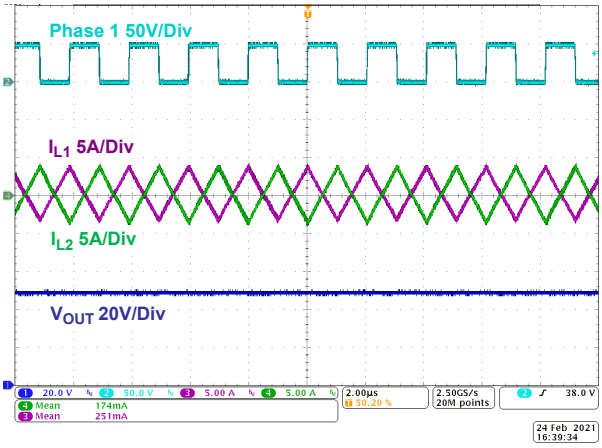

Figure 19. Dual-Phase Waveforms, V_{IN} = 24V, V_{OUT} = 48V, I_{OUT} = 0A, CCM Mode

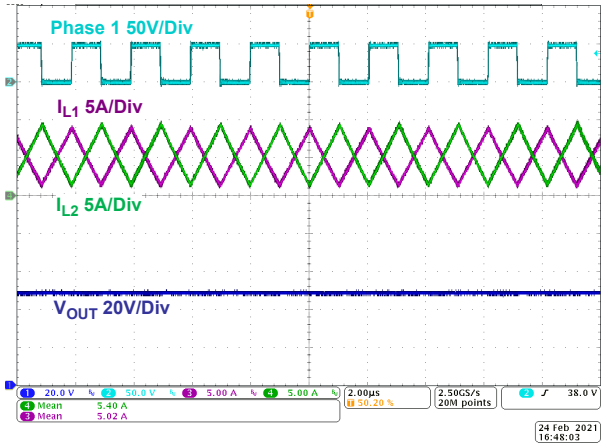

Figure 20. Dual-Phase Waveforms, V_{IN} = 24V, V_{OUT} = 48V, I_{OUT} = 5A, CCM Mode

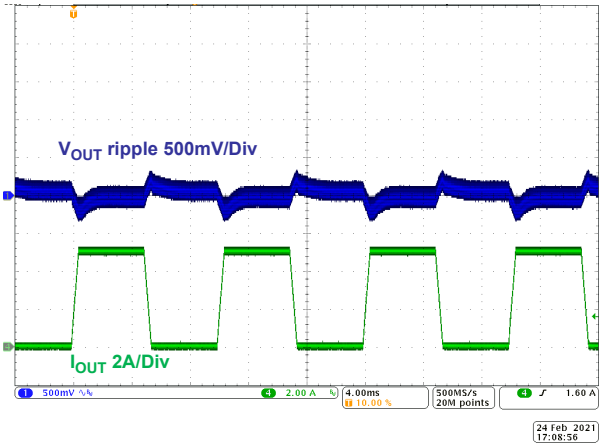

Figure 21. Dual-Phase Waveforms, V_{IN} = 24V, V_{OUT} = 48V, I_{OUT} = 0-5A Dynamic, CCM Mode

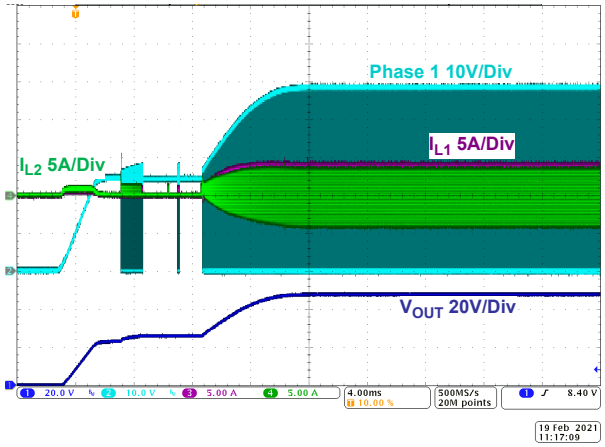

Figure 22. Dual-Phase Waveforms, Start-Up Waveform, V_{IN} = 24V, V_{OUT} = 48V, I_O = 0A, CCM

V_{IN} = 24V, V_{OUT} = 48V,T_A = 25°C, unless otherwise noted. (Cont.)

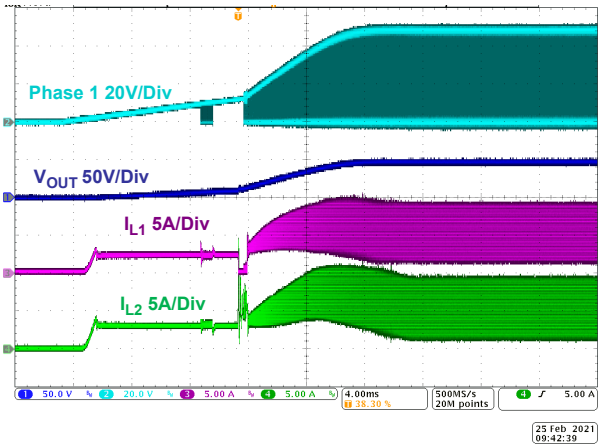

Figure 23. Dual-Phase Waveforms, Start-Up Waveform, V_{IN} = 24V, V_{OUT} = 48V, I_O = 5A, CCM

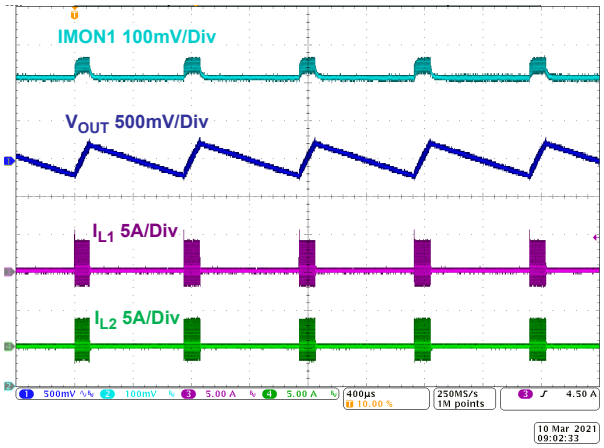

Figure 24. Dual-Phase Burst Mode V_{IN} = 24V, V_{OUT} = 48V,I_{OUT} = 0.5A

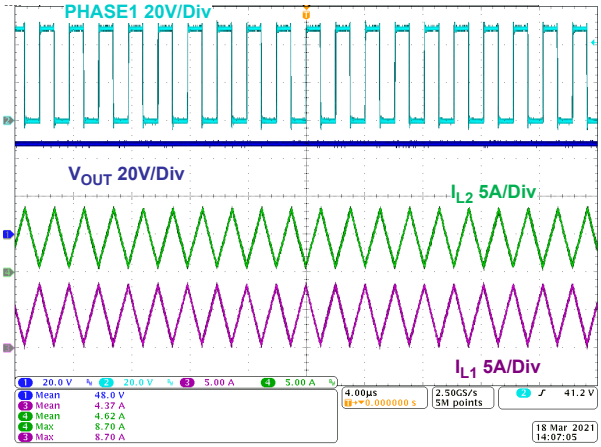

Figure 25. Dual-Phase PWM, V_{IN} = 24V, V_{OUT} = 48V, Shunt=10mΩ, Pulse by Pulse OCP test

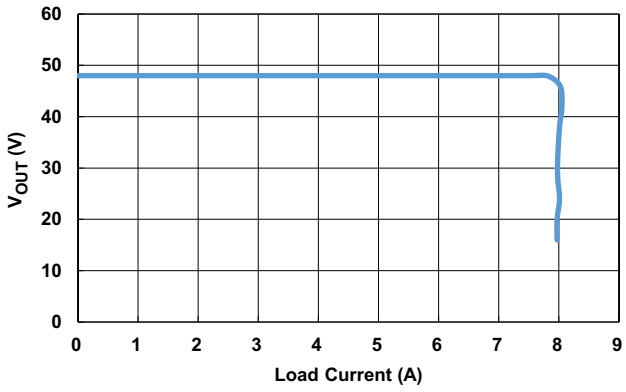

Figure 26. Dual-Phase Constant Voltage (CV) and Constant Current (CC) Operation, V_{IN} = 24V, V_{OUT} = 48V, CC = 8A

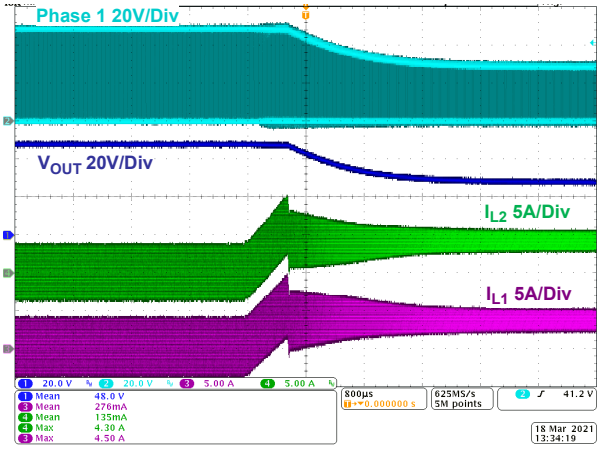

Figure 27. Dual-Phase Waveforms, V_{IN} = 24V, V_{OUT} = 48V,OCP Response, CC Mode, CCM Mode

4. Ordering Information

Part Number	Description
ISL81807EVAL1Z	High Voltage Dual-phase Boost Controller GaN Evaluation Board

5. Revision History

Rev.	Date	Description
1.00	Sep 24, 2021	Initial release

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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