Description

The ISL9000EV2 board is designed for customers' use in exploring the operation of the ISL9000 Low Dropout Regulator IC (LDO). In this capacity, it provides an easy to use platform for testing most of the datasheet specifications and functionalities. It is designed to show the small space required for all the components, while providing room to access the signals.

The layout is intended to minimize thermal effects, to better evaluate current limits and voltage regulation accuracy. In an actual implementation, the area for heat sinking may be smaller, so thermal effects may make the operation slightly different.

The ISL9000EV2 board constitutes a complete dual voltage regulator solution. The PCB board is 2 inches by 3 inches, however, the actual charger components easily fit within a 0.9 x 1.6 cm area (components on one side), demonstrating the space saving advantage of the ISL9000 in limited space applications.

A voltage source can be connected to the two pin connector (J2, default) or to the banana jacks (not populated). For monitoring the output, test instruments can be connected to the five pin connector (J13, default) or to the banana jacks or scope probe jacks (not populated). Additional test points provide a convenient way to monitor the POR outputs and the signal on the bypass capacitor. This can be especially important when testing the LDO in a temperature chamber. Several ground pins provide reference points for test leads. Additional "kelvin" test points are provided for VIN, VO1, VO2, and GND to monitor the actual performance of the IC. This removes the voltage drops across the PCB traces that occurs at higher currents.

The board has a jumper block for enabling each of the two LDO outputs. A shunt can be placed on J3 or J4 between "ENx" and "LOW" pins to provide a 100kΩ pull down on each EN pin of the device. If J3 or J4 "HI" pins are floating, the respective LDO output will be off, while connecting "HI" to "ENx" will enable the output.

When it is desired that an LDO always be enabled, connect a shunt between "ENx" and "HI" on J3 or J4. In this case the shunt between "ENx" and "LOW" is not needed.

If an external enable signal that drives both high and low is used to enable the LDO outputs, both shunts can be removed from ENx.

A jumper (J10) connects the CPOR input to a 10nF capacitor for POR timing. The jumper can be removed and replaced by a different capacitor to ground for different power on timing requirements.

The board also provides a connector (JP1, not populated) which can connect to a logic analyser/pattern generator for controlling and monitoring the output response. The connector provides both enable inputs and POR outputs.

Finally, a daughter card connector and a jumper (J14 and J9, not populated) allow specially assembled boards containing untrimmed LDOs to be programmed to custom voltage levels after board assembly. This is done at the factory, so no additional information will be provided in this document.

Ordering Information

PART NUMBER	DESCRIPTION
ISL9000**NJ**EV2	ISL9000NJ Evaluation board [3.3V/2.8V]
ISL9000**NF**EV2	ISL9000NF Evaluation board [3.3V/2.5V]
ISL9000**KK**EV2	ISL9000KK Evaluation board [2.85V/2.85V]
ISL9000**KJ**EV2	ISL9000KJ Evaluation board [2.85V/2.8V]
ISL9000**KF**EV2	ISL9000KF Evaluation board [2.85V/2.5V]
ISL9000**JB**EV2	ISL9000JB Evaluation board [2.8V/1.5V]
ISL9000**FJ**EV2	ISL9000FJ Evaluation board [2.5V/2.8V]
ISL9000**KC**EV2	ISL9000KC Evaluation board [2.85V/1.8V]
ISL9000**BJ**EV2	ISL9000BJ Evaluation board [1.5V/2.8V]
ISL9000**PL**EV2	ISL9000PL Evaluation board [1.85V/2.9V]
ISL9000**GC**EV2	ISL9000GC Evaluation board [2.7V/1.8V]
ISL9000**JC**EV2	ISL9000JC Evaluation board [2.8V/1.8V]
ISL9000**JR**EV2	ISL9000JR Evaluation board [2.8V/2.6V]
ISL9000**JM**EV2	ISL9000JM Evaluation board [2.8V/3.0V]
ISL9000**LL**EV2	ISL9000LL Evaluation board [2.9V/2.9V]
ISL9000**MM**EV2	ISL9000MM Evaluation board [3.0V/3.0V]

Features

- Complete dual low dropout regulator (LDO)
- Easy to use board for evaluation of the LDO in a target application.
- Exposed soldering pads/pins for monitoring VIN, VO1, VO2, POR1, POR2, and CBYP.
- Voltage monitoring using test pins, banana jacks and scope jacks.
- Enable jumpers for each supply, plus jumpered enable pull down resistors.
- The board has options for:
  - Changing the CPOR capacitor
  - Using a logic analyser/pattern generator to monitor enable/POR response.

What is Inside

The Evaluation Kit contains:

- ISL9000__EV2 Evaluation board
- The ISL9000 Data Sheet
- The ISL9000EV2 Users Guide (this document)

What is Needed

The following instruments will be needed to perform testing (not provided):

- DC 6.5V/1A Power supply
- Two Digital Voltmeters (4.5 digit or better).
- Oscilloscope
- 2 channel, 0 to 400mA electronic load
- Cables and wires

Quick Setup Guide

Step 1: Place shunts on J3 between “EN1” and HI”, on J4 between “EN1” and HI”, and on J10 (CPOR). This is the factory default connection.

Step 2: Set the power supply to 3.8V with a 1.0A current limit (then turn off).

Step 3: Connect the power supply between VIN and GND using connector J2.

Step 4: Connect two voltmeter positive leads to the VO1 “kelvin” connector (J13-1, “V1K”) and the VO2 “kelvin” connector (J13-5, “V2K”). The meters can also be connected to the VO power pins J2-2 and J2-4 or the banana jacks, but at higher currents, these won’t reflect the output voltage as accurately as the kelvin connections.
Connect the negative leads to GND J13-3. (To get the best representation of the IC output voltage under all output loading conditions, add a ground terminal to the GNDk pad and connect the meter ground leads there).

Step 5: Connect a third voltmeter to the input. This can be connected to the J2 terminal, but at higher inputs, the VIk terminal will give the most accurate reading of the voltage at the ISL9000 VIN pin.

Step 6: (Optional) Connect an electronic load to one or both of the outputs. For the VO1 output, use the VO1 power connector J2-2 (“V1P”). For the VO2 output, use the VO2 power connector J2-4 (“V2P”).

Step 7: Monitor VO1and VO2. The voltages should reflect the voltage of the selected part, i.e. the ISL9000NJ EV2 board should have 3.3V and 2.8V outputs. For a complete list of output voltages, see Table 1.

Step 8: Change the loading on each output and monitor the output voltages

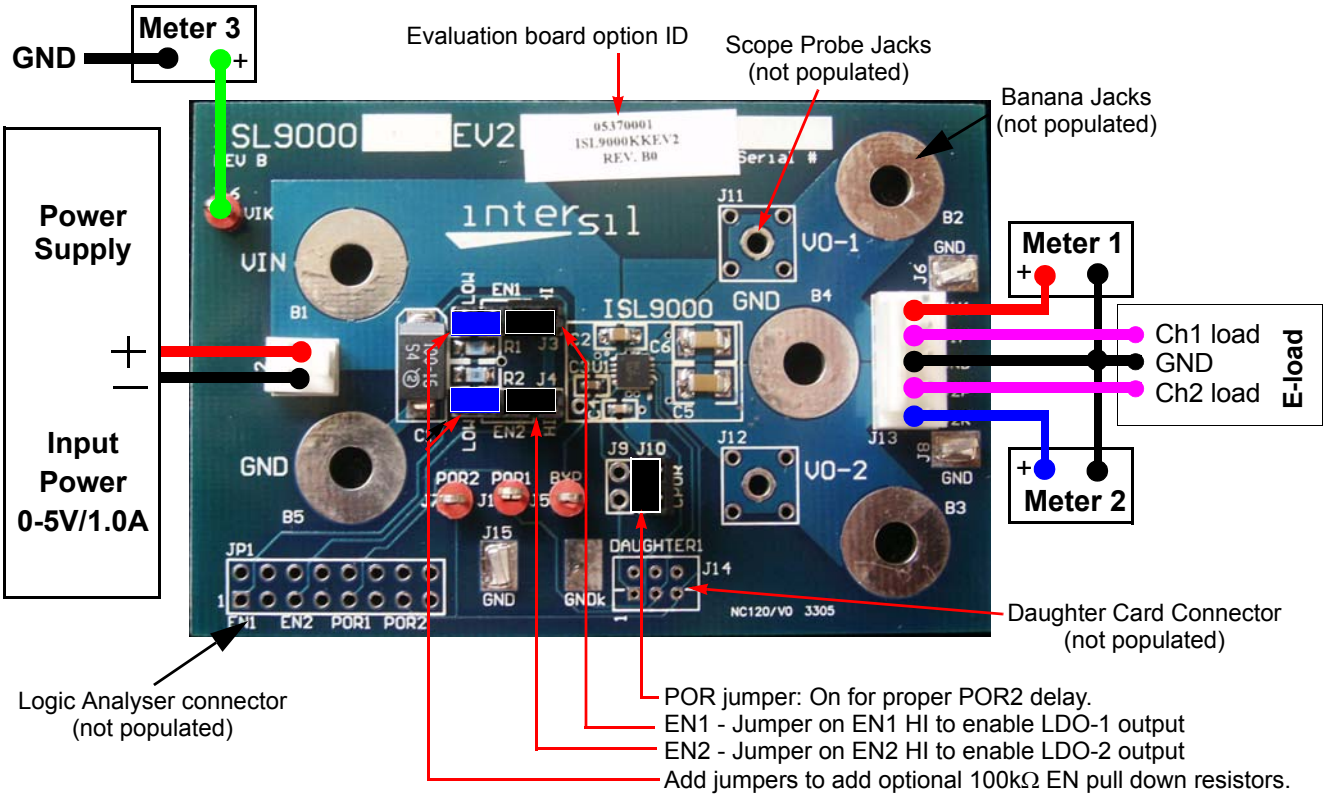

FIGURE 1. BOARD CONNECTION DIAGRAM

Step 9: Change the input voltage and monitor the effect on the output voltages

For additional testing, such as load transient and line transient response, adding the optional scope jacks will improve the measurement, by reducing external noise. The Scope Jack part number is included in the bill of materials as an optional component.

If desired, banana jacks can be added to the board to facilitate connection of the board to test equipment. Part numbers for these optional components are included in the bill of materials.

Improved PSRR and noise specs can be obtained by replacing the 0.01µF (C3) capacitor with a 0.1µF capacitor.

TABLE 1. OUTPUT VOLTAGES

	OUTPUT VOLTAGE 1		OUTPUT VOLTAGE 2	
PART NUMBER	MIN	MAX	MIN	MAX
ISL9000**NJ**EV2	3.267	3.333	2.772	2.828
ISL9000**NF**EV2	3.267	3.333	2.475	2.525
ISL9000**KK**EV2	2.821	2.879	2.821	2.879
ISL9000**KJ**EV2	2.821	2.879	2.772	2.828
ISL9000**KF**EV2	2.821	2.879	2.475	2.525
ISL9000**JB**EV2	2.772	2.828	1.485	1.515
ISL9000**FJ**EV2	2.475	2.525	2.772	2.828
ISL9000**KC**EV2	2.821	2.879	1.782	1.818
ISL9000**BJ**EV2	1.485	1.515	2.772	2.828
ISL9000**PL**EV2	1.831	1.869	2.871	2.929
ISL9000**GC**EV2	2.673	2.727	1.782	1.818
ISL9000**JC**EV2	2.772	2.828	1.782	1.818
ISL9000**JR**EV2	2.772	2.828	2.574	2.626
ISL9000**JM**EV2	2.772	2.828	2.970	3.030
ISL9000**LL**EV2	2.871	2.929	2.871	2.929
ISL9000**MM**EV2	2.970	3.030	2.970	3.030

Schematic

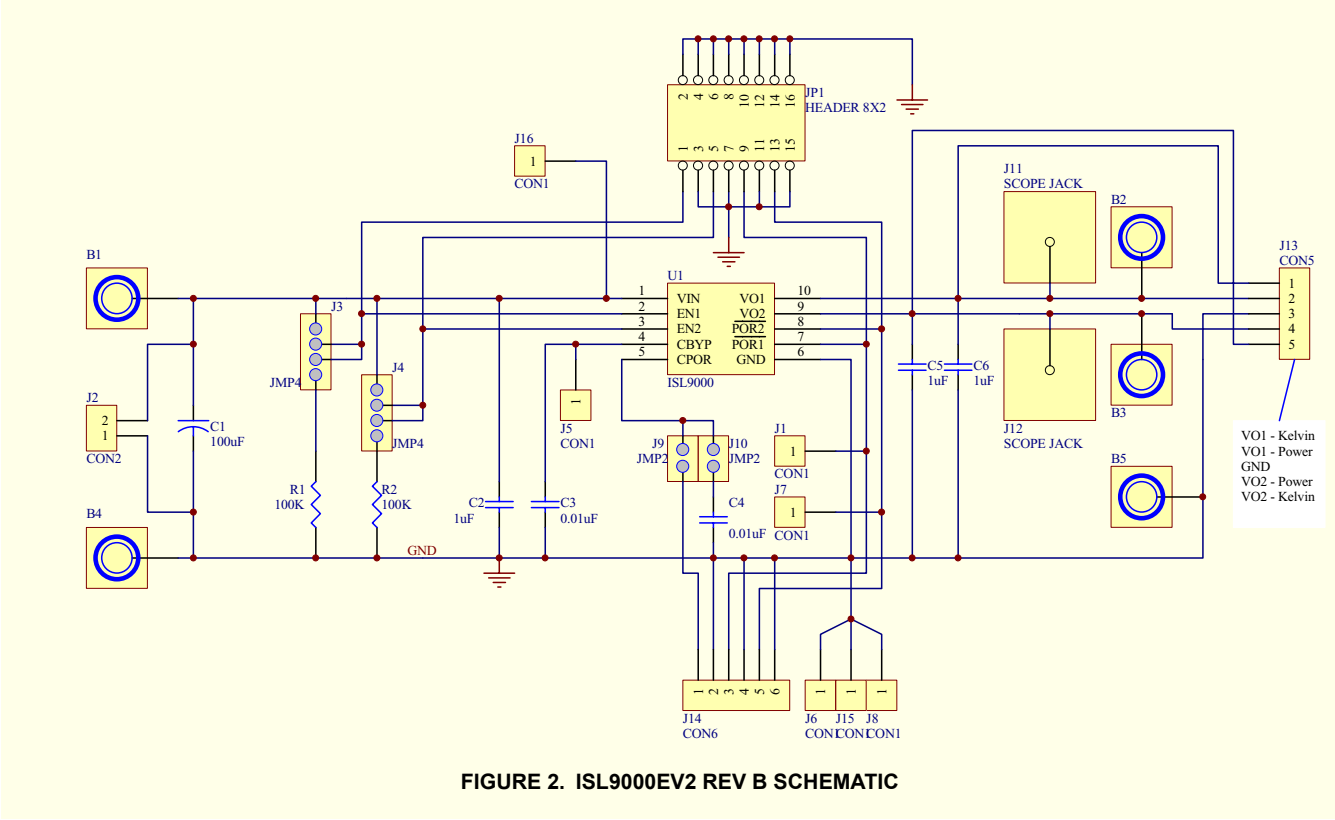

FIGURE 2. ISL9000EV2 REV B SCHEMATIC

Bill of Materials

ITEM	QTY	PART TYPE	DESIGNATOR	MFR	DIGIKEY	COMMENTS
COMPONENTS COMMON TO ALL BOARDS						
1	1	PCB	PCB	ISL9000EV2 REVB		
2	2	0.01µF	C3, C4	AVX: 06035C103KAT2A	478-1227-2-ND	0603 capacitor
3	1	1µF	C2	Panasonic: ECJ-2FB1C105K	PCC2249CT-ND	0805 capacitor
4	2	1µF	C5, C6	Panasonic: ECJ-3YB1E105K	PCC1893CT-ND	1206 or 1210 capacitor
5	2	100K	R1, R2	Panasonic: ERJ-3EKF-100KV	P100KHCT-ND	Any 0805 resistor
6	1	100µF	C1	KEMET: T491D107M016AS	Digikey: 399-1605-1-ND	
7	4	CON1	J1, J5, J7, J16	Keystone: 5010	Digikey: 5010K-ND	
8	3	CON1	J6, J8, J15	Keystone: 5016	Digikey: 5016KCT-ND	
9	1	CON2	J2	Molex: 22-23-2021	Digikey: WM4200-ND	
10	1	CON5	J13	Molex: 22-23-2051	Digikey: WM4203-ND	
11	1	JMP2	J10	Molex: 22-28-4020	Digikey: WM6402-ND	
12	2	JMP4	J3, J4	Molex: 22-28-4040	Digikey: WM6404-ND	
13	3	Shunt		AMP: 382811-8	Digikey: A26228-ND	Installed at test - ship 10 to a strip, but only 3 needed/board
COMPONENTS SPECIFIC TO EACH BOARD VARIATION						
14	1	ISL9000	U1	Intersil: ISL9000IR_ _Z	*	ISL9000_ _EV2 REVB only
15	1	Label	L1	_ _Label		ISL9000_ _EV2 REVB only
COMPONENTS OPTIONAL ON EACH BOARD						
16	2	SCOPE JACK	J11, J12	Tektronix #131-5031-00	*	Not populated
17	3	BANANA	B1, B2, B3	Keystone: 7006	7006K-ND	Not populated
18	2	BANANA	B4, B5	Keystone: 7007	7007K-ND	Not populated
19	1	JMP2	J9	Molex: 22-28-4020	Digikey: WM6402-ND	Not populated
20	1	CON6	J14	HRS: DF11-6DS-2DSA	Digikey: H2274	Not populated
21	1	HEADER 8X2	JP1	Molex: 10-88-1161	Digikey: WM6916-ND	Not populated