ISLRTPFDEMO1Z

Renesas RT Power Solution for Microchip RT PolarFire® FPGA

Description

The ISLRTPFDEMO1Z demonstration board provides a power management solution for the Microchip RT PolarFire FPGA family using Renesas' Radiation Tolerant Power Management devices. The RT PolarFire system requires various supply rails, including the core, digital, analog, GPIO, and DDR memory. The ISLRTPFDEMO1Z provides all rails for the user to evaluate the performance against the RT PolarFire DC and AC electrical specifications. The demonstration board provides a connection to support integration with the ISL71148VMREFEV2Z ADC voltage monitor board with GUI interface.

Features

- Includes regulators for all RT PolarFire rails, DDR4 memory and general 5V and 3.3V bus
- Power supply sequencing for power up and down for increased system reliability
- All DC-DC switching converters are clock synchronized
- Input bus current sense
- Voltage monitoring capability using the ISL71148VMREFEV2Z demo board

Power Supply Specifications

- $12V_{DC}$ ±10% (Supports bench top supply with banana jack or AC adapter using barrel jack)

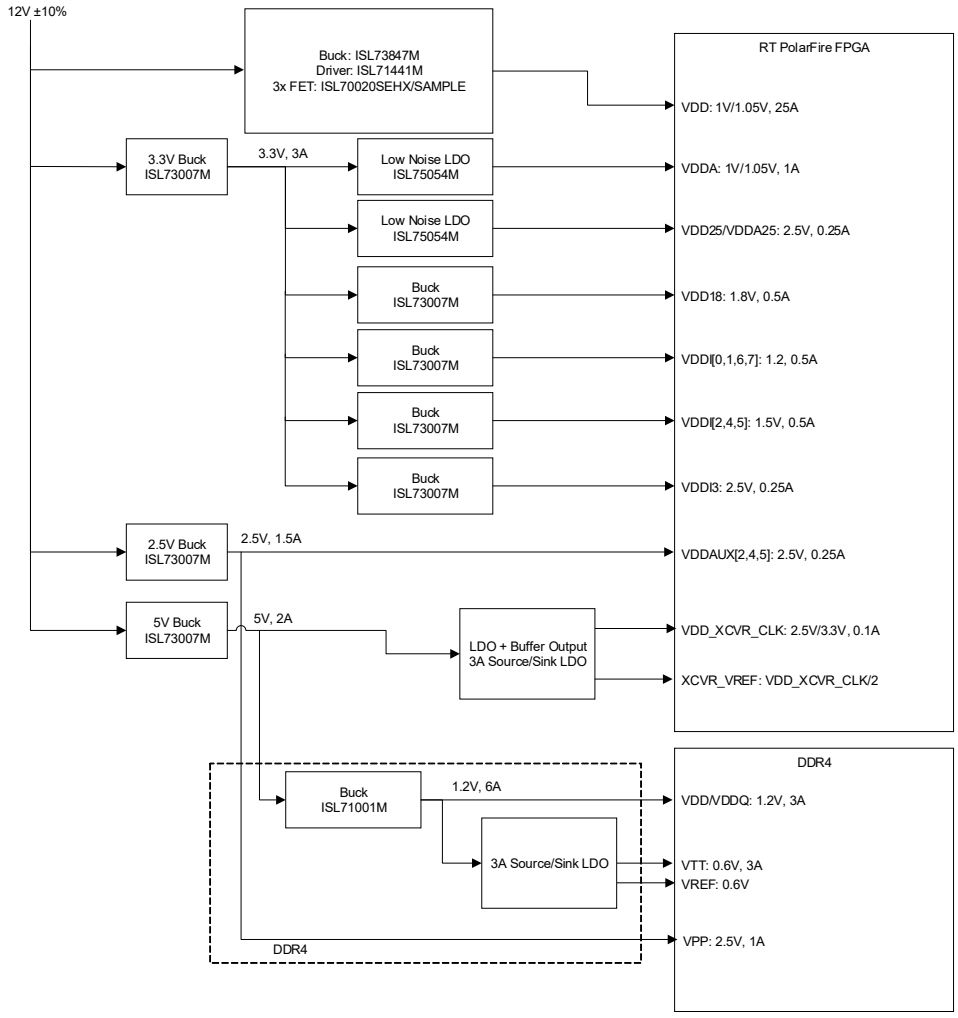


Figure 1. Power Management Block Diagram

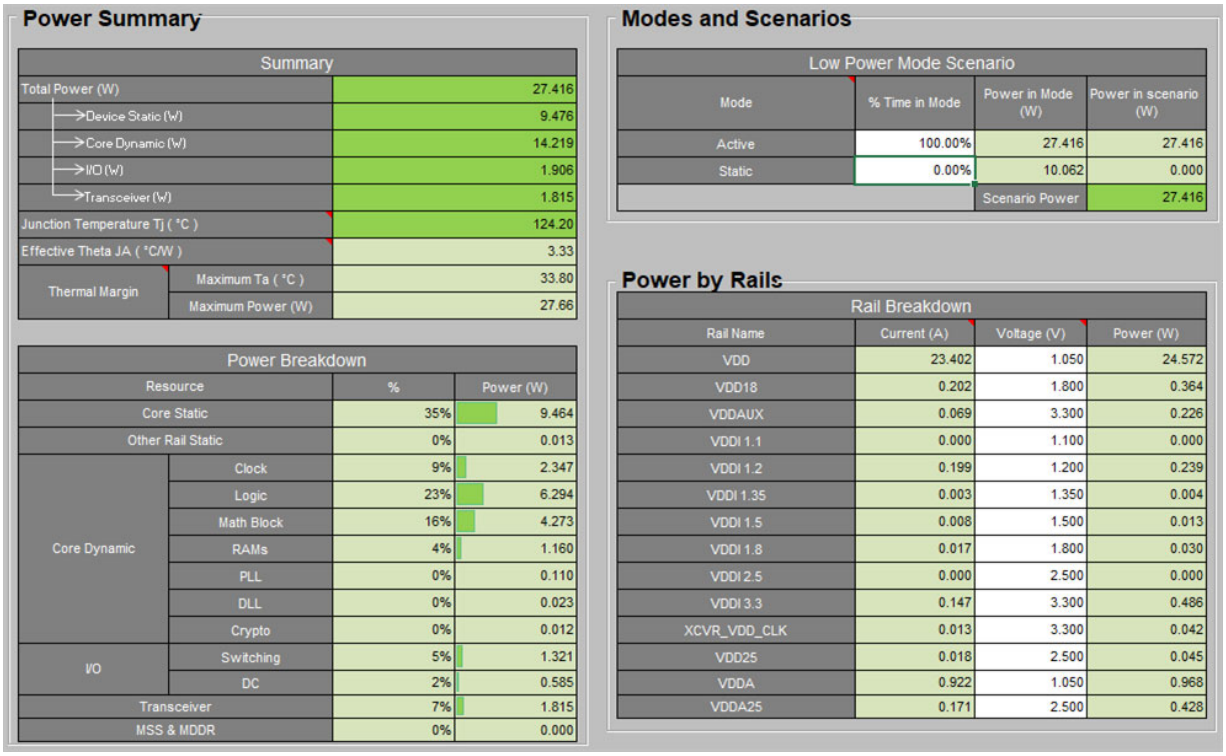
Contents

1. Functional Description

1.1 Power Tree

The power tree diagram is shown in Figure 3 and the Microchip RT PolarFire FPGA supply rail requirements are shown in Figure 2. The power management solution is developed for the maximum resource utilization to simulate worst case power consumption conditions.

The ISLRTPFDEMO1Z demonstration board operates on a +12V DC power supply. This design also includes Renesas solutions for current sense and voltage monitoring, clock generation, and sequencing.



Power Summary

Summary	
Total Power (W)	27.416
→Device Static (W)	9.476
→Core Dynamic (W)	14.219
→I/O (W)	1.906
→Transceiver (W)	1.815
Junction Temperature Tj (°C)	124.20
Effective Theta JA (°C/W)	3.33
Thermal Margin – Maximum Ta (°C)	33.80
Thermal Margin – Maximum Power (W)	27.66

Power Breakdown			
Resource		%	Power (W)
Core Static		35%	9.464
Other Rail Static		0%	0.013
Core Dynamic	Clock	9%	2.347
	Logic	23%	6.294
	Math Block	16%	4.273
	RAMs	4%	1.160
	PLL	0%	0.110
	DLL	0%	0.023
	Crypto	0%	0.012
I/O	Switching	5%	1.321
	DC	2%	0.585
Transceiver		7%	1.815
MSS & MDDR		0%	0.000

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (W)	Power in scenario (W)
Active	100.00%	27.416	27.416
Static	0.00%	10.062	0.000
		Scenario Power	27.416

Power by Rails

Rail Breakdown			
Rail Name	Current (A)	Voltage (V)	Power (W)
VDD	23.402	1.050	24.572
VDD18	0.202	1.800	0.364
VDDAUX	0.069	3.300	0.226
VDDI 1.1	0.000	1.100	0.000
VDDI 1.2	0.199	1.200	0.239
VDDI 1.35	0.003	1.350	0.004
VDDI 1.5	0.008	1.500	0.013
VDDI 1.8	0.017	1.800	0.030
VDDI 2.5	0.000	2.500	0.000
VDDI 3.3	0.147	3.300	0.486
XCVR_VDD_CLK	0.013	3.300	0.042
VDD25	0.018	2.500	0.045
VDDA	0.922	1.050	0.968
VDDA25	0.171	2.500	0.428

Figure 2. Power Management Specification from Microchip RT PolarFire FPGA Power Estimator Tool

Note: Actual power requirements vary based on user's design and FPGA resource utilization.

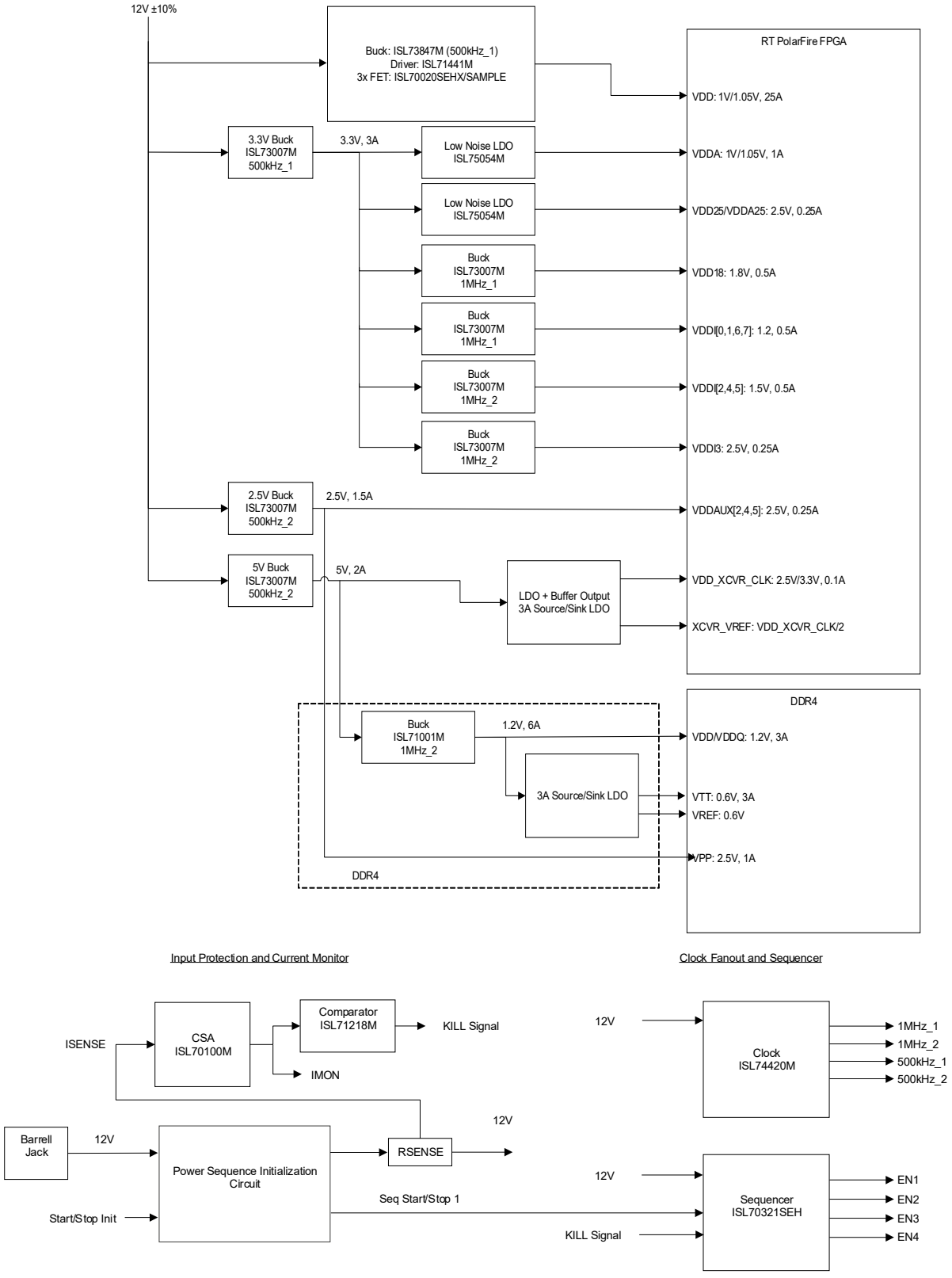


Figure 3. Renesas Radiation Tolerant Power Tree for Microchip RT PolarFire FPGA

1.2 Renesas Power Management Solution

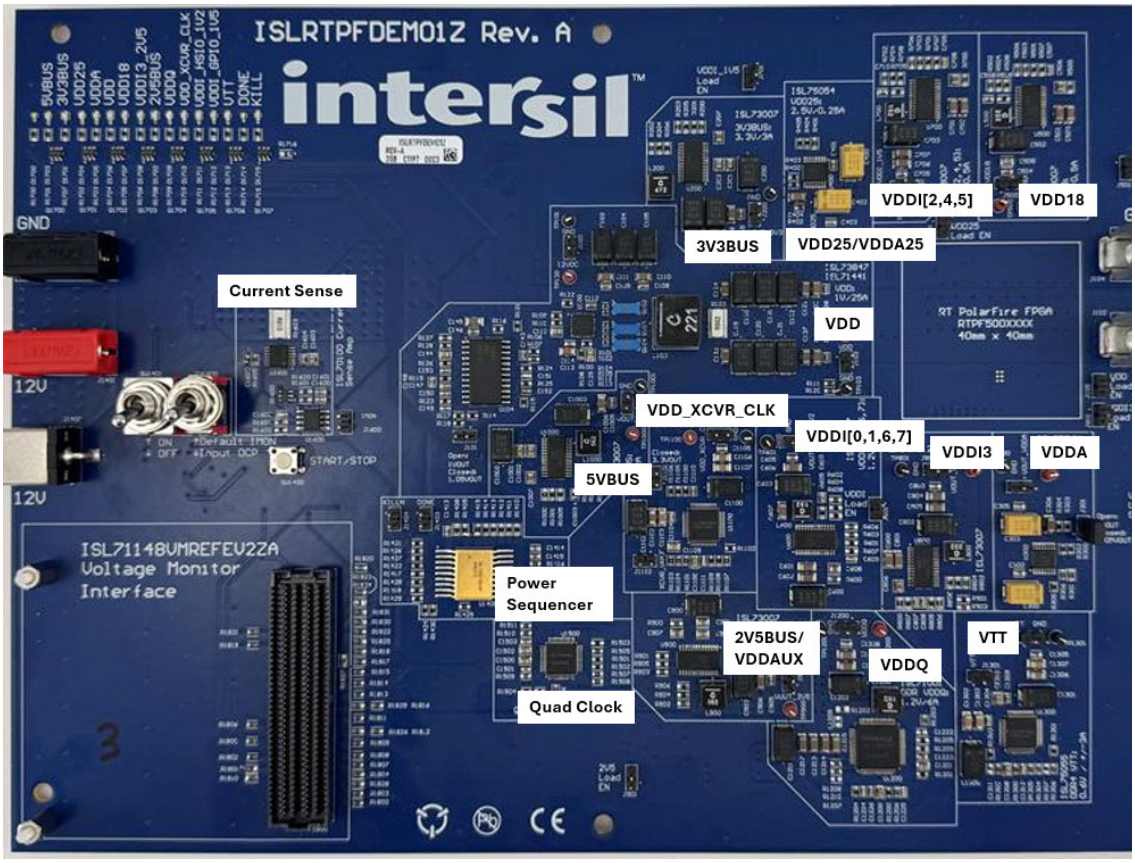


Figure 4. ISLRTPFDEMO1Z Board Photo

Table 1 shows the power management specifications for the Microchip RT PolarFire FPGA.

Table 1. Power Management Specifications for Microchip RT PolarFire FPGA

Rail Name	Rail Voltage (V)	Current Demand (A)	DC Tol + Ripple (mV)	AC Tol (mV)	Power Sequencing	Renesas Solution
VDD	1/1.05	25	±30	±130	2	ISL73847 - RT Current Mode PWM Controller ISL73041 - RT 12V Half-Bridge GaN FET Driver ISL70020SEHX - 40V, 65A Enhancement Mode GaN Power Transistors
VDDA	1/1.05	1	±30	±130	3	ISL75054 - RT Ultra Low Noise, 1A LDO
VDD25/VDDA25	2.5	0.25	±75	±200	2	ISL75054 - RT Ultra Low Noise, 1A LDO
VDD18	1.8	0.5	±90	±200	2	ISL73007 - RT 18V, 3A Point-of-Load Regulator
VDDI[0,1,6,7]	1.2	0.5	±60	±120	4	ISL73007 - RT 18V, 3A Point-of-Load Regulator
VDDI[2,4,5]	1.5	0.5	±60	±150	4	ISL73007 - RT 18V, 3A Point-of-Load Regulator
VDDI3	2.5	0.25	±90	±180	2	ISL73007 - RT 18V, 3A Point-of-Load Regulator
VDDAUX[2,4,5]	2.5	0.25	±125	±200	2	ISL73007 - RT 18V, 3A Point-of-Load Regulator
VDD_XCVR_CLK	2.5/3.3	0.1	±125	±200	3	RT 3A Source and Sink DDR Terminator/LDO with Buffered Reference
XCVR_VREF	VDD_XCVR_CLK/2	N/A	N/A	N/A	-	
5VBUS	5	2	N/A	N/A	1	ISL73007 - RT 18V, 3A Point-of-Load Regulator

Table 1. Power Management Specifications for Microchip RT PolarFire FPGA (Cont.)

Rail Name	Rail Voltage (V)	Current Demand (A)	DC Tol + Ripple (mV)	AC Tol (mV)	Power Sequencing	Renesas Solution
3V3BUS	3.3	3	N/A	N/A	1	ISL73007 - RT 18V, 3A Point-of-Load Regulator
DDR_VDDQ	1.2	3	±60	±120	3	ISL71001 - RT 6A Sync Buck Regulator with Integrated MOSFETs
DDR_VTT	0.6	3	±30	±60	4	RT 3A Source and Sink DDR Terminator/LDO with Buffered Reference
DDR_VPP/2V5BUS	2.5	1.5	±125	±200	2	ISL73007 - RT 18V, 3A Point-of-Load Regulator

The most prominent power supply rail for the RT PolarFire power management solution is the VDD core rail, which consumes up to 25A while delivering either 1V or 1.05V. This is provided by the Renesas radiation tolerant point-of-load regulator that consists of: (1) ISL73847M radiation tolerant single/dual-phase current mode PWM controller, (1) ISL71441M radiation tolerant 12V half-bridge GaN FET driver, and (3) ISL70020SEH 40V, 65A, 3.5mΩ GaN FET in a die bump package.

The VDD core supply is stepped down directly from 12V operating at 500kHz switching frequency.

The ISL75054M radiation tolerant low noise low-dropout linear regulator is used for the noise sensitive 1V/1.05V VDDA and 2.5V VDDA25 supplies.

The ISL73007M radiation tolerant 3A point-of-load regulator is used for HSIO, GPIO, and auxiliary supplies. It also generates 3.3V and 5V bus rails.

A complete DDR4 memory power solution is also included using the ISL71001 6A radiation tolerant synchronous buck regulator with integrated MOSFETs for 1.2V VDDQ, a 3A sink source LDO for 0.6V VTT, and ISL73007 for 2.5V VPP.

The ISL70321 quad power supply sequencer manages the power up/down of all voltage rails. Outputs from the sequencer are tied to the enable pins on all power devices to satisfy the RT PolarFire timing requirements.

The ISL74420 quad clock generator generates 2x 1MHz clocks and 2x 500kHz clocks that are distributed to all switching converters across the board.

The ISL70100 current-sense amplifier is used for input current sensing and the ISL71218 op amp is used in a comparator configuration to detect input overcurrent.

1.3 Adjustable Output Voltages

The RT PolarFire FPGA specifies options for different operating voltages on certain rails depending on system requirements. The ISLRTPFDEMO1Z includes the necessary jumpers to change the feedback resistors to set the different output voltages on certain key rails.

The VDD rail can be adjusted for 1V or 1.05V.

Table 2. VDD Output Voltage Setting

VOUT (V)	Jumper J101
1	Open
1.05	Closed

The VDDA rail can be adjusted for 1V or 1.05V.

Note: 1.0V VDDA is only supported on RTPF500T and not on RTPF500ZT.

Table 3. VDDA Output Voltage Setting

VOUT (V)	Jumper J301
1	Closed
1.05	Open

The VDD_XCVR_CLK rail can be adjusted for 2.5V or 3.3V

Table 4. VDD_XCVR_CLK Output Voltage Setting

VOUT (V)	Jumper J1101
2.5	Open
3.3	Closed

1.4 Output Voltage Test Points and Load Transient Control

The ISLRTPFDEMO1Z provides test points for monitoring the output voltage and applying an external load. Some output rails also provide an on-board transient load step generator. The on-board transient load generator can be turned on by populating the enable jumpers as described in Table 5. Table 5 summarizes the output rail test points and load transient generator control for the voltage rails.

The transient load generator is comprised of a FET driver controlling a common source NFET that pulls a load resistor to GND to provide a transient load to the supply rail. The VDD core rail uses an ISL71040MRTZ GaN FET driver. A typical schematic is shown in Figure 5. All other load generators use the HIP2211 half-bridge driver. A typical schematic is shown in Figure 6. When the transient load generator is enabled, supporting circuitry automatically generates load step pulses.

The automatically generated load step pulses and period can also be altered by changing the resistors and capacitor around the gate drive circuit. Use Equation 1 to set the ON-time and Equation 2 to set the OFF-time. For HIP2211, the VIH is 2.1V typical and the VIL is 1.4V typical. For the ISL71040M, the VIH is 1.7V typical and the VIL is 1.4V typical. By default, for all the HIP2211 load transient circuits R_{ON} is 124Ω, R_{OFF} is 7.15kΩ, and C is 10µF. By default, for the ISL71040M load transient circuit R_{ON} is 261Ω, R_{OFF} is 17.4kΩ, and C is 10µF.

(EQ. 1)
$$R_{ON} = \frac{t_{ON}}{-C \times \ln\left(\frac{VIL}{VIH}\right)}$$

where:

- R_{ON} is the active ON-time resistor.
- t_{ON} is the required active ON-time.
- C is the active ON-charge and active OFF-discharge capacitor.
- VIH is FET driver input high level voltage.
- VIL is the FET driver input low-level voltage.

(EQ. 2)
$$R_{OFF} = \frac{t_{OFF}}{-C \times \ln\left(\frac{VIH - 12V}{VIL - 12V}\right)} - R_{ON}$$

where:

- R_{OFF} is the active OFF-time resistor.
- t_{OFF} is the required active OFF-time.

Table 5. Output Voltage Test Points and Load Transient Control

Voltage Rail	Oscilloscope VOUT Test Point	VOUT DC Test Point/External Load Access (VOUT/GND)	On-board Load Transient Enable (Closed = ON)
12VDC	J100	TP100/TP101	-
VDD	J103	TP102/TP103 (Test Point) J102/J104 (Load Point)	J105
3V3BUS	J200	TP200/TP201	-
VDDA	J300	TP300/TP301	J302
VDD25/VDDA25	J400	TP400/TP401	J401
VDD18	J500	TP500/TP501	J501
VDDI[0,1,6,7]	J600	TP600/TP601	J601
VDDI[2,4,5]	J700	TP700/TP701	J701
VDDI3	J800	TP800/TP801	J801
VDDAUX[2,4,5]	J900	TP900/TP901	J901
5VBUS	J1000	TP1000/TP1001	-
VDD_XCVR_CLK	J1100	TP1100/TP1101	-
XCVR_VREF	J1102	-	-
VDDQ	J1200	TP1200/TP1201	-
VTT	J1300	TP1300/TP1301	-
VTT_REF	J1301	-	-

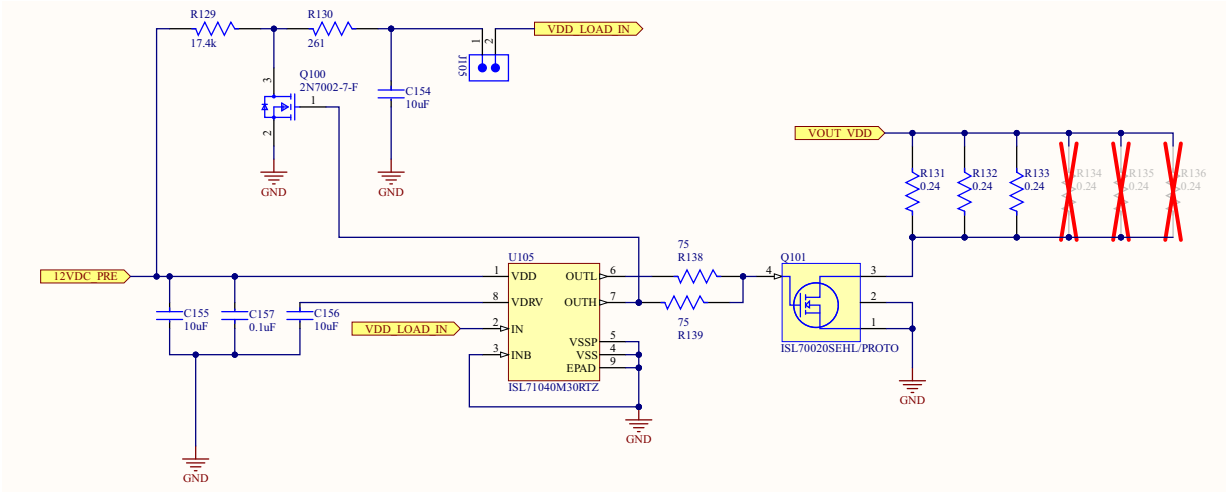


Figure 5. 12.5A VDD Load Transient Circuit using ISL71040 RT GaN FET Driver and ISL70020 GaN Power Transistor

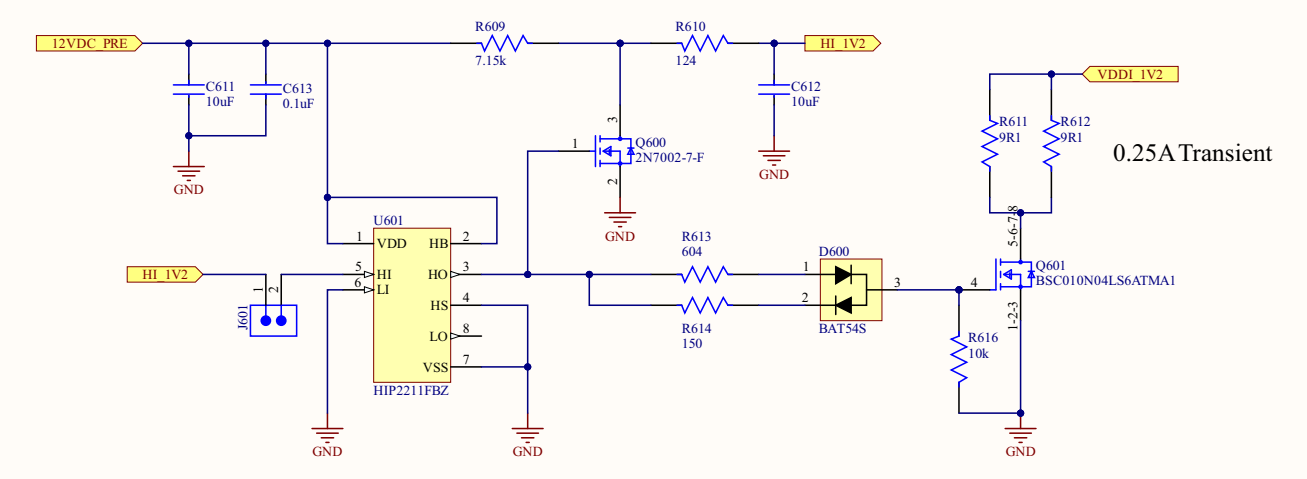


Figure 6. Typical Load Transient Circuit using HIP2211 HB Driver

1.5 Power Sequencing and Monitoring

The ISL70321SEH quad power supply sequencer controls the power sequencing of all supply rails. When a sequence up or down is initiated, the supply rails are enabled or disabled in a sequence, as shown in Figure 37 through Figure 42.

The sequencer uses a total of four EN signals to enable or disable all converters in four groups. One rail from each of the groups is monitored by the sequencer VM pins to detect the rising and falling threshold needed for proper sequencing. This grouping is shown in Table 6 and Table 7.

The DONE pin asserts high to signify completion of the power-up sequence. The DONE signal can be measured on test point J1403.

Table 6. Sequencing Enable Signal for Corresponding Power Rail

ENx Output	Voltage Rail
EN1	5VBUS, 3V3BUS
EN2	VDD, VDDA, VDD25/VDDA25, VDD18, VDDAUX/2V5BUS, VDDI3
EN3	VDD_XCVR_CLK, DDR_VDDQ
EN4	VDDI[0,1,6,7], VDDI[2,4,5], DDR_VTT

Table 7. Voltage Monitoring for Sequencing Enable Thresholds

VMx Input	Voltage Rail
VM1	5VBUS
VM2	VDD
VM3	VDDQ
VM4	VDDI[2,4,5]

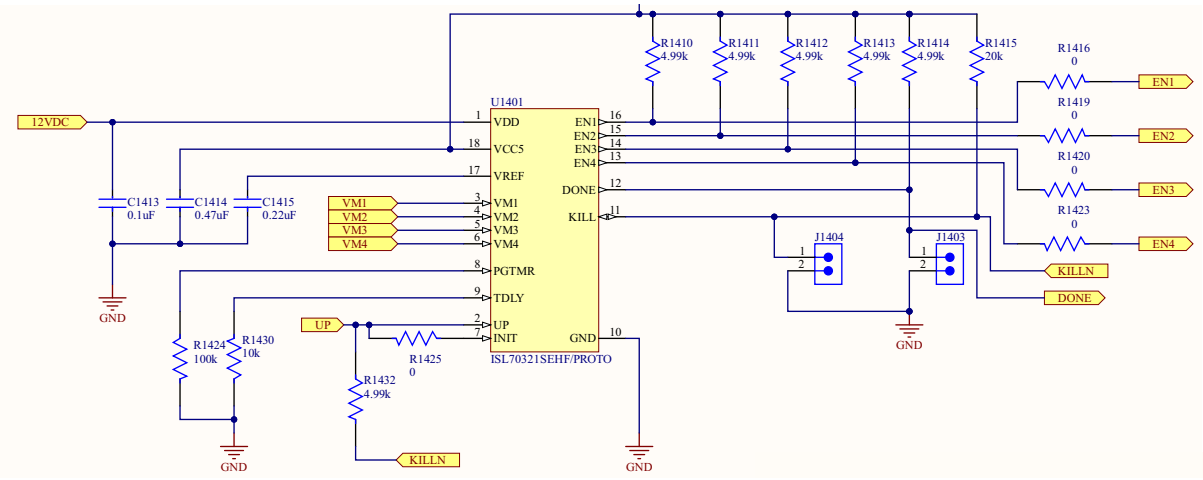


Figure 7. Power Supply Sequencer Schematic

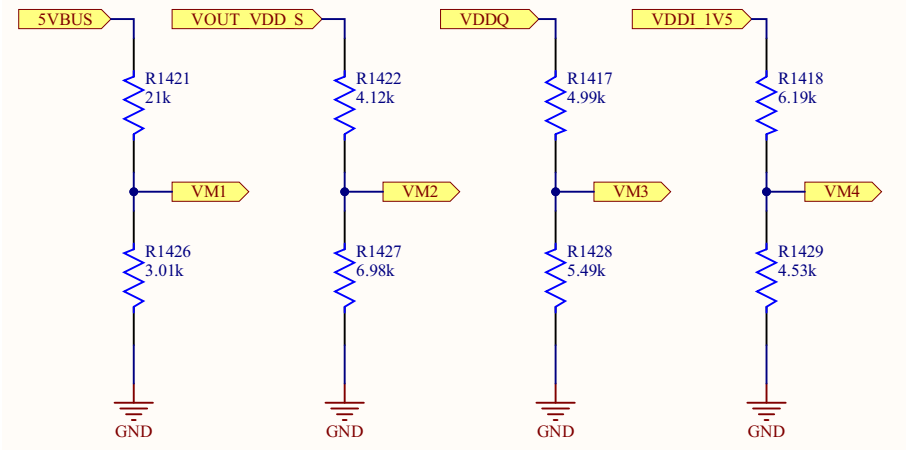


Figure 8. Power Supply Sequence Voltage Monitor Dividers

1.6 12V Power Supply and Sequencing Initialization

The +12V_{DC} power supply to the ISLRTPFDEMO1Z is provided by banana jack inputs to the board. Back-to-back PMOS FETs prevent reverse current flow back to the power supply. A mechanical switch (SW1401) turns the power on and off for the board. Power sequence initialization is provided by a push button switch (SW1400) and the CD4027B JK flip flop (U1400). Pushing the button switch provides one pulse, which latches the JK flip flop high and low, alternating with every push. The flip flop output signal drives ISL70321 to initiate startup and shutdown sequencing. The main power switch, SW1401, also controls the RESET pin of the JK flip flop. When the power switch is thrown off, the RESET signal triggers a power-down sequence of the ISL70321SEH sequencer instead of an uncontrolled shutdown of the power rails. At the same time, a large RC time constant to the gate of Q1402 PMOS delays the turn-off of the 12V supply to the board for the power-down sequence to be completed.

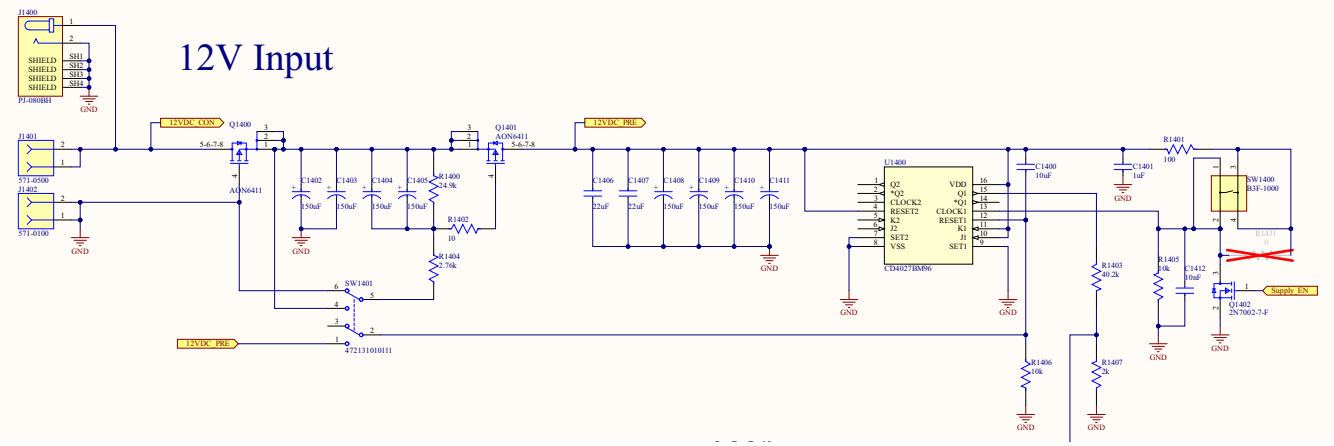


Figure 9. 12V Input and Sequencer Initialization

1.7 Switching Converter Clock Synchronization

All DC/DC switching converters on the ISLRTPFDEMO1Z are clock synchronized with a single ISL74420 quad clock generator configured as a master. The circuit generates 0V to 5V clocks at 500kHz and 1MHz frequencies. Distribution to the various power rails is described in Table 8.

Table 8. Switching Converter Clock Synchronization

Voltage Rail	Clock Net Name	Frequency (kHz)
VDD	500kHz_1	500
3V3BUS	500kHz_1	500
VDD18	1MHz_1	1000
VDDI[0,1,6,7]	1MHz_1	1000
VDDI[2,4,5]	1MHz_2	1000
VDDI3	1MHz_2	1000
VDDAUX[2,4,5]	500kHz_2	500
5VBUS	500kHz_2	500
VDDQ	1MHz_2	1000

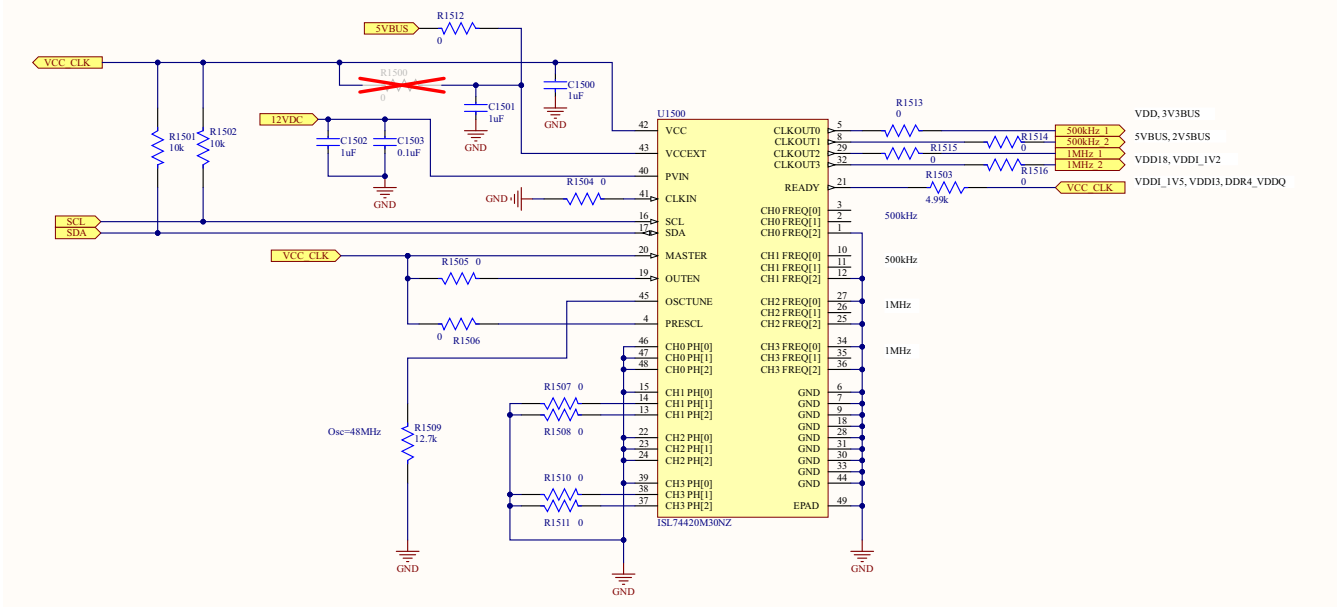


Figure 10. ISL74420 Quad Clock Schematic

1.8 12V Bus Current Sensing and KILL Comparator

The total +12V bus supply current to the system can be monitored as a voltage (IMON) using the ISL70100M current-sense amplifier. The circuit converts 0A to 10A to an output voltage of 0V to 1V. The output voltage range can be scaled by adjusting the output load resistor R1605. R1605 is 7.5kΩ by default and should be considered in parallel with R1820 and R1825. R1820 and R1825 are required to divide down the voltage read by the ADC.

Use Equation 3 to convert the IMON voltage to the 12V input supply current. The default R_{SENSE} on the board is 15mΩ. R_{OUT} is calculated by R1605 in parallel with R1820 and R1825, an equivalent value of 3.39kΩ.

(EQ. 3) $$I_{SENSE} = \frac{IMON}{R_{SENSE} \times R_{OUT} \times 0.002A/V}$$

where:

- IMON is the OUT voltage of the current sense amp.
- I_{SENSE} is the 12V bus supply current in amps.
- R_{SENSE} is the 12V bus current sense resistance in ohms.
- R_{OUT} is the output load scaling resistance

The IMON signal is tied to the inverting input of the ISL71218M op amp. The circuit in Figure 11 shows how to configure the op amp as a comparator, which disables all the power outputs simultaneously by pulling the KILL pin low on the ISL70321 power sequencer. KILL is pulled low by the comparator when IMON is greater than or equal to 1.0V (VIH). When IMON is less than or equal to 0.8V (VIL), the KILL pins are released and the power supplies automatically start up sequentially again. R1601, R1602, and R1604 can be adjusted to change VIH and VIL. Use Equation 4 to calculate the resistors for the required VIH threshold.

(EQ. 4) $$R1602 = \frac{R1601 \times R1604 \times (12V - VIH)}{R1601 \times VIH - R1604 \times (12V - VIH)}$$

where:

- R1602 is the top resistor in the comparator non-inverting input voltage-divider reference in volts.
- R1604 is the bottom resistor in the comparator non-inverting input voltage divider reference in volts.
- R1601 is the hysteresis resistor in ohms.

- VIH is the required comparator high level threshold in volts.

When the VIH resistors are determined, the VIL threshold can be calculated using Equation 5. Verify the hysteresis (VIH- VIL) is acceptable. If it is not, increase R1601 and recalculate R1602 and VIL.

(EQ. 5) $$VIL = \frac{R1601 \times R1602 \times 12V}{R1602 \times (R1601 + R1604) - R1601 \times R1604}$$

Use SW1600 to toggle between default current monitoring and simulated OCP conditions.

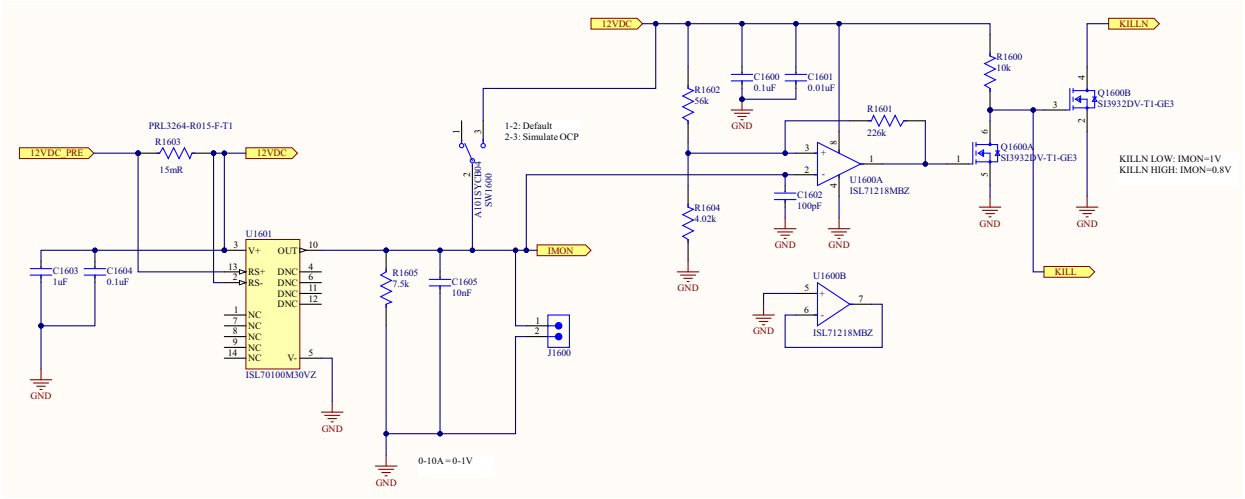


Figure 11. ISL70100 Input Current Sense Schematic

1.9 Voltage Rail Monitoring

Refer to the *ISL71148VMREFEV2Z Evaluation Board Manual* for more information on voltage monitoring and instructions to interface with GUI. The voltage monitor reference design connects to the board using connector J1800 as shown in the schematic in Figure 12. Using voltage dividers ensures that no signal greater than 2.5V is applied to the ADC inputs.

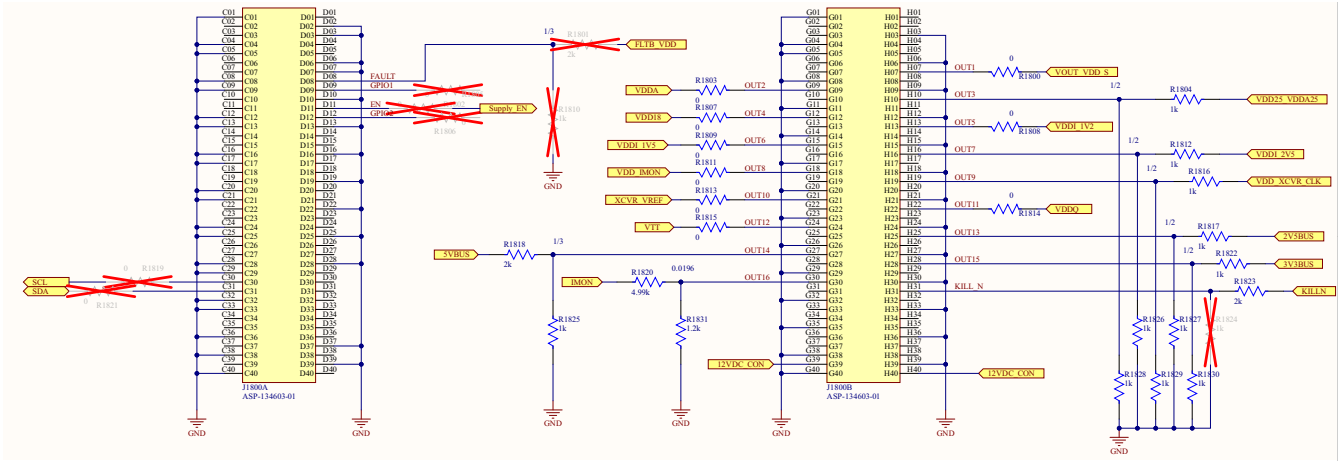


Figure 12. Voltage Monitoring Board Connection

1.10 Layout Guidelines

The ISLRTPFDEMO1Z board represents what a typical power system layout can look like with the high current point-of-load regulators places around the edges of the FPGA. For detailed layout recommendations of the individual components, refer to the respective datasheets and evaluation board manuals. The ISLRTPFDEMO1Z schematic diagram, bill of materials, and board layout files, can be downloaded from the board product page on the Renesas website.

2. Typical Performance Curves

2.1 Steady State Output Voltage Ripple

The recommended power supply tolerances, as described by the *Microchip RT PolarFire Datasheet*, include DC offset of the supply plus any power supply ripple over the customer design frequencies of interest, as measured at the device package pins. An example for a valid power supply that meets the recommendations for the VDD supply is 1.0V ±10mV or 1.05V ±10mV for DC offset with an additional power supply ripple of ±20mV for a total of 1.0V ±30mV or 1.05V ±30mV.

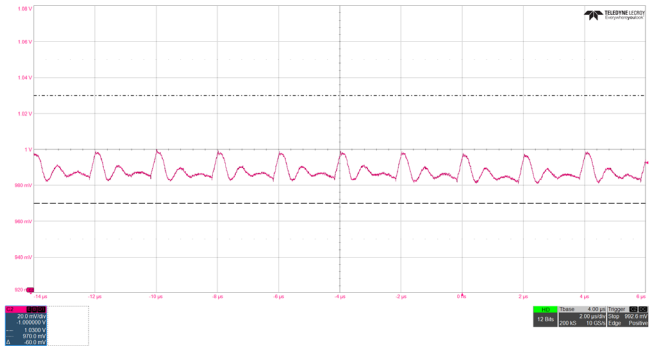


Figure 13. VDD Output Voltage Ripple, ISL73847, 1V/25A, ±30mV Limits

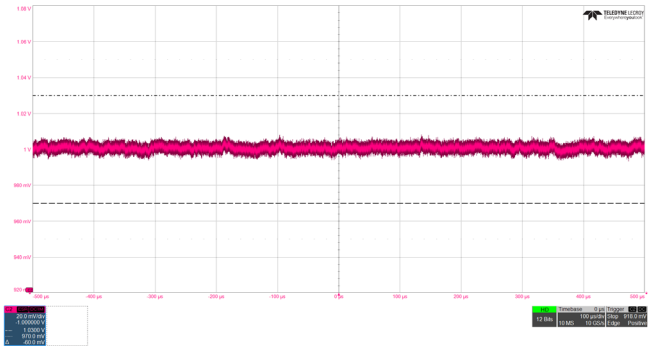


Figure 14. VDDA Output Voltage, ISL5054, 1V/1A, ±30mV Limits

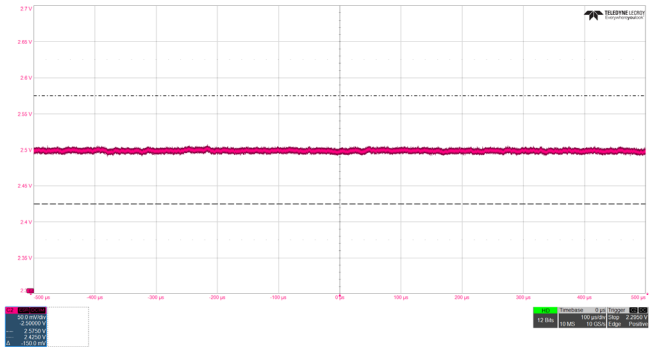


Figure 15. VDD25/VDDA25 Output Voltage, ISL75054, 2.5V/0.25A, ±75mV Limits

Figure 16. Figure 14. VDD18 Output Voltage Ripple, ISL73007, 1.8V/0.5A, ±90mV Limits

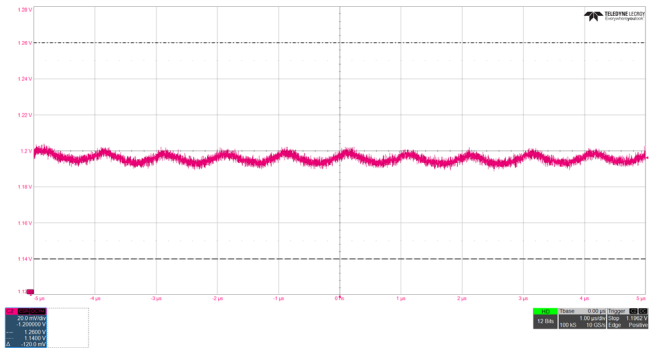


Figure 17. VDDI[0,1,6,7] Output Voltage Ripple, ISL73007, 1.2V/0.5A, ±60mV Limits

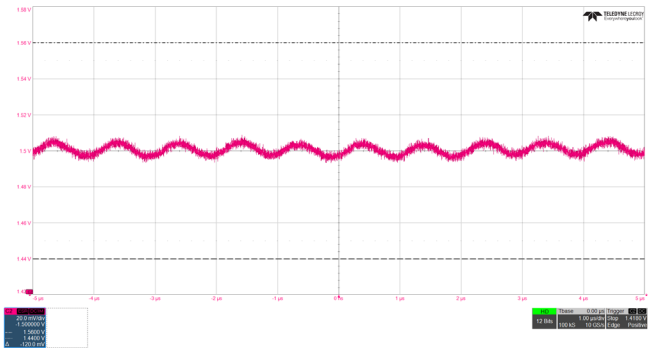


Figure 18. VDDI[2,4,5] Output Voltage Ripple, ISL73007, 1.5V/0.5A, ±60mV Limits

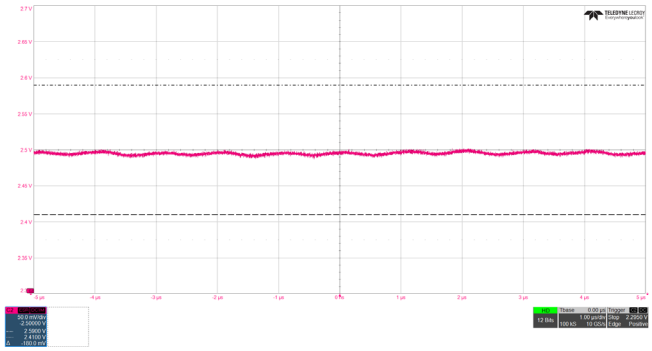


Figure 19. VDDI3 Output Voltage Ripple, ISL73007, 2.5V/0.25A, ±90mV Limits

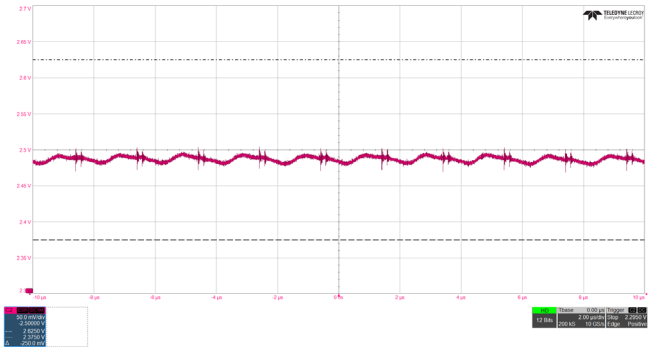


Figure 20. VDDAUX[2,4,5]/VPP/2V5BUS Output Voltage Ripple, ISL73007, 2.5V/1.5A, ±125mV Limits

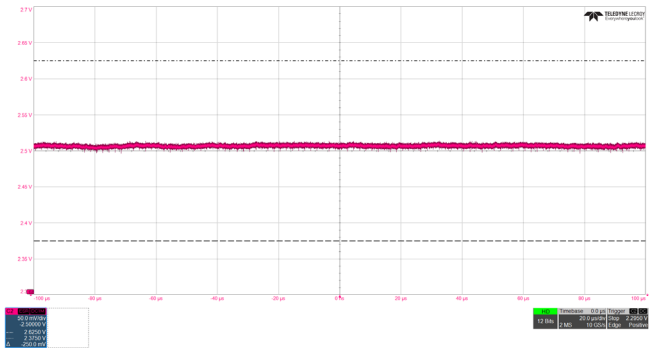


Figure 21. VDD_XCVR_CLK Output Voltage, 3A Source/Sink LDO, 2.5V/0.1A, ±125mV Limits

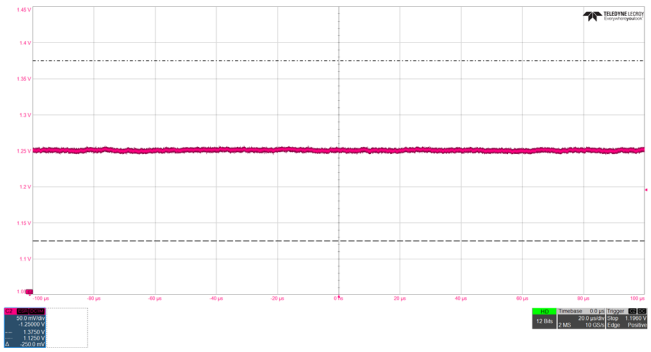


Figure 22. XCVR_VREF Output Voltage, 3A Source/Sink LDO, 1.25V

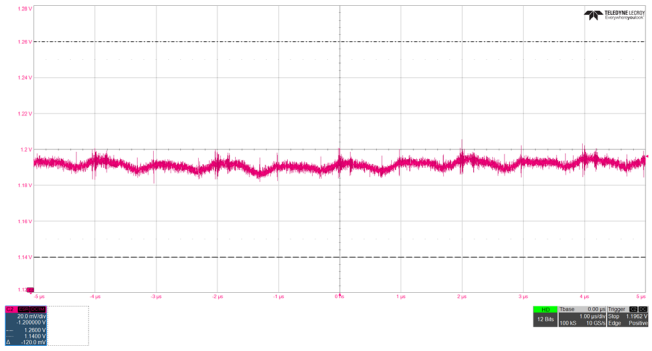


Figure 23. DDR_VDDQ Output Voltage Ripple, ISL71001, 1.2V/6A, ±60mV Limits

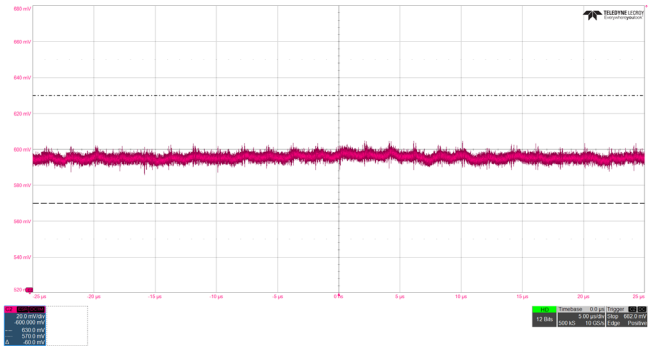


Figure 24. DDR_VTT Output Voltage, 3A Source/Sink LDO, 0.6V/3A, ±30mV Limits

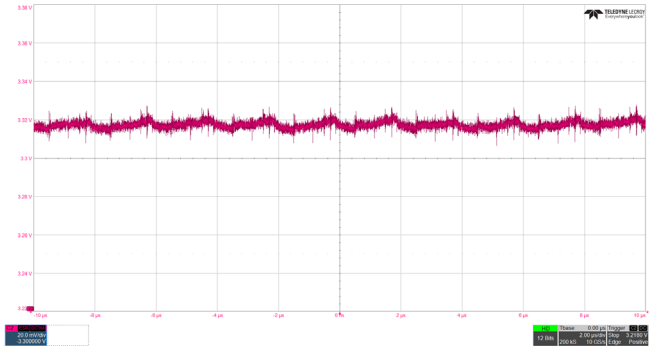


Figure 25. 3V3BUS Output Voltage Ripple, ISL73007, 3.3V/3A

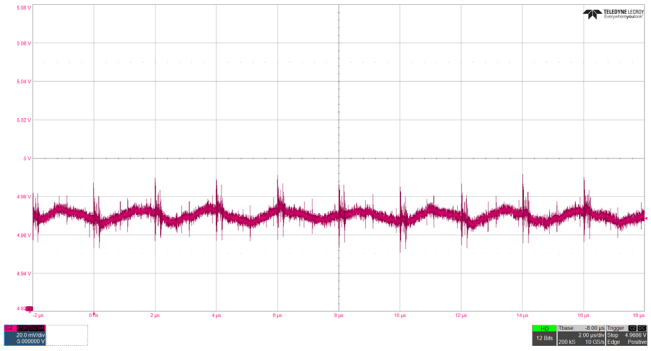


Figure 26. 5VBUS Output Voltage Ripple, ISL73007, 5V/2A

2.2 Load Transient / AC Performance

All overshoots and undershoots must be within the absolute maximum ratings provided in the RT PolarFire FPGA Datasheet. The transient current is half of the maximum current. Maximum current is taken from the Microchip Power Estimator (MPE).

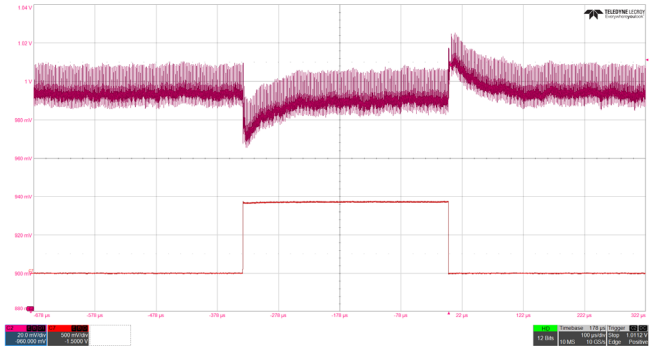


Figure 27. VDD Output Voltage, Load Transient Response, ISL73847, 1V at 25% to 75% Load Step, ±130mV Limits (C2 = VOUT, C7 = VLOAD)

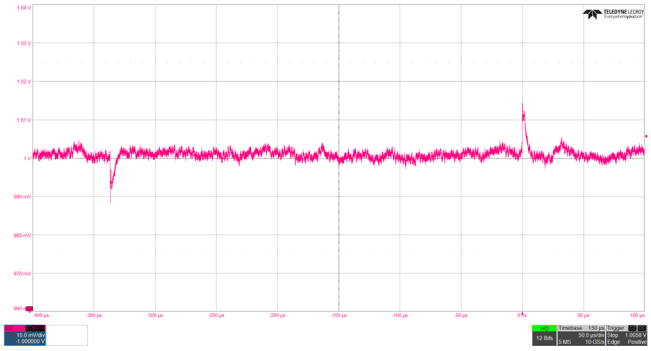


Figure 28. VDDA Output Voltage, Load Transient Response, ISL5054, 1V at 25% to 75% Load Step, ±130mV Limits

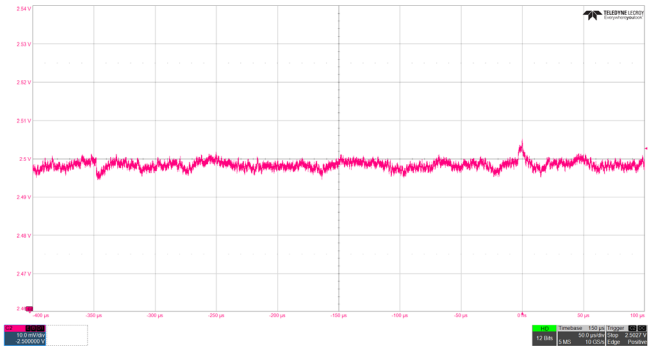


Figure 29. VDD25/VDDA25 Output Voltage, Load Transient Response, ISL75054, 2.5V at 25% to 75% Load Step, ±200mV Limits

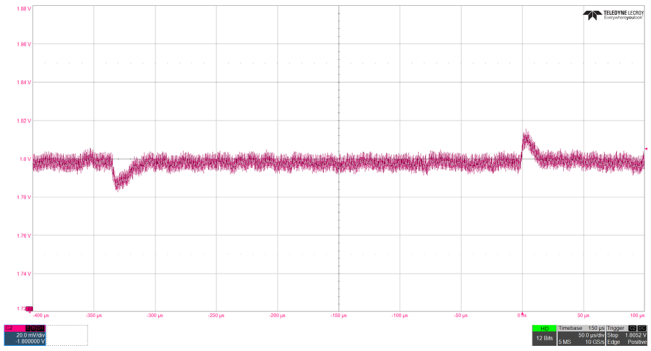


Figure 30. VDD18 Output Voltage, Load Transient Response, ISL73007, 1.8V at 25% to 75% Load Step, ±200mV Limits

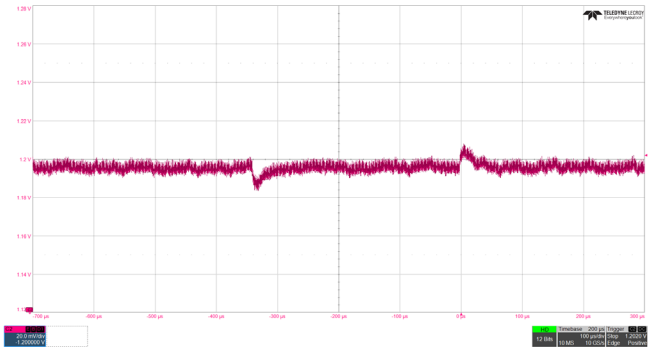


Figure 31. VDDI[0,1,6,7] Output Voltage, Load Transient Response, ISL73007, 1.2V at 25% to 75% Load Step, ±120mV Limits

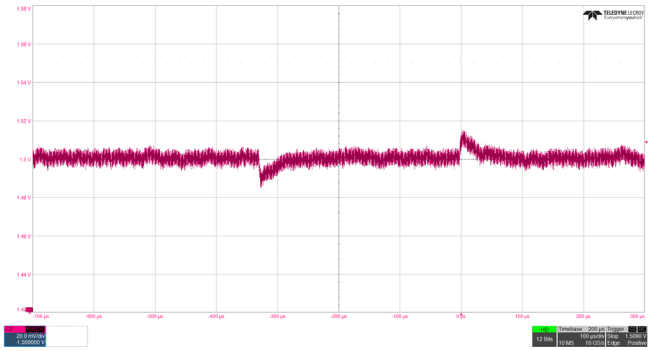


Figure 32. VDDI[2,4,5] Output Voltage, Load Transient Response, ISL73007, 1.5V at 25% to 75% Load Step, ±150mV Limits

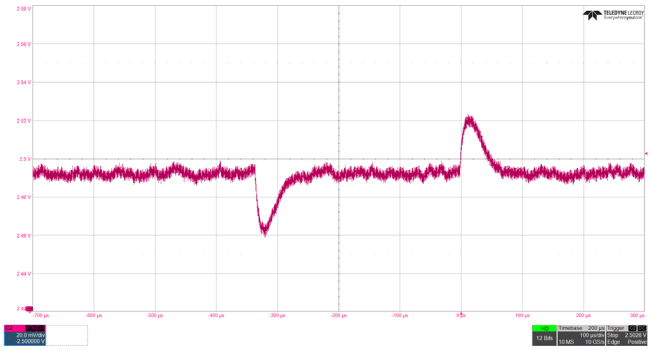


Figure 33. VDDI3 Output Voltage, Load Transient Response, ISL73007, 2.5V at 25% to 75% Load Step, ±180mV Limits

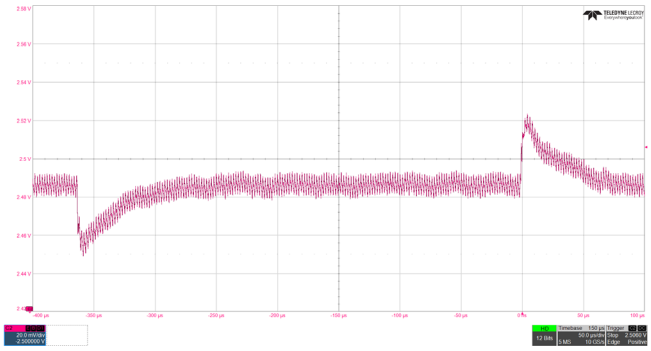


Figure 34. VDDAUX[2,4,5]/VPP/2V5BUS Output Voltage, Load Transient Response, ISL73007, 2.5V at 25% to 75% Load Step, ±200mV Limits

Figure 35. 3V3BUS Output Voltage, Load Transient Response, ISL73007, 3.3V w/ Downstream Transient Generators Enabled (VDDA, VDD25, VDD18, VDDI[0,1,6,7], VDDI[2,4,5], VDDI3)

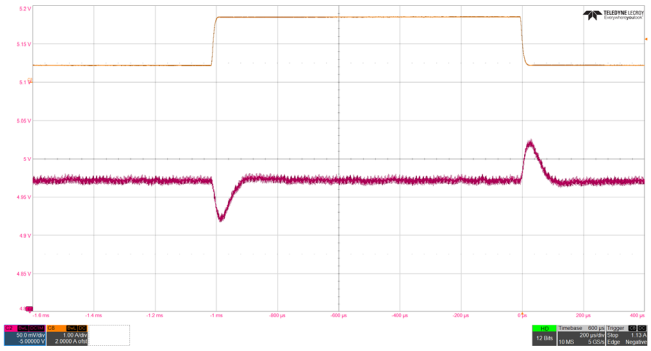


Figure 36. 5VBUS Output Voltage Ripple, Load Transient Response, ISL73007, 5V at 25% to 75% Load Step from External E-Load (C2 = V_{OUT}, C8 = I_{OUT})

2.3 Power Sequencing

As described by the Microchip RT PolarFire Datasheet, power supply ramp-up time must be between 0.2ms to 50ms. All supplies must rise and fall monotonically.

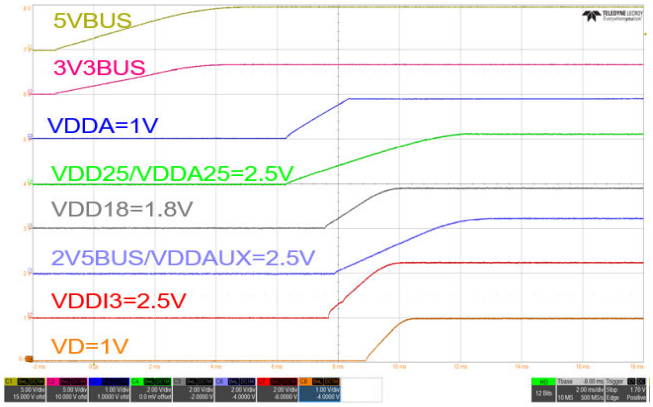


Figure 37. Startup, Rails 1-8, No Load

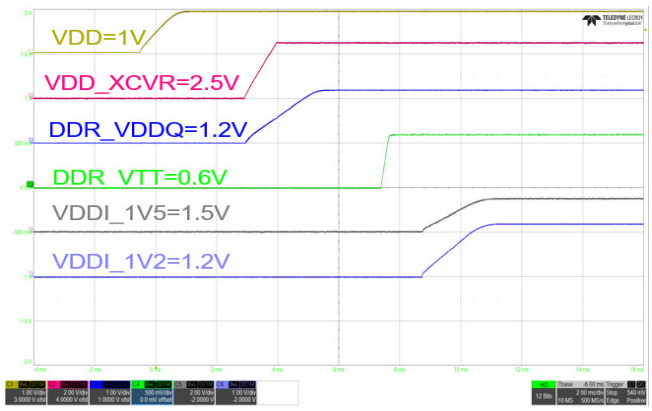


Figure 38. Startup, Rails 8-13, No Load

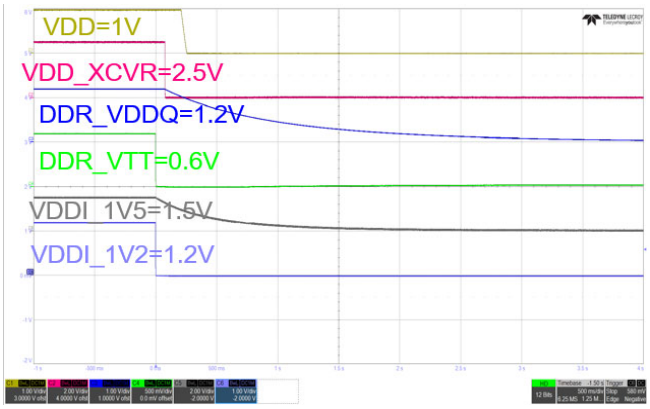


Figure 39. Shutdown, Rails 8 to 13, 50mA on VDD, VDDI_1V2

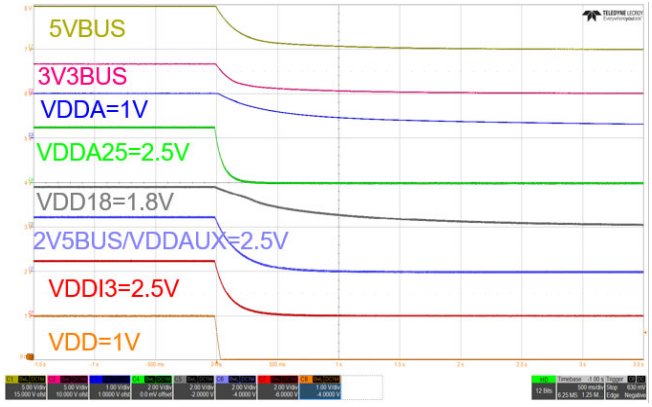


Figure 40. Shutdown, Rails 1-8, 50mA on VDD

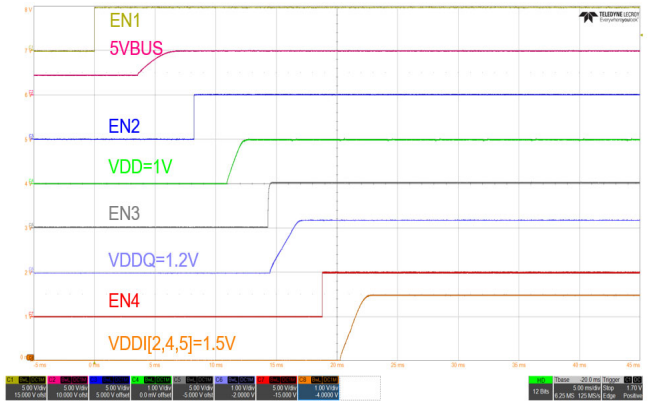


Figure 41. Sequencer Startup, No Load

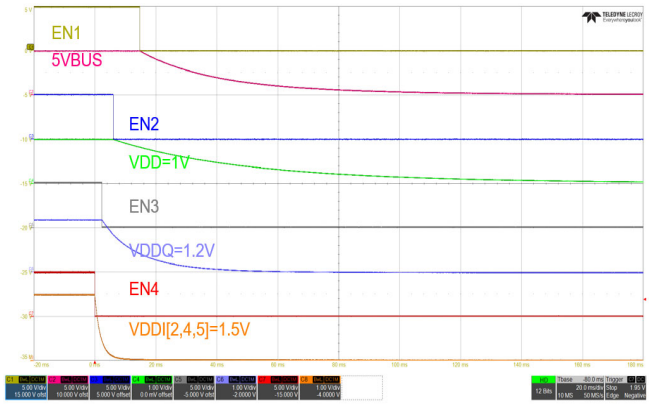


Figure 42. Sequencer Shutdown, 50mA Load (All Four Rails)

2.4 Clock Synchronization

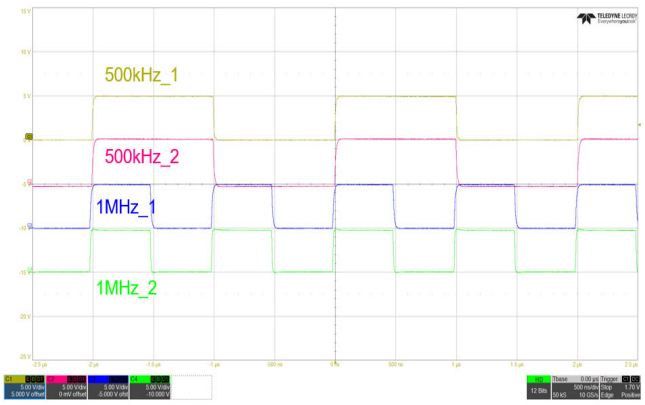


Figure 43. Quad Clock Signals, ISL74420

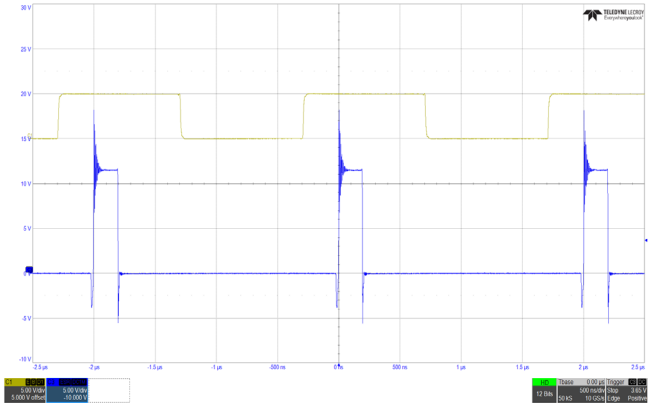


Figure 44. VDD Switching Waveform, ISL73847, 1V/25A (C1 = SYNC, C3 = LX)

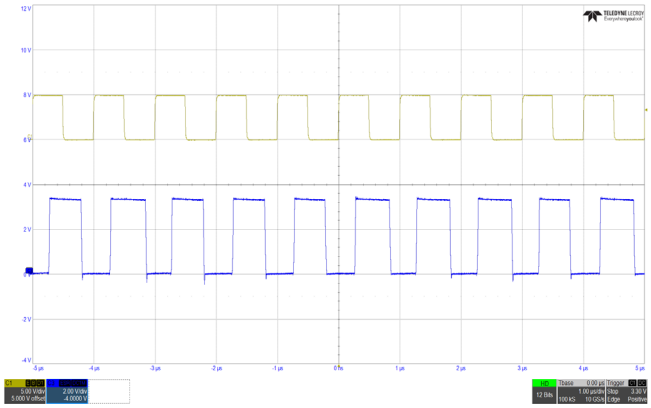


Figure 45. VDD18 Switching Waveform, ISL73007, 1.8V/0.5A, (C1 = SYNC, C3 = LX)

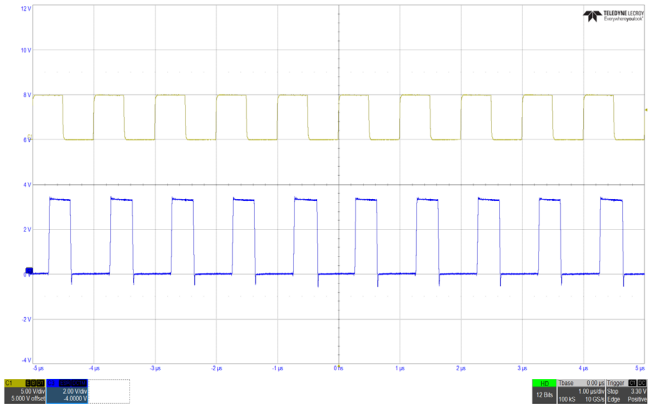


Figure 46. VDDI[0,1,6,7] Switching Waveform, ISL73007, 1.2V/0.5A, (C1 = SYNC, C3 = LX)

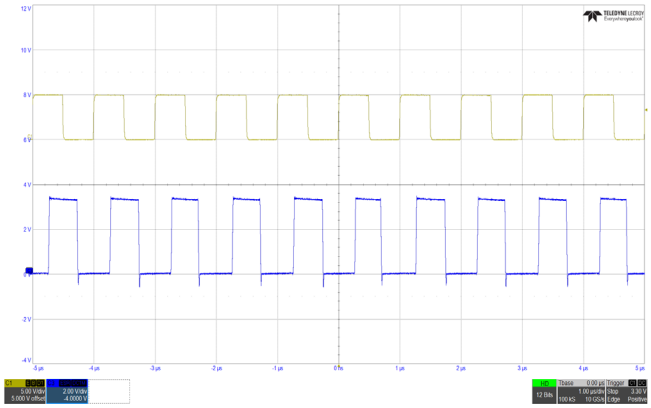


Figure 47. VDDI[2,4,5] Switching Waveform, ISL73007, 1.5V/0.5A, (C1 = SYNC, C3 = LX)

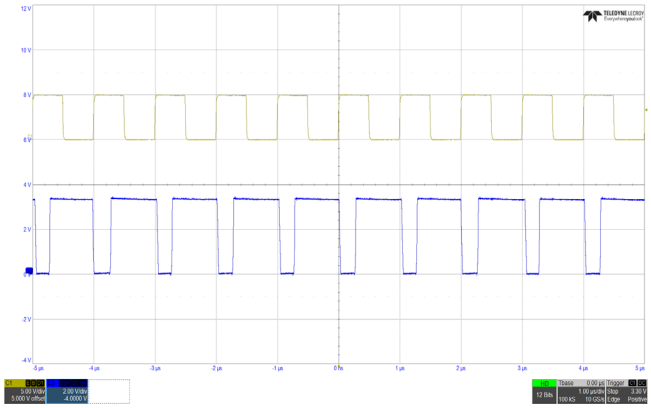


Figure 48. VDDI3 Switching Waveform, ISL73007, 2.5V/0.25A, (C1 = SYNC, C3 = LX)

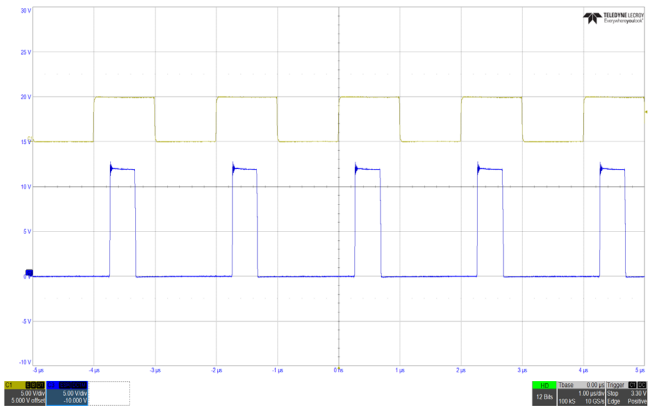


Figure 49. VDDAUX[2,4,5]/VPP/2V5BUS Switching Waveform, ISL73007, (C1 = SYNC, C3 = LX)

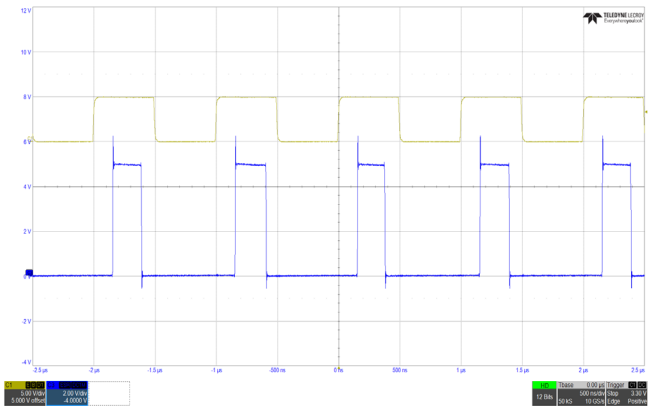


Figure 50. DDR_VDDQ Switching Waveform, ISL71001, 1.2V/6A, (C1 = SYNC, C3 = LX)

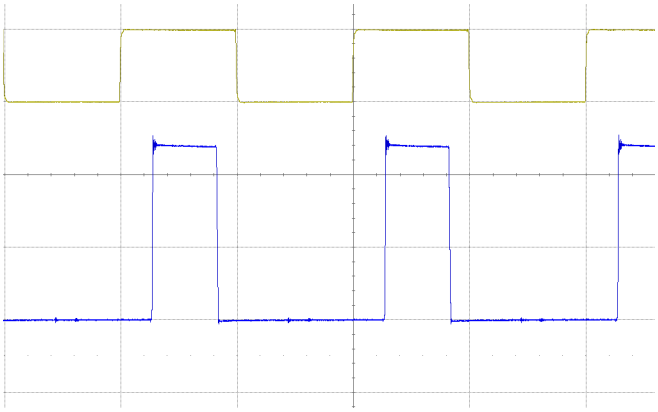


Figure 51. 3V3BUS Switching Waveform, ISL73007, 3.3V/3A, (C1 = SYNC, C3 = LX)

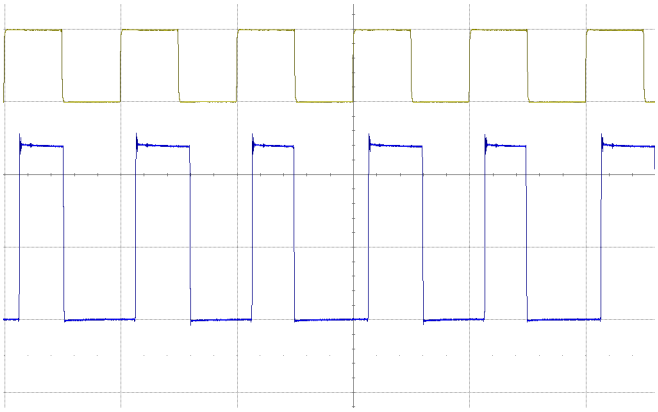


Figure 52. 5VBUS Switching Waveform, ISL73007, 5V/2A, (C1 = SYNC, C3 = LX)

2.5 Thermal Performance

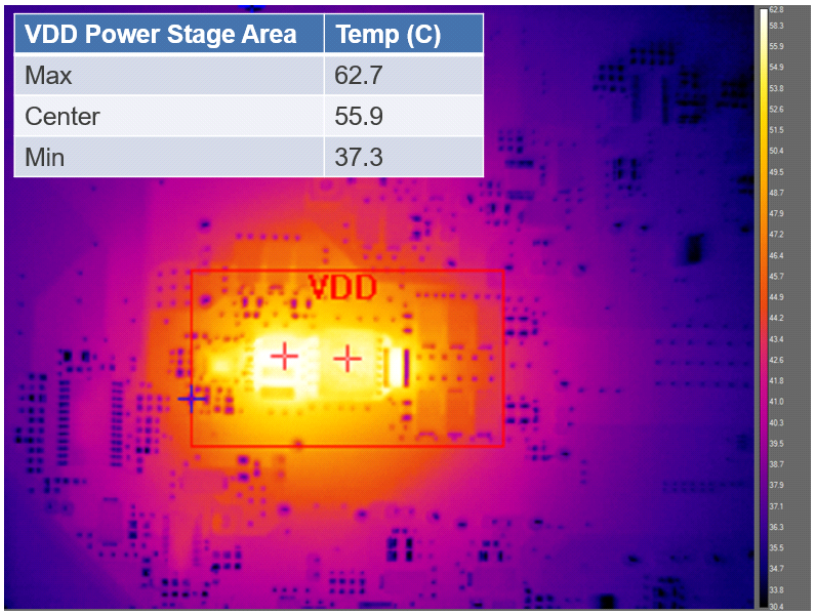


Figure 53. VDD Core Rail Thermal Image, 1V/25A, Open Air (25C Ambient)

3. Ordering Information

Part Number	Description
ISLRTPFDEMO1Z	Renesas RT Power Solution for Microchip RT PolarFire® FPGA

4. Revision History

Revision	Date	Description
1.00	Jul 10, 2025	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.