QCIOT-COMPMPOCZ

The QCIOT-COMPMPOCZ power board enables quick prototyping of both the DA9313, a 5.5V to 10.5V 10A inductor-less power converter with power efficiency up to 98%, and the ISL80103, a low voltage 6V, high-current 3A single-output LDO in a custom system design. The ISL28025, a precision digital power monitor, measures and controls the regulator output of the ISL80103 with margining.

The board provides a standard Pmod™ Type 6A (extended I^2C) connection for the on-board sensor to plug into any required MCU evaluation kit with a matching connector. The QCIOT-COMPMPOCZ features Pmod connectors on both sides of the board to allow additional Type 6/6A boards to connect in a daisy-chained solution with multiple devices on the same MCU Pmod connector.

The software support that is included with the Renesas IDE (e^2 studio) provides code generation to connect the device and the MCU so that the development time is significantly reduced. With its standard connector and software support, the QCIOT-COMPMPOCZ is ideal for the Renesas Quick-Connect IoT to rapidly create an IoT system.

Features

- 5.6 to 10.6V input supply range
- Adjustable output voltage (1.8V to 5V)
- Variable load current, up to 3A
- ΔΣADC, 16-bit native resolution
- System voltage/current monitoring
- Overvoltage/undervoltage and current fault monitoring with 500ns detection delay
- Battery power conversion with up to 98% efficiency
- Standardized type 6A Pmod connector supports I^2C extended interface
- Dual connectors allow pass-through signals for daisy-chained solutions
- Software support in e^2 studio minimizes development time with one-click code generation

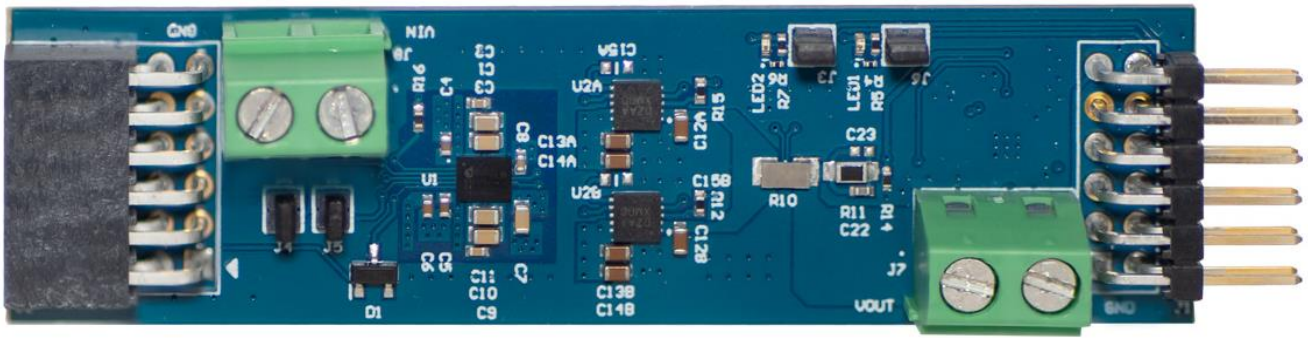

Figure 1. QCIOT-COMPMPOCZ Board

Contents

1. Functional Description

The QCIOT-COMPMPOCZ is a quick connect prototyping solution for a high-efficiency, dual-cell switching capacitor divider, linear regulator, and digital power monitoring. This board can enable the designer to quickly evaluate applications where low noise, high-current regulated solution is required for sensitive applications. The QCIOT-COMPMPOCZ takes external voltages between 5.5V to 10.5V and can deliver up to 3A to an external load. A digital power monitor can monitor both input and output voltage. It can only monitor input current, and it can report diagnostics like power efficiency, peaks, and faults.

The block diagram below highlights the main parts of the system:

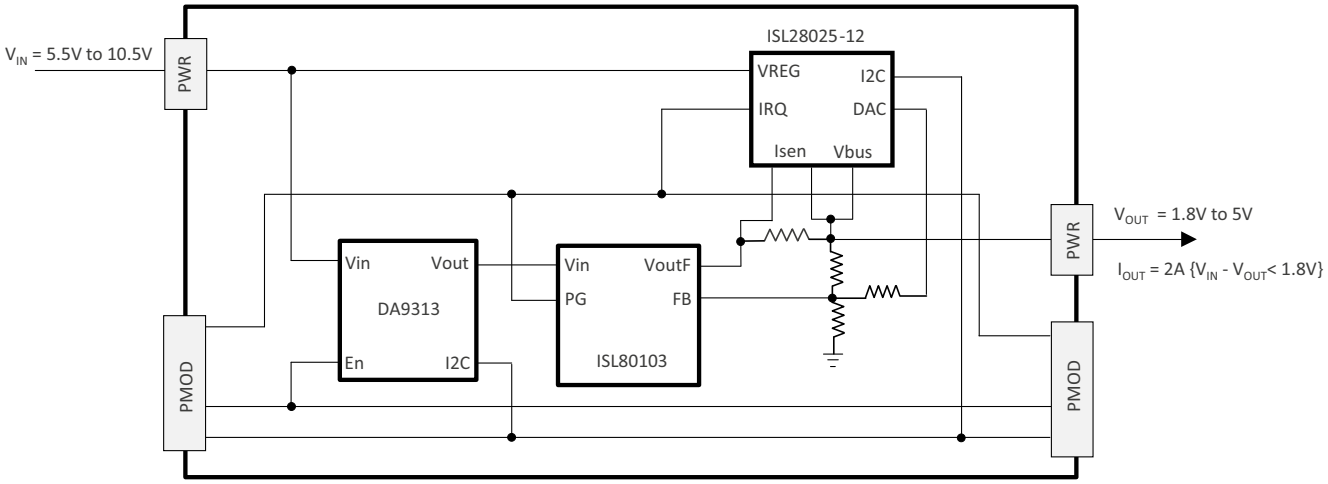

Figure 2. QCIOT-COMPMPOCZ Block Diagram

The building blocks of QCIOT-COMPMPOCZ and their functionality are as listed:

- DA9313 – High-voltage power converter with a maximum output current of 10 A, suitable for applications supplied from a dual (2S) Li-ion or Li-polymer stacked cell battery pack, or any input voltage between 5.5 V and 10.5 V. The converter operates with efficiency during conversion of up to 98 %.
- ISL80103 – Low voltage, high-current, single output LDOs specified for 2A and 3A output current, respectively. These LDOs operate from input voltages of 2.2V to 6V and can provide the output voltages of 0.8V to 5.5V.
- ISL28025 – Bidirectional high-side and low-side digital current sense and voltage monitor with a serial interface. The device monitors power supply current, voltage and provides digital results along with calculated power. The ISL28025 provides tight accuracy of 0.1% for both voltage and current monitoring.

1.1 Operational Characteristics

The QCIOT-COMPMPOCZ can be used as a starting point for providing low noise, high current regulated solution for sensitive applications like battery power banks, DSLR cameras, notebooks, tablets etc.

The board has been designed to the following specifications:

- Input voltage range = 5.5V – 10.5V
- Output voltage range = 1.8V - 5V
- Output current = 0A - 3A
- Battery power conversion efficiency up to 98%

While the DA9313 is capable of outputting high current of up to 10A, the range is constrained to be up to 3A since LDO is specified for 3A output current. The minimum output voltage is 1.8V and is set by the internal reference voltage of the ISL80103. While the LDO can provide output voltages of 0.8V, it has a very less dropout out voltage (120mV at 3A) and the minimum input voltage to the LDO is 2.8V, which is coming from the output of the DA9313.

(EQ. 1) $$VOUTmax = \frac{0.5}{[R14]} \times R11 + 0.5$$

The output range is set by resistors R14 and R11 on the board, which forms a resistor divider in a feedback loop between the output voltage and reference voltage. Users who wish to change the output range can change the values of these resistors, but also must consider the values for the output filter components. Renesas provides a spreadsheet to help calculate these parameters.

1.1.1 Adjusting Output

While the output voltage range is set by resistors R14 and R11, the output voltage can be changed within the range by adjusting the voltage applied across R13. This can be done using the voltage margining feature of the IS28025, where the user can program the margin DAC output voltage using I^2C.

The ISL80103 output voltage is in a feedback loop with its FB pin, which is compared to a reference voltage of 0.5V. The feedback loop attempts to make the FB pin match 0.5V, therefore, the current across R14 equals 0.5V divided by R14.

Applying a voltage across R11 and injecting a current into the node results in lowering the output voltage required to maintain 0.5V at the FB pin. The output voltage change is in proportion to R11 and R13.

(EQ. 2) $$VOUT = \left(\frac{0.5}{R14} - \frac{(VDAC - 0.5)}{R13}\right) \times R11 + 0.5$$

1.1.2 Fault Monitoring

The QCIOT-COMPMPOCZ features fault monitoring circuitry to detect when power exceeds thresholds. The digital power monitor ISL28025 can set thresholds for overvoltage, undervoltage, and overcurrent. In addition, ISL80103 provides a power-good signal that communicates whether the regulator is operating normally. The following signals are available for fault monitoring:

- SMBALERT1
- SMBALERT2
- Power Good

1.1.2.1 SMBALERT1

The SMBALERT1 pin on the ISL28025 is an open-drain pin that requires an external pull up. During normal operation, SMBALERT1 is pulled high to 3.3V using R7 if jumper J3 is in place. The user can set overvoltage, undervoltage, and overcurrent levels that would trigger SMBALERT1 to pull down. SMBALERT1 signals the host MCU on any threshold cross event through pin 7 of the Pmod interface. In addition, LED2 on the board turns on. When the user is ready, SMBALERT1 can be reset through clearing the fault status registers.

1.1.2.2 SMBALERT2

The SMBALERT2 pin of ISL28025 is a push-pull output that is high on normal operation, and low after threshold cross detection. This pin is triggered by the same overvoltage, undervoltage, and overcurrent levels that trigger SMBALERT1. SMBALERT2 is connected to the enable pin of ISL80103, and it is used as a failsafe shutoff to the power regulator. This pin is not connected to the host MCU.

1.1.2.3 Power Good

ISL80103 provides a power-good (PG) pin to signal normal operation. This is an open-drain NMOS that is pulled up by R5 if jumper J6 is in place. The PG pin should not be pulled up to a voltage source greater than VIN. PG faults can be caused by the output voltage going below 84% of the nominal output voltage, or the current limit fault, or low input voltage. PG does not function during thermal shutdown. PG signals the host MCU using Pin 10 of the Pmod interface, and it turns on LED1(RED) when pulled down during fault.

1.2 Setup and Configuration

The following additional lab equipment is required for using the board (sold separately):

- FPB-RA2E1

1.2.1 Software Installation and Usage

Visit the Renesas website for the latest version of the e^2 studio installer. Renesas recommends version 2024 or later. The minimum FSP version supporting the QCIOT-COMPMPOCZ is FSP 5.1.0. For the latest sensor support, ensure that the latest release is used.

Visit the Renesas Quick-Connect IoT site for more information about creating your customized system solution.

1.2.2 Kit Hardware Connections

Follow these procedures to set up the kit (see Figure 3).

1. Ensure that the MCU evaluation kit in use has a Pmod connector set to Type 6A (refer to the kit hardware manual for details). Renesas recommends using FPB-RA2E1.
   a. If no Type 6A Pmod is available, ensure that the MCU evaluation kit can use the US082-INTERPEVZ interposer board. Insert the board into the MCU connector before adding any sensor boards.
2. Plug in the QCIOT-COMPMPOCZ to the Type 6A connector. Be careful to align Pin 1 on the sensor board and MCU kit.
3. Connect the J3 and J6 jumpers to place the 4.7k pull-up resistors on the IRQ and PG bus lines, respectively. Also, if needed, connect J4 and J5 to place 4.7k pull-up resistors on I^{2}C if the MCU does not have internal pull-up. RA2E1 has no internal pull-ups.
   a. Only one set of I^{2}C pull-up resistors should be used on the bus. If multiple Pmod connected boards are used, only one board should have the jumpers present.
   b. If multiple modules use the IRQ# line on the PMOD, only one pull-up jumper should be present.
   c. MCU kits typically do not have pull-up resistors present on the bus lines but ensure to check for them.
4. Connect power source to VIN and GND of screw terminal connector J8, and load to VOUT and GND of J7 using wires or terminal pins. If using wires, ensure the wire gauge is of sufficient thickness to carry the operating current load. Apply VIN between 5.5V to 10.5V.

5. The device is now ready to be used in the system. Follow the MCU kit instructions for connecting and powering up the evaluation kit.

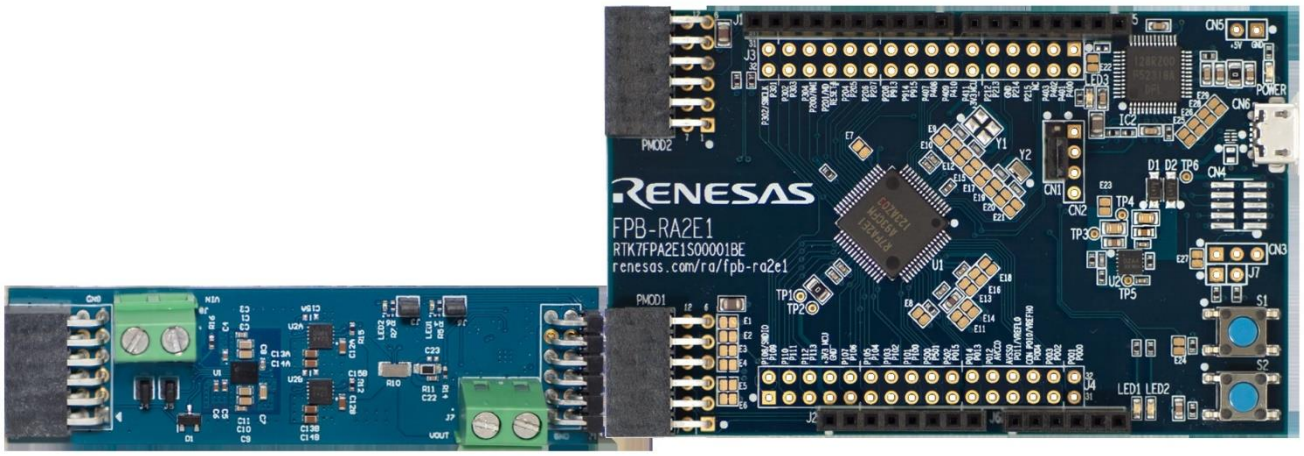

Figure 3. QCIOT-COMPMPOCZ with FPB-RA2E1 MCU Kit

1.2.3 I²C Address Select

The QCIOT-COMPMPOCZ has a default I²C address of 1011 111 for binary, 0x5F for the 7-bit address, or 0xBE/F for the 8-bit address. If this conflicts with another device on the I²C line, the user can change the I²C address by removing the 0Ω resistor R3 on the board. To change the address, connect A2 to GND or SDA. A1 and A0 are connected to SCL, so changing A2 gives an option for three I²C addresses.

For details on I²C addresses, see the I²C Slave Addresses table in the *ISL28025 Datasheet*.

2. Board Design

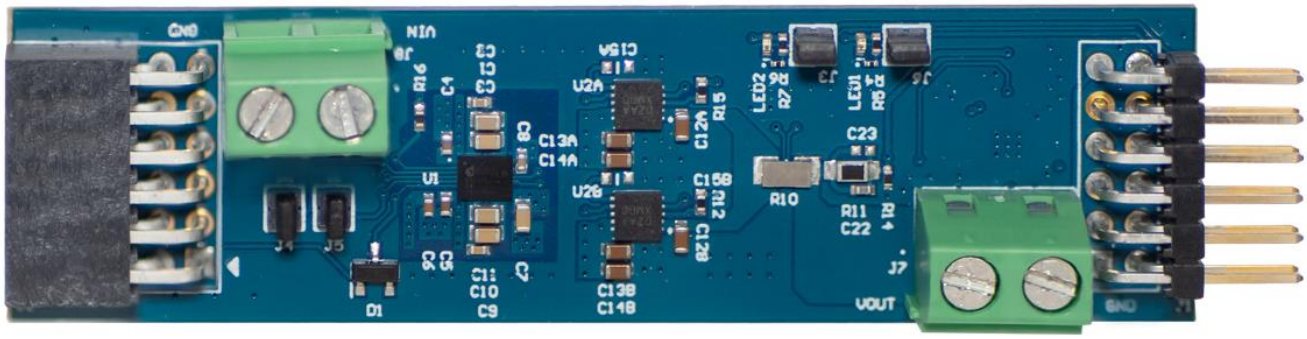

Figure 4. QCIOT-COMPMPOCZ Evaluation Board (Top)

Figure 5. QCIOT-COMPMPOCZ Evaluation Board (Bottom)

2.1 Schematic Diagrams

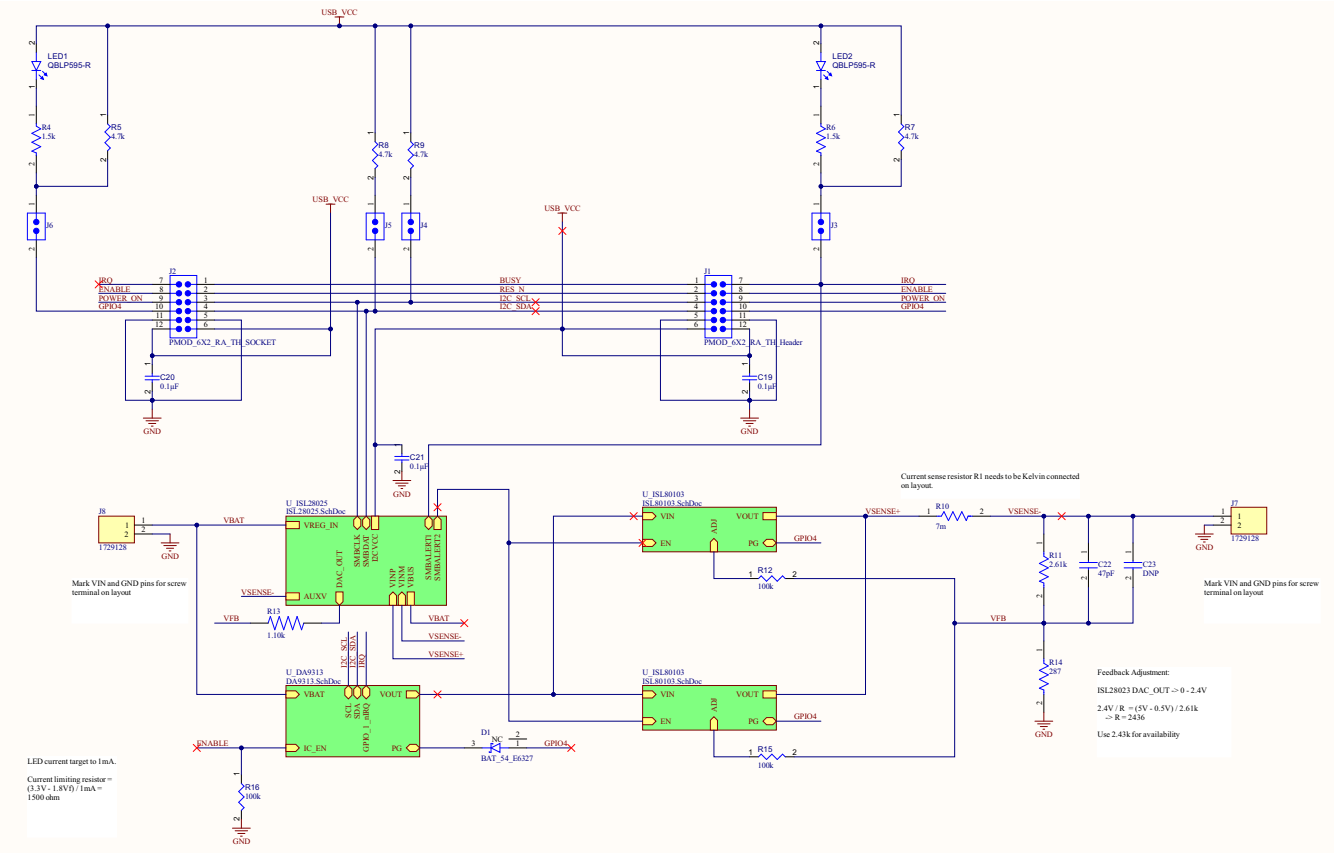

Figure 6. QCIOT-COMPMPOCZ Schematic

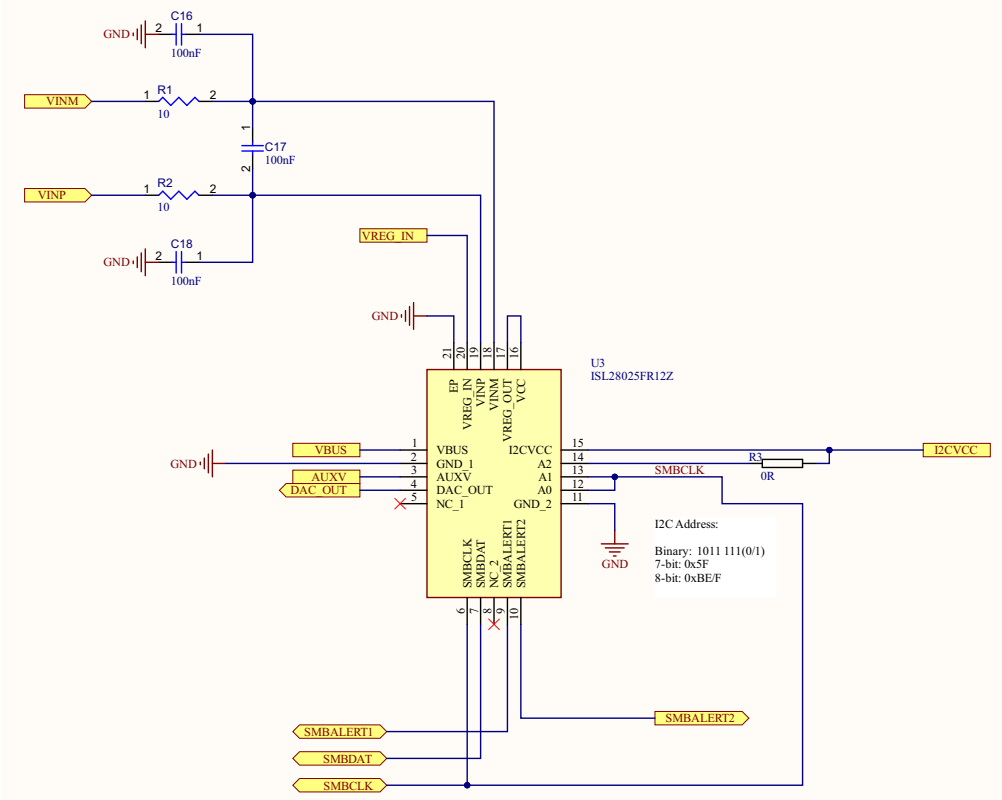

Figure 7. ISL28025 Digital Power Monitor Schematic

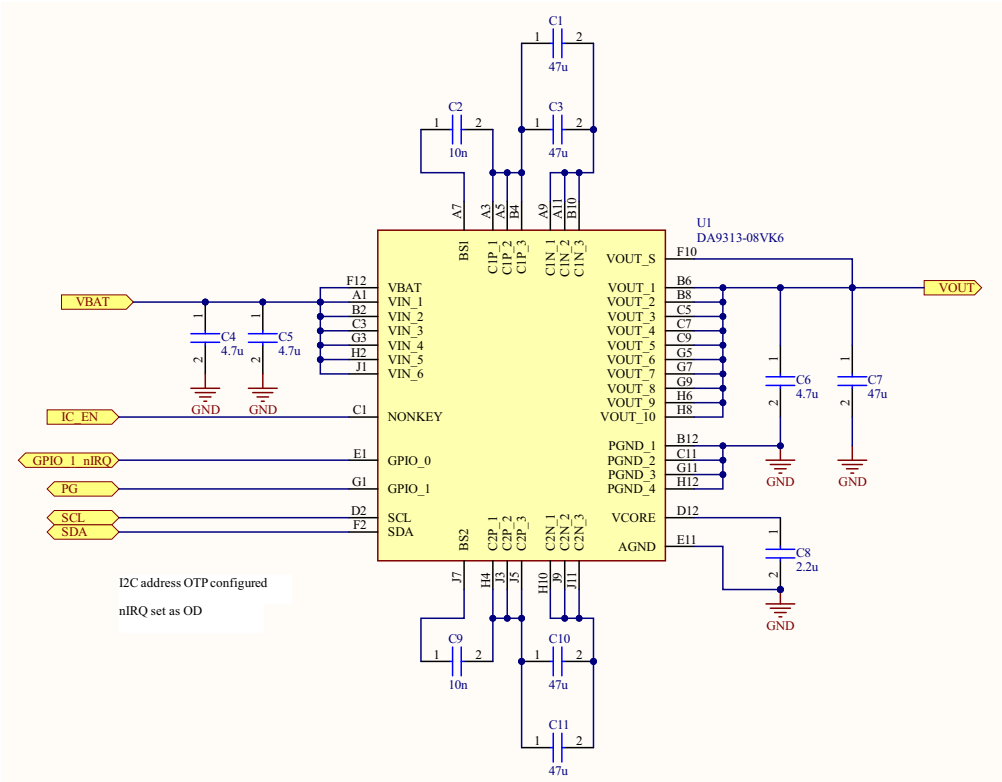

Figure 8. DA9313 Dual Switch Capacitor Schematic

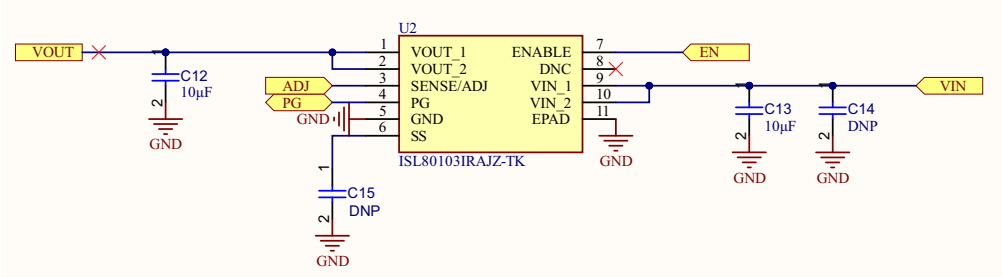

Figure 9. ISL80103 LDO Schematic

2.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
5	C1, C3, C7, C10, C11	0603 6.3V 47µF ±20% Tolerance X5R SMT Multilayer Ceramic Chp Capacitor	Murata	GRM188R60J476ME15D
2	C2, C9	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0.01µF 16 VDC 10% 0402 X7R	Murata	GRM155R71C103KA01D
2	C4, C5	Chip Monolithic Ceramic Capacitor, X5R, 4.7µF, 16V, ±20%, 0402	Murata Electronics	GRM155R61C475ME15
1	C6	Multilayer Ceramic Capacitors MLCC - SMD/SMT 4.7µF 10 VDC 20% 0402 X5R	Murata	GRM155R61A475MEAAD
1	C8	Cap Ceramic 2.2µF 6.3V X5R 20% Pad SMD 0402 85C T/R	Murata	GRM155R60J225ME95D
4	C12A, C12B, C13A, C13B	Chip Capacitor, 10µF ±20%, 10V, 0603, Thickness 1mm	TDK	C1608X5R1A106K080AC
2	C14A, C14B	Chip Capacitor, 10µF ±20%, 10V, 0603, Thickness 1mm	Samsung	CL10A106KP8NNNC
2	C15A, C15B	0.1 µF ±10% 10V Ceramic Capacitor X7R 0603 (1608 Metric)	Vishay Vitramon	VJ0603Y104MXQCW1BC
3	C16, C17, C18	Chip Capacitor, 0.1µF, ±5%, 16 V, 0402 (1005 Metric)	KEMET	C0402C104J4RACTU
3	C19, C20, C21	Multilayer Ceramic Capacitor, 0.1µF, 10V, ±10%, X7R, 0603 [1608 Metric]	Kyocera AVX	0603ZC104KAT2A
1	C22	Multilayer Ceramic Capacitors MLCC - SMD/SMT 16V 47pF X7R 0402 10%	Kyocera AVX	0402YC470KAT2A
1	D1	DIODE SCHOTT 30V 200MA SOT323-3	Infineon	BAT54E6327HTSA1
1	J1	Male Header 0.1" pitch PMOD 2x6 Right Angle, through hole	Wurth Electronics	61301221021
1	J2	Female socket 0.1" pitch PMOD 2x6 Right Angle, through hole	Wurth Electronics	613012243121
4	J3, J4, J5, J6	CONN HEADER VERT 2POS 1.27 MM	Samtec	FTS-102-01-L-S
2	J7, J8	Conn PC Terminal Block 2 POS 5.08mm Solder ST Thru-Hole 17.5A Cardboard	Phoenix Contact	1729128
4	JMP3, JMP4, JMP5, JMP6	2 C, Closed Top, 050" CC; No Mounting, 105°C, Nylon 66; Phos Bronze, Gold Flash	Sullins	NPB02SVFN-RC

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
2	LED1, LED2	Chip LED 0402, Red, 0.02A, 2.0 to 2.5V, -40 to 80°C, 2-Pin SMD, RoHS, Tape and Reel	QT-Brightek	QBLP595-R
2	R1, R2	Chip Resistor, 10Ω, ±1%, 63mW, -55 to 155°C, 0402	Panasonic	ERJ-2RKF10R0X
1	R3	Chip Resistor, 0Ω, 0.063W, -55 to 155°C, 0402 (1005 Metric)	Yageo	RC0402JR-070RL
2	R4, R6	Res Thin Film 0201 1.5KΩ 0.1% 0.05W(1/20W) ±25ppm/°C Pad SMD T/R	Panasonic	ERA-1AEB152C
4	R5, R7, R8, R9	Chip Resistor, 4, 7kΩ, ±1%, 63mW, -55 to 155°C, 0402	Panasonic	ERJ-2RKF4701X
1	R10	0.007Ω, Metal Strip, Current Sensing Resistor, 1%, 2 Termination, 1206, Taped & Reeled, 1W, ±50 ppm/°C, Solder, Height 024 in [0.6mm], CGS TLR	TE Connectivity	2176117-8

2.3 Board Layout

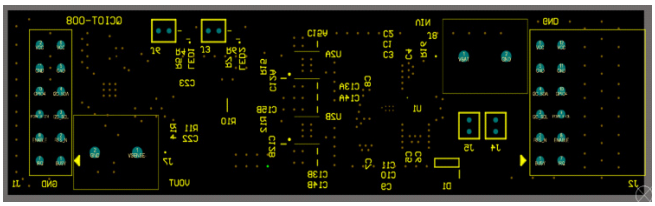

Figure 10. Top Overlay

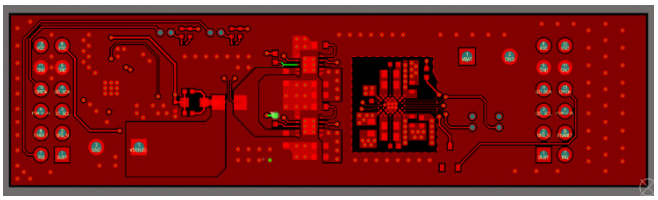

Figure 11. Top Layer

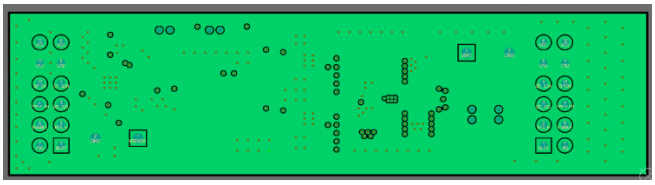

Figure 12. Layer 2 (GND)

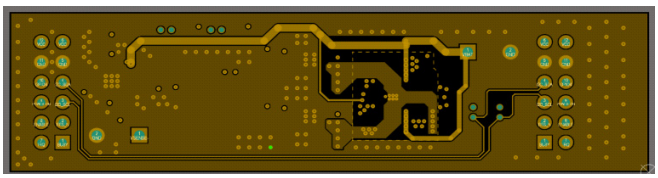

Figure 13. Layer 3 (Signal)

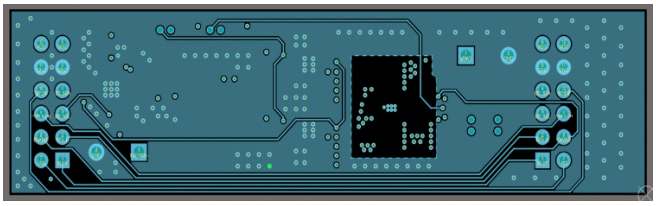

Figure 14. Layer 4 (Signal)

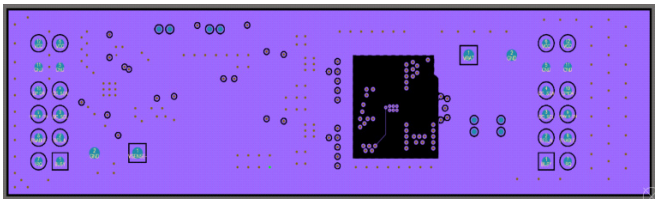

Figure 15. Layer 5 (GND)

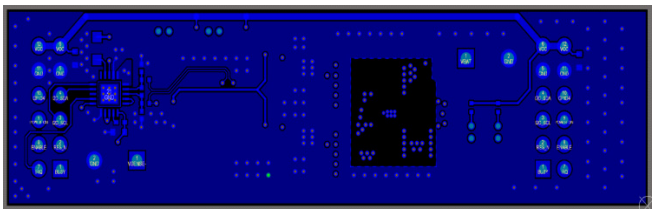

Figure 16. Bottom Layer

Figure 17. Bottom Overlay

3. Typical Performance Graphs

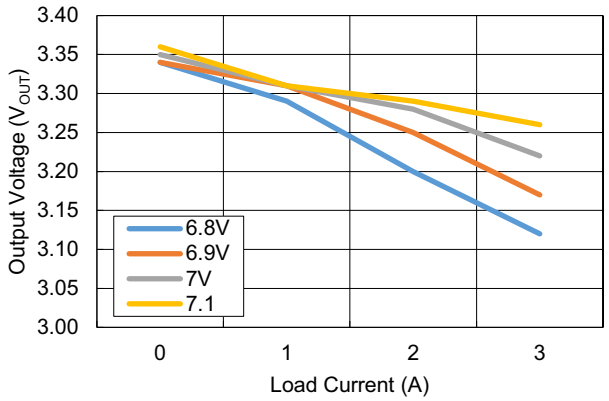

Figure 18. Line Regulation

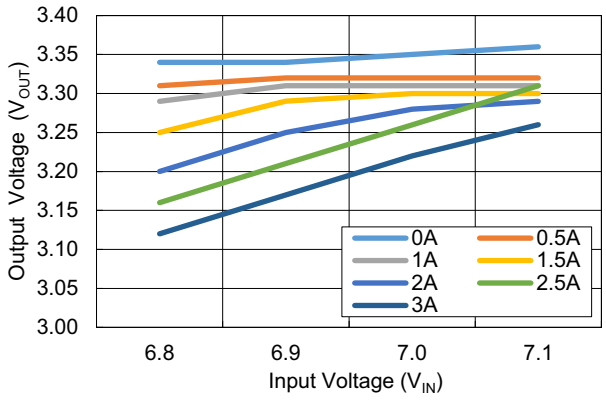

Figure 19. Load Regulation

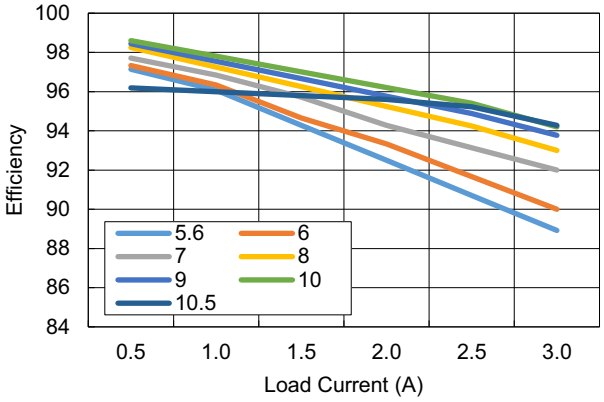

Figure 20. Efficiency of DA9313

4. Software Design

The following sections give an overview of the software implementation for the QCIOT-COMPMPOCZ, which is based on the Renesas RA Family's Flexible Software Package (FSP). These sections detail the code structure of the project, the system software modules, and the main system flow. Information such as the software API, pin functions, and fault handling is also provided.

4.1 Project Code Structure

The Quick Connect DPM project is a highly modular solution, where each device has an associated module folder that can be easily configured independently of other modules (if required) or ported to other end applications.

The project is split into three main modules:

- ISL28025 driver – Device driver code for power monitoring that includes the I^2C communications driver.
- Application code – Main system code that enables the driver code and implements system flow.

The driver module contains the C source files and header files. The specific user configurations are included in the application code. Refer to User Settings for details regarding user configurations.

Figure 21 shows the structure of the project in e2 studio.

ra – automatically generated files for FSP drivers
ra_gen – includes main file and generated files for FSP driver settings
src – ISL28025 driver source code, Header file and Application code that is used 28025 driver
rm_isl28025.h – ISL28025 driver header file
rm_isl28025.c – ISL28025 driver source file
rm_isl28025_api.h – ISL28025 API header file
rm_isl28025_ra_driver.c – software delay function
ra_isl28025.c – digital power monitor source file
hal_entry.c – start of code execution, which calls system main

Figure 21. Compact PM Code Structure

Figure 22 shows the general code structure in terms of its dependencies. Execution begins in hal_entry.c which calls the start_isl28025_demo function in ra_isl28025.c. Next, this function begins the main system flow that uses the rm_isl28025 module to execute the project. All associated header files reference the lower-level Flexible Software Package (FSP) drivers.

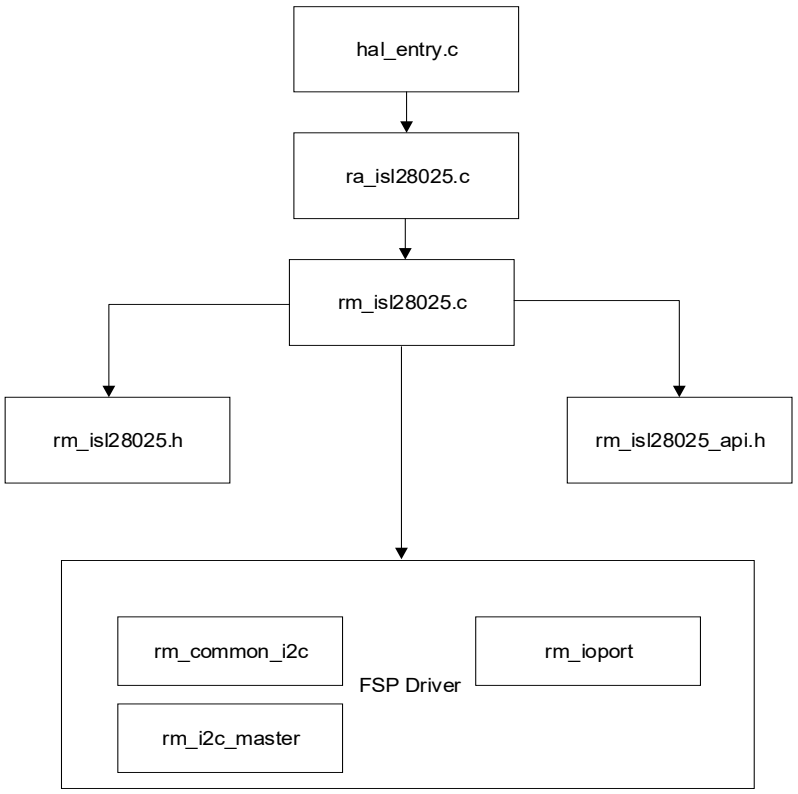

Figure 22. Code Dependency Graph

4.2 Software Module Overview

The ra_isl28025 module contains the main system algorithm that is described in the main system flow. This module is responsible for initializing and setting up the driver that is used in the main algorithm. Also, this module makes calls to the other modules to initialize and setup. After initialization, this module is responsible for monitoring the system, displaying faults (if any), and shutting down the system in the event of faults. This module also keeps a continuous check of the I^2C connection. The algorithm is responsible for initializing and setting up the DPM module and adjusting DAC to the required output.

4.2.1 DPM - ISL28025 (Digital Power Monitor)

The ISL28025 driver is a device driver that can monitor the current and voltage in the system for added protection.

This module is responsible for initializing the FSP I^2C driver and setting up the DPM device with the user-configured settings.

After setup, the module provides the following features:

- Performing various device commands (clear faults, reset, and others)
- Reading the bus voltage and shunt voltage
- Reading the system for the primary side current, power, primary and auxiliary side voltage
- Reading device faults (overvoltage, undervoltage, overcurrent, and others)
- Reading from and writing to all device registers
- Adjusting the DAC according to the voltage set by the user

4.2.2 Algorithm Flowchart

4.2.2.1 hal_entry()

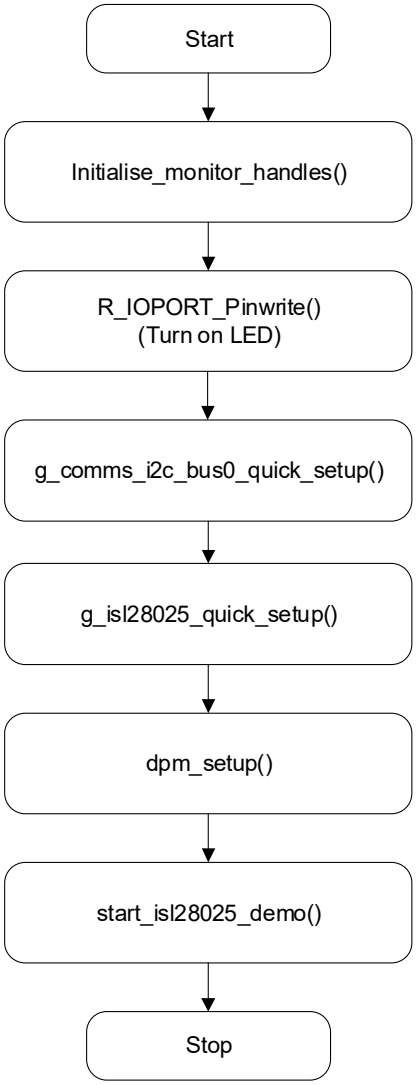

Figure 23. Algorithm Flowchart at a High Level

The I^2C bus is opened by g_comms_i2c_bus0_quick_setup(). Next, the ISL28025 instance is opened by g_isl28022_quick_setup(). If the device is opened successfully, LED1 and LED2 turn on.

The dpm_setup() function does a soft reset and configures the ISL28025 DPM registers.

The main program runs once to get the DPM readings by isl28025_update_reading() function calls. The Vbus, Vshunt, Current, power, Temperature, Vaux, Peak Max Current, and Peak Min Current are displayed in the Renesas Debug Virtual Console if in debug mode.

4.2.2.2 start_isl28025_demo()

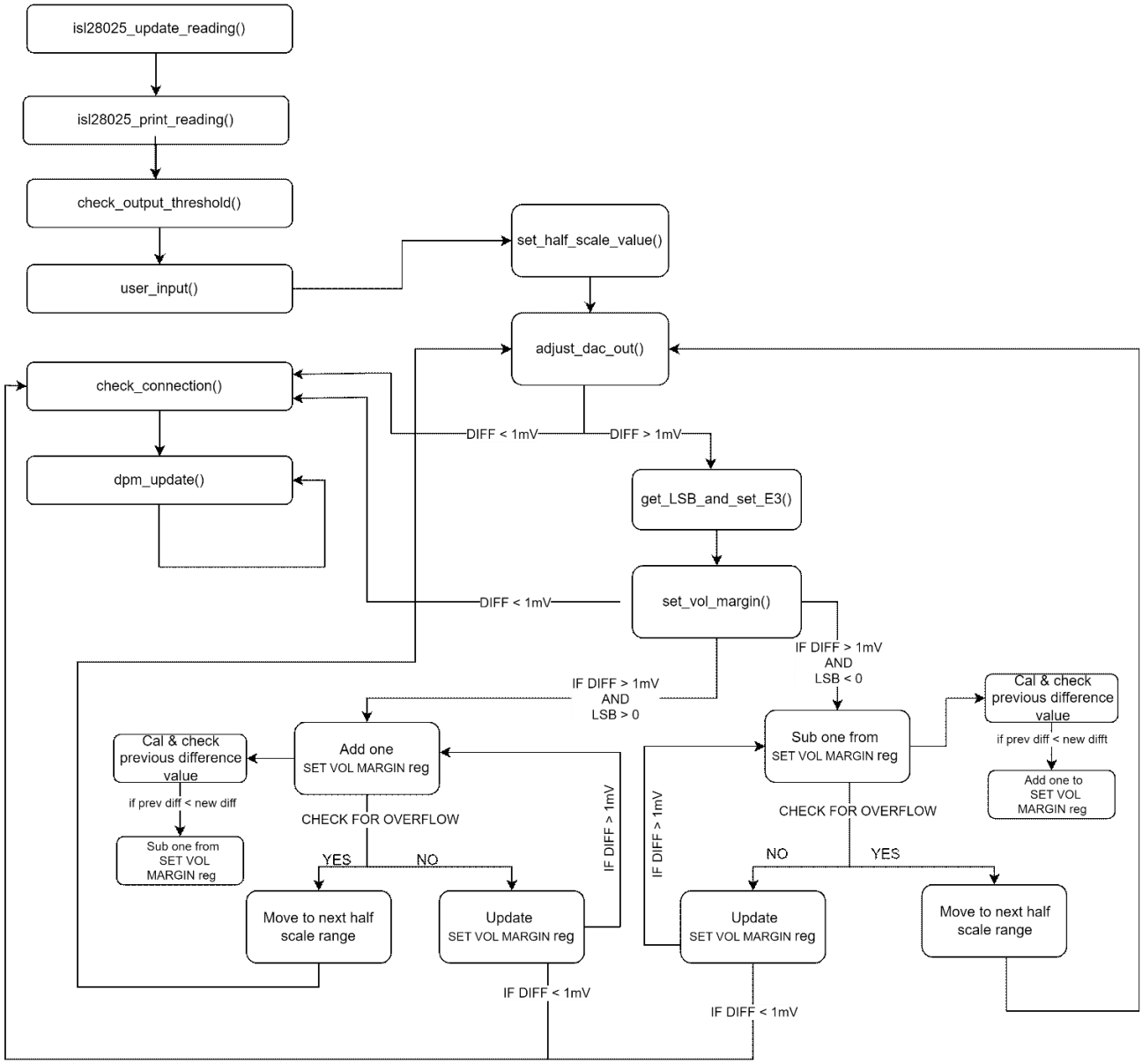

Figure 24. Algorithm Flowchart

The functions outlined in Figure 24 are described as follows:

start_isl28025_demo()

- Calls isl28025_update_reading() function
- Calls isl28025_print_reading() function
- Calls check_output_threshold() function
- Calls set_reg_vol_to() function
- Calls check_connection() function
- Calls dpm_update() function
- lsl28025_update_reading()

- Read Vbus, Vshunt, Current, Power, Vaux, Temperature, Peak Max/Min Current and gets the status of the Vout Register for setting up the Input Threshold detection

Isl28025_print_reading()

- Prints Vbus, Vshunt, Current, Power, Vaux, Temperature, Peak Max/Min Current of ISL28025 on the Rensas Debug Virtual Consol

check_output_threshold()

- Check for system faults on the output side

set_reg_vol_to()

- Calls dpm_set_dac_out() function

Check_connection()

- Continuously check for I^2C connection

dpm_update()

- Update the DPM
- Take updated DPM reading

dpm_set_dac_out()

- Calls the dpm_set_half_scale_value() function
  - Calls the dpm_cal_Vdac() function to calculate Vdac
  - Depending on the Vdac value the half scale range is set
  - Voltage margin is set and configure accordingly
- Calls the adjust_dac_out() function
  - Calculates the diff = VOL_REG_USER - g_dpm.vout_aux
  - If diff is greater than 1mV, get_LSB_and_set_SET_VOL_MARGIN_E3_reg () function is called.

get _LSB_and_SET_VOL_MARGIN_E3_reg ()

- Calculates the Delta value
- Calculates the no of LSB required
- Reconfigure voltage margin registers
- If diff > 0 and no of LSB > 0, add 1 to the SET_VOL_MARGIN register else subtract 1 from SET_VOL_MARGIN register

add_one_to_SET_VOL_MARGIN_E3_reg ()

- Check for overflow
- If no overflow, add one to the SET_VOL_MARGIN register
- Reconfigure voltage margin registers
- If overflow detected, move to next half scale range

set_vol_margin()

- Clear the load bit
- Set the voltage margin register with the updated value
- Set the load bit

sub_one_from_SET_VOL_MARGIN_E3_reg

- Check for overflow.
- If no overflow, subtract one from SET_VOL_MARGIN register.
- Reconfigure voltage margin registers.
- If overflow detected, move to next half scale range.

4.2.3 Hierarchy Chart

Figure 25 outlines the hierarchy of function calls.

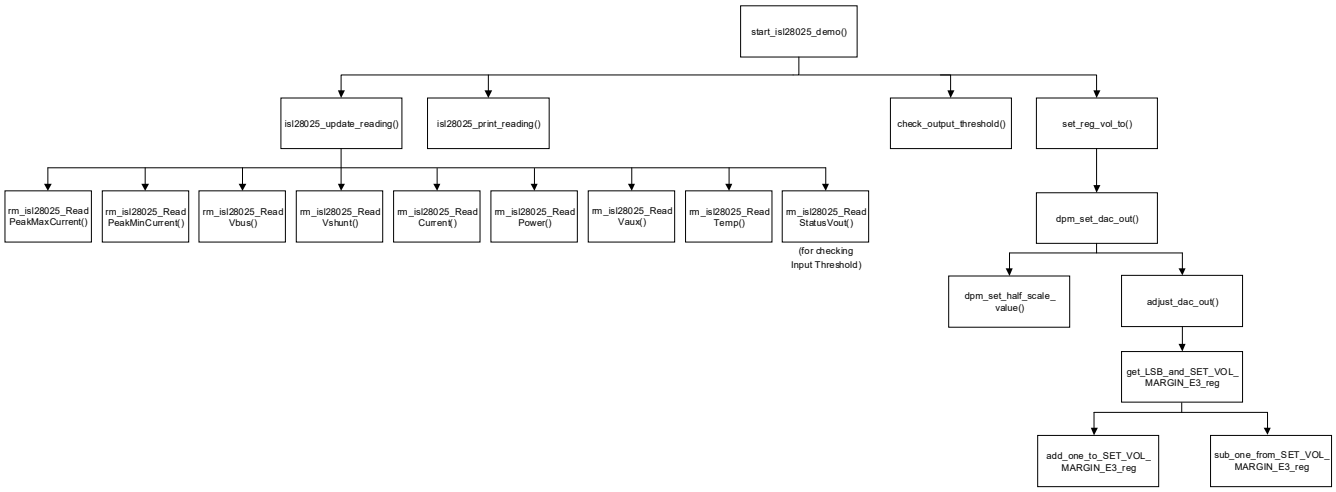

Figure 25. Function Call Hierarchy

4.3 User Settings

4.3.1 Configure DPM

This section outlines all the configurable user settings in the demo project. Configurable settings are included mainly in the Profile header files for the DPM. These configurations are defined macros with the _USER suffix. The list of user-configurable settings for the DPM device is not exhaustive. The most common settings are included in the Profile headers, but all register settings in the DPM setup functions can be adjusted directly. Refer to the datasheet for guidance on register settings and values. *Note*: An E2 emulator is required to make changes to the project. The user settings are detailed in Table 1. The user can adjust these values to fit the end application. *Note*: Some register settings adhere to multiple settings, and those settings are not fully listed. Refer to the datasheet for more information.

Table 1. Register Settings

Name	Usage	Default Value
RSHUNT_USER	Primary shunt resistance value in ohms	0.007
DPM_MODE_USER	Selects options for which elements to scan (voltage, current, temperature)	0x000F(All)
IOUT_CAL_USER	Current gain calibration value	0x0831
OC_THRESHOLD_USER	The OC threshold value in amperes	3A
IOUT_DIR_USER	Direction of current flow (1 is negative to positive)	0
VSHUNT_RNG_USER	Primary shunt full-scale range (0 is 80mV)	0
OV_THRESHOLD_USER	OV threshold for the 12V supply to the system	10.6V
UV_THRESHOLD_USER	UV threshold for the 12V supply to the system	5.6V
OV_THRESHOLD_USER_OUTPUT	OV threshold on the output side	5.1V
UV_THRESHOLD_USER_OUTPUT	UV threshold on the output side	1.7V

4.3.2 Set Output DAC Voltage

The set_reg_vol_to(USER_VOLTAGE) API sets the output voltage.

The dropout voltage of the LDO ISL80103 is significantly less than 120mV at a maximum current of 3A. Ensure the difference between the Input voltage and the required output voltage is minimal so that the LDO is effective.

For example, to set an output voltage of 3.3V, the API for this is set_reg_vol_to(3.3f). Ensure the input voltage to the LDO does not exceed 3.6V, which is around 7.2V on the input voltage to the ISL28025 DPM and DA9313 Dual Switched Capacitor.

Figure 26 shows this user settings.

```
    return FSP_SUCCESS;
}
void start_isl28025_demo(void)
{
    isl28025_Read_OPERATION_REG();
    isl28025_update_reading(&g_isl28025_dpm);
    isl28025_print_reading(&g_isl28025_dpm);
    check_output_threshold(&g_isl28025_dpm);
    set_reg_vol_to(3.3f); // user input
}
```

Figure 26. User Settings

5. Ordering Information

Part Number	Description
QCIOT-COMPMPOCZ	QCIOT-COMPMPOCZ evaluation board

6. Revision History

Revision	Date	Description
1.00	Jun 10, 2024	Initial release

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