

RA6Wx EK Hardware

Renesas Evaluation Kit (EK) supports RA6W1 family of SoCs, the RA6W2 SoC, and the RRQ610x1 family of modules. This manual describes the system functions of the hardware as well as the guidelines of how to enable or disable features of the evaluation kit.

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1. Terms and Definitions

Bluetooth® LE	Bluetooth Low Energy
DK	Development Kit
EK	Evaluation Kit
FSP	Flexible Software Package
GPIO	General Purpose Input Output (pin)
IC	Integrated Circuit
JTAG	Joint Test Action Group
NP	Not Populated
OTP	One-Time Programmable Memory
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembled
POR	Power-On Reset
RF	Radio Frequency
SoC	System-on-Chip
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
WLCSP	Wafer Level Chip Scale Package

2. References

- [1] RA6W1 Datasheet, Renesas Electronics.
- [2] RA6W2 Datasheet, Renesas Electronics.
- [3] RRQ61001 Datasheet, Renesas Electronics.
- [4] RRQ61051 Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

This document describes the hardware of RA6W1 Evaluation Kit (is referred from now-on as EVK). EK-RA6W1 consists of a Motherboard and one of the available daughterboards. Daughterboards vary according to IC type and/or package. All daughterboards present the same form factor and same interface as Motherboard. Different daughterboard combined with the same Motherboard produce different evaluation kits. In total three EVKs are described in this document:

- RA6W1 Evaluation Kit, consists of Motherboard and RA6W1 daughterboard and is used for the development of RA6W1, Wi-Fi System on Chip.
- RA6W2 Evaluation Kit, consisted of Motherboard and RA6W2 daughterboard and is used for the development of RA6W2, Wi-Fi and Bluetooth LE System in Package.
- RRQ610x1-00x Evaluation Kit consists of Motherboard and RRQ610x0-00x daughterboard and is used for RRQ610x1-00x, family of Modules. There are four variants of RRQ610x1-00x Modules.

[Figure 1](#) shows the hardware components of the Evaluation Kit. The Evaluation Kit, combined with Software package (FSP) and Smart Snippets tools, provides an easy to use and complete platform for software/hardware development.

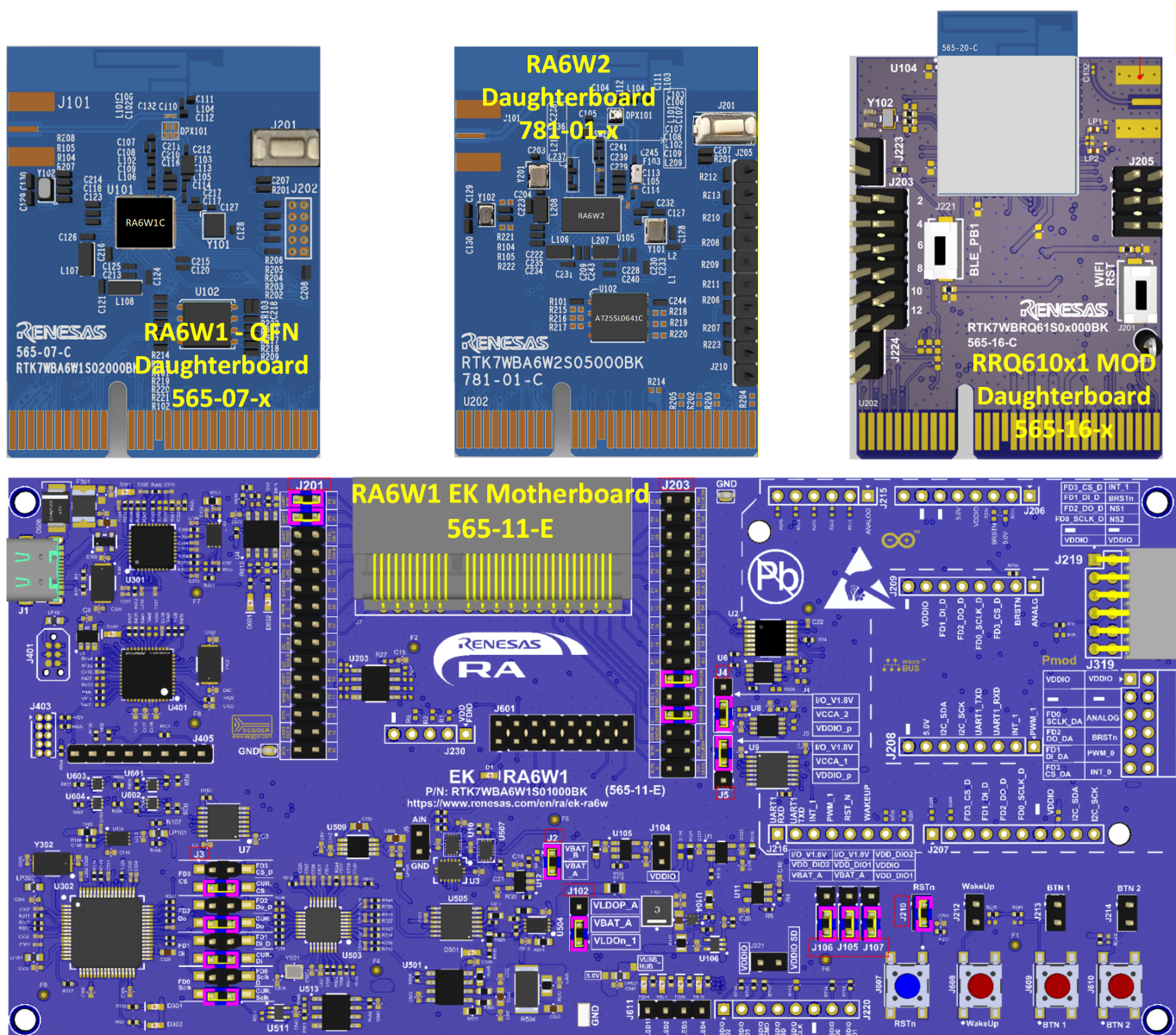


Figure 1. The hardware components for RA6W1, RA6W2 and RRQ610x1 EKs

The following sections describe the system setup, the different available configuration options, as well as the tools provided to debug, develop, and evaluate the system performance. The Motherboard of EK is presented first whereas the various daughterboards are described separately, see Table 1.

Table 1. Components of Evaluation kit

Part number	Description	Name	Board name
RTK7WBA6W1S01000BK	Motherboard for RA6W1, RA6W2 and RRQ610x1 - 00x Modules evaluation, integrating Low Power measuring circuit. A slot to connect evaluation daughterboards of RA6W1, RA6W2 and RRQ610x1-00x Module	EK-RA6W1Mother-board	565-11-E or later
RTK7WBA6W1S02000BK P0_8 to P0_13	Evaluation daughterboard with RA6W1 SoC, QFN 66 pin - Wi-Fi6 Dual-band 2.4/5 GHz 802.11a/b/g/n/ax, 8 MB Flash. PCB trace antenna and option to support SMA connector.	RA6W1 Evaluation Daugh-terboard	565-07-x

Part number	Description	Name	Board name
RTK7WBA6W2S05000BK	Evaluation daughterboard with RA6W2 SoC, BGA 93pin. Wi-Fi6/Bluetooth LE combo. Wi-Fi6 Dual-band 2.4/5 GHz 802.11a/b/g/n/ax, Bluetooth LE v5.1, 8 MB Flash. PCB trace antenna and option to support SMA connector	RA6W2 Evaluation Daughterboard	781-01-x
RTK7WBRQ61S01000BK	Evaluation daughterboard with RRQ61001 Module. Wi-Fi6 Dual-band 2.4/5GHz 802.11a/b/g/n/ax, 8 MB Flash and PCB trace antenna.	RRQ61001-008 Evaluation Daughterboard	565-16-x
RTK7WBRQ61S02000BK	Evaluation daughterboard with RRQ61001 Module. Wi-Fi6 Dual-band 2.4/5 GHz 802.11a/b/g/n/ax, 8 MB Flash and u.FL connector	RRQ61001-009 Evaluation Daughterboard	565-16-x
RTK7WBRQ61S03000BK	Evaluation daughterboard with RRQ61051 Module. Wi-Fi6/Bluetooth LE combo. Wi-Fi6 Dual-band 2.4/5GHz 802.11a/b/g/n/ax, Bluetooth LE v5.1, 8 MB Flash and PCB trace antenna	RRQ61051-008 Evaluation Daughterboard	565-16-x
RTK7WBRQ61S04000BK	Evaluation daughterboard with RRQ61051 Module. Wi-Fi6/Bluetooth LE combo. Wi-Fi6 Dual-band 2.4/5 GHz 802.11a/b/g/n/ax, Bluetooth LE v5.1, 8 MB Flash and u.FL connector	RRQ61051-009 Evaluation Daughterboard	565-16-x

3.1. Evaluation Kit Hardware Block Diagram

Figure 2 shows the complete system block diagram of the EK.

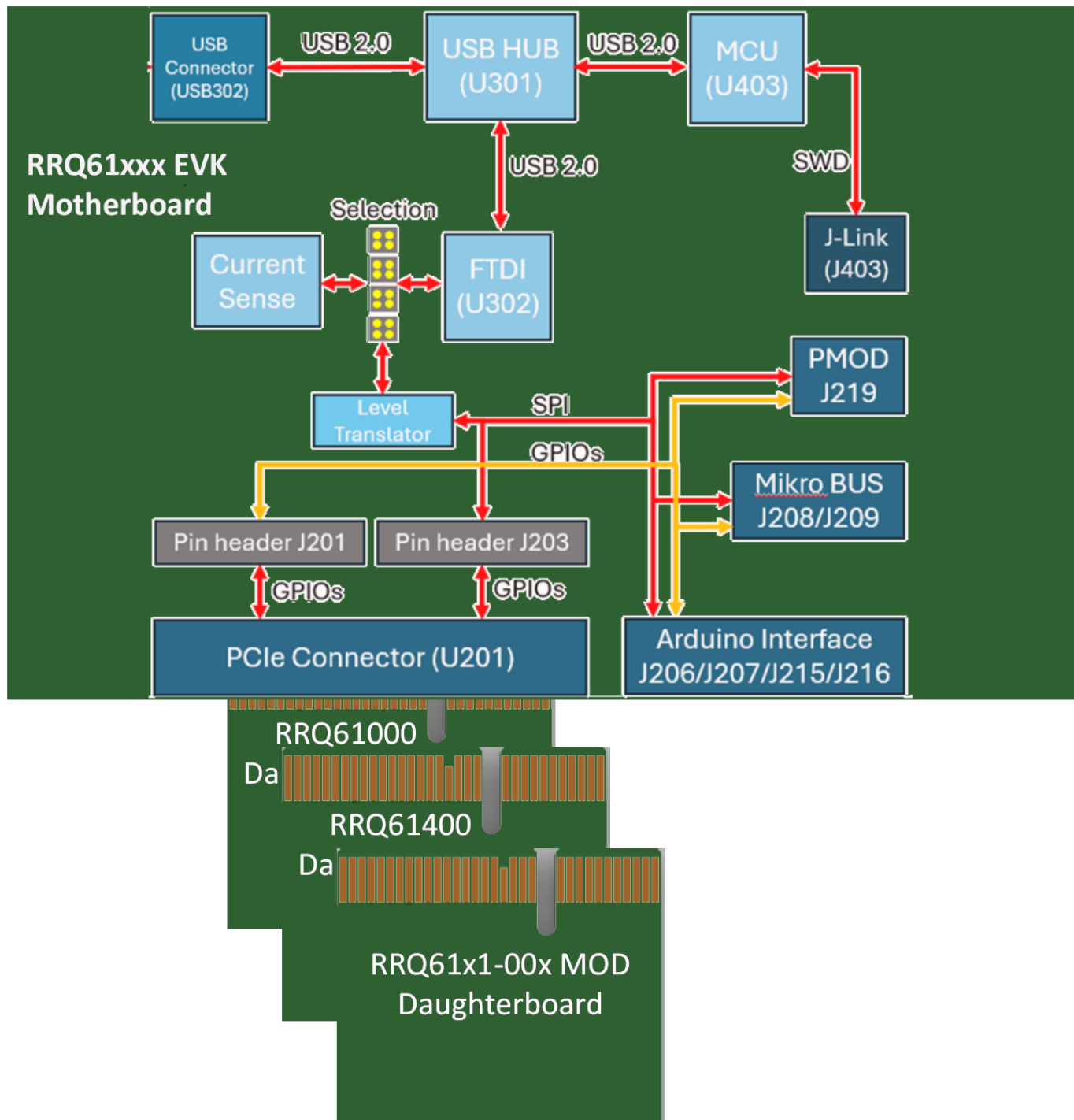


Figure 2. Block diagram of the Evaluation kit

4. Get to Know Evaluation Kits for RA6W1/RA6W2/RRQ610x1

4.1. Evaluation Kits Hardware Components

The three variants of RA6W1EVK consist of the following parts:

- RA6W1 EVK
 - Motherboard, EK-RQ61, PCBA reference number 565-11-x
 - Daughterboard, RA6W1_db-wlcsp70, PCBA reference number 565-09-x
- Or
- Daughterboard, RA6W1_db-fcqn66, PCBA reference number 565-07-x
- RA6W2 EVK
 - Motherboard, EK-RQ61, PCBA reference number 565-11-x
 - Daughterboard, RA6W2_db, PCBA reference number 781-01-x
- RRQ610x1-00x EVK
 - Motherboard, EK-RQ61, PCBA reference number 565-11-x
 - Daughterboard RRQ610xxMOD_db PCBA reference number 565-16-x with four variants based on module type assembled:
 - RRQ61001-008, Wi-Fi only with printed Antenna
 - RRQ61001-009, Wi-Fi only with uFL
 - RRQ61051-008, Wi-Fi and Bluetooth LE with printed Antenna
 - RRQ61051-009, Wi-Fi and Bluetooth LE with uFL.



Figure 3. RA6W1 complete system of Motherboard, Daughterboard

Table 2. Headers and jumper settings of RA6W1 EVK Motherboard

HDR	Function of headers	Jumper options		Default jumper setting
J3	SPI interface switch between power measurement circuit and UART1/SPI to RA6W1	- Option 1: SPI bus of power measurement section is connected to FT2232HL (USB to UART, U302) - Option 2: UART1 / SPI bus of RRQ610xxx is connected to FT2232HL (USB to UART, U302) Note 1 Only one option is permitted.	Option 1: Mount pos. 1-2 Option 2: Mount pos. 3-4 Option 1: Mount pos. 1-2 Option 2: Mount pos. 3-4 Option 1: Mount pos. 1-2 Option 2: Mount pos. 3-4 Option 1: Mount pos. 1-2 Option 2: Mount pos. 3-4	Enable UART1/SPI Bus (Option 2) Mount J302: 3-4 J303: 3-4 J304: 3-4 J305: 3-4
J105	VDD_DIO1 voltage selection (1.8 V, 3.3 V)	1.8 V	Mount pos. 1-2	3.3 V Mount pos. 1-2
		VBAT_A (=3.25 V – default)	Mount pos. 2-3	
J106	VDD_DIO1 voltage selection (1.8 V, 3.3 V)	1.8 V	Mount pos. 1-2	3.3 V Mount pos. 1-2
		VBAT_A (=3.25 V – default)	Mount pos. 2-3	
J102	VBAT_A Power supply for Wi-Fi (3.3 V)	Use with power measurement circuit	Mount pos. 1-2	Bypass Power measurement circuit Mount pos. 2-3
		Bypass power measurement circuit	Mount pos. 2-3	
J2	VBAT_B Power supply for Bluetooth LE subsection	Connect VBAT_A with VBAT_B		Mount
J201	UART (Wi-Fi)	External (Personal Computer) Access to daughterboards through UART pins P0_00 and P0_01 connected to	Mount pos. 1-2 Mount pos. 3-4	Mount pos. 1-2 Mount pos. 3-4
		No external access to UART	Not Mount jumpers	
J203	SWD (Wi-Fi)	External (Personal Computer) access to daughterboards through SWD pins SWDIO and SWCLK	Mount pos. 21-22 Mount pos. 25-26	Mount pos. 21-22 Mount pos. 25-26
		No external access to UART	Not Mount jumpers	
J210	Jumper for connecting push-button J607 to RST_N of the Wi-Fi section	Connect to RST_N	Mount pos. 1-2	Mount pos. 1-2
J212	Switch for waking-up the board from Sleep mode	Wake-up is connected to push-button J608.	Mount pos. 1-2	No Mounted

Note 1 Jumpers must be also placed on pairs of pins 1-2, 3-4, 4-5 and 5-6 of J203. SPI/UART is assigned to P1_00, P1_01, P1_02 and P1_03 respectively.

4.2.2. RRQ61051 Module Daughterboard

Table 3 shows the jumper settings for the daughterboard of RRQ61051 Module.

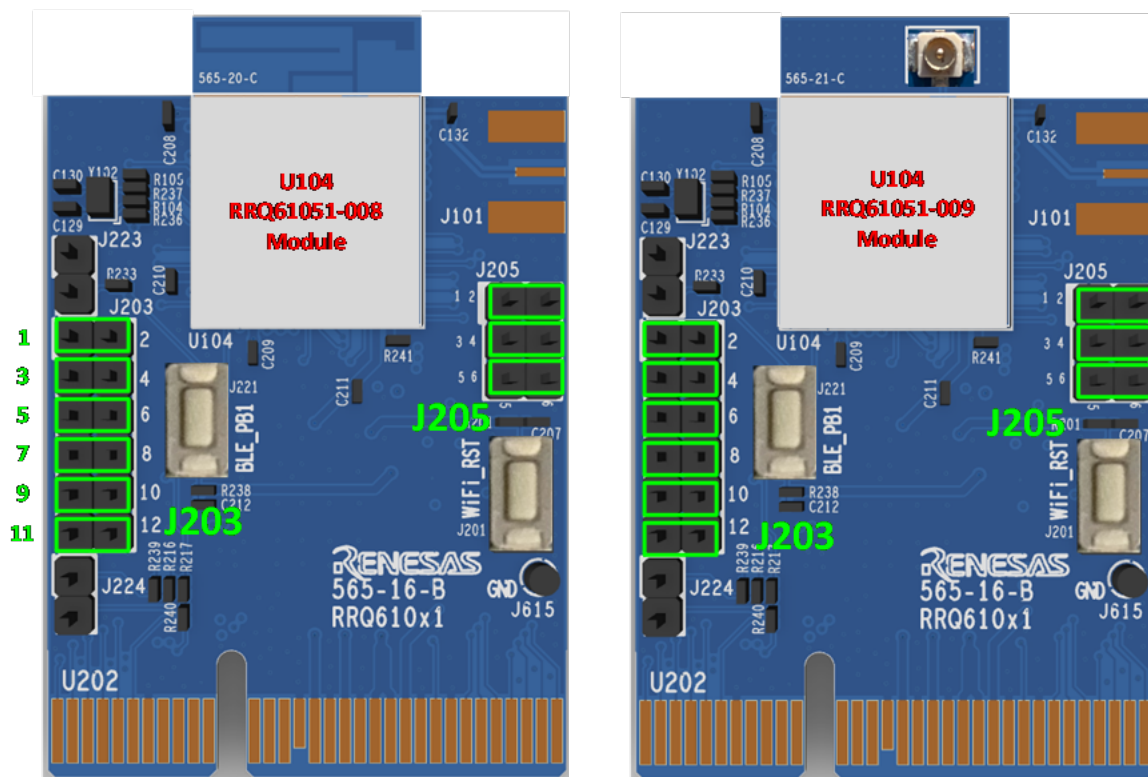


Figure 5. Default Jumper settings of the RRQ61051 Module daughterboard

Table 3. Jumper settings of RRQ61051-00x Module Daughterboard

HDR	Function of headers	Jumper options		Default jumper setting
J203	Pin1: B_P0_00 Pin2: P1_10	Connect UTX (Bluetooth LE) to URX (Wi-Fi)	Mount pos. 1-2	Mount pos. 1-2
	Pin3: B_P0_01 Pin4: P1_11	Connect URX (Bluetooth LE) to URX (Wi-Fi)	Mount pos. 3-4	Mount pos. 3-4
	Pin5: B_P0_03 Pin6: P1_12	Connect URTS (Bluetooth LE) to UCTS (Wi-Fi)	Mount pos. 5-6	Mount pos. 5-6
	Pin7: B_P0_04 Pin8: P1_13	Connect UCTS (Bluetooth LE) to URTS (Wi-Fi)	Mount pos. 7-8	Mount pos. 7-8
	Pin9: B_P0_02 Pin10:P1_14	Connect RST (Bluetooth LE) to RST_N (Wi-Fi)	Mount pos. 9-10	Mount pos. 9-10
	Pin11: B_P0_05 Pin12: P1_15	Connect iBtAct (Bluetooth LE) to Coex (Wi-Fi)	Mount pos. 11-12	Mount pos. 11-12
J205	pin1: P0_06 pin2: RFSW1	Activate RF Switch. Connect P0_06 with RFSW1	Mount pos. 1-2	Mount pos. 1-2
	Pin3: P0_07 Pin4: RF_SW2	Activate RF Switch Connect P0_07 with RFSW2	Mount pos. 3-4	Mount pos. 3-4
	Pin5: VBAT_BLE Pin6: VBAT_BLE+M	Supply Bluetooth LE	Mount pos. 5-6	Mount pos. 5-6

NOTE

No jumpers are required for the Daughterboard with RRQ61001 Module.

5. RTK7WBA6W1S01000BK-EK-RA6W1 Motherboard (565-11-x)

The block diagram and the actual component locations of the Motherboard are shown in [Figure 6](#) and [Figure 7](#).

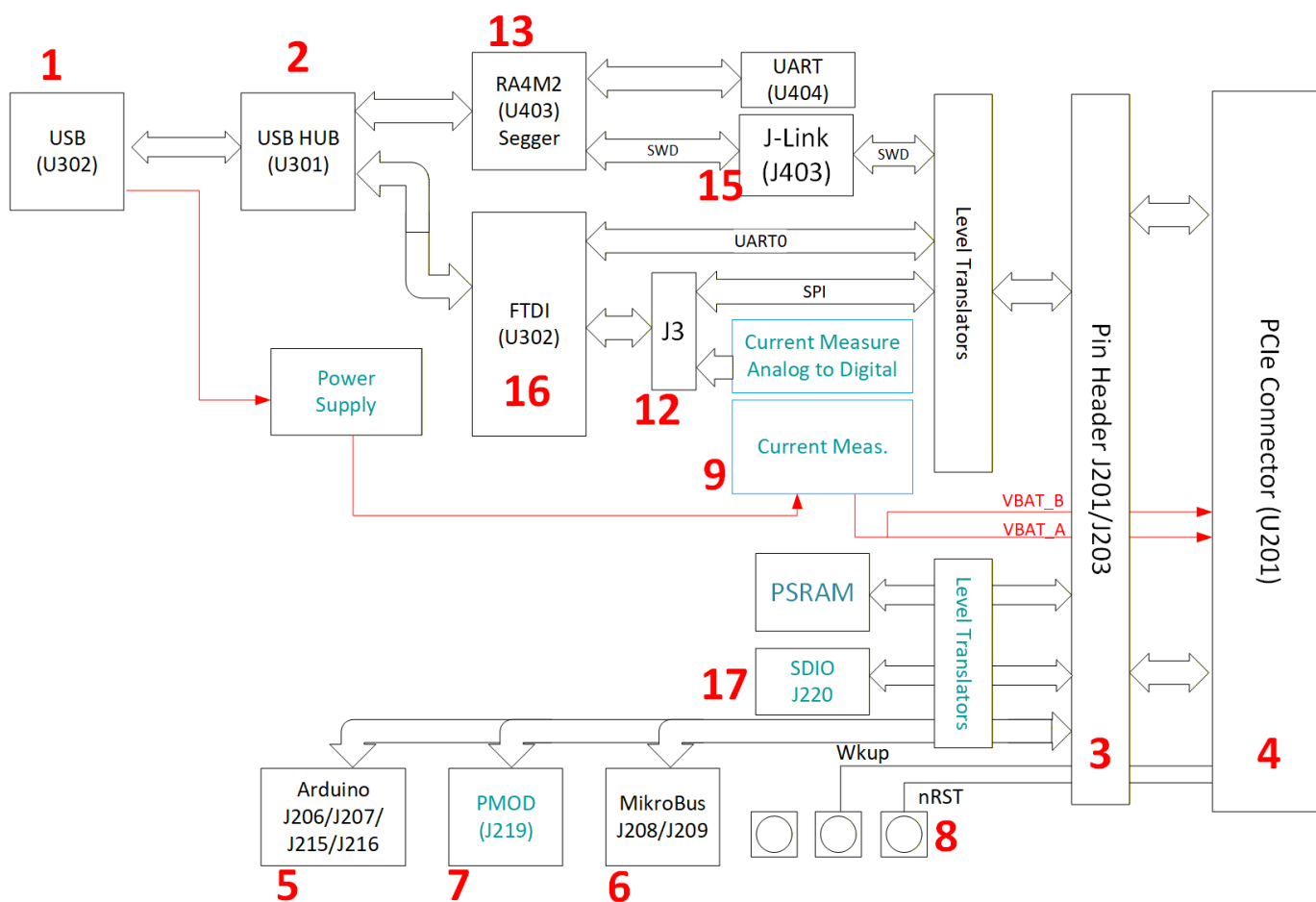


Figure 6. EK - RA6W1 Motherboard block diagram

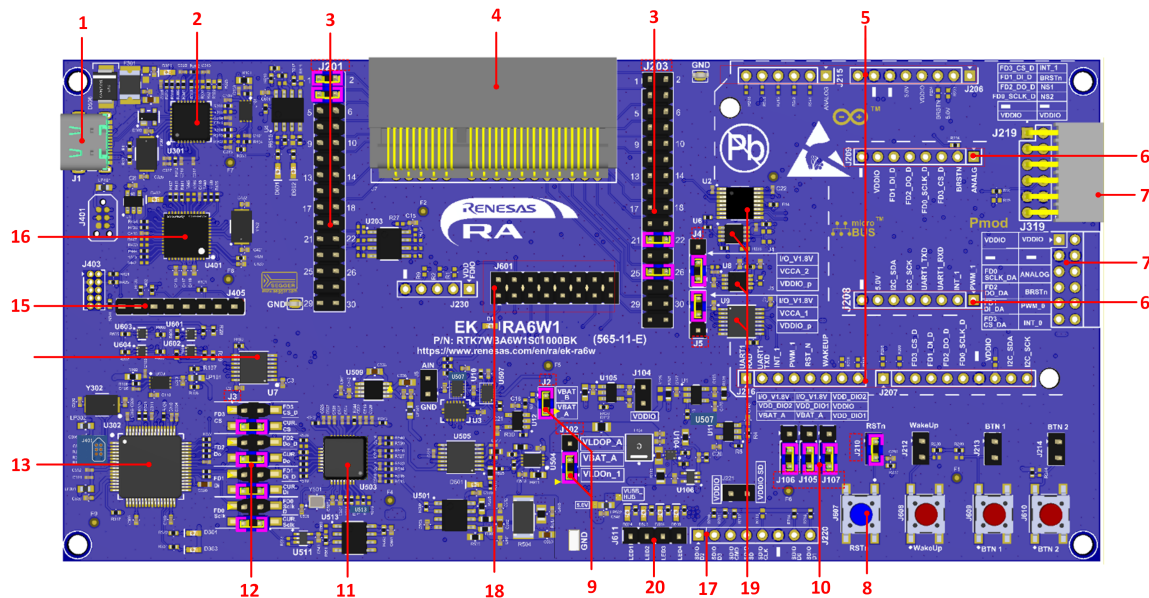


Figure 7. EK - RA6W1 motherboard

1. EVK Motherboard Type C - USB connector (**USB302**), power and data port for the EK - RA6W1.
2. **USB hub (U301)**: connects JTAG and UART interfaces to the PC.
3. **Signal/Power breakout headers (J201/J203)**: exposes all the pins of the Daughterboard and Motherboard to allow wiring for custom configurations as well as monitoring of the hardware signals.
4. **Daughterboard connector (U201)**: an interface mating connector for the Daughterboard.
5. **Arduino sockets (J206/J207/J215/J216)**: sockets for plugging in Arduino interface add-on boards.
6. **MikroBUS™ sockets (J208/J209)**: sockets for plugging in MikroBUS™ interface add-on boards. It is multiplexed with PMOD (to be used with DA1453x).
7. **PMOD connector (J219)**: socket for plugging in PMOD interface add-on boards. It is multiplexed with MikroBUS™.
8. **Push-buttons (J607/ J608/J609/J610)**: J607 push-button used to reset Daughterboard, J608/J609/J610 push buttons for general use.
9. **Power selection (J102/J103)**: the current sense circuit option. Using this current measurement circuit, you can monitor the current consumption of Daughterboard through Smart Snippets Toolbox software application.
10. **I/O voltage selection (J101)**: selects the I/O voltage generated for the Daughterboard (1.8 V, 3.3 V).
11. **Current sense (U503)**: the current sense circuit.
12. **SPI interface switch (J302/J303/J304/J305)**: selects the I/O voltage generated for the Daughterboard board (1.8 V, 3.3 V).
13. **USB to UART - (U302)**: provides communication between Daughterboard UART port and PC. It also transfers the current measurement samples to PC.
14. **Level translators (U7)**: transfer the data between Daughterboard and FTDI (U302) in proper voltage level.
15. **External J-link connector (J403)** for accessing Wi-Fi SoC or Bluetooth LE SoC.
16. **MCU (U403)** where the SWD implementation of SEGGER applied.
17. **SDIO header (J220)**: it must be mounted.
18. **Trigger (J601)**: the trigger signals monitored and presented on Smart Snippets Toolbox.
19. **Level translators (U2/U6/U8/U9)**: for the interface section (PMOD, Android and MikroBUS).
20. **LEDs (J611)**: Four LEDs are connected to this header. For enabling an LED, a jumper wire must be connected between a GPIO and one of the pins of J611.

5.1. Power Section

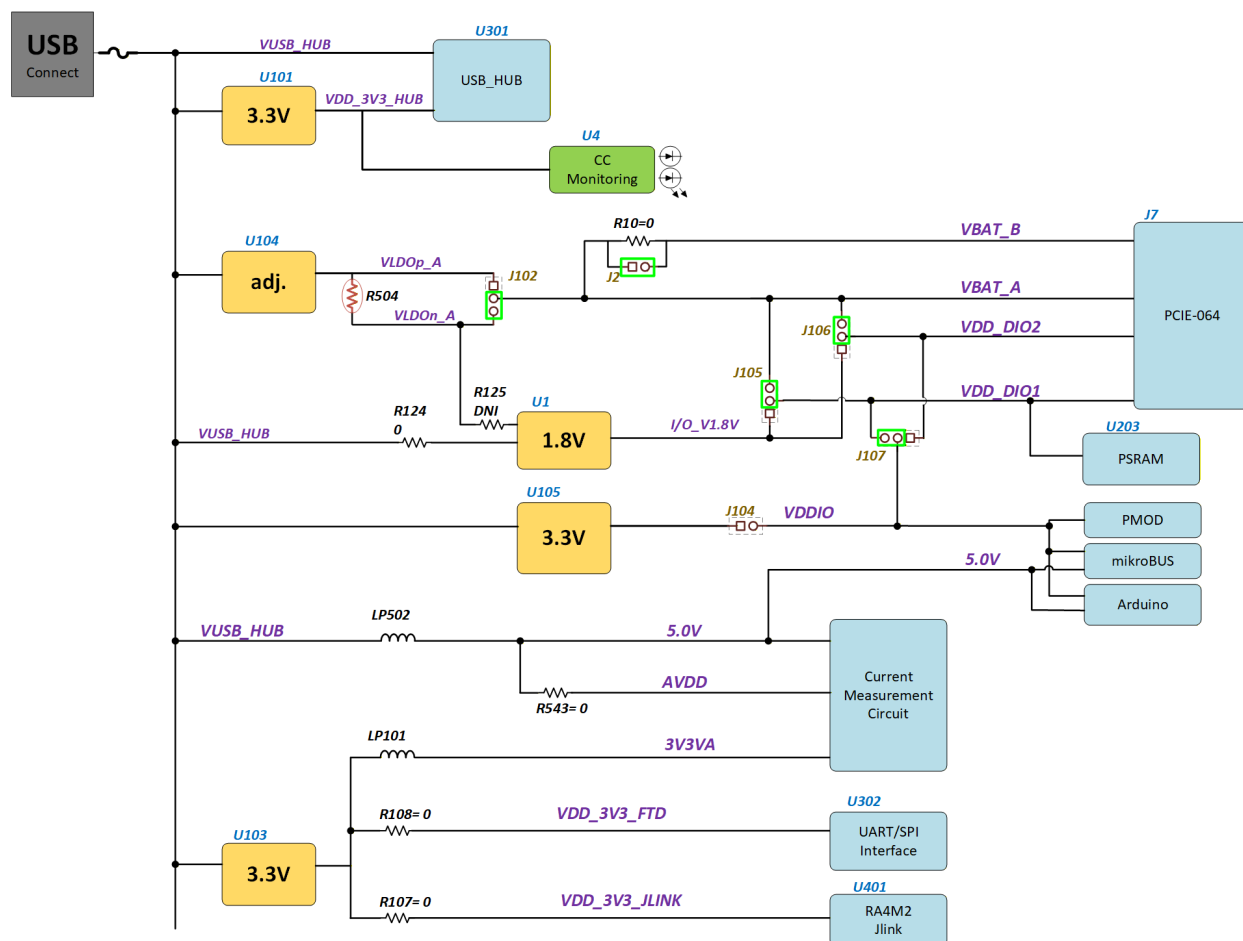


Figure 8. EK - RA6W1 Motherboard power tree block diagram

The power tree of the EK - RA6W1 Motherboard, [Figure 8](#) consists of several power domains, the VUSB_HUB (=5 V) power supply, the 3.3 V voltage rail supply for the supporting circuits of Motherboard (RA4M2-jlink, USB Hub, FTDI), the main supply for Daughterboards (VBAT_A and VBAT_B), the I/O voltage supplies for Daughterboards (VDD-DIO1, VDD_DIO2) and the I/O voltage supply for interfaces (PMOD, MikroBUS and Arduino).

Table 4. Power section default setup of RAW1 EK Motherboard

Voltage rate	Jumper settings	Description
VBAT_A = 3.25 V	No jumper required	Wi-Fi subsection main supply
VBAT_B = 3.25 V	J2 mounted	Bluetooth LE subsection main supply
VDD_DIO1 = 3.25 V	Jumper is mounted on J105, 1-2	IO1 of Wi-Fi Subsystem and PSRAM
VDD_DIO2 = 3.25 V	Jumper is mounted on J106, 1-2	IO1 of Wi-Fi Subsystem
VDDIO = 3.25 V	Jumper is mounted on J107, 1-2	PMOD, MikroBUS and Arduino
VDD_3V3_FTD = 3.3 V	No jumper required	USB to UART/SPI, U302, FT232HL
VDD_3V3_JLINK = 3.3 V	No jumper required	USB to JTAG, U403, RA4M2
VDD_3V3_HUB = 3.3 V	No jumper required	U301, USB HUB, USB2512B

The Daughterboard is powered from the J102/J103:

- I/O voltage (1.8 V or 3.3 V)
- 3.3 V system power for Daughterboard.

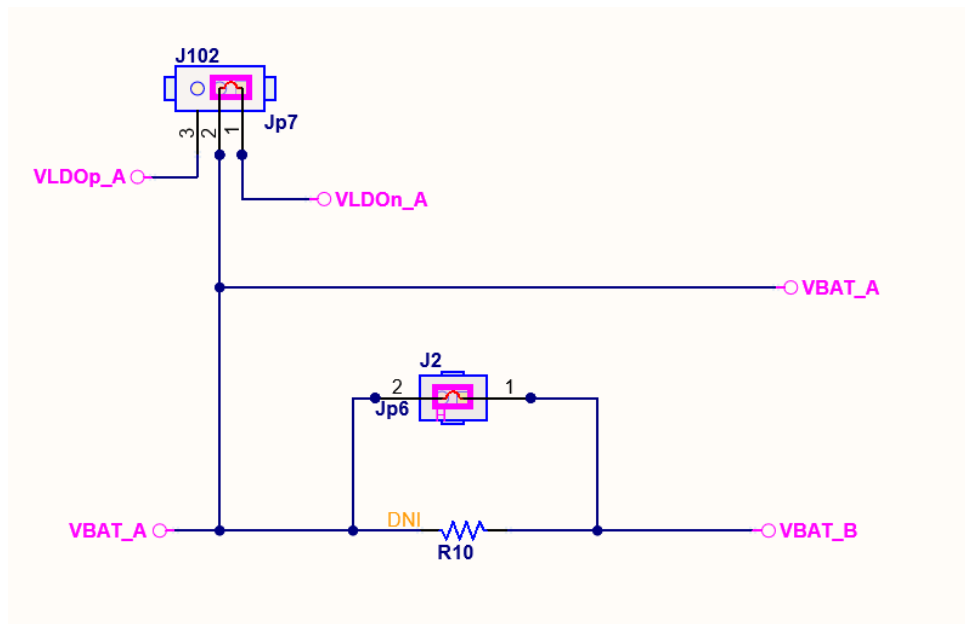
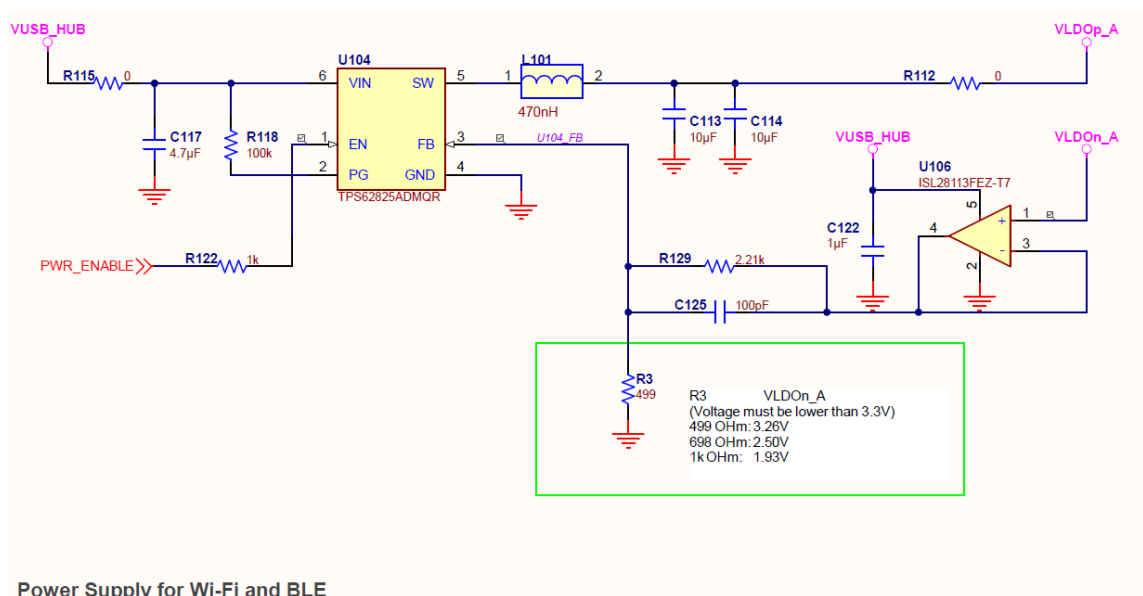


Figure 9. EK - RA6W1 Motherboard power circuit for I/O voltage

Daughterboards are supplied from:

- J102: provides VBAT_A, the main power supply for the Wi-Fi subsystem voltage. VBAT_A is equal to 3.25 V and it is supplied from a 1 Amp DCDC converter (U104), see Figure 8.
- For changing VBAT_A, resistor R3 must be changed. Do not set VBAT_A higher than 3.25 V.



Power Supply for Wi-Fi and BLE

Figure 10. The power supply of VBAT_A

- J2: provides VBAT_B, the power supply for Bluetooth, where it is applicable. VBAT_B is connected directly to VBAT_A. J2 is used for current consumption measurement using an external Amp-meter.
- J105: provides VDD_DIO1 to Wi-Fi subsystem. It can be set equal to VBAT_A (default) or I/O_V1.8V = 1.8 V I/O_V1.8 V is generated from U1
- J106: provides VDD_DIO1 to Wi-Fi subsystem. It can be set equal to VBAT_A (default) or I/O_V1.8 V = 1.8 V I/O_V1.8 V is generated from U1
- U1 is LDO which can be supplied by either the USB port of Motherboard (VUSB_HUB) or VBAT_A. By default, U1 is supplied from VUSB_HUB.

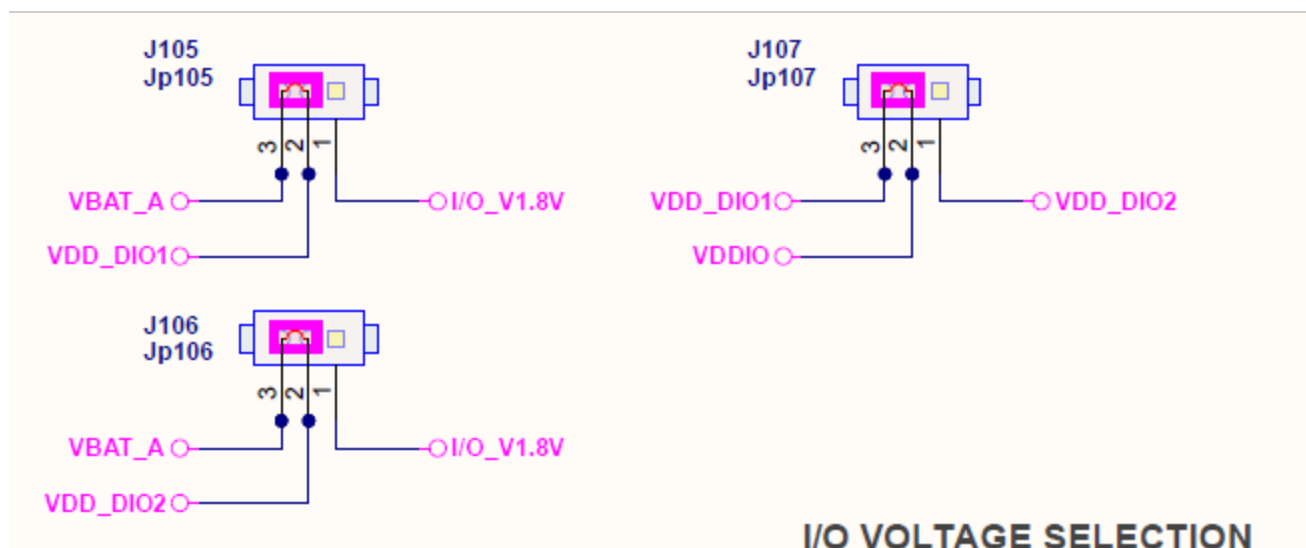


Figure 11. EK RA6W1Motherboard 3.3 V power circuit to Daughterboard

- J107: provides VDDIO to the interface section, PMOD, Arduino and MikroBUS. VDDIO can be either supplied from VDD_DIO1 or VDD_DIO2 or with 3.3 V generated from LDO, U105.
- For supplying interface section with 3.3 V, jumper must be removed from J107. A jumper must be applied on J104, see [Figure 12](#).
- J230: on pin 1, VDD_FDIO is monitored. VDD_FDIO is produced by RA6W1 or RA6W2. It is not available on the daughterboards of the RRQ610x1 modules. J203 is not mounted.

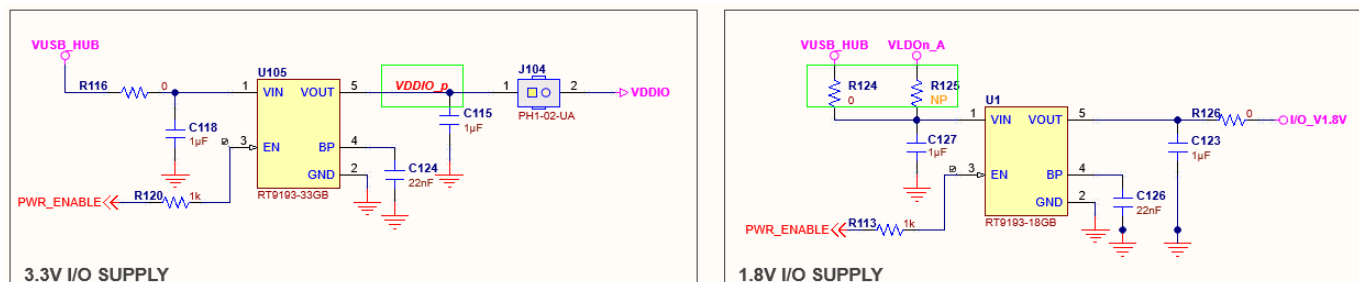


Figure 12. The LDOs for I/O_V1.8V and VDDIO

[Figure 13](#) shows the configuration on PCB of EK - RA6W1 Motherboard for the jumpers, J2/J102/J104/J105/J106/J1073.

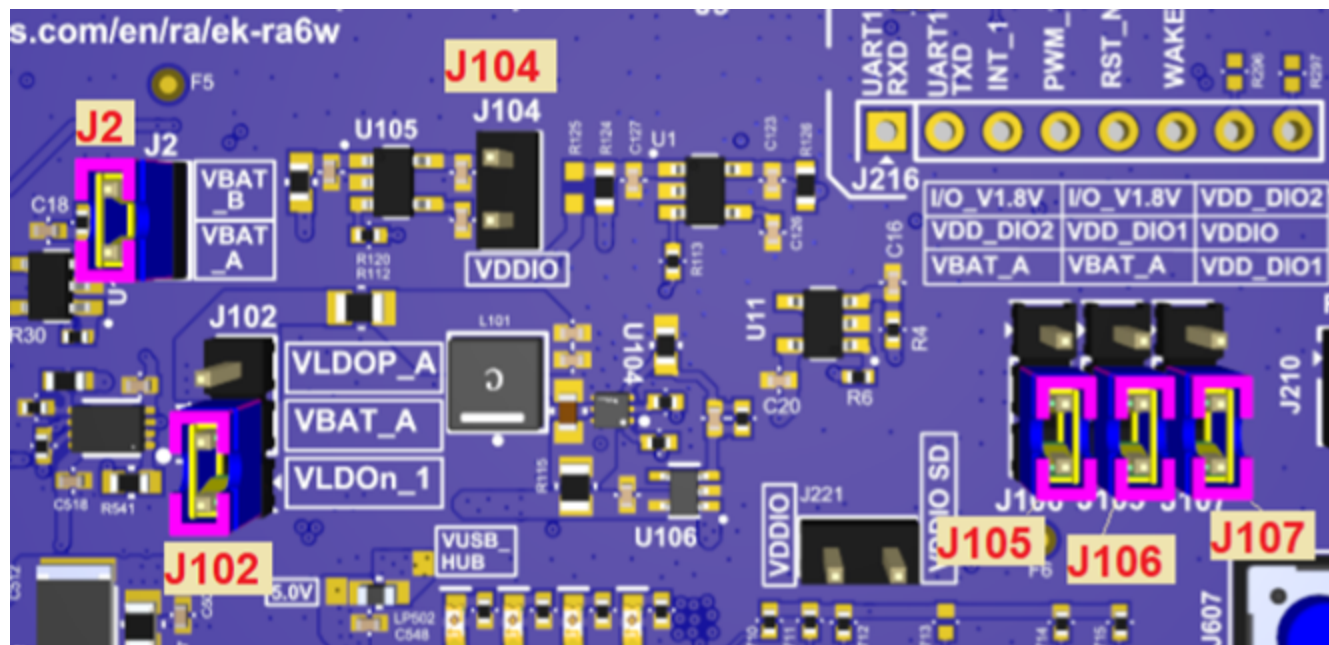


Figure 13. J2/J102/J104/J105/J106/J1073 headers configuration

5.2. Power Measurement Circuit

A power measurement circuit is applied on the EK - RA6W1 Motherboard.

NOTE

SmartSnippets Toolbox software application is required for the monitoring of the voltages and the signals triggering.
[SmartBond™ Development Tools | Renesas](#)

In the EK - RA6W1 Motherboard the power measurement circuit is placed on board and measures the current drawn from daughterboards. It provides the capability of measuring separately the current Wi-Fi and Bluetooth LE (for the daughterboards which support Bluetooth LE). In addition to power measurements up to eight software trigger signals can be monitored and depicted to Smart Snippet toolbox.

The power measurement unit has the following features:

- Full scale range 500 mA at 3.3 V
- Measure accurately down to 1 μ A
- Current sense resistors
 - 2.37 Ω in series to VLDO for Wi-Fi
 - 2.37 Ω in series to VLDO for Bluetooth LE
- Analog processing blocks
- Fast quad channel 24-bit ADC with SPI interface
- FTDI chip for transferring data to the PC
- Software trigger circuit.

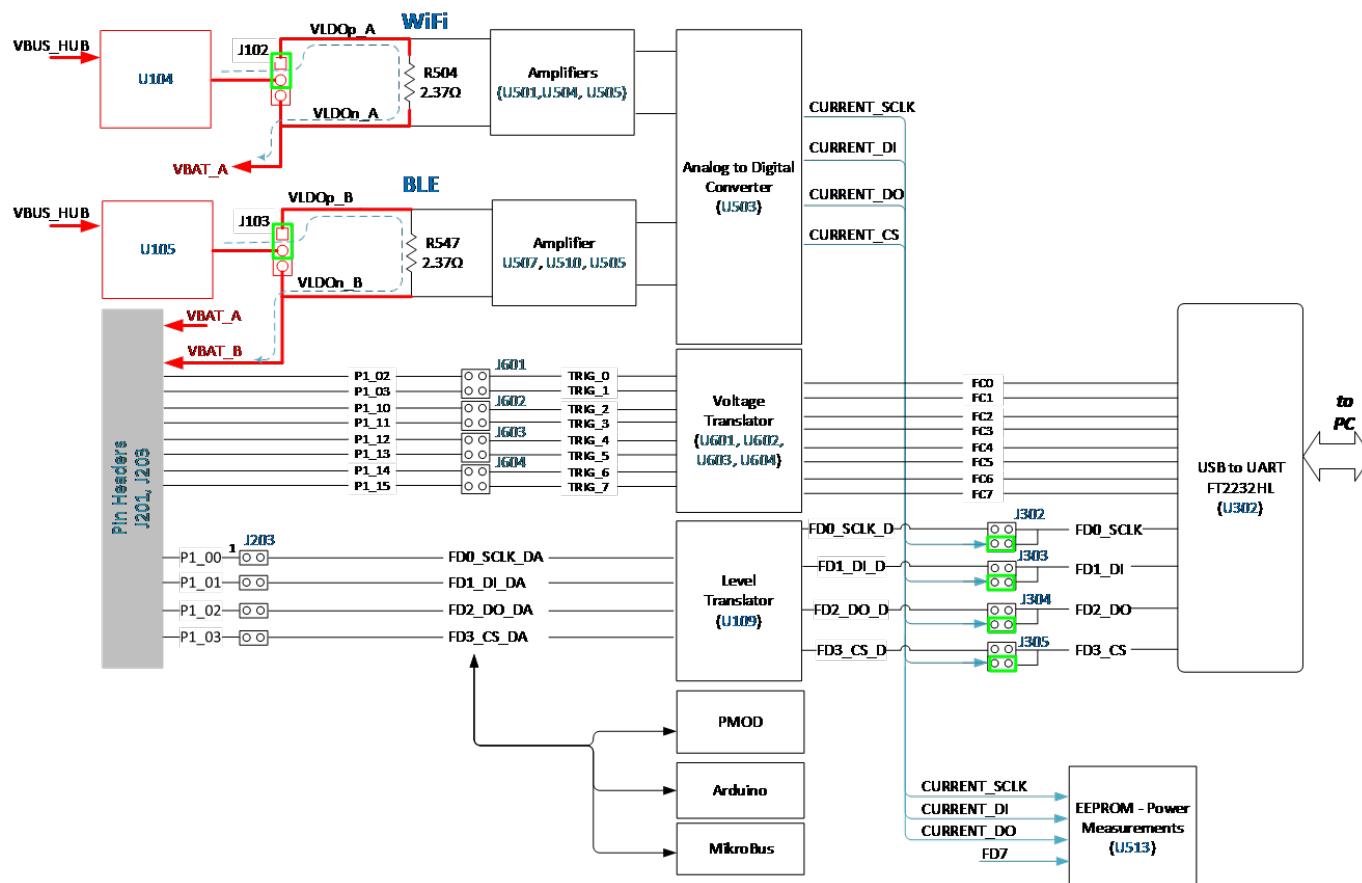


Figure 14. Power measurement circuit block diagram

The input to the circuit is the voltage across the sense resistors R504 and R547. The voltage across the sense resistors is sampled simultaneously by two differential amplifier stages and is converted by the ADC to a digital value. The low range has a conversion gain of 6.114 V/A and covers up to about 500 mA depending on the VBAT voltage. Both channels are sampled simultaneously, and the host software selects the correct channel using a threshold of 750 μ A.

An EEPROM memory is used to store production data and allows the host software to autdetect the module. For enabling Power measurement circuit, apply the following jumpers, see [Table 5](#).

Table 5. Jumper settings for enabling Power measurement circuit

HDR	Function of headers	Jumper options		Jumper setting for enabling Power measurement circuit
J3	SPI interface switch between power measurement and UART1/SPI to RA6W1	Option 1: SPI bus of power measurement section is connected to FT2232HL (USB to UART, U302) Option 2: UART1 / SPI bus of RRQ610xxx is connected to FT2232HL (USB to UART, U302) Only one option is permitted.	Option 1: Mount pos. 3-4 Option 2: Mount pos. 1-2	Mount J3: 3-4
			Option 1: Mount pos. 7-8 Option 2: Mount pos. 5-6	Mount J3: 7-8
			Option 1: Mount pos. 11-12 Option 2: Mount pos. 9-10	Mount J3: 11-12
			Option 1: Mount pos. 15-16 Option 2: Mount pos. 13-14	Mount J3: 15-16
J2	Power supply for Bluetooth LE (3.3 V)	Connect VBAT_A to		Mount pos. 1-2

HDR	Function of headers	Jumper options		Jumper setting for enabling Power measurement circuit
		VBAT_B. VBAT_B supplies Bluetooth LE Sub-section (where it is available)		
J102	Power supply for Daughterboard VBAT_A	Use with power measurement circuit	Mount pos. 1-2	Mount pos. 1-2
		Bypass power measurement circuit	Mount pos. 2-3	

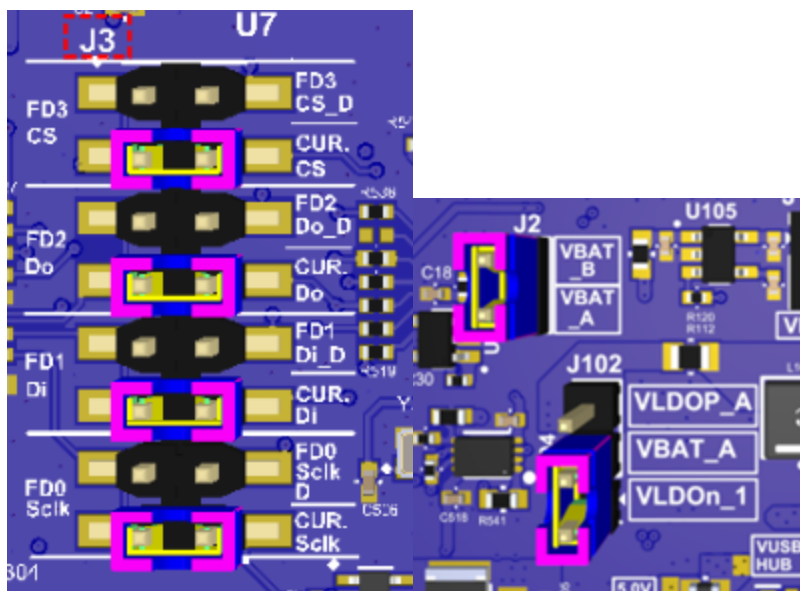


Figure 15. Jumper setting for activating power measurements circuit

Finally, there are eight trigger options defined (TRIG_0 to TRIG_7).

As shown in Figure 13 suitable jumpers on headers J601, J602, J603 and J604 allow you to directly select any of the available signals.

Any other GPIO can be used as a trigger source by connecting any of TRIG_x pins with a jumper wire to the desired position at breakout headers (J201 or J203).

Dual MOSFET U601 to U604, buffer the signals to provide compatibility with 1.2 to 5 V I/O levels.

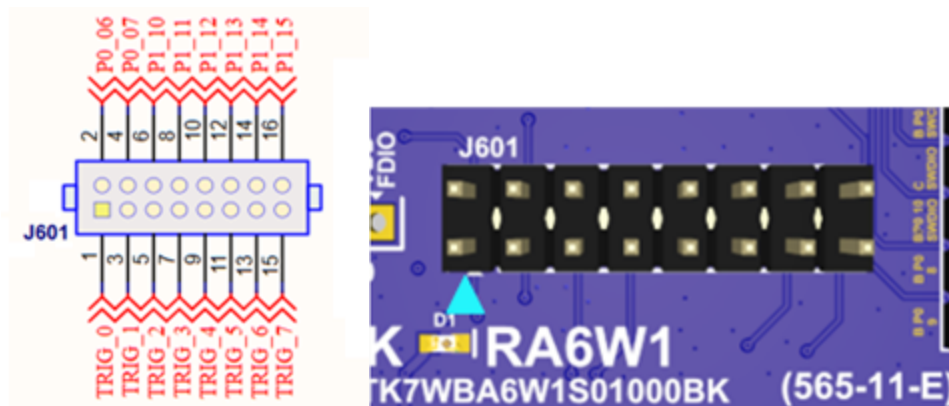


Figure 16. Apply jumper between Px_xx and TRIGx for enabling trigger

Dual MOSFET U601 to U604, buffer the signals to provide compatibility with 1.2 to 5 V I/O levels.

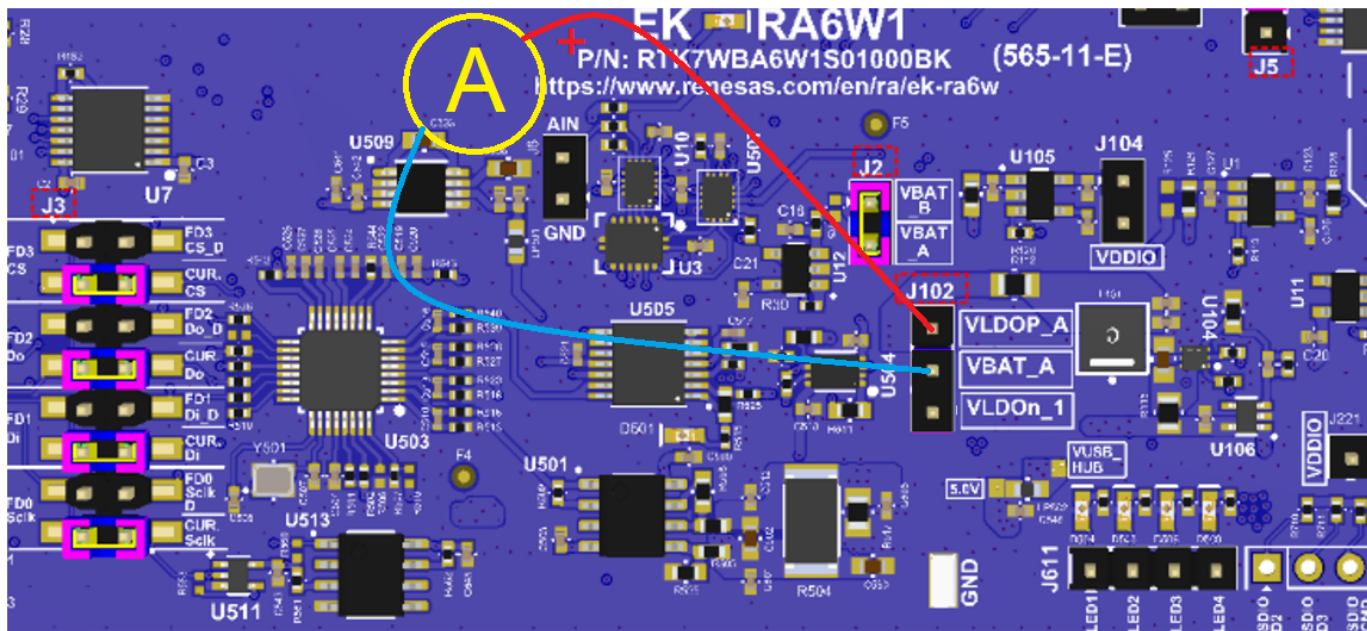


Figure 18. Hardware configuration for power measuring with external equipment

5.2.1.2. Case 2: Power Measurements of Current Consumption of the Wi-Fi Section on Combo (Wi-Fi/Bluetooth LE) Systems

This is applied on following evaluation boards/SoC or Modules:

- RTK7WBA6W2S05000BK, RA6W2 SoC
- RTK7WBRQ61S03000BK, RRQ61051-008 Module
- RTK7WBRQ61S04000BK, RRQ61051-009 Module

Measurement options:

- Use on-board Power Measurement Circuit:
 - Remove jumper from J2.
 - Connect a wire between J104 pin 1 and J2 pin 1.

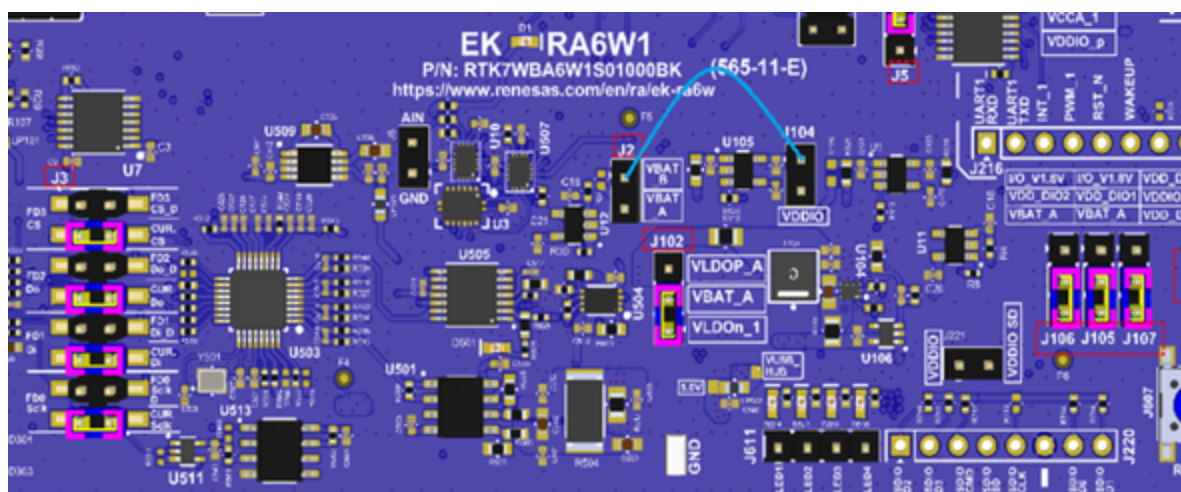


Figure 19. Hardware configuration for power measuring with on-board Power Measurement Circuit

- Use External Equipment: Current measurement can be performed by connecting an external equipment to J102 pins, VLDO_P and VBAT_A. Settings are:
 - Removing jumpers from J102 and J2.
 - Connecting an amp-meter to J102 pins VLDO_P and VBAT_A.
 - Connecting a wire between J104 pin 1 and J2 pin 1.



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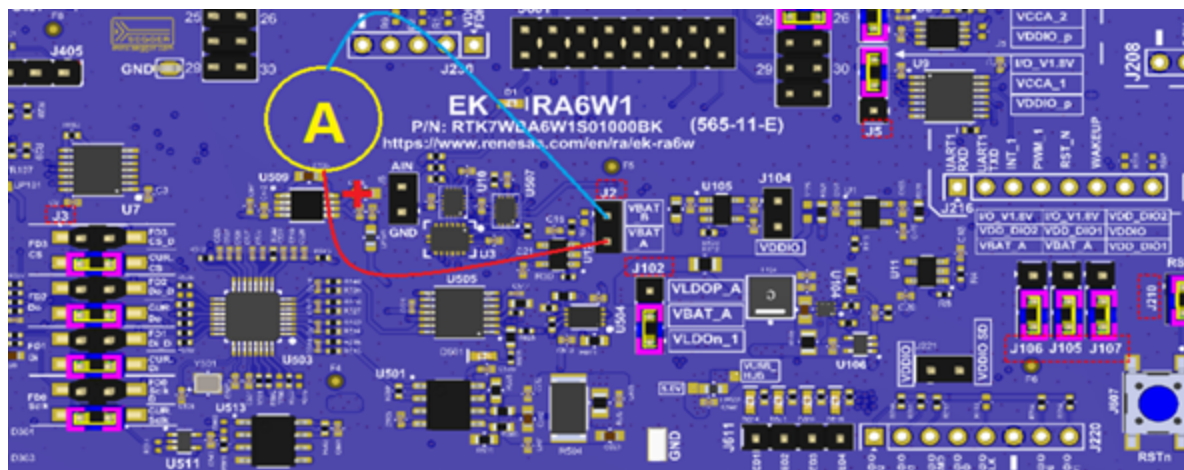


Figure 21. Hardware configuration for power measuring with external equipment

5.2.1.4. Case 4: Power Measurements of Current Consumption of the Wi-Fi and Bluetooth LE Sections on Combo (Wi-Fi/Bluetooth LE) Systems

This is applied on following evaluation boards/SoC or Modules:

- RTK7WBA6W2S05000BK, RA6W2 SoC
- RTK7WBRQ61S03000BK, RRQ61051-008 Module
- RTK7WBRQ61S04000BK, RRQ61051-009 Module

Measurement options:

USB HUB operation is indicated through the green LED D301 on EK - RA6W1 Motherboard. A 24 MHz crystal (Y301) is required for chip operation.

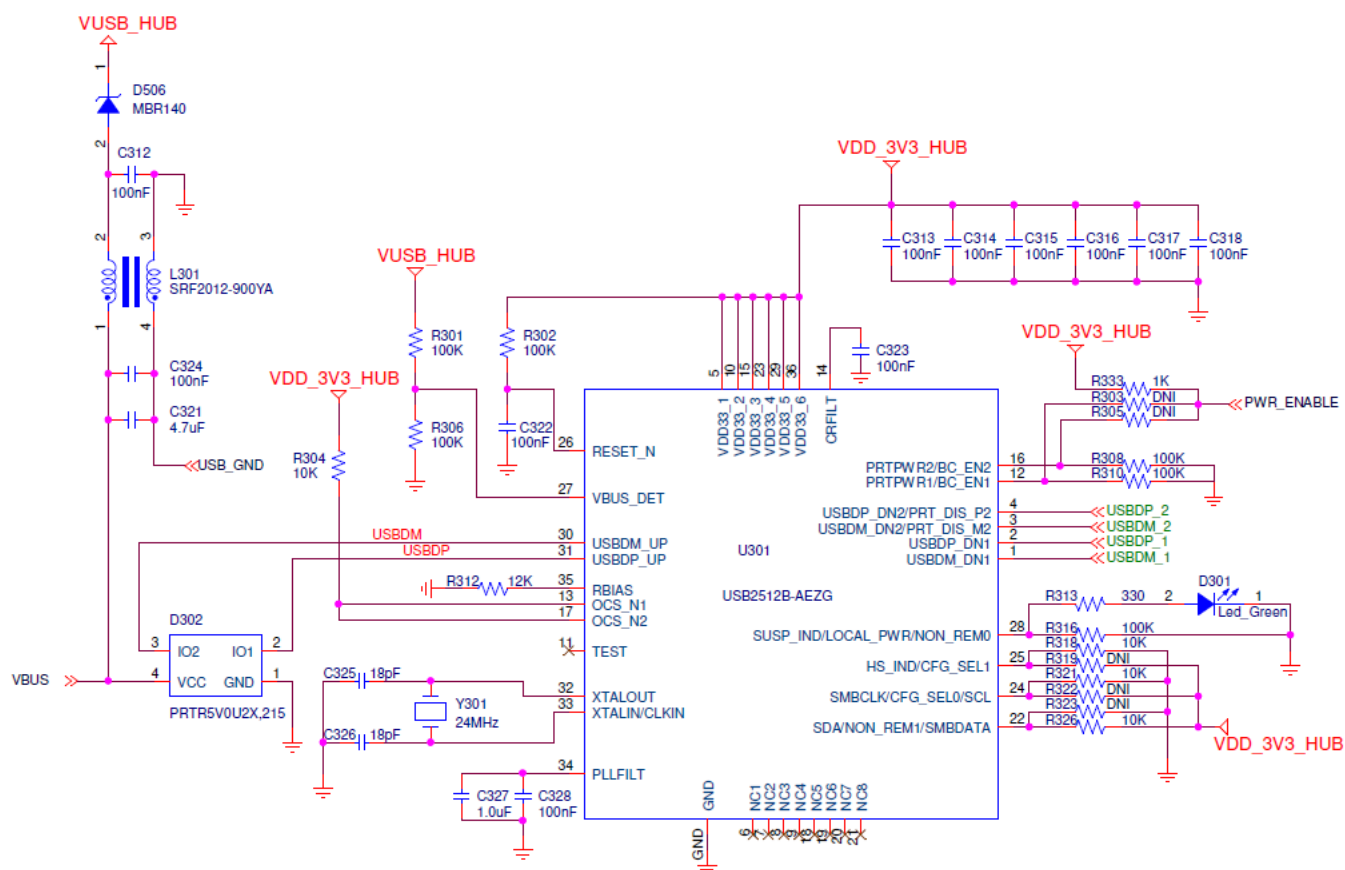


Figure 24. USB HUB circuitry

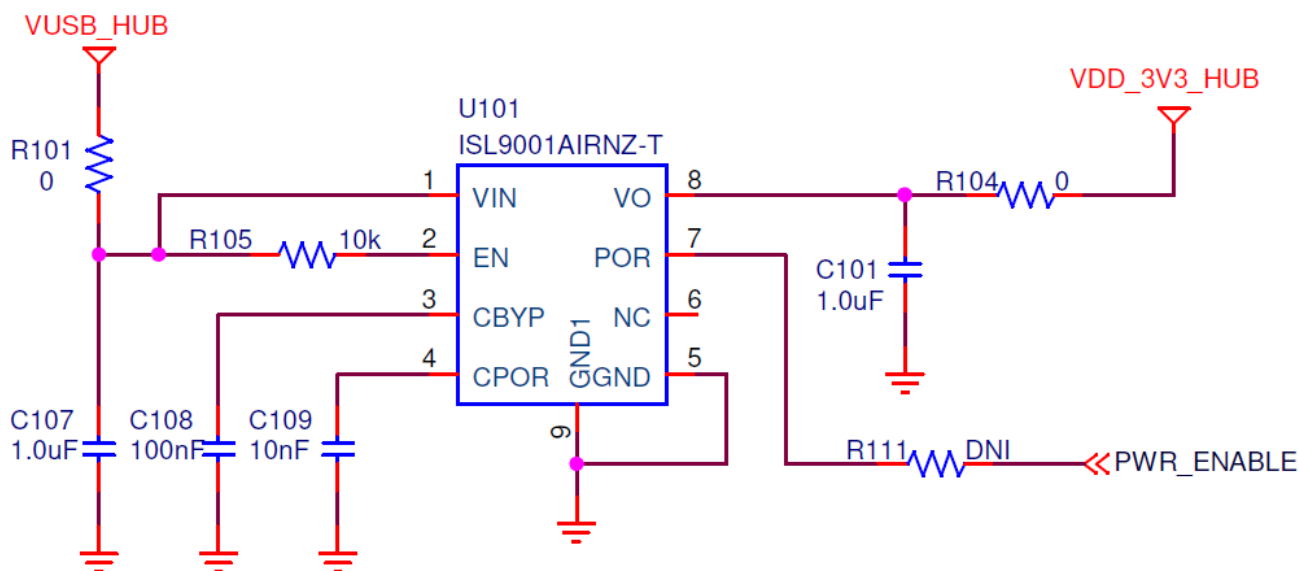


Figure 25. USB HUB power supply

5.4. USB to UART, (U302)

The USB to UART function is implemented by U302, FT2232HL (Figure 26). A 12 MHz crystal (Y302) is required for the chip operation. This chip is supplied with 3.3 V from U103 (Figure 27).

U302 functions are the following:

- Connecting a PC to the UART ports established on Daughterboards.
- The signals of a full UART, through level translators can be connected to U302.
By default, P0_00 and P0_01 are assigned to UART0_TX and UART0_Rx, through jumpers on J201, pins 1-2 and J201, pins 3-4. P0_00 and P0_01 are the booting UART of the Wi-Fi subsection.
- Connecting a PC to the power measurement circuit:
 - SPI connection with ADC (U503)
 - Up to eight triggers including Software cursor triggering (TRIG_x).

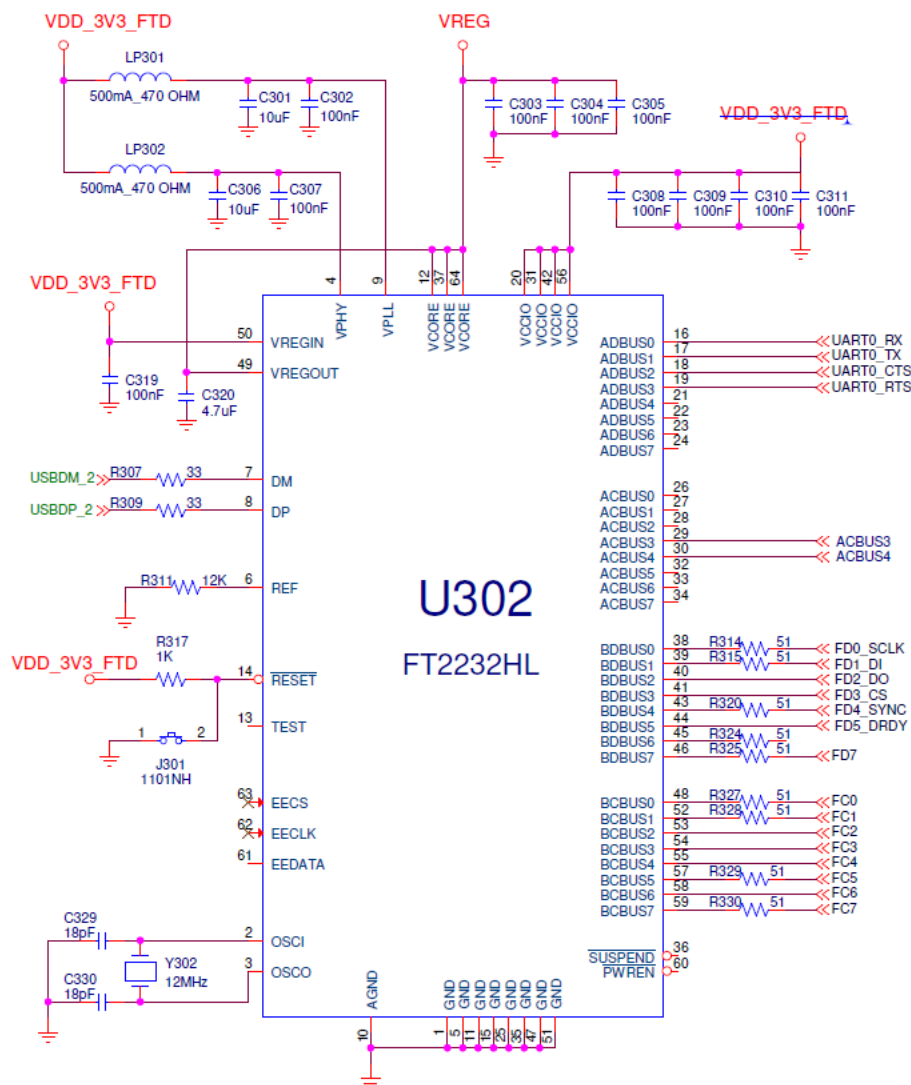


Figure 26. USB to UART circuitry

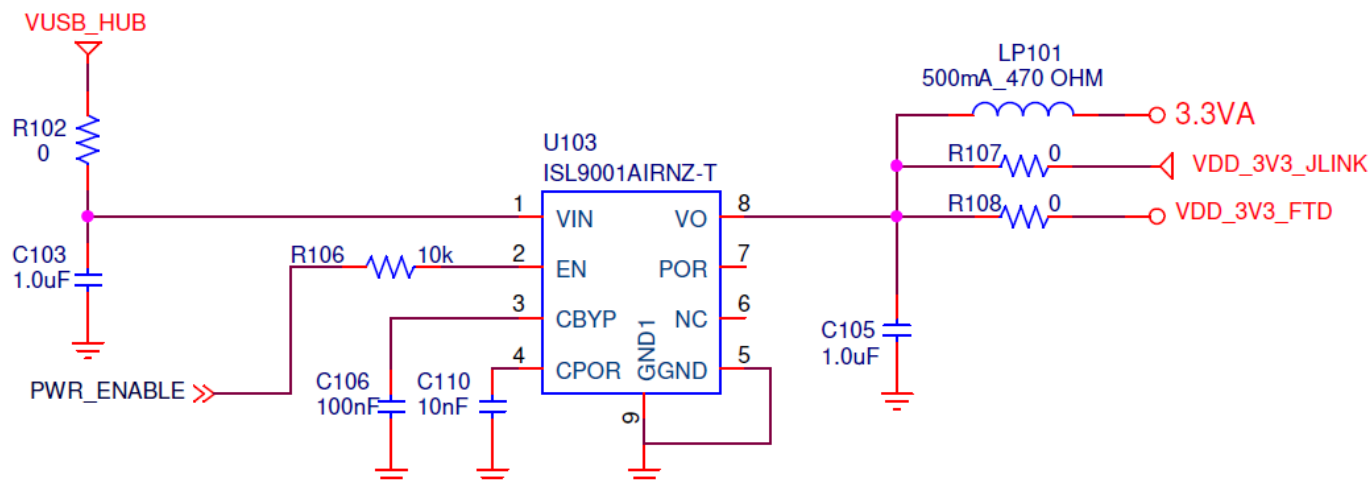


Figure 27. USB to UART power supply

5.5. USB to SWD/UART, (U401)

The USB to SWD function is implemented by U401, R7FA4M2AB3CNE. Its operation is indicated through the green LED D402 on the EK - RA6W1 Motherboard. This chip is supplied with 3.3 V from U103.

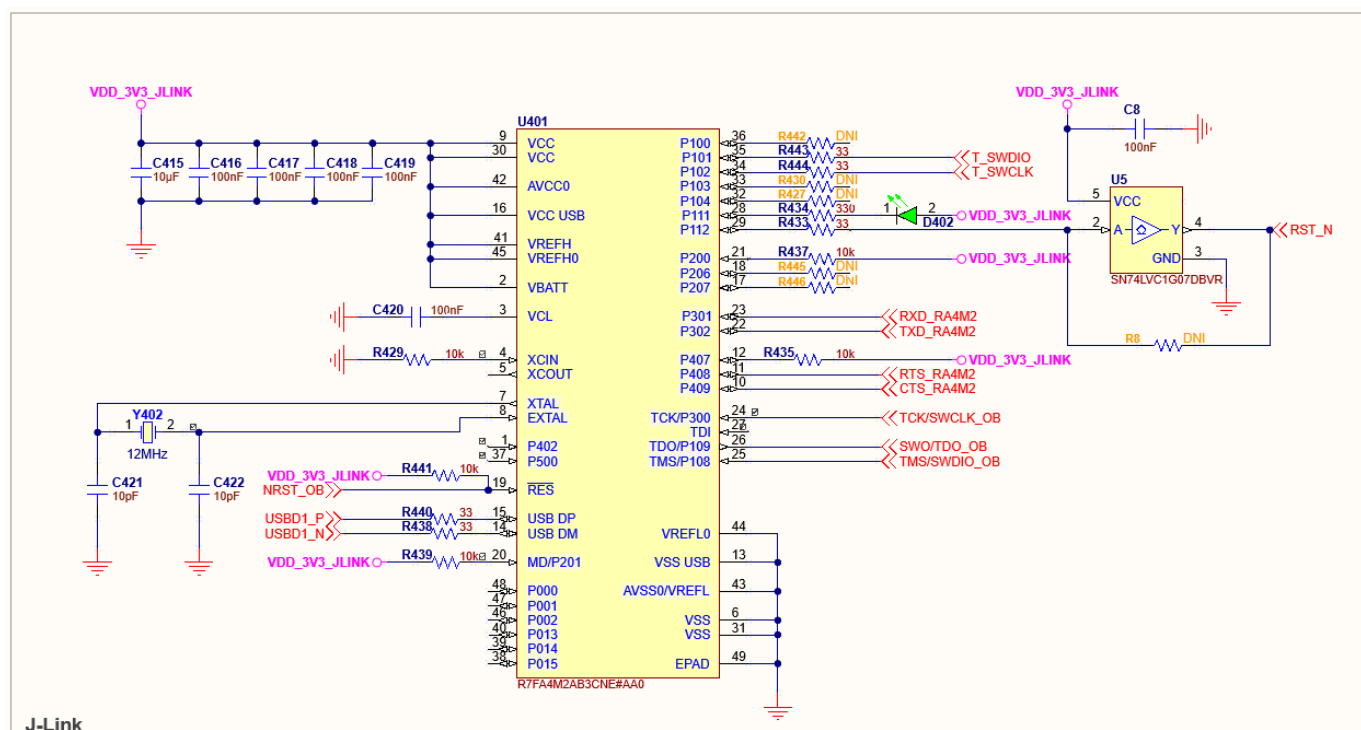


Figure 28. USB to JTAG/UART circuitry (U401) and UART header (J405)

U401 functions are the following:

- Connecting user's PC to SWD signals SWCLK, SWDIO of Wi-Fi subsection. Jumpers must be connected on J203 pins 21- 23 (C_SWCLK to SWCLK) and J203 pins 25 to 26, (C_SWDIO to SWDIO). This is the default configuration, see [Figure 29](#)
- Connecting user's PC to SWD signals SWCLK, SWDIO of Bluetooth LE subsection (available in RA6W2 and RRQ61051 Module). Jumpers must be connected on J203 pins 23- 24, (B_P0_2 SWCLK to SWCLK) and J203

pins 27 to 28, (B_P0_10_SWDIO to SWDIO). The signals on Bluetooth LE subsection must be connected to other signals.

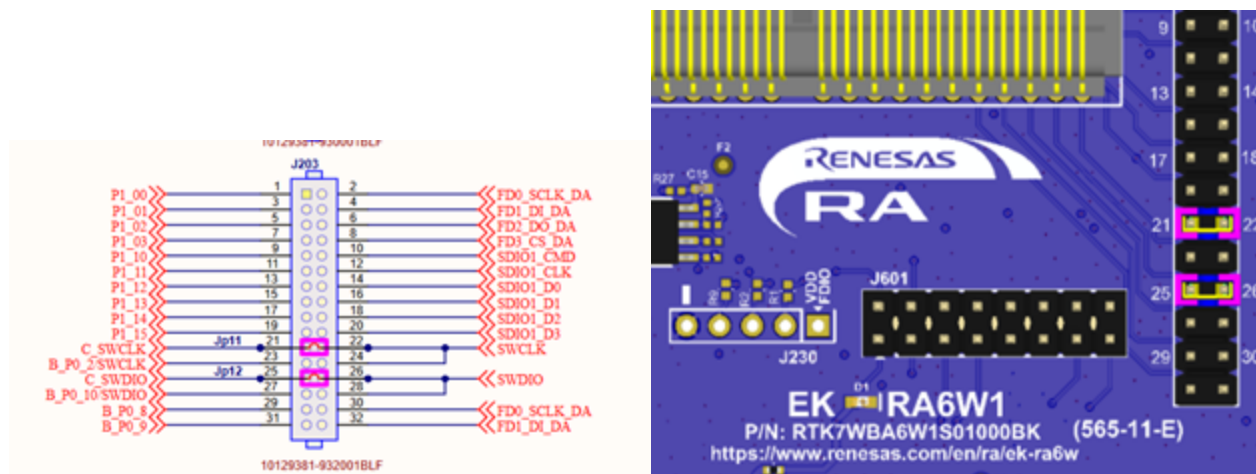


Figure 29. Default SWD connection to Wi-Fi subsection

- Connecting a PC to UART signals TXD_RA4M2, RXD_RA4M2, CTS_RA4M2, RTS_RA4M2 (J405 - Header). The UART can be utilized by using jumping wires between J405 and UART interfaces of the daughterboards.
https://kb.segger.com/Using_J-Link_VCOM_functionality#Hardware_flow_control

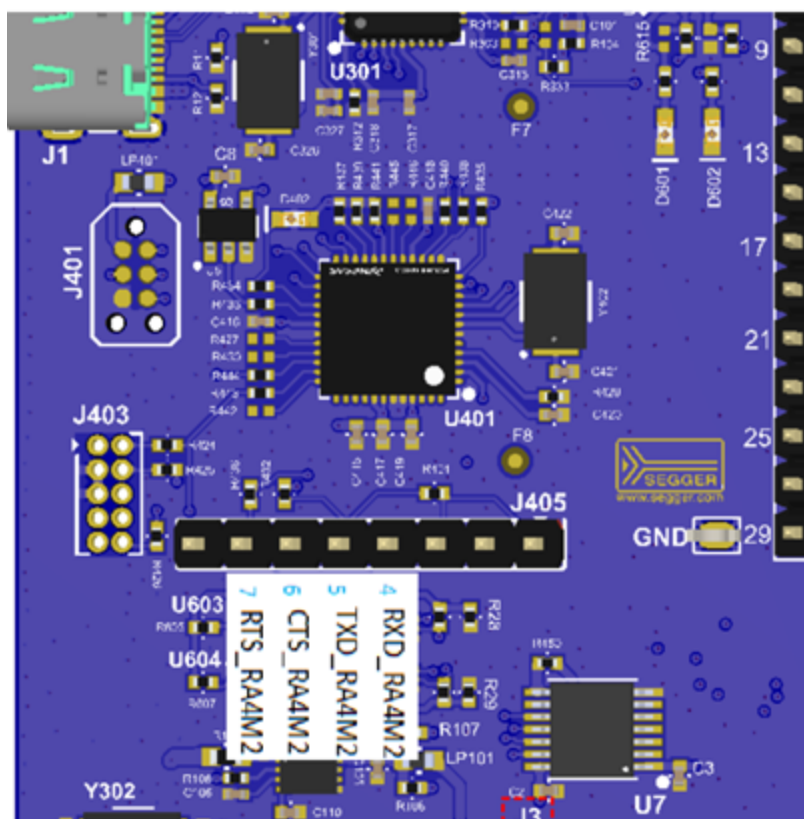


Figure 30. USB to SWD/UART circuitry – UART header, J405

NOTE

SWCLK and SWDIO signals can be accessed on J403. J403 is used for RA6W1 EK Motherboard validation during production and it must not be used in normal operation. Do not apply any external SWD signals on J403 because it causes conflict.

5.6. Level Translator

There are five Level translators on EK-RA6W1 Motherboard. They are applied on UART, SWD signals as well as the signals of interface section (PMOD, MikroBUS and Arduino). The purpose of the level translators is to match the voltage levels of the GPIOs of RA6W1/RAW2 to the ICs on Motherboard. As the GPIOs can be supplied from VDD_DIO1 and VDD_DIO2, user must select the appropriate power supply for the translators. Figure 31 shows the block diagram of the level translators, and Figure 32 shows the electrical circuits. Table 6 shows the connectivity of level translators, whereas on the electrical circuit.

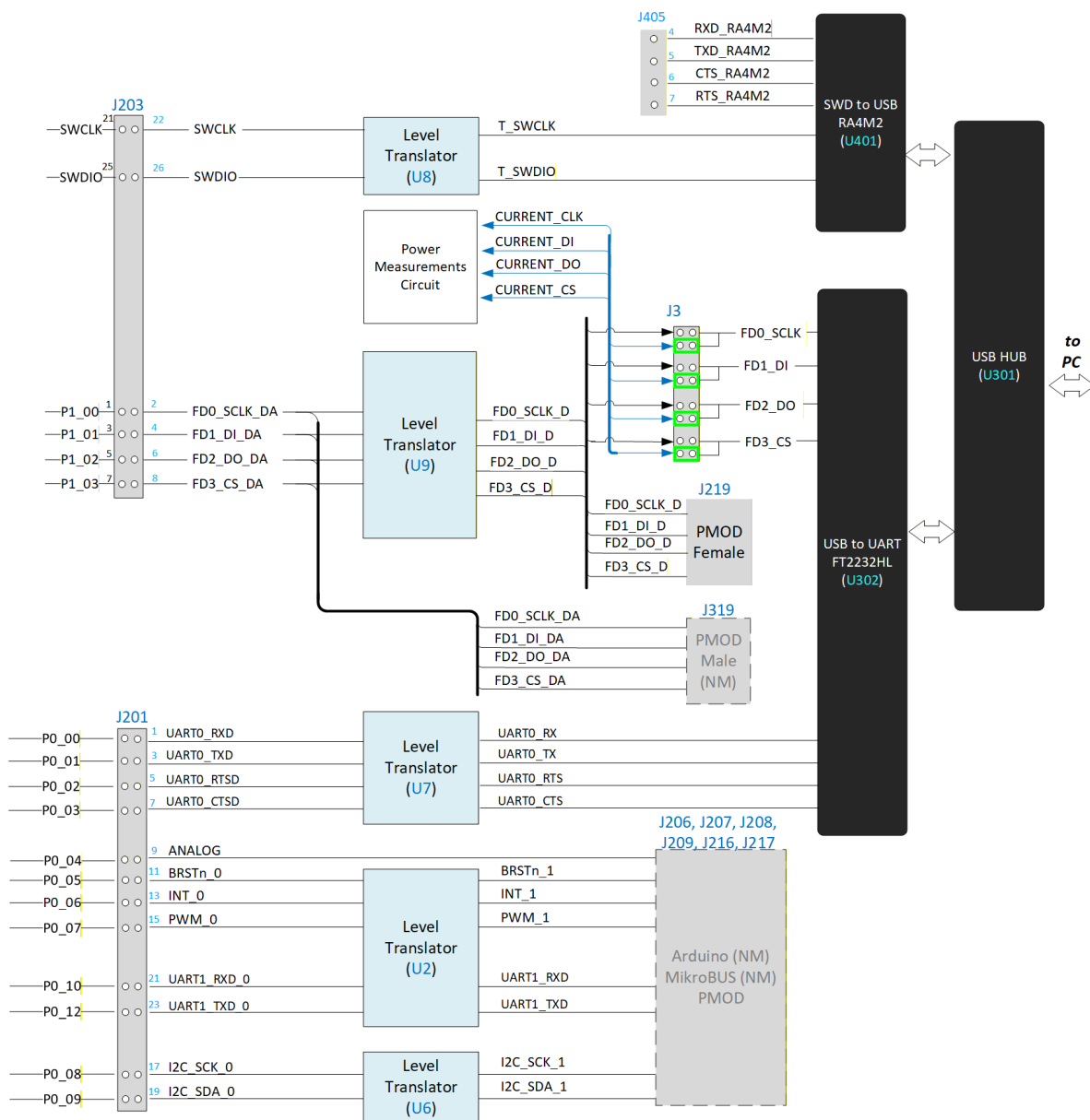


Figure 31. Level translators block diagram

Table 6. Connectivity of Level translators

Part number	Side A Evaluation daughterboard		Side B RA6W1 EK motherboard Interfaces		
	Signal	Voltage A	Signal	Voltage B	Interface
U2	INT_0	VDD_DIO1	INT_1	VDDIO_p (=3.3 V)	PMOD MikroBUS Arduino
	BRSTn_0		BRSTn		
	PWM_0		PWM_1		
	UART1_RXD_0		UART1_RXD		
	UART1_TXD_0		UART1_TXD		
U6	I2C_SCK_0	VDD_DIO1	I2C_SCK	VDDIO_p (=3.3 V)	PMOD MikroBUS Arduino
	I2C_SDA_0		I2C_SDA		
U7	UART0_RXD	VBAT_A	UART0_Rx	VDD_3V3_ FTDI	UART0
	UART0_TXD		UART0_Tx		
	UART0_CTSD		UART0_Tx		
	UART0_RTSD		UART0_Tx		
U8	SWCLK	I/O_V1.8 V (=1.8 V) or VDDIO_p (=3.3 V)	T_SWCLK	VDD_3V3_ JLINK	SWD
	SWDIO		T_SWDIO		
U9	FD0_SCLK_D	I/O_V1.8 V (=1.8 V) or VDDIO_p (=3.3 V)	FD0_SCLK_ DA	VDDIO_p (=3.3 V)	SPI
	FD1_DI_D		FD1_DI_DA		
	FD2_DO_D		FD2_DO_DA		
	FD3_CS_D		FD3_CS_DA		

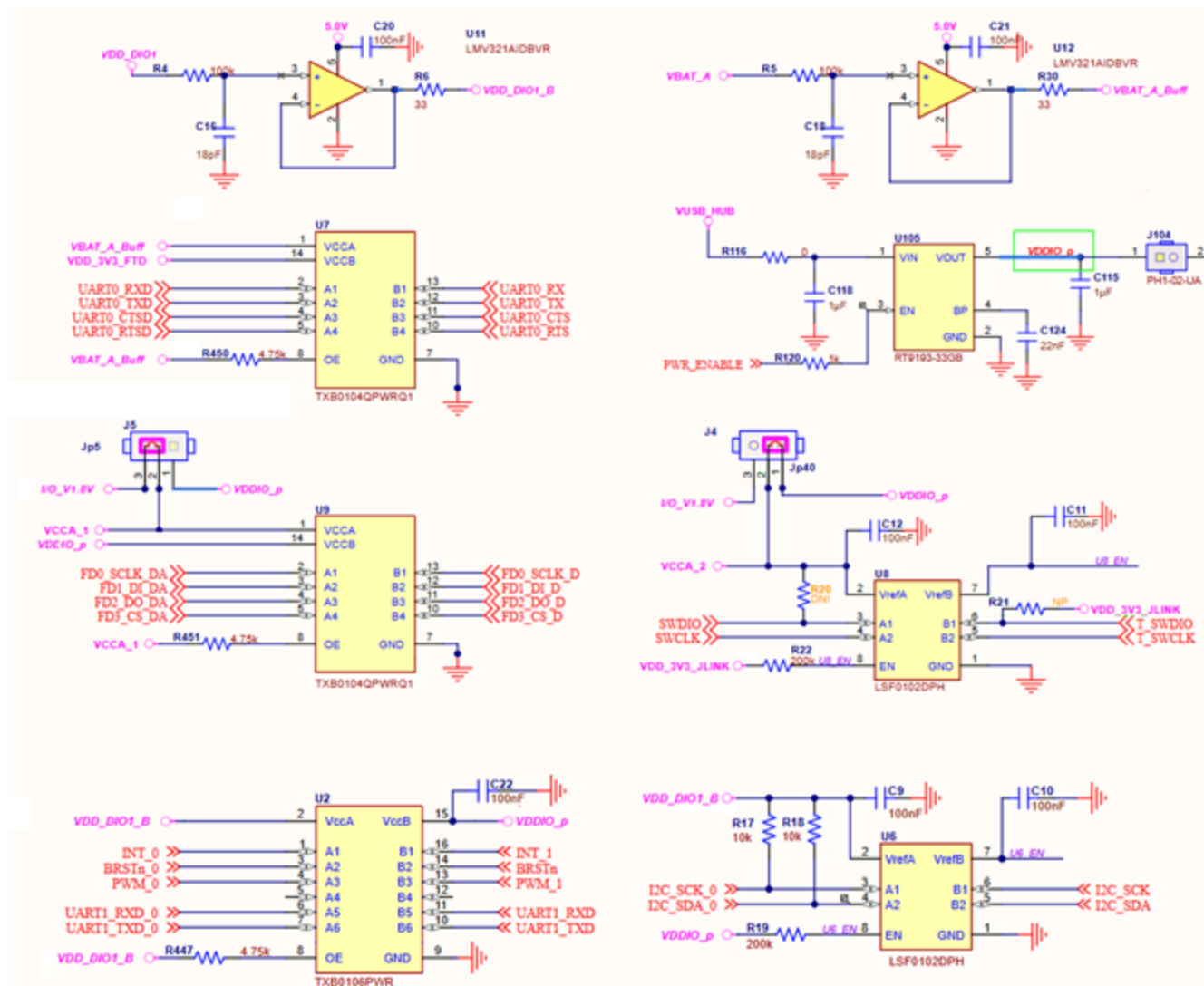


Figure 32. Voltage translator circuitry

VDDIO is a replica of VDD_DIO1/2, and it generated from an Operational amplifier (U108) configured as current buffer.

5.7. GPIOs and Breakout Headers J201/J203

All P0_x GPIOs from daughterboards are driven to the EK - RA6W1 Motherboard for monitoring on the breakout header J201/J203. The schematic of the J201/J203 is shown in Figure 33 and the position of the J201/J203 header on EK- RA6W1 Motherboard in Figure 34.

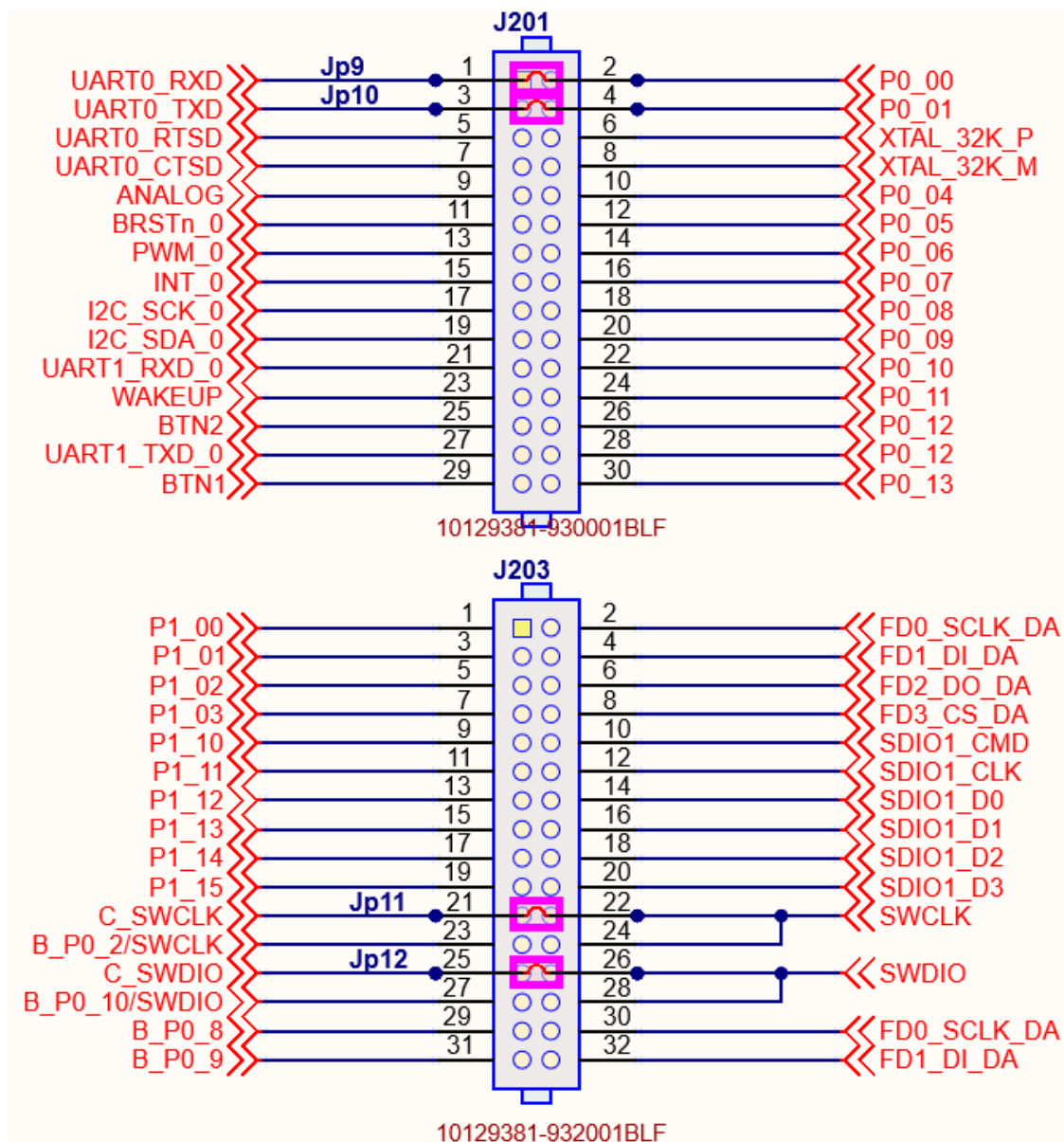


Figure 33. J201/J203 schematic

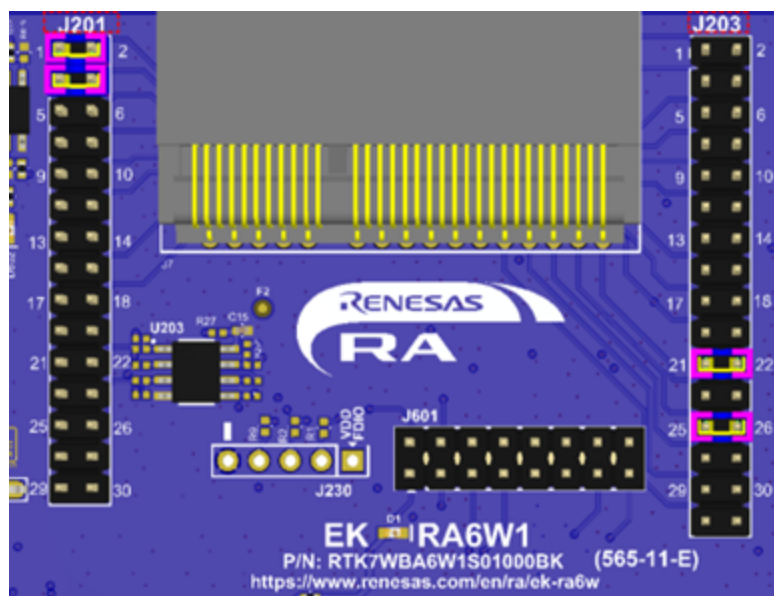


Figure 34. J201/J203 position on RA6W1 EVK Motherboard

NOTE

On break-out headers, one row is assigned to the GPIOs of the daughterboards, whereas the other row is assigned to signals of the various interfaces, which are applied on the Motherboard (SDIO, PSRAM, MikroBUS™, PMOD and so on).

For activating the interfaces, connect the signals of the two rows with a jumper. The potential signals assignments of EK - RA6W1 are shown in the following tables. More combinations can be achieved by using jumper wires.

Table 7. Signals connectivity Evaluation Kit for RA6W1, RA6W2 and RRQ610x

Names of available signals	Subsystem	Power domain	POR default	Alternative usage 1	Pins assignments on EK-RA6W1 Motherboard				
					RA6W1 daughterboard	RA6W2 daughterboard	RRQ61001-00x Mod daughterboard	RRQ61051-00x Mod daughterboard	
B_P0_00	Bluetooth LE	VBAT_B	RST		Not Available	P1_10/URX (Wi-Fi)	Not Available	P1_10/URX (Wi-Fi)	
B_P0_01	Bluetooth LE	VBAT_B	GPIO			P1_11/UTX (Wi-Fi)		P1_11/ UTX (Wi-Fi)	
B_P0_02	Bluetooth LE	VBAT_B	SWCLK			P1_14/BLE_RST		P1_14/ BLE_RST	
B_P0_03	Bluetooth LE	VBAT_B	GPIO			P1_12/UCTS (Wi-Fi)		P1_12/UCTS (Wi-Fi)	
B_P0_04	Bluetooth LE	VBAT_B	GPIO			P1_13/URTS (Wi-Fi)		P1_13/URTS (Wi-Fi)	
B_P0_05	Bluetooth LE	VBAT_B	GPIO			P1_15/Coex		P1_15/ Coex	
B_P0_06	Bluetooth LE	VBAT_B	GPIO			Not Available			GPIO
B_P0_07	Bluetooth LE	VBAT_B	GPIO						GPIO
B_P0_08	Bluetooth LE	VBAT_B	GPIO						GPIO
B_P0_09	Bluetooth LE	VBAT_B	GPIO						GPIO
B_P0_10	Bluetooth LE	VBAT_B	SWDIO						GPIO
B_P0_11	Bluetooth LE	VBAT_B	GPIO						GPIO
RST_N	Wi-Fi	VBAT_A	RST_N		RST_N	RST_N	RST_N	RST_N	
P0_00	Wi-Fi	VBAT_A	rtc_wup1		UART0_RXD	UART0_RXD	UART0_RXD	UART0_RXD	
P0_01	Wi-Fi	VBAT_A	sen_out		UART0_TXD	UART0_TXD	UART0_TXD	UART0_TXD	
P0_02	Wi-Fi	VBAT_A	xtal32k_m		UART0_RTSD	UART0_RTSD	UART0_RTSD	UART0_RTSD	
P0_03	Wi-Fi	VBAT_A	xtal32k_p		UART0_CTSD	UART0_CTSD	UART0_CTSD	UART0_CTSD	
P0_04	Wi-Fi	VDDIO_DIO1	GPIO		ANALOG	ANALOG	ANALOG	ANALOG	
P0_05	Wi-Fi	VDDIO_DIO1	GPIO		BRSTn	BRSTn	BRSTn	BRSTn	
P0_06	Wi-Fi	VDDIO_DIO1	GPIO		PWM_1	RFSW1	PWM_1	RFSW1	
P0_07	Wi-Fi	VDDIO_DIO1	GPIO		INT1	RFSW2	INT1	RFSW2	
P0_08	Wi-Fi	VDDIO_DIO1	GPIO	QSPIR_CLK	I2C_SCK	I2C_SCK	I2C_SCK	I2C_SCK	

Table 8. Signals connectivity Evaluation Kit for RA6W1, RA6W2 and RRQ610x1 (continued)

Names of available signals	Subsystem	Power domain	POR default	Alternative usage 1	Pins assignments on EK-RA6W1 Motherboard			
					RA6W1 daughterboard	RA6W2 daughterboard	RRQ61001-00x Mod daughterboard	RRQ61051-00x Mod daughterboard
P0_09	Wi-Fi	VDDIO_DIO1	GPIO	QSPIR_CS	I2C_SDA	I2C_SDA	I2C_SDA	I2C_SDA
P0_10	Wi-Fi	VDDIO_DIO1	GPIO	QSPIR_D0	BTN1	BTN1	BTN1	BTN1
P0_11	Wi-Fi		GPIO	QSPIR_D1	BTN2	BTN2	BTN2	BTN2
P0_12	Wi-Fi		GPIO	QSPIR_D2	WAKE_UP UART1_RXD	WAKE_UP UART1_RXD	WAKE_UP UART1_RXD	WAKE_UP UART1_RXD
P0_13	Wi-Fi	VDDIO_DIO1	GPIO	QSPIR_D3	UART1_TXD	UART1_TXD	UART1_TXD	UART1_TXD
P1_00	Wi-Fi	VDDIO_FDIO	GPIO		FD0_SCLK_DA	FD0_SCLK_DA	FD0_SCLK_DA	FD0_SCLK_DA
P1_01	Wi-Fi	VDDIO_FDIO	GPIO		FD1_DI_DA	FD1_DI_DA	FD1_DI_DA	FD1_DI_DA
P1_02	Wi-Fi	VDDIO_FDIO	GPIO		FD2_DO_DA	FD2_DO_DA	FD2_DO_DA	FD2_DO_DA
P1_03	Wi-Fi	VDDIO_FDIO	GPIO		FD3_CS_DA	FD3_CS_DA	FD3_CS_DA	FD3_CS_DA
P1_04	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_D0	OQSPI_D0	Connections applied internally to Module. Not Available on Motherboard.	Connections applied internally to Module. Not Available on Motherboard.
P1_05	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_D1	OQSPI_D1		
P1_06	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_D2	OQSPI_D2		
P1_07	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_D3	OQSPI_D3		
P1_08	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_CLK	OQSPI_CLK		
P1_09	Wi-Fi	VDDIO_FDIO	GPIO		OQSPI_CS	OQSPI_CS		
P1_10	Wi-Fi	VDDIO_DIO2	GPIO		SDIO1_CMD	B_P0_00/UTX (Bluetooth LE)	SDIO1_CMD	B_P0_00/UTX (Bluetooth LE)
P1_11	Wi-Fi	VDDIO_DIO2	GPIO		SDIO1_CLK	B_P0_01/URX (Bluetooth LE)	SDIO1_CLK	B_P0_01/URX (Bluetooth LE)
P1_12	Wi-Fi	VDDIO_DIO2	GPIO		SDIO1_D0	B_P0_03/URTS (Bluetooth LE)	SDIO1_D0	B_P0_03/URTS (Bluetooth LE)
P1_13	Wi-Fi	VDDIO_DIO2	GPIO		SDIO1_D1	B_P0_04/UCTS (Bluetooth LE)	SDIO1_D1	B_P0_04/UCTS (Bluetooth LE)
P1_14	Wi-Fi	VDDIO_DIO2	GPIO		SDIO1_D2	B_P0_02/BLE_RST	SDIO1_D2	B_P0_02/BLE_RST
P1_15	Wi-Fi	VDDIO_	GPIO		SDIO1_D3	B_P0_05/Coex	SDIO1_D3	B_P0_05/Coex

Names of available signals	Subsystem	Power domain	POR default	Alternative usage 1	Pins assignments on EK-RA6W1 Motherboard			
					RA6W1 daughterboard	RA6W2 daughterboard	RRQ61001-00x Mod daughterboard	RRQ61051-00x Mod daughterboard
		DIO2						
P1_16	Wi-Fi	VDDIO_DIO2	SWCLK		SWCLK	SWCLK	SWCLK	SWCLK
P1_17	Wi-Fi	VDDIO_DIO2	SWDIO		SWDIO	SWDIO	SWDIO	SWDIO

5.7.1. Enable UART for Wi-Fi

You must use jumpers between P0_00 and P0_01 to UART0_RXD and UART0_TXD respectively.

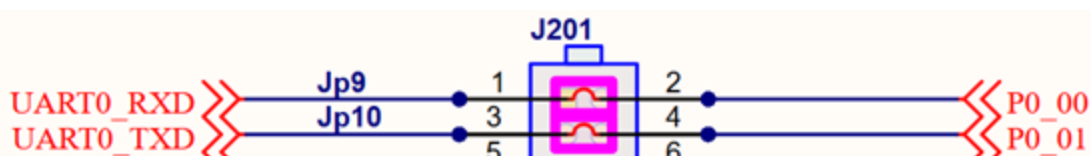


Figure 35. Enabling UART0 on motherboard

5.7.2. Enable SWD

You must use jumpers between SWCLK and T_SWCLK as well as SWDIO and T_SWCLK on J203 for Wi-Fi.

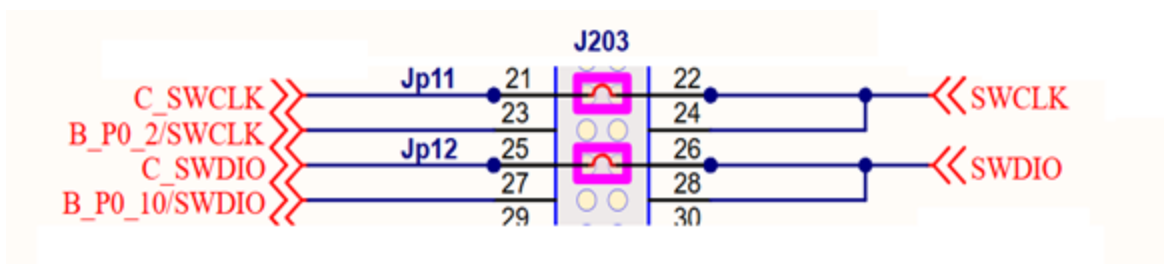


Figure 36. Enabling SWD for Wi-Fi (jumper settings on J203)

For Bluetooth LE, jumpers must be applied between B_P0_2/SWCLK and T_SWCLK as well as between B_P0_10/SWCLK and T_SWCLK.

Only one SWD interface can be enabled at a time, either Wi-Fi or Bluetooth LE.

5.8. Push-buttons

There are four push-buttons available on the EK - RA6W1 Motherboard: the J607, J608, J609 and J610. J607 is assigned to RST_N and J608 to WAKEUP, J609/J610 are reserved to BTN1 and BTN2.

By default, the jumpers on J210 are mounted. The circuit schematic is shown in [Figure 37](#), the position of the push-buttons in [Figure 38](#), and the position of the J210 header in [Figure 39](#).

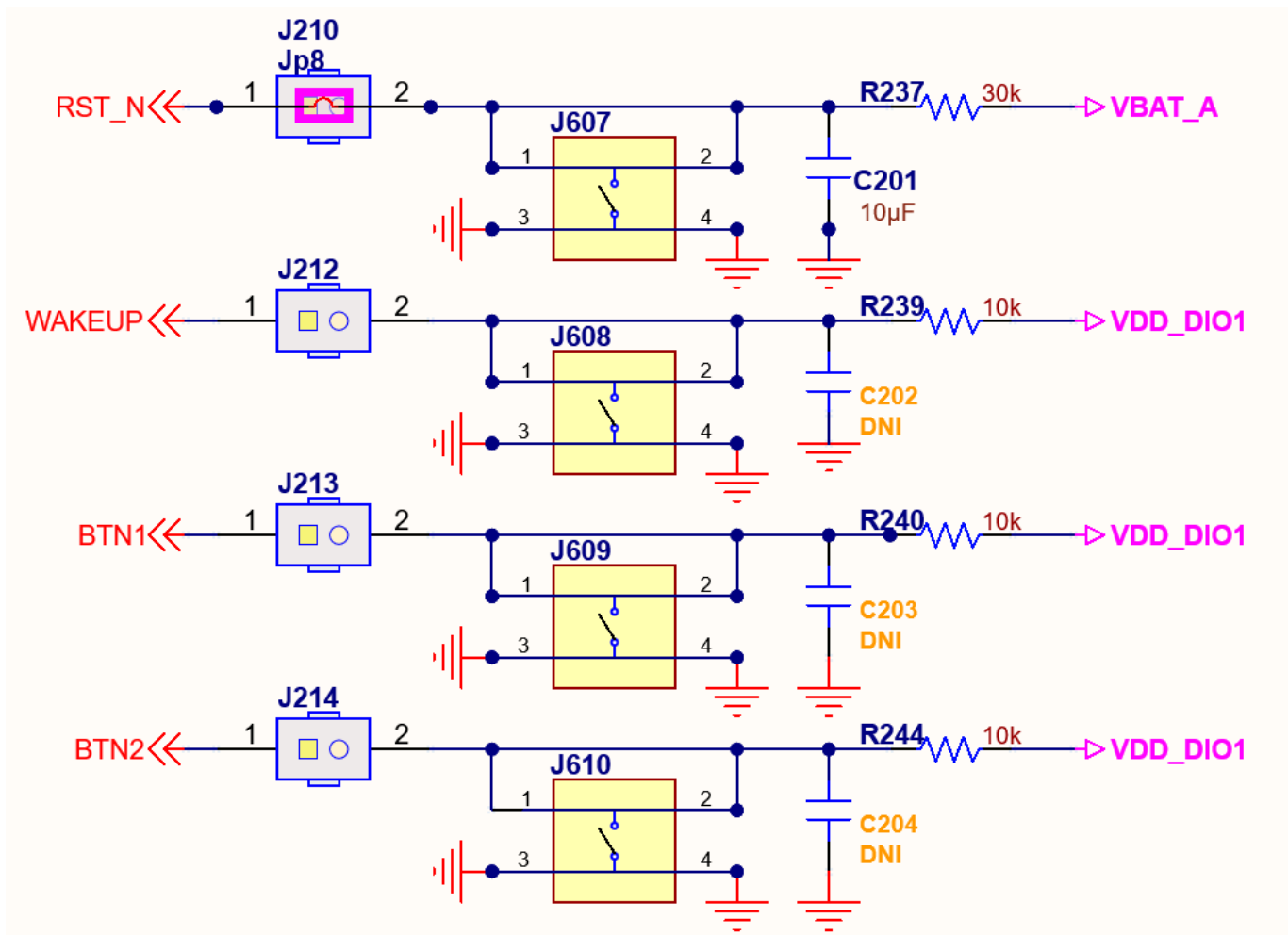


Figure 37. Push-buttons J607/J608/J609/J610

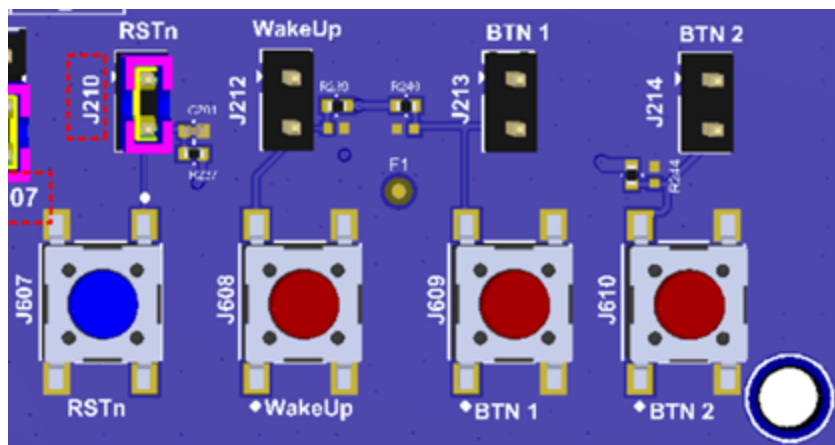


Figure 38. Push-buttons position on the EK - RA6W1 Motherboard

5.9. PSRAM Memory

In EK - RA6W1 Motherboard, a QSPI PSRAM (U203) option is available, not enabled by default. U203, is the APS6404L-SQRH-SNL, a 1.8 V, 64 Mbits PSRAM memory, connected to P0_09 to P0_13, (Wi-Fi subsystem), which is available to all daughterboards.

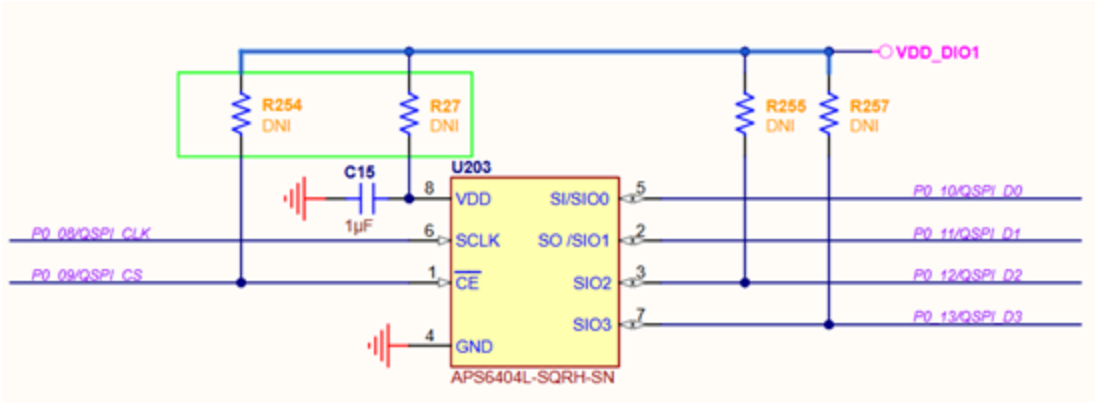


Figure 39. QSPI NOR Flash place holder on EK - RA6W1 Motherboard

For enabling QSPI NOR Flash (U202), modify the hardware setup of both motherboard and daughterboard,for details, see [Table 9](#).

Table 9. Hardware modifications for enabling QSPI Flash (U202) on Motherboard

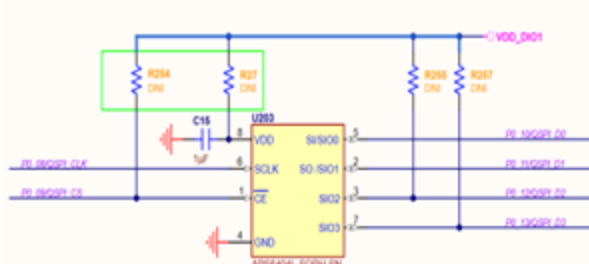
Development board	Modifications	Schematic
EK - RA6W1 Motherboard (565-11-x)	Mount R27 = 0 (0402) Mount R254 =10K (0402) Mount R247, R248, R249, R250, R256 and R258 with a 0 Ohm Resistor (package 0402)	 Figure 40. EK - RA6W1 Motherboard (565-11-x)  Figure 41. The connectivity to PSRAM



Figure 42. QSPI PSRAM (U203) on EK - RA6W1 Motherboard

5.10. SDIO Interface

RA6W1 SoC and RA6W2 SiP provide SDIO interface (two alternative pin assignments, P0_08 to P0_13 and P1_10 to P1_15). On RA6W1 EVK Motherboard, J220 is the header (not mounted) for SDIO1. SDIO1 is available on RA6W1 and RRQ61001 Module daughterboards. For daughterboards of RA6W2 and RRQ61051 Module, pins assignment of P1_10 to P1_15 is not available, as these pins are used for the Wi-Fi to Bluetooth LE communication.

You can activate the SDIO interface by hardware modifications described in [Table 10](#).

Table 10. SDIO pin configuration

Signal	Pin assignment alternative 1	Pin assignment alternative 2	Description
SDIO_CMD	P1_10	P0_09	Command line
SDIO_CLK	P1_11	P0_08	Input serial clock
SDIO_D0	P1_12	P0_10	Bi-directional data line
SDIO_D1	P1_13	P0_11	Bi-directional data line
SDIO_D2	P1_14	P0_12	Bi-directional data line
SDIO_D3	P1_15	P0_13	Bi-directional data line

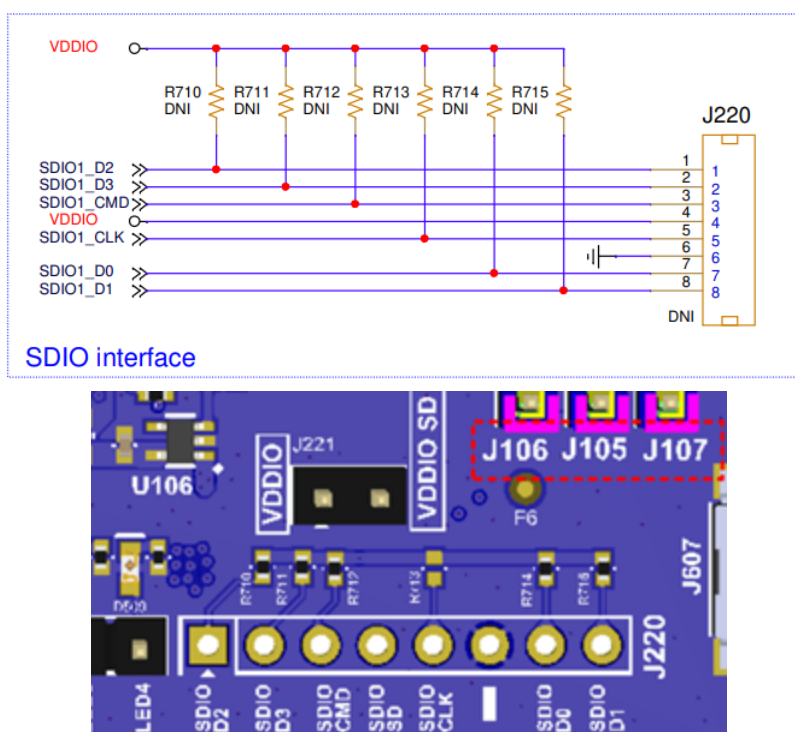


Figure 43. SDIO interface

SDIO connection between RA6W1, RA6W2 or RRQ610x1 EKs and an external MPU or MCU is implemented through E-R6W1 Motherboard and jumper wires, see [Figure 44](#).

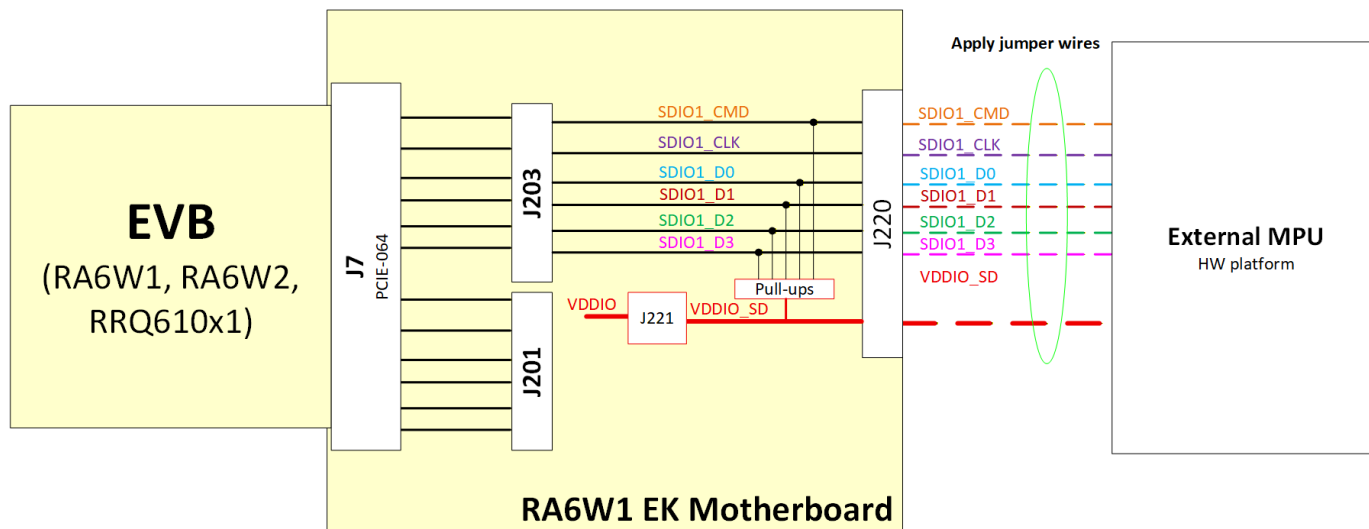


Figure 44. SDIO connection to an external MPU/MCU hardware platform

5.10.1. Configure SDIO

5.10.1.1. Enable GPIOs P1_10 to P1_15 for SDIO bus on EK-RA6W1

Mount jumpers on J203 as below:

- J203: 9- 10
- J203: 11- 12
- J203: 13- 14
- J203: 15- 16
- J203: 17- 18
- J203: 19- 20
- J220 must be mounted. Use a 1x8 Single row Male header, 2.54 mm.
- J221: see VDDIO_SD power setting below

NOTE

Software modifications are also required.

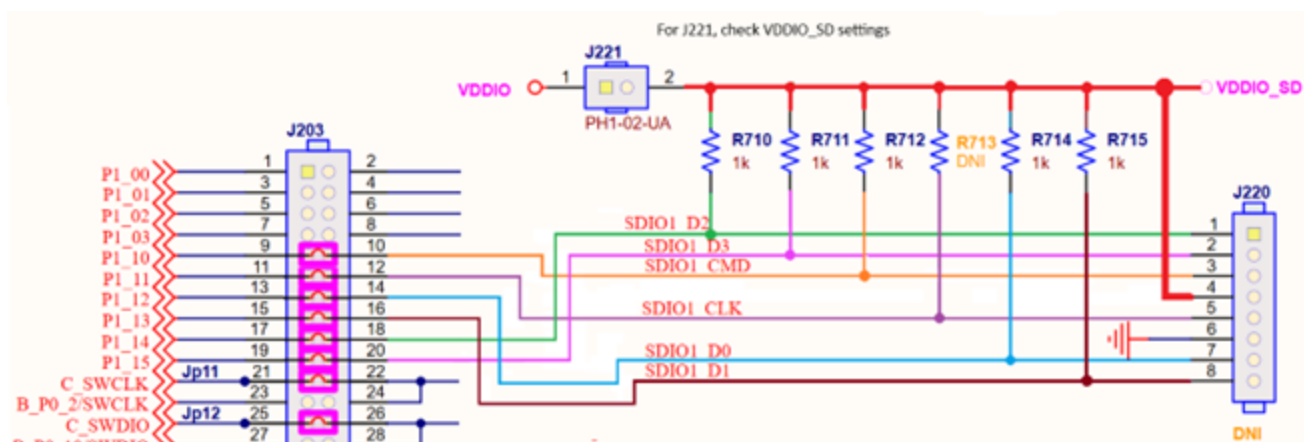


Figure 45. P1_10 to P1_15 assignment to SDIO

5.10.1.2. Enable GPIOs P0_8 to P0_13 for SDIO bus on EK-RA6W1

Use the following jumper wires between J201 and J2:

- J203:10 to J201:20
- J203:12 to J201:18

- J203:14 to J201:22
- J203:16 to J201:24
- J203:18 to J201:26
- J203:20 to J201:30
- J220 must be mounted. Use a 1x8 Single row Male header, 2.54 mm.
- J221: see VDDIO_SD power setting below

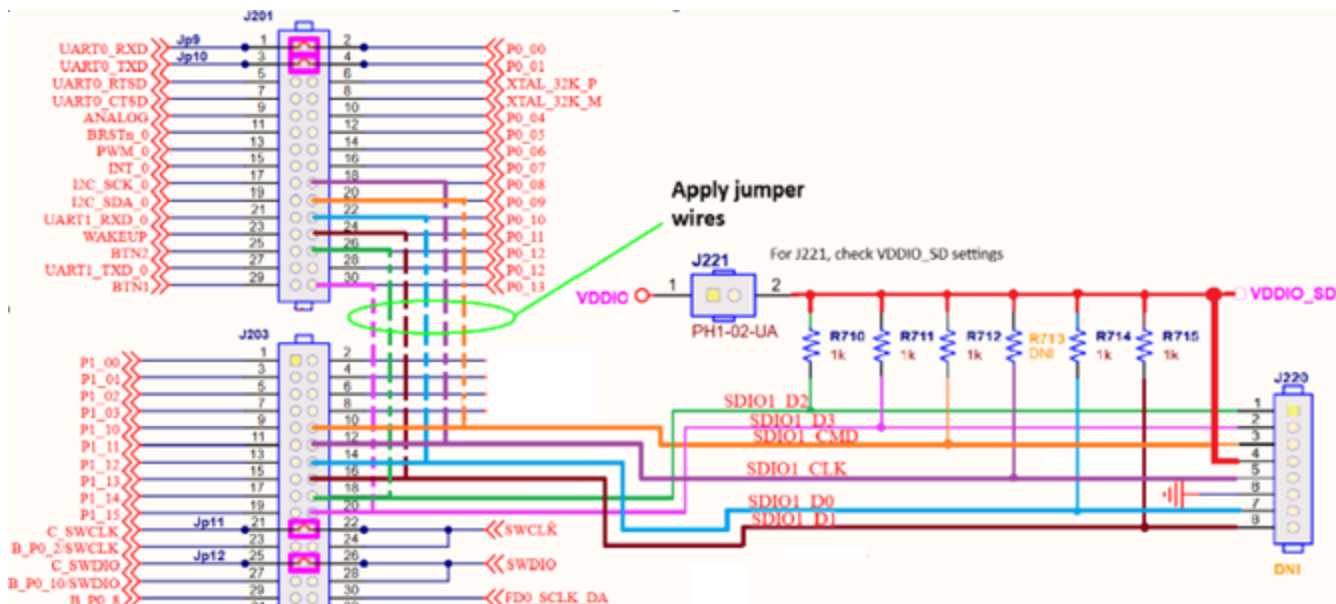


Figure 46. P0_8 to P0_13 for SDIO bus on EK-RA6W1

5.10.1.3. VDD_SDIO Power Setting

SDIO operation is not feasible without enabling the pull-ups for the data and command lines.

As pull-ups are already placed on the EK-RA6W1 Motherboard, you must only enable VDD_SDIO voltage rail. There are two cases, supplying VDD_SDIO from either the external MCU/MPC hardware platform or from the voltage generated on EK-RA6W1 Motherboard.

SDIO signals use same voltage range on both sides (EK-RA6W1 and external MCU/MPU hardware platform).

- Case 1: Supplying SDIO pull-ups from External MCU/MPU hardware platform
 - Connect VDDIO_SD to voltage pin (3.3 V) of external MPU/MCU platform through jumper wire
 - Do not apply jumper on J221

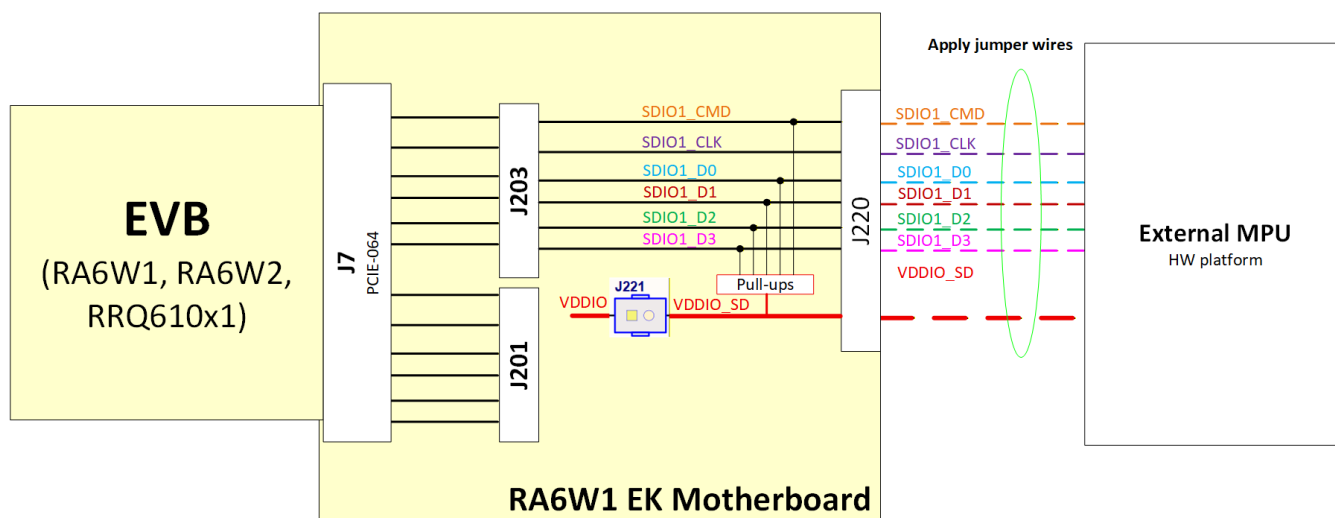


Figure 47. Supply SDIO pull-ups from external MCU/MPU hardware platform

- Case 2: Supplying SDIO pull-up from EK-RA6W1 Motherboard:
 - Do not connect VDDIO_SD to voltage pin (3.3 V) of external MPU/MCU platform through jumper wire
 - Apply jumper on J221
 - VDDIO = 3.3 V

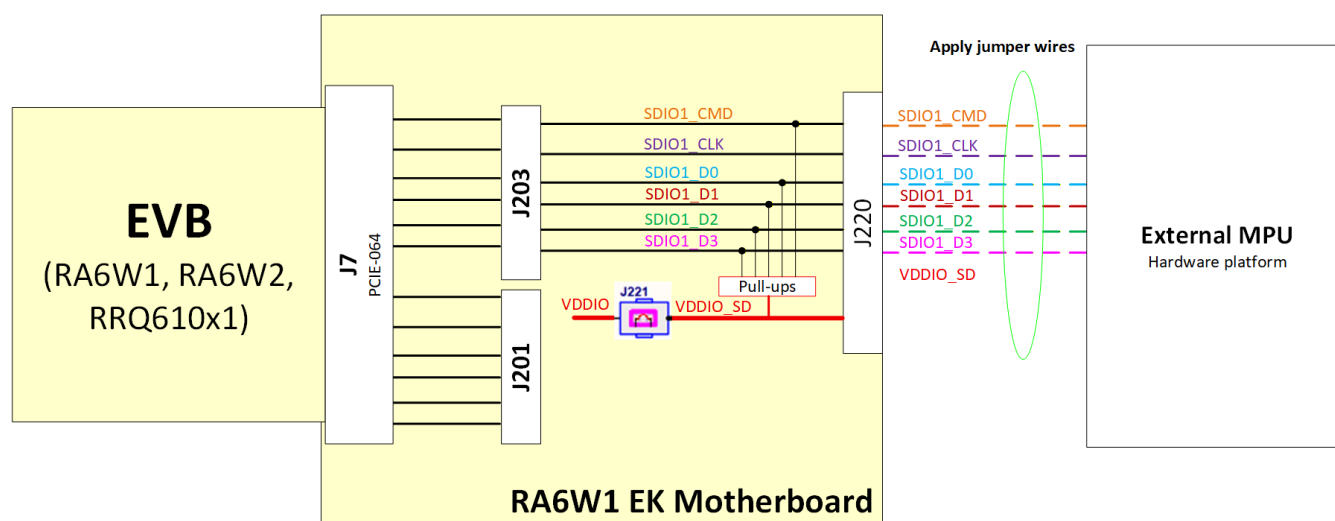


Figure 48. Supplying SDIO pull-up from EK-RA6W1 motherboard

5.11. MikroBUS™ Interface

RA6W1 Motherboard can support one MikroBUS™ module. The available slot is compatible with MikroBUS™ standard click boards for additional expandability requirements. Two female headers (8 position 0.100", through hole, socket type) are mounted (by default) on J208 and J209. The schematic circuit is shown in [Figure 49](#) and the position of the MikroBUS™ slot in [Figure 50](#).

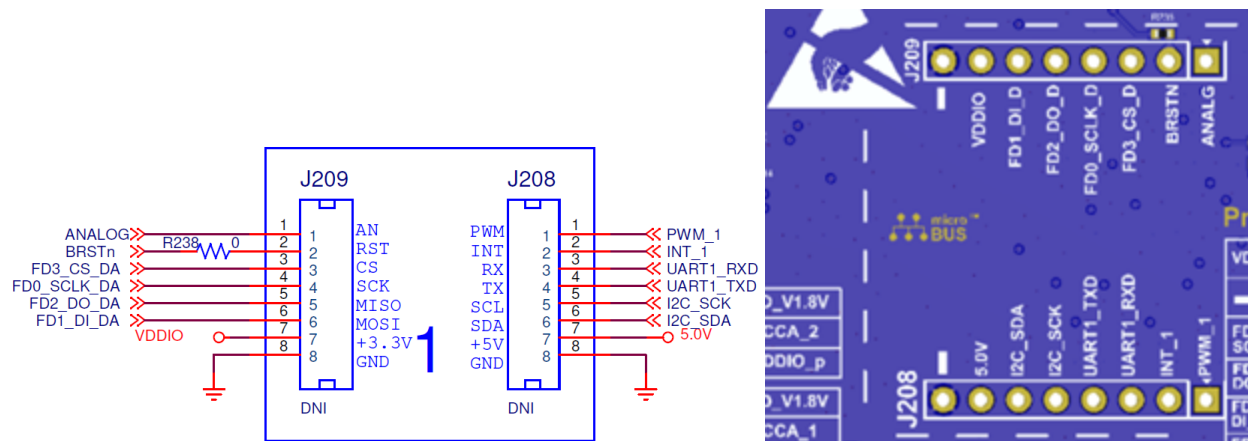


Figure 49. MikroBUS™ slot circuitry

To activate MikroBUS™, connect the appropriate signals to GPIOs of daughterboard on headers J201 and/or J203.

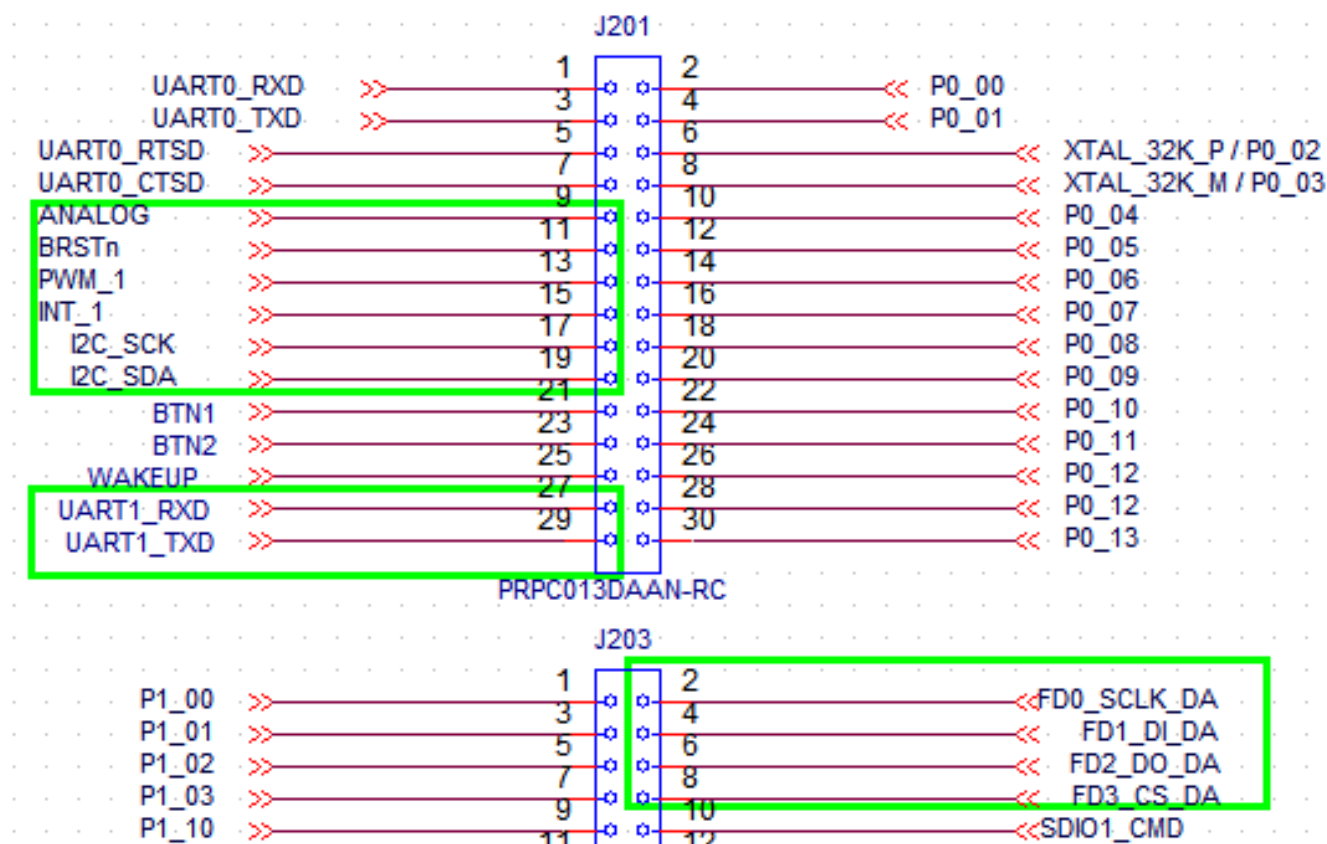


Figure 50. How to enable MikroBUS™ signals on breakout headers J201/J203

5.12. PMOD Interface

EK - RA6W1 Motherboard can support one PMOD module. The female header (J219) is mounted (by default). The schematic circuit is shown in Figure 51.

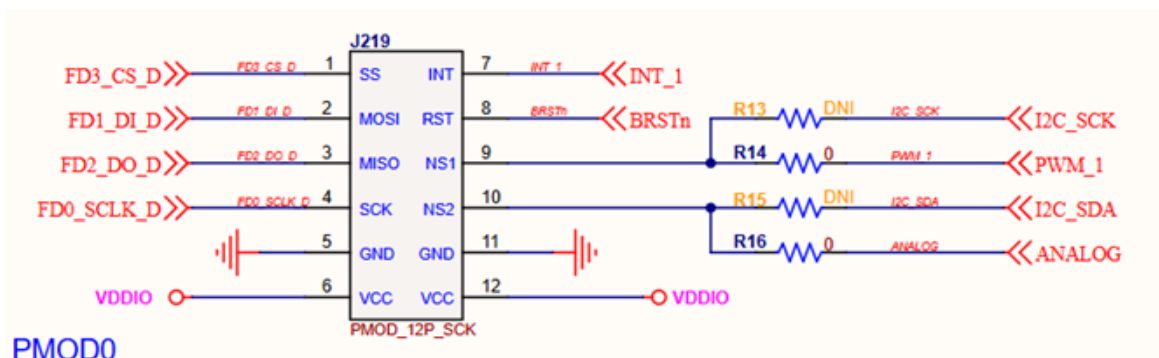


Figure 51. PMOD female connector (mounted) slot circuitry

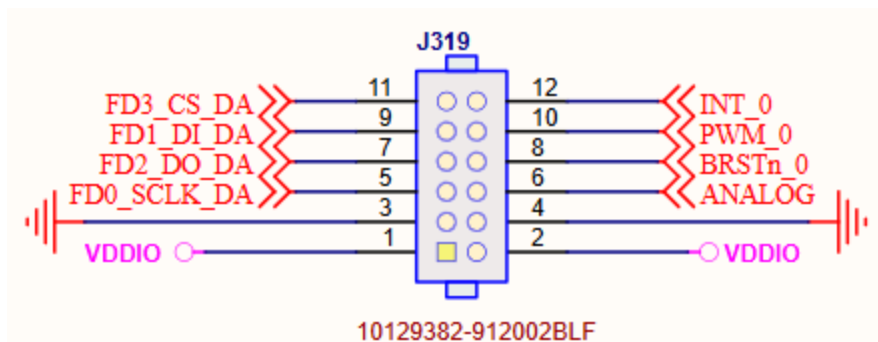


Figure 52. PMOD male connector (not mounted)

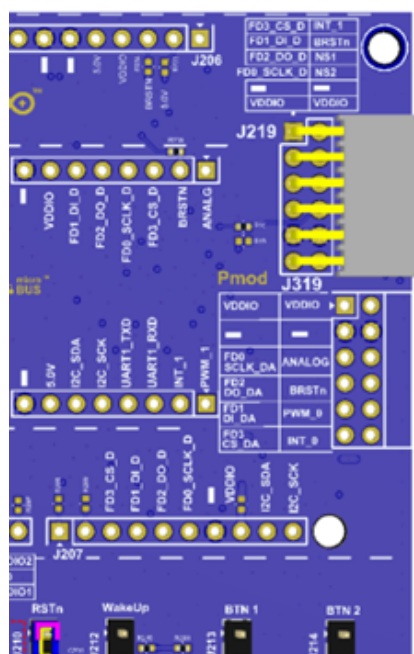


Figure 53. PMOD position on the EK-RA6W1 motherboard

On the breakout header J201/J203 of the EK - RA6W1 Motherboard, you must make the connections between daughterboard GPIOs and the MikroBUS™ or PMOD interface.

5.13. Wake-up

Wake-up function is applied to the Wi-Fi, and it is available in all daughterboards (RA6W1, RA6W2, and RRQ610x1). GPIOs which can be assigned to Wake-up are shown in [Table 11](#).

Table 11. GPIOs that can be used as Wake-up

Pin	Support wake-up	Retention group	Power domain	Header
P0_00	yes	VBAT	VBAT	J201. Pin 2
P0_04	ana wake	DIO1_1	VDDIO_DIO1	
P0_05	ana wake	DIO1_1	VDDIO_DIO1	
P0_06	ana wake	DIO1_1	VDDIO_DIO1	
P0_07	ana wake	DIO1_1	VDDIO_DIO1	
P0_08	yes	DIO1_2	VDDIO_DIO1	J201. Pin 18
P0_09	yes	DIO1_2	VDDIO_DIO1	J201. Pin 20
P0_10	yes	DIO1_2	VDDIO_DIO1	J201. Pin 22
P0_11	yes	DIO1_2	VDDIO_DIO1	J201. Pin 24
P0_12	yes	DIO1_2	VDDIO_DIO1	J201. Pins 26 and 28
P0_13	yes	DIO1_2	VDDIO_DIO1	J201. Pin 30
P1_10	yes	DIO2	VDDIO_DIO2	J203. Pin 9
P1_11	yes	DIO2	VDDIO_DIO2	J203. Pin 11
P1_12	yes	DIO2	VDDIO_DIO2	J203. Pin 13
P1_13	yes	DIO2	VDDIO_DIO2	J203. Pin 15

On RA6W1 Motherboard, wake-up function can be assigned to P0_12 by adding a jumper between pins J201:25 (Wake-up) and J201:26 (P0_12) or any other available pin using a jumping wire.

Wake-up is active high, and it is manually enabled by pressing push-button J608, [Figure 54](#).

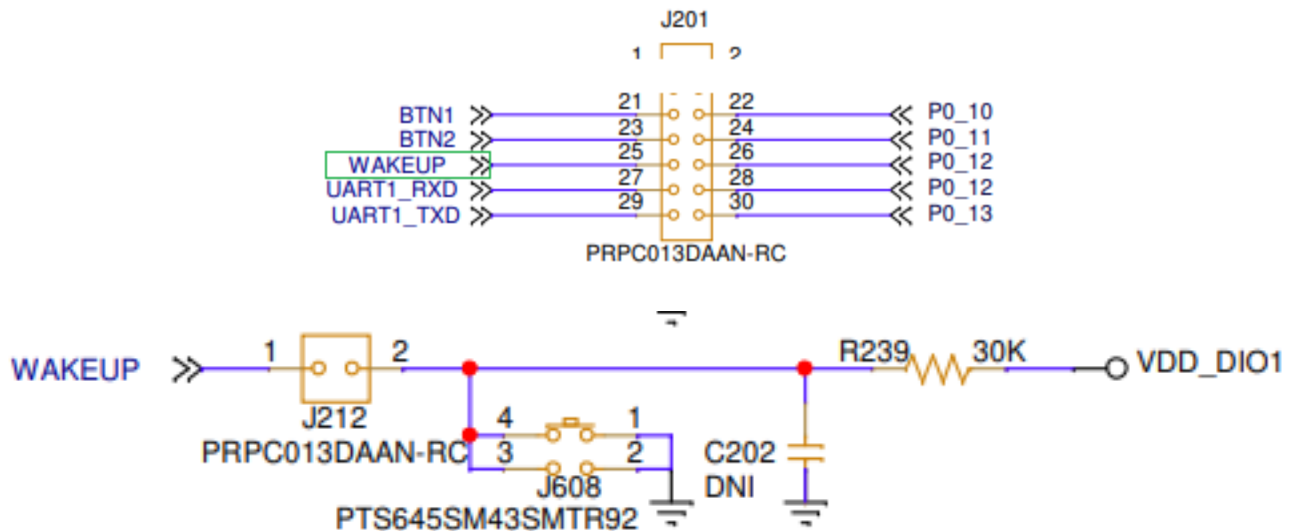


Figure 54. Wake-up function on EK - RA6W1 Motherboard

5.14. LEDs

Four General purpose LEDs are available on EK-RA6W1 Motherboard. They are connected to header J611, and they are Green LEDs, with 2.1 V voltage drop. Each Led is connected through 1 k Ω resistor to GND and for enabling it, a jump wire must be applied on J611 pin, see [Figure 55](#).



Figure 55. LEDs interface, circuit (left) and PCB locationing

6. RTK7WBA6W1S02000BK-RA6W1 QFN Evaluation Daughterboard (565-09-x)

RA6W1 SoC (U101): the RA6W1 is a highly integrated ultra-low power Wi-Fi system on a chip (SoC) integrating an Arm® Cortex®-M33 system processor with a dual band 802.11a/b/g/n/ax Wi-Fi subsystem, on-chip memory, flexible peripheral interfaces, and power management features.

On RA6W1 daughterboard with board number 565-09-x, the WLCSP package of RA6W1 is applied as well as all necessary components required for the system setup. The daughterboard, accompanied by the Motherboard, provides the capabilities for RA6W1 system evaluation and development.

The block diagram and the actual component locations of the RA6W1 Daughterboard are shown in [Figure 56](#) and [Figure 57](#).

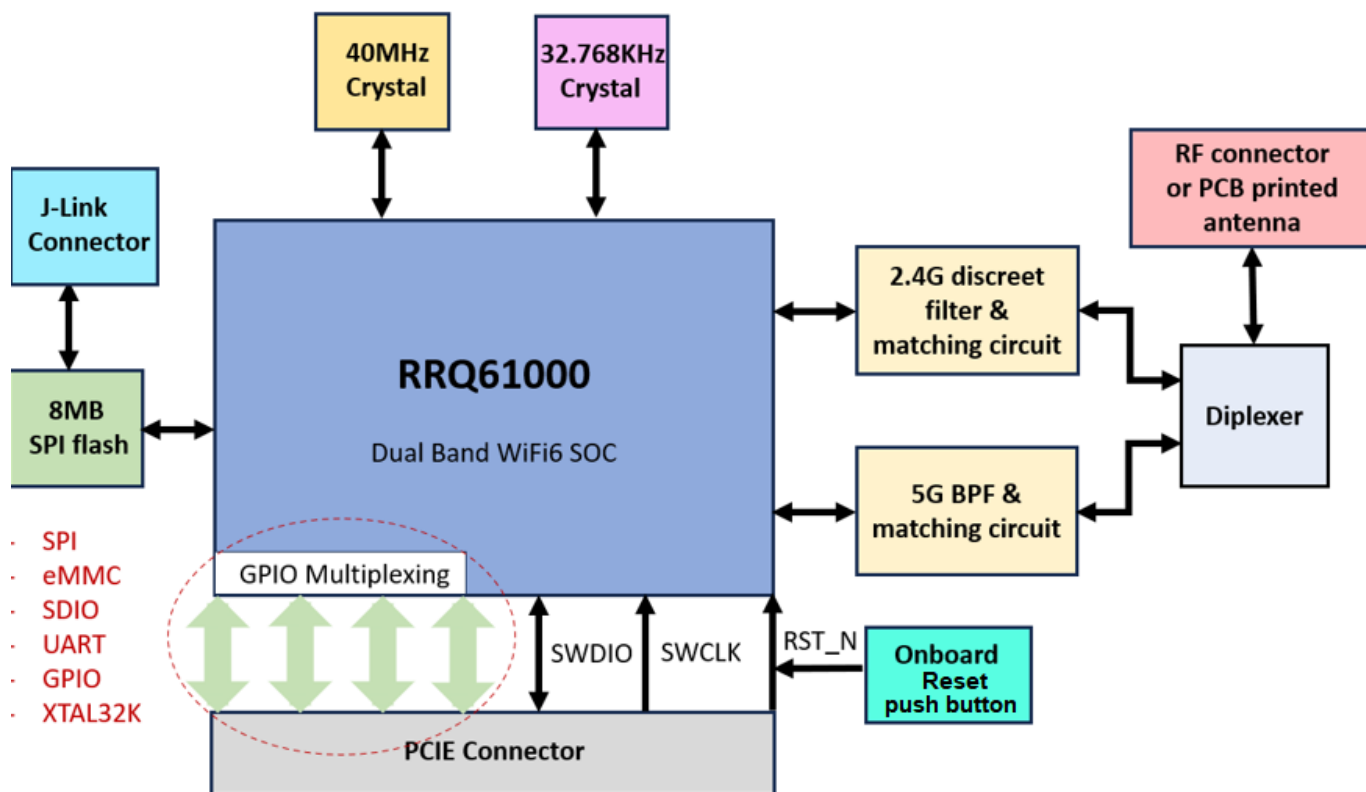


Figure 56. System block diagram of RA6W1 Daughterboard

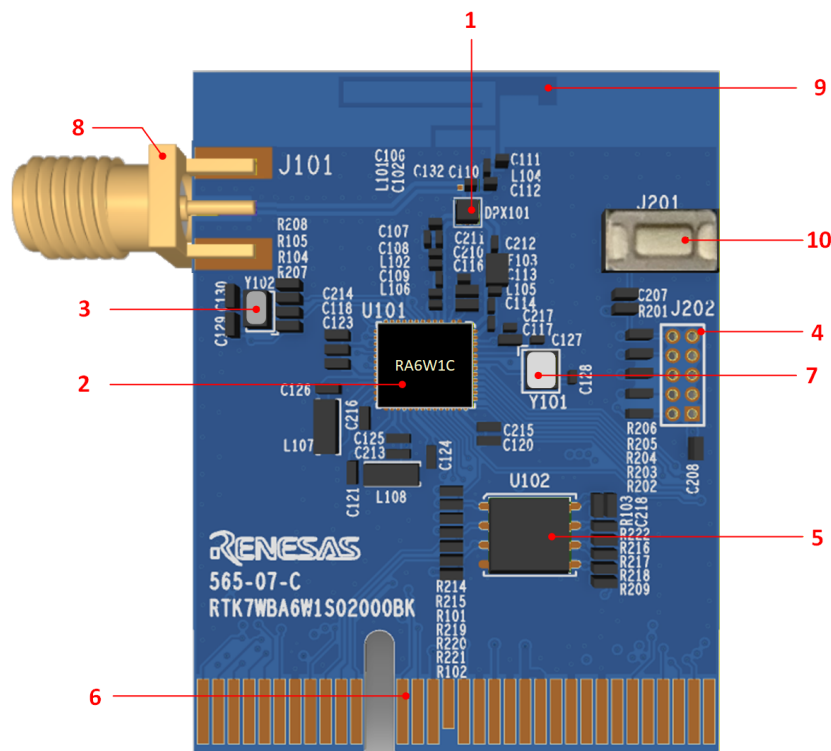


Figure 57. RA6W1 Daughterboard component's placement

Table 12. RA6W1 daughterboard part numbers and description

No	Name	Location
1	Antenna selection network	
2	RA6W1 SoC	U101
3	32.768 kHz XTAL	Y102
4	J-Link connector for QSPI NOR Flash programming	J202
5	QSPI NOR Flash	U102
6	PCIE Interface Connector with RA6W1	
7	40 MHz XTAL	Y101
8	SMA RF Connector	J101
9	PCB Printed Antenna	
10	Onboard reset button	J201

6.1. RA6W1 GPIOs and Interface to Motherboard

RA6W1 SoC provides 26 GPIOs (including SWD signals). All GPIOs are available to Motherboard through PCIE-64, PCB connector (U202).

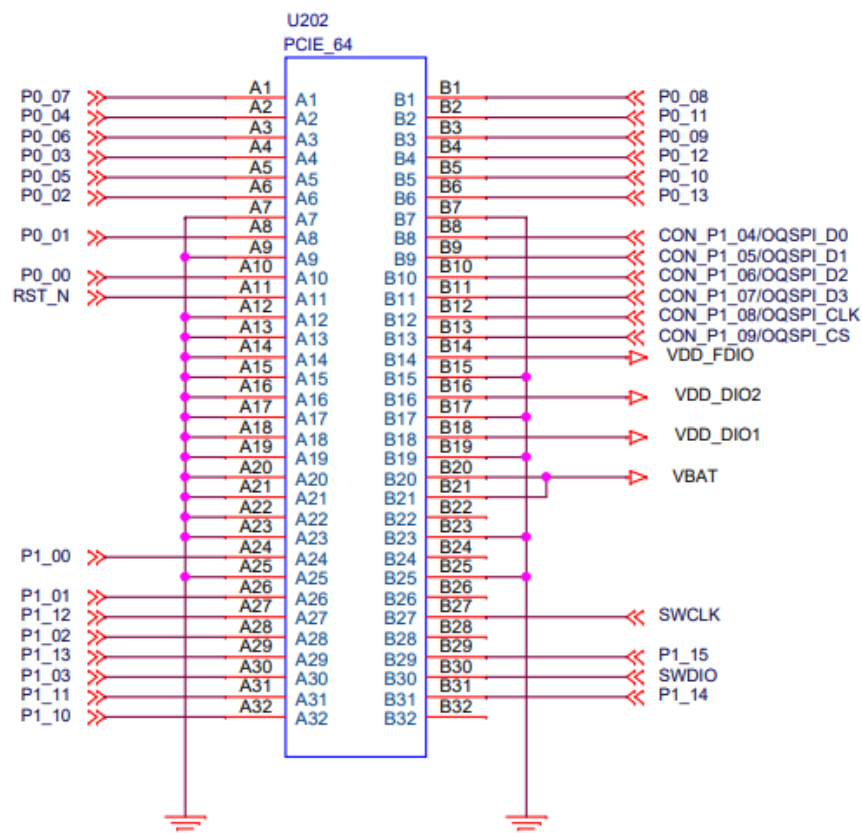


Figure 58. RA6W1 interface to Motherboard, Schematic

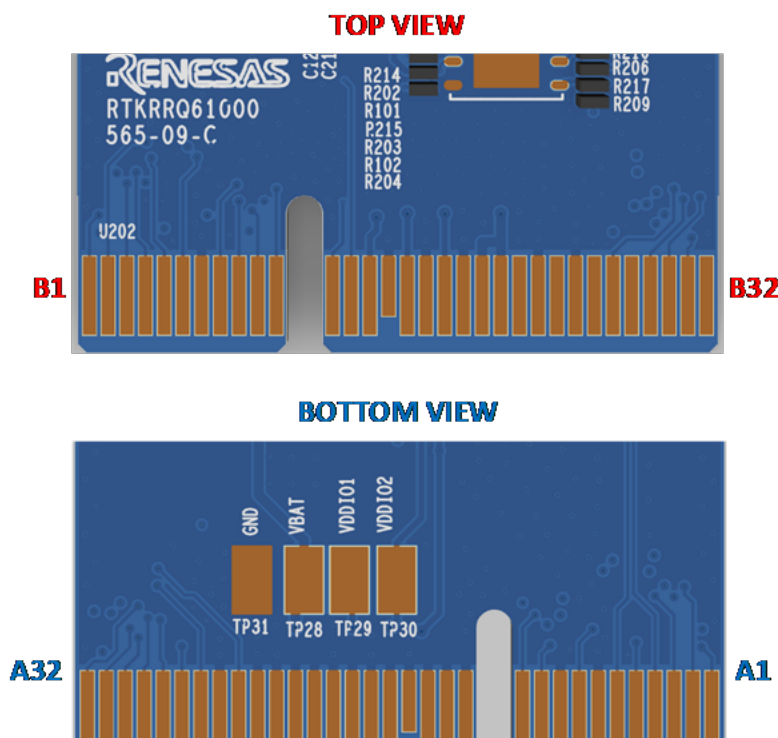


Figure 59. RA6W1 interface to Motherboard PCB

Table 13. Pins assignment for RRQ61600 daughterboard

Pins	Section	PWR domain	Access	Connection
RST_N	Wi-Fi	VBAT	U202, Pin A11	
P0_00	Wi-Fi	VBAT	U202, Pin A10	
P0_01	Wi-Fi	VBAT	U202, Pin A8	
P0_02	Wi-Fi	VBAT	U202, Pin A6	32 kHz crystal
P0_03	Wi-Fi	VBAT	U202, Pin A4	32 kHz crystal
P0_04	Wi-Fi	VDDIO_DIO1	U202, Pin A2	
P0_05	Wi-Fi	VDDIO_DIO1	U202, Pin A5	
P0_06	Wi-Fi	VDDIO_DIO1	U202, Pin A3	
P0_07	Wi-Fi	VDDIO_DIO1	U202, Pin A1	
P0_08	Wi-Fi	VDDIO_DIO1	U202, Pin B1	
P0_09	Wi-Fi	VDDIO_DIO1	U202, Pin B3	
P0_10	Wi-Fi	VDDIO_DIO1	U202, Pin B5	
P0_11	Wi-Fi	VDDIO_DIO1	U202, Pin B2	
P0_12	Wi-Fi	VDDIO_DIO1	U202, Pin B4	
P0_13	Wi-Fi	VDDIO_DIO1	U202, Pin B6	
P1_00	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A24	
P1_01	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A26	
P1_02	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A28	
P1_03	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A30	
P1_04	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B8	Connected to U202 through R209 (Not Mounted). Assigned to OQSPI_D0
P1_05	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B9	Connected to U202 through R203 (Not Mounted). Assigned to OQSPI_D1
P1_06	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B10	Connected to U202 through R204 (Not Mounted). Assigned to OQSPI_D2
P1_07	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B11	Connected to U202 through R205 (Not Mounted). Assigned to OQSPI_D3
P1_08	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B12	Connected to U202 through R206 (Not Mounted). Assigned to OQSPI_CLK
P1_09	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B13	Connected to U202 through R202 (Not Mounted). Assigned to OQSPI_CS
P1_10	Wi-Fi	VDDIO_DIO2	U202, Pin A32	
P1_11	Wi-Fi	VDDIO_DIO2	U202, Pin A31	
P1_12	Wi-Fi	VDDIO_DIO2	U202, Pin A27	
P1_13	Wi-Fi	VDDIO_DIO2	U202, Pin A29	
P1_14	Wi-Fi	VDDIO_DIO2	U202, Pin B31	
P1_15	Wi-Fi	VDDIO_DIO2	U202, Pin B29	
P1_16	Wi-Fi	VDDIO_DIO2	U202, Pin B27	SWCLK
P1_17	Wi-Fi	VDDIO_DIO2	U202, Pin B30	SWDIO

6.2. Reset

Push-button J201 is used for resetting RA6W1. Reset can be enabled also from button J607 on Motherboard, see [Section 5.8 Push-buttons](#)

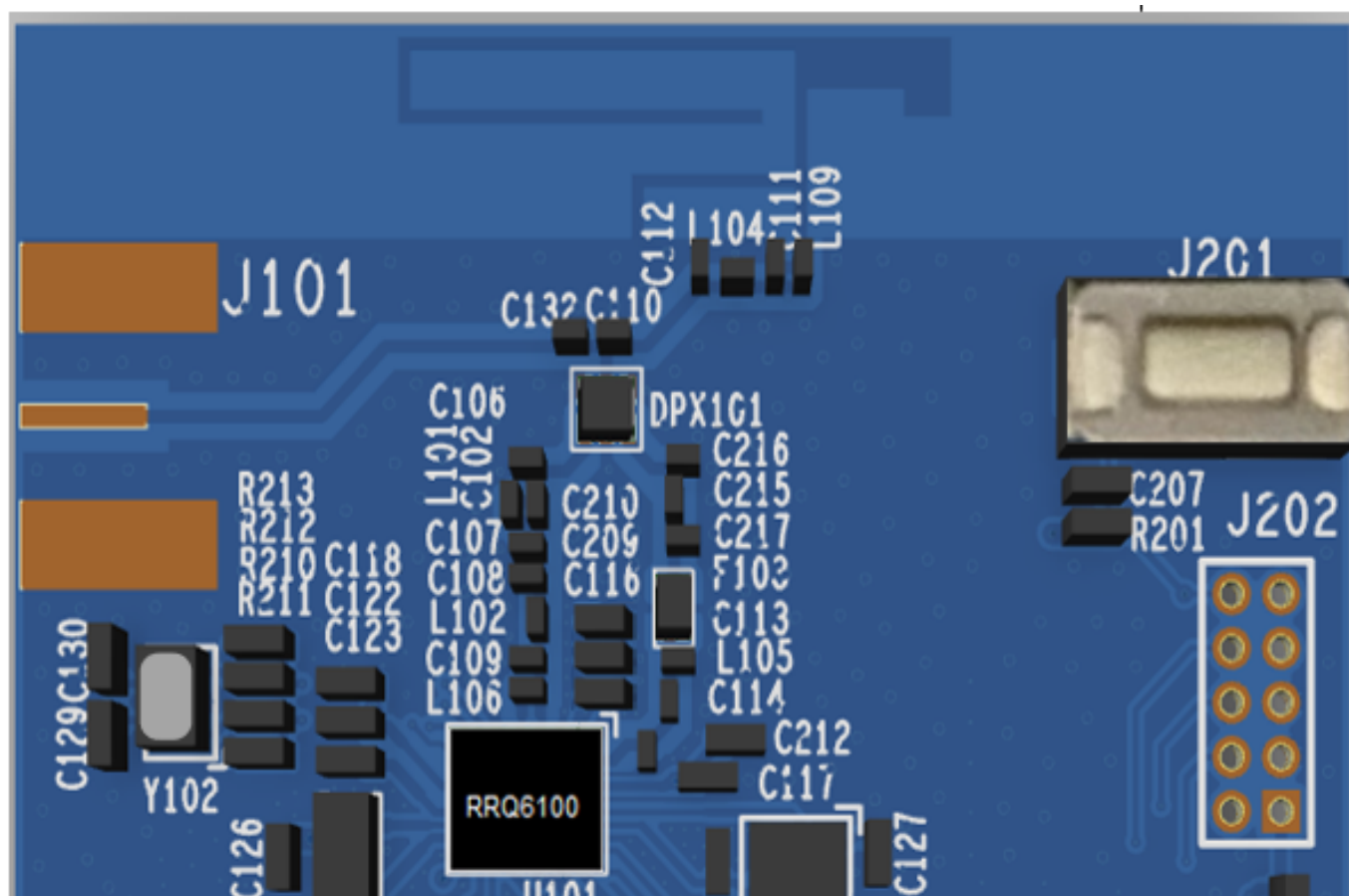
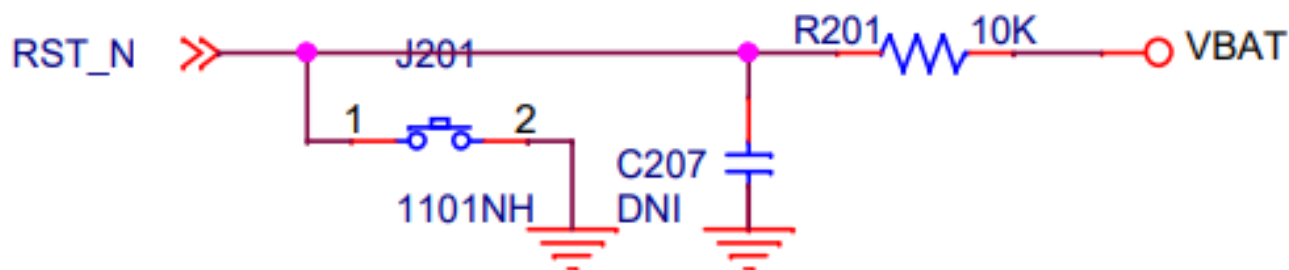


Figure 60. Reset Button (J201) on RA6W1 daughterboard

6.3. Clocks

- **40MHz XTAL (Y101):** the main clock of RA6W1 SoC is generated from a 40 MHz XTAL which is connected to the internal clock oscillator. The selected crystal is the CX2016DB40000D0FLJCC of [KYOCERA AVX](#).
- **32.768KHz XTAL (Y102):** for applications with more demanding accuracy/drift characteristics, such as time-keeping, using an external 32.768 kHz crystal is a suitable solution and the selected crystal is the FC-12M 32.7680KA-A5 of EPSON timing. By default, the external 32.768 kHz crystal is assembled on RA6W1. 32.768 kHz is connected to RA6W1 through P0_02 (XTAL32K_M) and P0_03 (XTAL32K_P).

6.4. QSPI NOR Flash

The component used is the Renesas AT25SL641-MHE-T or AT25SL641C-MHE-T. By default, the QSPI Flash (U102) is mounted on the daughterboard. QSPI NOR Flash is connected to the QSPI bus of RA6W1, and it operates in eXecution in Place (XiP) mode. The Flash can be programmed directly from the 1.27 mm pitch header (J202). Header is connected through Not Mounted resistors.

QSPI bus is connected to the PCIE connector through Not Mounted resistors (R202 to R206 and R209). By default, QSPI bus is not available to the Motherboard.

QSPI NOR Flash is supplied from $VDD_FDIO = 1.8\text{ V}$, which is generated from the RA6W1 SiP. Operating frequency is equal to 80 MHz.

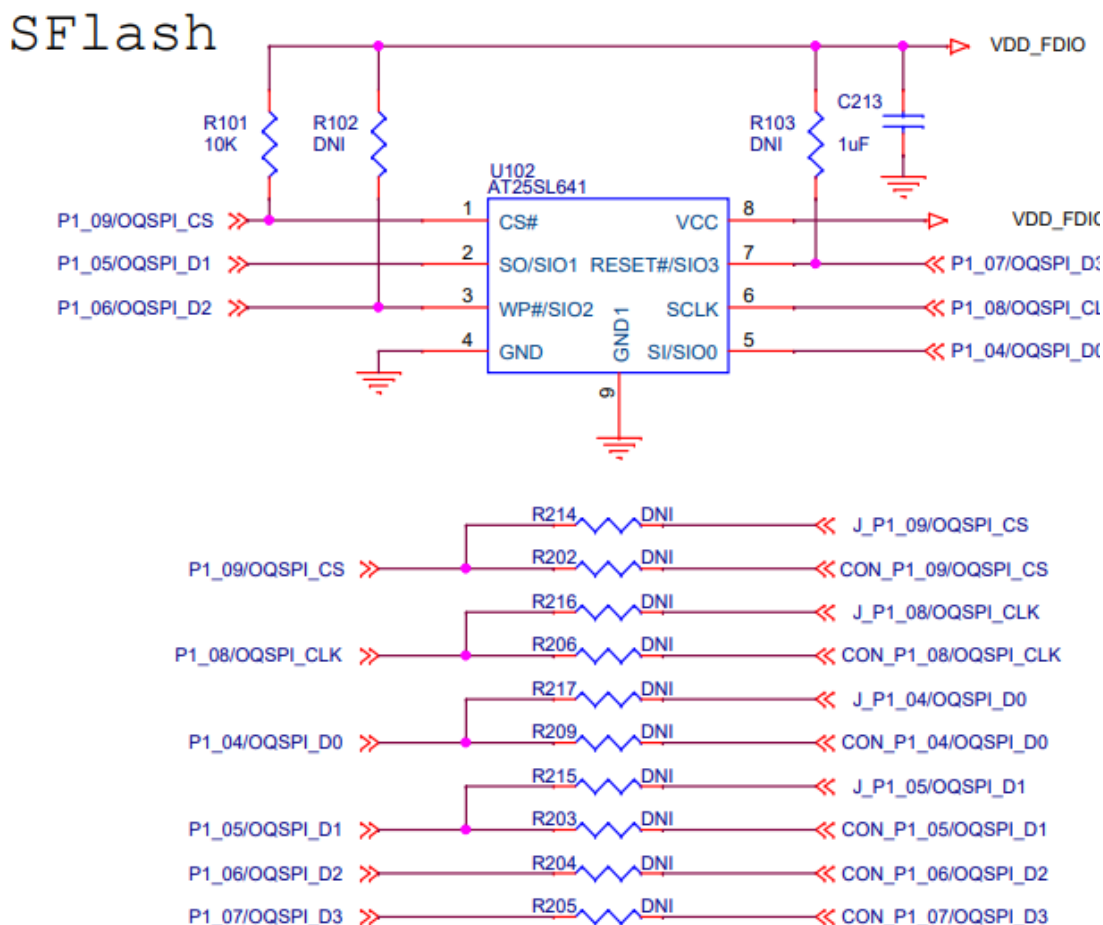


Figure 61. QSPI-Flash circuitry on RA6W1 daughterboard

A J-link connector (J202) for programming QSPI flash directly, is available on the RA6W1 Daughterboard. It utilizes SPI bus. You must mount the header J202 and resistors R214 to R217 (0 Ω).

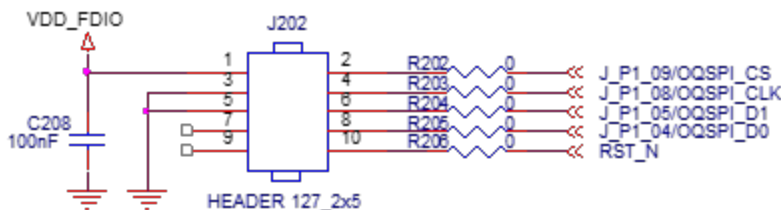


Figure 62. Connector (J202) for direct QSPI Flash programming

6.5. RF Section

To perform conducted RF measurements, do the following hardware modifications.

- Remove C110
- Assemble C132 = 10 pF

To perform OTA measurements, do the following hardware modifications.

- Remove C132
- Assemble C110 = 10 pF

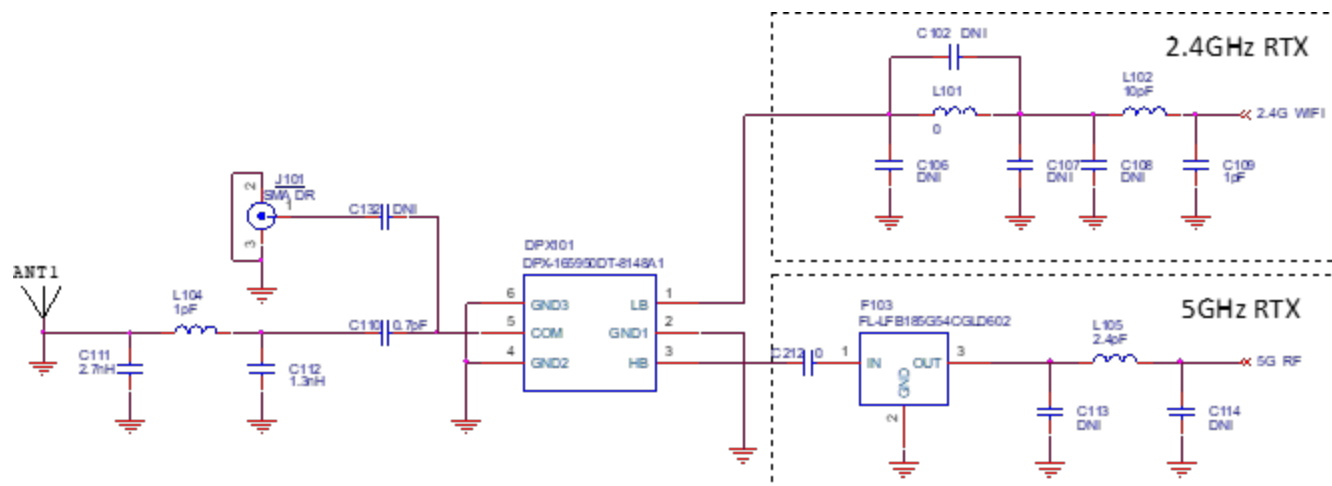


Figure 63. RF section circuitry of RA6W1 daughterboard

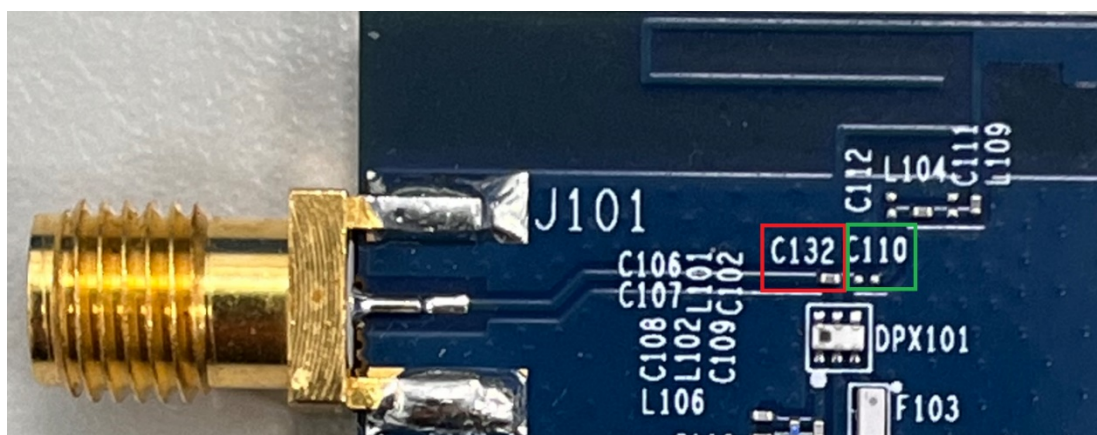


Figure 64. RF section of RA6W1 daughterboard

7. RTK7WBA6W2S05000B-RA6W2 Daughterboard (781-01-x)

RA6W2 SoC (U105): the RA6W2 is a highly integrated ultra-low-power Wi-Fi + Bluetooth® Low Energy Combo IC solution. This product includes the Wi-Fi that is a highly integrated ultra-low power Wi-Fi system on a chip (SoC) integrating an Arm® Cortex®-M33 system processor with a dual band 802.11a/b/g/n/ax Wi-Fi subsystem, on-chip memory, flexible peripheral interfaces and power management features

On RA6W2 daughterboard (board number 781-01-x) all necessary components required for the system setup are applied. Daughterboard, accompanied by the Motherboard, provides the capability for RA6W2 system evaluation and development.

The block diagram and the actual component locations of the RA6W2 daughterboard are shown in Figure 65 and Figure 66.

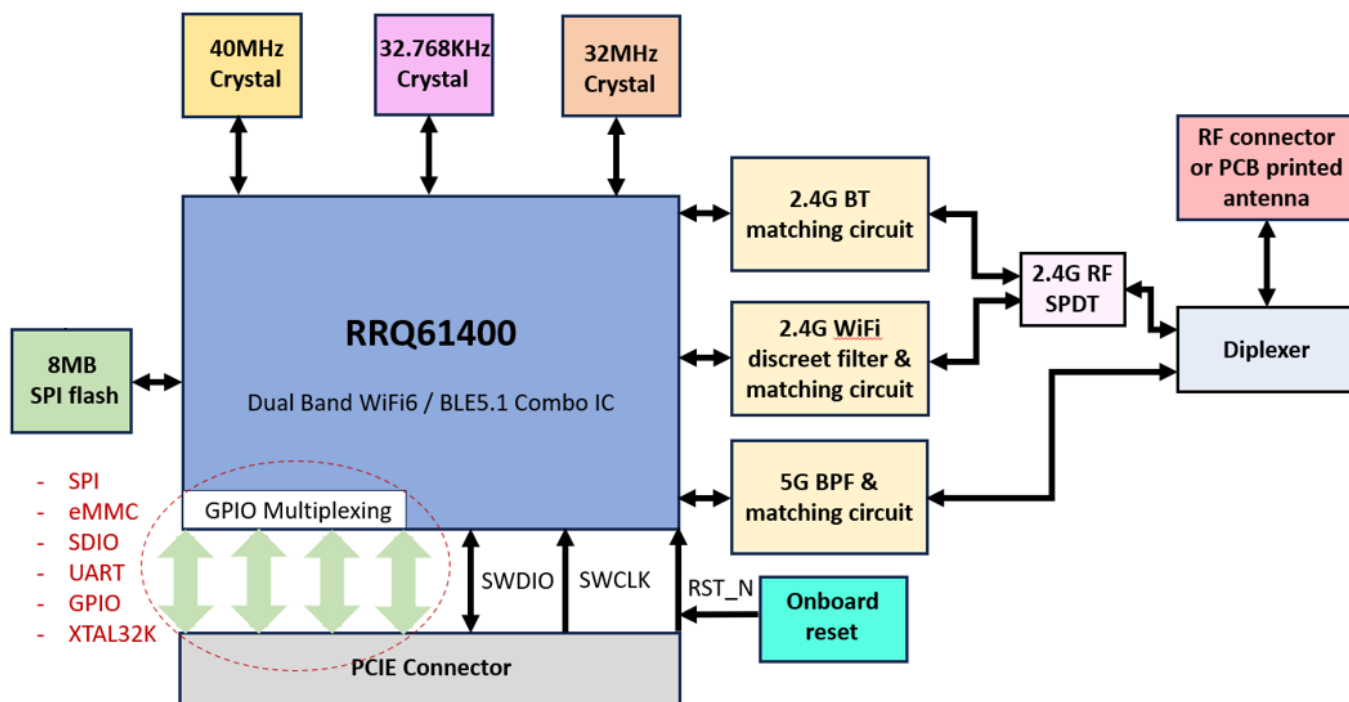


Figure 65. System block diagram of RA6W2 daughterboard

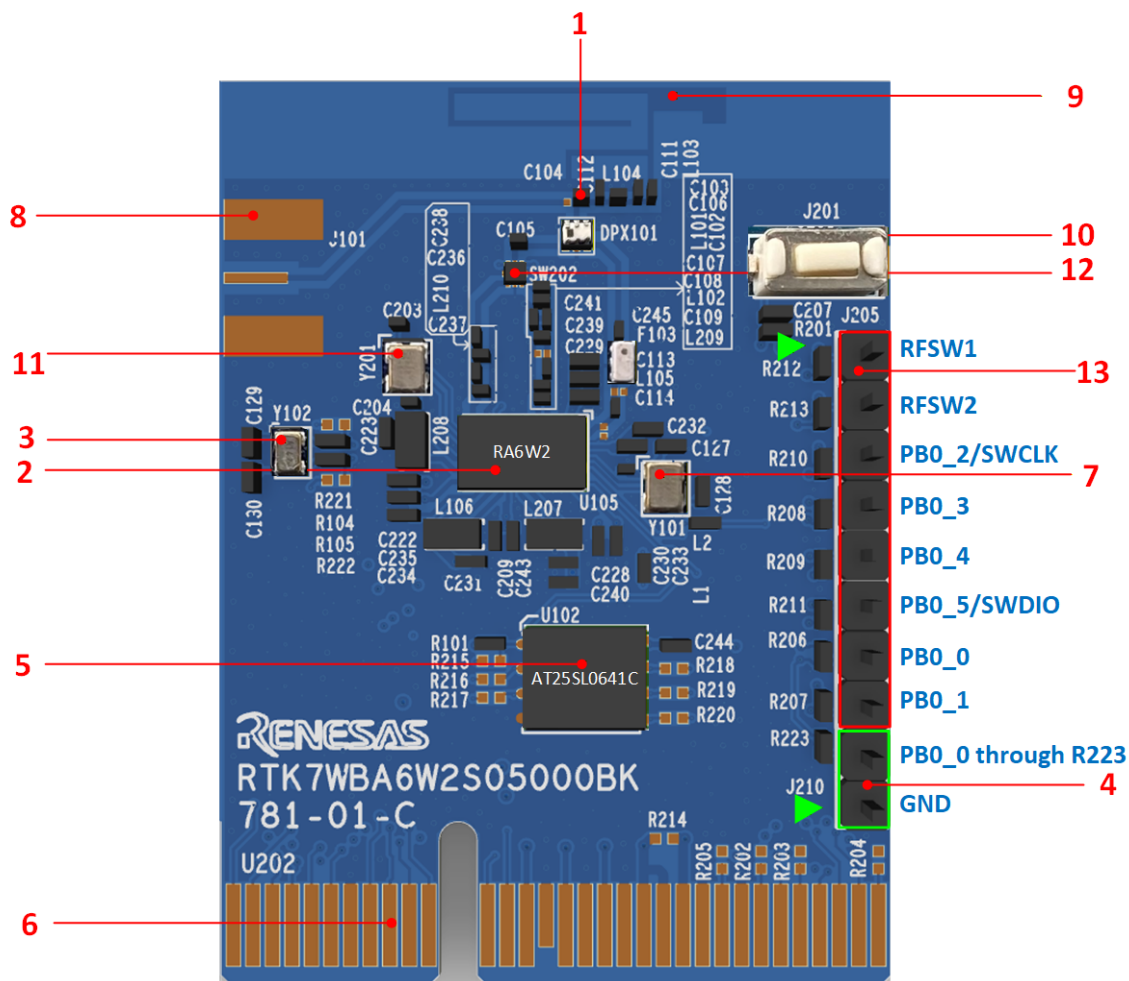


Figure 66. RA6W2 daughterboard component's placement

Table 14. RA6W2 daughterboard part numbers and description

No	Name	Location
1	Antenna selection network	
2	RA6W2 SoC	U105
3	32.768 kHz XTAL	Y102
4	PB0_0 through resistor R223 and GND pin	J210
5	QSPI NOR Flash	U102
6	PCIE Interface Connector with RA6W1	
7	40 MHz XTAL	Y101
8	SMA Connector	J101
9	PCB Printed Antenna	
10	Onboard reset button for Wi-Fi section	J201
11	32 MHz XTAL	Y201
12	RF SPDT switch	SW202
13	PIN header for RF SPDT switch control pins and Bluetooth LE pins	J205

7.1. RA6W2 GPIOs and Interface to Motherboard

RA6W2 SiP provides 18 GPIOs from Wi-Fi section and 6 GPIOs from Bluetooth LE section. All GPIOs are available on the daughterboard. Daughterboard is connected to Motherboard through a PCIe-64, PCB connector (U202). Only power and Wi-Fi signals are connected to the interface [Figure 67](#) and [Figure 68](#). Bluetooth LE GPIOs are accessible on header J205. The same interface is used for the daughterboards of RA6W1 and RRQ610x1 Modules.

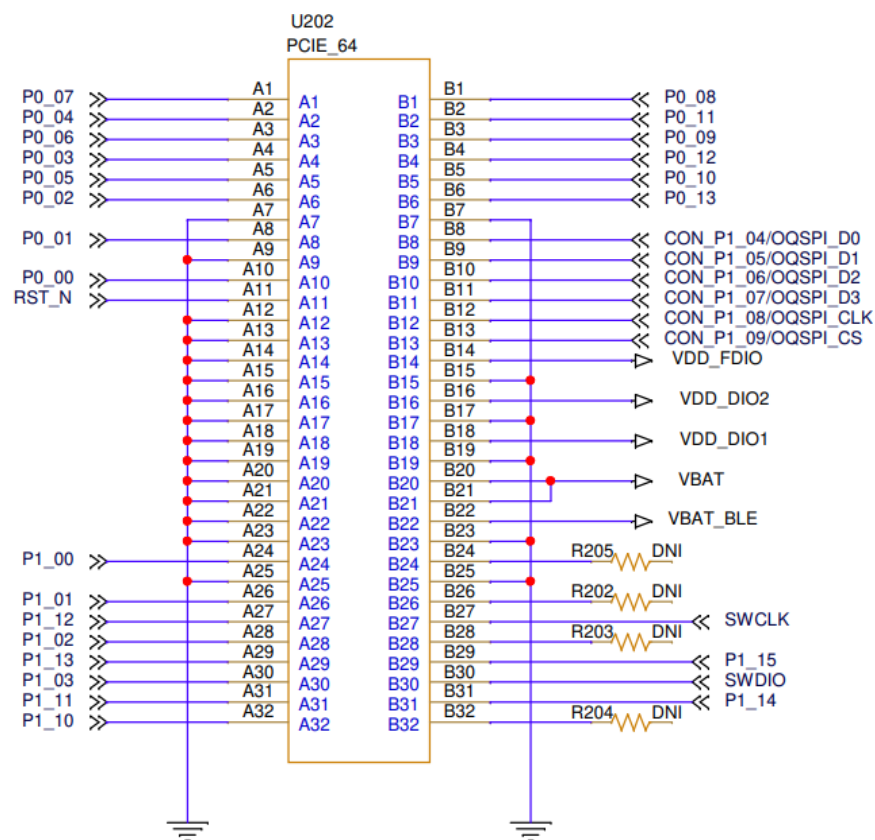


Figure 67. RA6W2 interface to Motherboard, Schematic

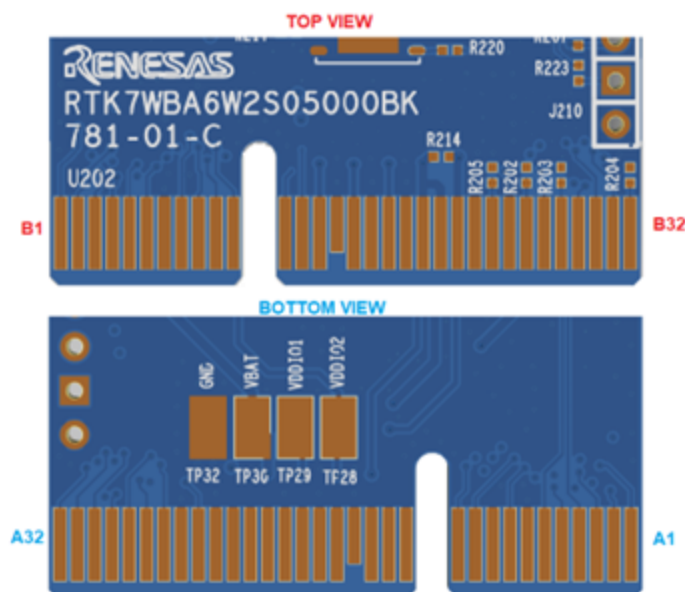


Figure 68. RA6W2 interface to Motherboard PCB

Table 15. Pins assignment for RRQ61640 daughterboard

Pins	Section	PWR domain	Access	Connection
PB0_0	Bluetooth LE	VBAT_B	J205. Pin 7	Connected to P1_10
PB0_1	Bluetooth LE	VBAT_B	J205. Pin 8	Connected to P1_11
PB0_2	Bluetooth LE	VBAT_B	J205. Pin 3	Connected to P1_14
PB0_3	Bluetooth LE	VBAT_B	J205. Pin 4	Connected to P1_12
PB0_4	Bluetooth LE	VBAT_B	J205. Pin 5	Connected to P1_13
PB0_5	Bluetooth LE	VBAT_B	J205. Pin 6	Connected to P1_15
RST_N	Wi-Fi	VBAT	U202, Pin A11	
P0_00	Wi-Fi	VBAT	U202, Pin A10	
P0_01	Wi-Fi	VBAT	U202, Pin A8	
P0_02	Wi-Fi	VBAT	U202, Pin A6	32 kHz crystal
P0_03	Wi-Fi	VBAT	U202, Pin A4	32 kHz crystal
P0_04	Wi-Fi	VDDIO_DIO1	U202, Pin A2	
P0_05	Wi-Fi	VDDIO_DIO1	U202, Pin A5	
P0_06	Wi-Fi	VDDIO_DIO1	U202, Pin A3	RFSW1
P0_07	Wi-Fi	VDDIO_DIO1	U202, Pin A1	RFSW2
P0_08	Wi-Fi	VDDIO_DIO1	U202, Pin B1	
P0_09	Wi-Fi	VDDIO_DIO1	U202, Pin B3	
P0_10	Wi-Fi	VDDIO_DIO1	U202, Pin B5	
P0_11	Wi-Fi	VDDIO_DIO1	U202, Pin B2	
P0_12	Wi-Fi	VDDIO_DIO1	U202, Pin B4	
P0_13	Wi-Fi	VDDIO_DIO1	U202, Pin B6	
P1_00	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A24	
P1_01	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A26	
P1_02	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A28	
P1_03	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A30	
P1_04	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B8	Connected to U202 thru R220 (Not Mounted) – Assigned to OQSPI_D0
P1_05	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B9	Connected to U202 thru R216 (Not Mounted) – Assigned to OQSPI_D1
P1_06	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B10	Connected to U202 thru R217 (Not Mounted) – Assigned to OQSPI_D2
P1_07	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin B11	Connected to U202 through R218 (Not Mounted). Assigned to OQSPI_D3
P1_08	Wi-Fi	VDDIO_	U202, Pin	Connected to U202 thru R219 (Not Mounted) – Assigned to OQSPI_

Pins	Section	PWR domain	Access	Connection
		FDIO=1.8 V	B12	CLK
P1_09	Wi-Fi	VDDIO_ FDIO=1.8 V	U202, Pin B13	Connected to U202 thru R215 (Not Mounted) – Assigned to OQSPI_ CS
P1_10	Wi-Fi	VDDIO_DIO2	U202, Pin A32	Connected to P_B0_0
P1_11	Wi-Fi	VDDIO_DIO2	U202, Pin A31	Connected to P_B0_1
P1_12	Wi-Fi	VDDIO_DIO2	U202, Pin A27	Connected to P_B0_3
P1_13	Wi-Fi	VDDIO_DIO2	U202, Pin A29	Connected to P_B0_4
P1_14	Wi-Fi	VDDIO_DIO2	U202, Pin B31	Connected to P_B0_2
P1_15	Wi-Fi	VDDIO_DIO2	U202, Pin B29	Connected to P_B0_5
P1_16	Wi-Fi	VDDIO_DIO2	U202, Pin B27	SWCLK
P1_17	Wi-Fi	VDDIO_DIO2	U202, Pin B30	SWDIO

7.2. Wi-Fi to Bluetooth LE Connectivity and Coexistence

RA6W2 is a System in Package (SiP) that supports Wi-Fi and Bluetooth LE technology. Wi-Fi and Bluetooth LE sections of RA6W2 are standalone and independent to each other. On Daughterboard the two sections are connected to each other through resistors, R206 to R211.



Figure 69. Wi-Fi and Bluetooth LE sections connections on RA6W2 Daughterboard

The connections implement a full-UART interface and the coexistence between the two sections. Pin assignment and functions are shown in [Table 16](#).

Table 16. Connectivity Wi-Fi and Bluetooth LE section of RA6W2

Bluetooth LE pins		Connected through Resistor	Wi-Fi Pins	
Bluetooth LE Pins	Function	Function	Wi-Fi pins	
PB0_0	UTX (Bluetooth LE)	R206	URX (Wi-Fi)	P1_10
PB0_1	URX (Bluetooth LE)	R207	UTX (Wi-Fi)	P1_11
PB0_2	BLE_RST / SWCLK	R210	BLE_RST	P1_14
PB0_3	URTS (Bluetooth LE)	R208	UCTS (Wi-Fi)	P1_12
PB0_4	UCTS (Bluetooth LE)	R209	URTS (Wi-Fi)	P1_13
PB0_5	iBtAct / SWDIO	R211	Coex	P1_15

NOTE

Wi-Fi pins are supplied from VDD_DIO2 whereas Bluetooth LE pins are supplied from VBAT_BLE. Both voltage rails must have the same voltage level or leakages may occur.

7.3. Reset

Push-button J201 is used for resetting Wi-Fi section of RA6W2. Reset can be enabled also from button J607 on Motherboard, see [Section 5.8 Push-buttons](#).

RESET

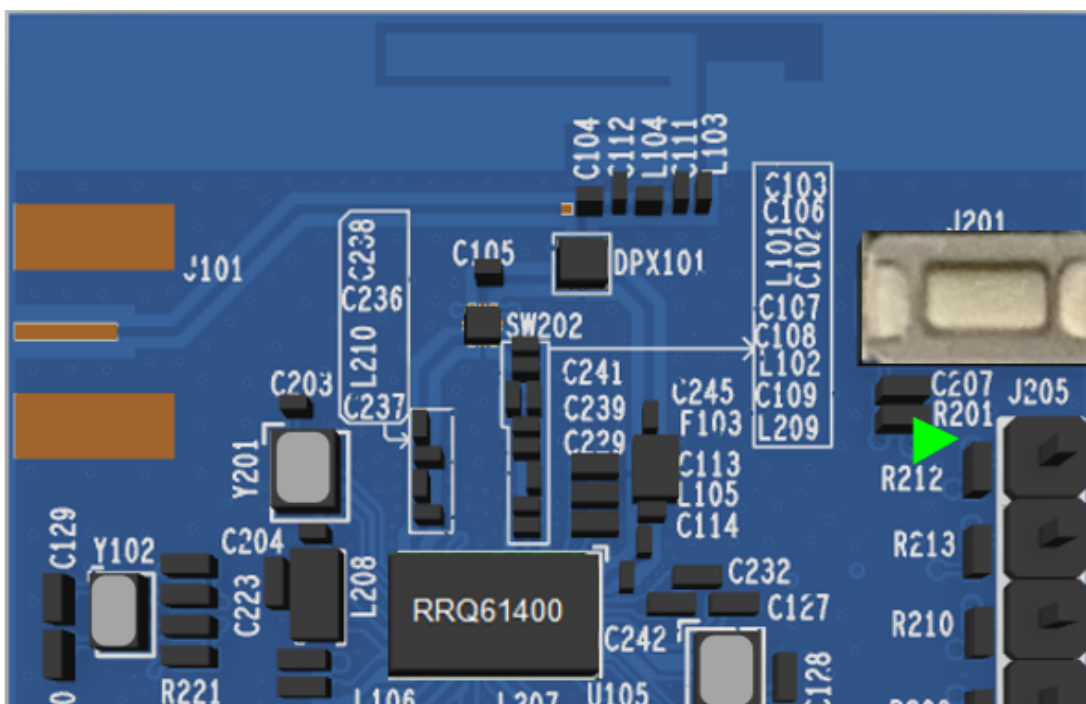
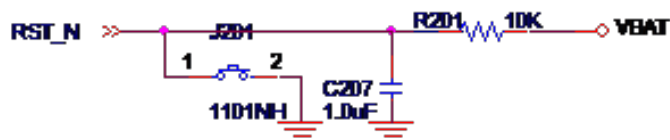


Figure 70. Reset push-button. J201

7.4. Clocks

- **40 MHz XTAL (Y101):** the main clock of the Wi-Fi system is generated from a 40 MHz XTAL which is connected to the internal clock oscillator. The selected crystal for RA6W1 is the CX2016DB40000D0FLJCC of [KYOCERA AVX](#).
- **32.768 kHz XTAL (Y102):** the RTC can be clocked with a 32.768 kHz crystal or from a calibrated internal 32 kHz RC oscillator. For applications with more demanding accuracy/drift characteristics, such as timekeeping, using an external 32.768 kHz crystal is a suitable solution and the selected crystal is the FC-12M 32.7680KA-A5 of EPSON timing. By default, the external 32.768 kHz crystal is assembled on RA6W2. 32.768 kHz is connected to RA6W2 (Wi-Fi section) through P0_02 and P0_03.
- **32 MHz XTAL (Y201):** the main clock of the BT system is generated from a 32 MHz XTAL which is connected to the internal clock oscillator. The selected crystal for RA6W2 is the CX2016DB32000D0FLJCC of [KYOCERA AVX](#).

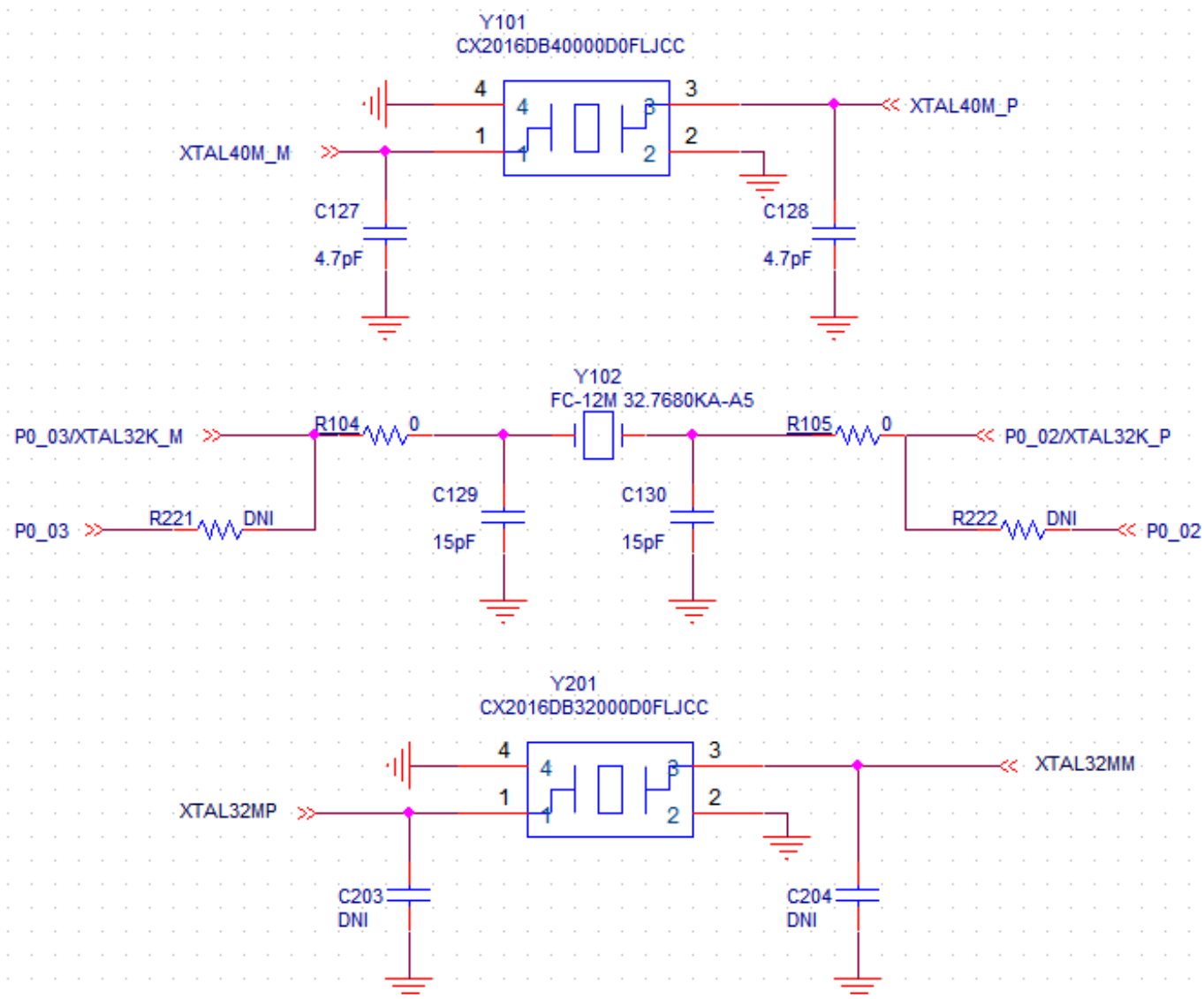


Figure 71. XTALs of RA6W2 daughterboard

7.5. QSPI NOR Flash

The used component is the Renesas AT25SL641-MHE-T or AT25SL641C-MHE-T for RA6W2. By default, the SPI Flash (U102) is mounted on this daughterboard. QSPI NOR Flash is connected to the QSPI bus of Wi-Fi of the SiP and operates as an eXecution in Place (XiP) memory.

QSPI bus is connected to the PCI bus through Not Mounted resistors R215 to R220. Consequently, by default, QSPI bus is not available to the Motherboard.

QSPI NOR Flash is supplied from VDD_FDIO = 1.8 V, generated from the RA6W2. Operating frequency is equal to 80 MHz.

SFlash

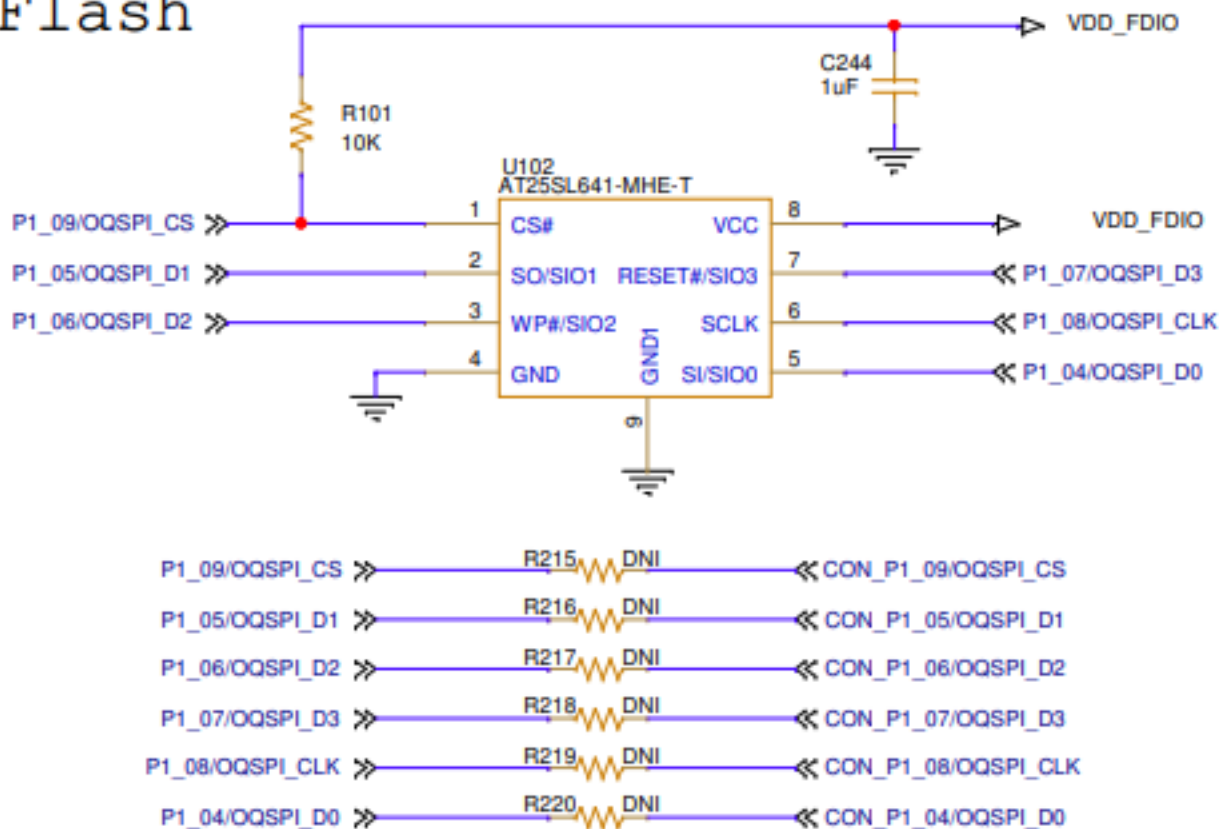


Figure 72. SPI-Flash circuitry on RA6W2 daughterboard

7.6. RF Section

RF section consists of three RF paths, two for Wi-Fi (2.4 GHz and 5 GHz) one for Bluetooth LE (2.4 GHz). The two 2.4 GHz lines are connected on an RF Switch (SW202), resulting in a single 2.4 GHz path, which is combined with the Wi-Fi 5 GHz line through diplexer DPX101. After the diplexer a single RF path is driven to either a Printed antenna or a SMA connector. The selection is done by soldering capacitor C104 (=10 pF) on the appropriate position, for details, see [Figure 74](#).



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8. RTK7WBRQ61S0x000BK-RRQ610x1 Module Daughterboard (565-16-x)

RRQ610x1-00x Module presents four variants. The variants are shown in [Table 18](#).

Table 18. RRQ610x1-00x variants

Part number	Board number	Description
RRQ61001-008	565-20-C	Wi-Fi 6 Dual Band 2.4/5 GHz, 802.11 a/b/g/n/ax, 8 MB Flash, PCB Trace antenna
RRQ61001-009	565-21-C	Wi-Fi 6 Dual Band 2.4/5 GHz, 802.11 a/b/g/n/ax, 8 MB Flash, External antenna connector, uFL
RRQ61051-008	565-20-C	Wi-Fi/Bluetooth LE combo module, Wi-Fi 6 Dual Band 2.4/5 GHz, 802.11 a/b/g/n/ax, 8 MB Flash, PCB Trace antenna
RRQ61051-009	565-21-C	Wi-Fi/Bluetooth LE combo module, Wi-Fi 6 Dual Band 2.4/5 GHz, 802.11 a/b/g/n/ax, 8 MB Flash, External antenna connector, uFL

The two RRQ61001-00x module variants (-008 for printed antenna and -009 for uFL), offer highly integrated wireless communication solutions, based on Wi-Fi. They include the RA6W1 system on chip (SoC) that has an 802.11 a/b/g/n/ac/ax radio (PHY), a baseband processor, a media access controller (MAC), on-chip memory, and an Arm® Cortex®-M33 core processor running at 160 MHz.

The two Renesas RRQ61051-00x module variants (-008 for antenna and -009 for uFL), offer highly integrated Combo Wi-Fi + Bluetooth® Low Energy (LE). These modules include the RA6W1 system on chip (SoC) and a DA14531 SoC. DA14531 has a 2.4 GHz transceiver and an Arm® Cortex®-M0+ microcontroller with a RAM of 48 kB and a One-Time Programmable (OTP) memory of 32 kB. The radio transceiver, the baseband processor, and the qualified Bluetooth LE stack is fully compliant with the Bluetooth LE 5.1 standard.

All variants of the module use an 8 MB Flash.



Figure 76. RRQ610x1-009 uFL (left) and RRQ610x1-008 printed antenna (right)

The RRQ610x1 daughterboard (565-16-x) carries all four variants of RRQ610x1 Modules. When combined with the Motherboard (565-11-x), it provides the capability to test, evaluate, and develop applications.

The block diagram and the actual component locations of the RRQ610x1 daughterboard are shown in [Figure 77](#) and [Figure 78](#).

Table 19. Part numbers of the Evaluation Daughterboard for RRQ610x1-00x Module

Part number	Name	Board number
RTK7WBRQ61S01000BK	Evaluation Daughterboard for RRQ61001-008	565-16-x
RTK7WBRQ61S02000BK	Evaluation Daughterboard for RRQ61001-009	565-16-x
RTK7WBRQ61S03000BK	Evaluation Daughterboard for RRQ61051-008	565-16-x
RTK7WBRQ61S04000BK	Evaluation Daughterboard for RRQ61051-009	565-16-x

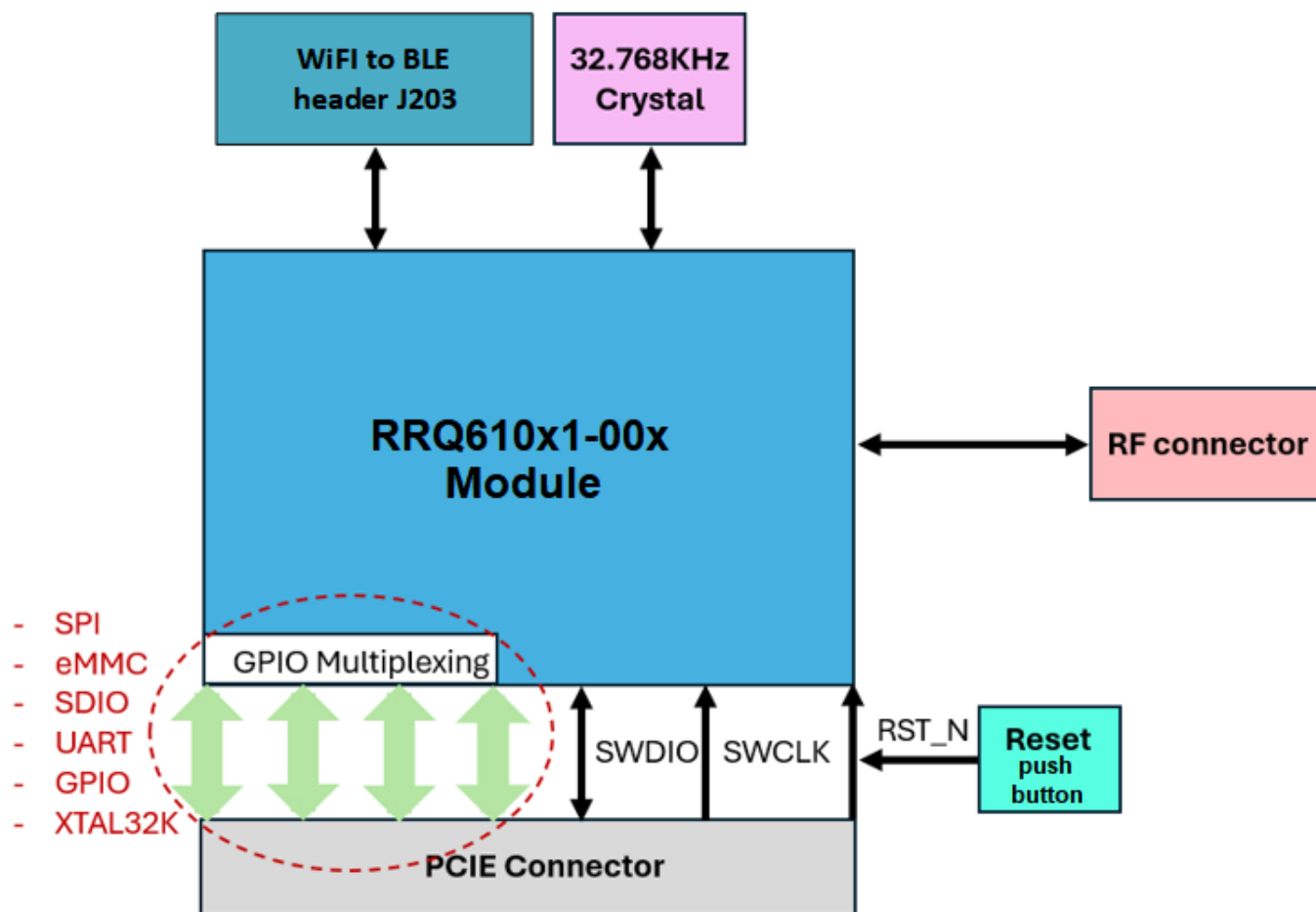


Figure 77. System block diagram of RRQ61051 module

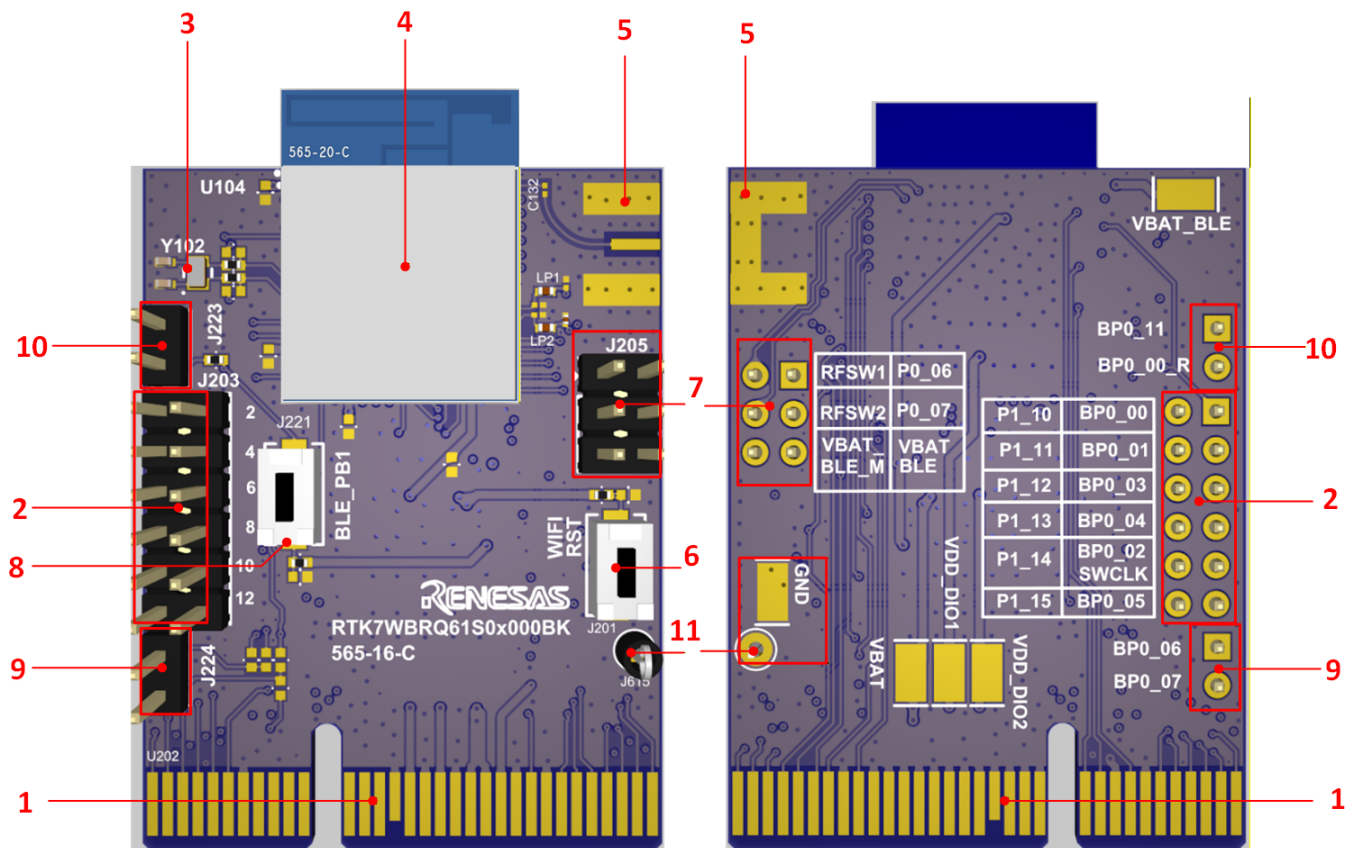


Figure 78. RRQ610x1 Daughterboard Component's placement (top left, bottom right)

Table 20. RRQ610x1-00x Daughterboard main components

No	Name	Location
1	PCIE PCB Connector. Interface to Motherboard (565-11-x) of EVK	U202
2	Pin header for Wi-Fi and Bluetooth LE sections of RRQ610x1 Modules. For the RRQ61051 Module, the header is used for connecting signals of Wi-Fi and Bluetooth LE for communication and coexistence.	J203
3	32.768KHz XTAL	Y102
4	RRQ610x1 module. Four variants of Module are mounted on Daughterboard	U104
5	SMA Connector – Not in use	U101
6	Reset push-button	J201
7	PIN header for RF switch and Bluetooth LE power supply. Jumpers must be applied to enable the connections.	J205
8	Push-button connecting B_P0_00 of Bluetooth LE to VBAT_BLE	J221
9	Monitoring header for B_P0_06 and B_P0_07	J224
10	Monitoring header for B_P0_11 and B_P0_00 through resistor R233	J223
11	GND	J615, TP32

8.1. RRQ610x1-00x Module GPIOs and Interface to Motherboard

RRQ61001 Modules provide 26 GPIOs whereas RRQ61051 Modules provide 38 GPIOs, 26 GPIOs from Wi-Fi, and 12 GPIOs from Bluetooth LE. All GPIOs are available to be accessed on Daughterboard or Motherboard through a PCIE-64, PCB connector (U202), see [Figure 79](#).

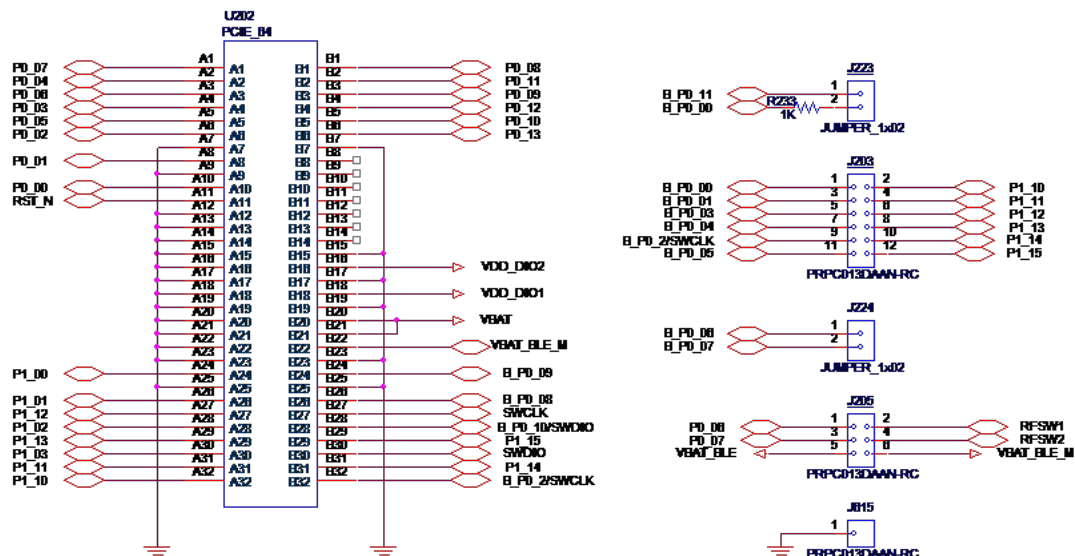


Figure 79. RRQ610x1 Daughterboard Interface to Motherboard (left) and headers (right)

As daughterboard is used for all variants of the Module, the Bluetooth LE signals are not available when the RRQ61001 are mounted. Table 21 and Table 22 show which GPIOs are available, their connectivity and their function.

Table 21. Daughterboard pins assignment for RRQ61001 Modules

Pins	Section	PWR domain	Access	Connection
P_B0_0				Not Available
P_B0_1				Not Available
P_B0_2				Not Available
P_B0_3				Not Available
P_B0_4				Not Available
P_B0_5				Not Available
P_B0_6				Not Available
P_B0_7				Not Available
P_B0_8				Not Available
P_B0_9				Not Available
P_B0_10				Not Available
P_B0_11				Not Available
RST_N	Wi-Fi	VBAT	U202, Pin A11	
P0_00	Wi-Fi	VBAT	U202, Pin A10	
P0_01	Wi-Fi	VBAT	U202, Pin A8	
P0_02	Wi-Fi	VBAT	U202, Pin A6	32 kHz crystal
P0_03	Wi-Fi	VBAT	U202, Pin A4	32 kHz crystal
P0_04	Wi-Fi	VDDIO_DIO1	U202, Pin A2	
P0_05	Wi-Fi	VDDIO_DIO1	U202, Pin A5	
P0_06	Wi-Fi	VDDIO_DIO1	U202, Pin A3	
P0_07	Wi-Fi	VDDIO_DIO1	U202, Pin A1	
P0_08	Wi-Fi	VDDIO_DIO1	U202, Pin B1	
P0_09	Wi-Fi	VDDIO_DIO1	U202, Pin B3	
P0_10	Wi-Fi	VDDIO_DIO1	U202, Pin B5	
P0_11	Wi-Fi	VDDIO_DIO1	U202, Pin B2	
P0_12	Wi-Fi	VDDIO_DIO1	U202, Pin B4	
P0_13	Wi-Fi	VDDIO_DIO1	U202, Pin B6	
P1_00	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A24	
P1_01	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A26	
P1_02	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A28	
P1_03	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A30	
P1_10	Wi-Fi	VDDIO_DIO2	U202, Pin A32	
P1_11	Wi-Fi	VDDIO_DIO2	U202, Pin A31	
P1_12	Wi-Fi	VDDIO_DIO2	U202, Pin A27	
P1_13	Wi-Fi	VDDIO_DIO2	U202, Pin A29	
P1_14	Wi-Fi	VDDIO_DIO2	U202, Pin B31	
P1_15	Wi-Fi	VDDIO_DIO2	U202, Pin B29	
P1_16	Wi-Fi	VDDIO_DIO2	U202, Pin B27	SWCLK
P1_17	Wi-Fi	VDDIO_DIO2	U202, Pin B30	SWDIO

Table 22. Daughterboard pins assignment for RRQ61051 Modules

Pins	Section	PWR domain	Access	Connection
P_B0_0	Bluetooth LE	VBAT_B	J203. Pin 1	Connected to P1_10
P_B0_1	Bluetooth LE	VBAT_B	J203. Pin 3	Connected to P1_11
P_B0_2	Bluetooth LE	VBAT_B	J203.Pin 9, U202.Pin B32	Connected to P1_14
P_B0_3	Bluetooth LE	VBAT_B	J203. Pin 5	Connected to P1_12
P_B0_4	Bluetooth LE	VBAT_B	J203. Pin 7	Connected to P1_13
P_B0_5	Bluetooth LE	VBAT_B	J203. Pin 11	Connected to P1_15
P_B0_6	Bluetooth LE	VBAT_B	J224, Pin 1	
P_B0_7	Bluetooth LE	VBAT_B	J224, Pin 2	
P_B0_8	Bluetooth LE	VBAT_B	U202, Pin B26	
P_B0_9	Bluetooth LE	VBAT_B	U202, Pin B24	
P_B0_10	Bluetooth LE	VBAT_B	U202, Pin B28	
P_B0_11	Bluetooth LE	VBAT_B	J223, pin 1	
RST_N	Wi-Fi	VBAT	U202, Pin A11	
P0_00	Wi-Fi	VBAT	U202, Pin A10	
P0_01	Wi-Fi	VBAT	U202, Pin A8	
P0_02	Wi-Fi	VBAT	U202, Pin A6	32 kHz crystal. Not available on U202
P0_03	Wi-Fi	VBAT	U202, Pin A4	32 kHz crystal. Not available on U202
P0_04	Wi-Fi	VDDIO_DIO1	U202, Pin A2	
P0_05	Wi-Fi	VDDIO_DIO1	U202, Pin A5	
P0_06	Wi-Fi	VDDIO_DIO1	U202, Pin A3	RFSW1
P0_07	Wi-Fi	VDDIO_DIO1	U202, Pin A1	RFSW2
P0_08	Wi-Fi	VDDIO_DIO1	U202, Pin B1	
P0_09	Wi-Fi	VDDIO_DIO1	U202, Pin B3	
P0_10	Wi-Fi	VDDIO_DIO1	U202, Pin B5	
P0_11	Wi-Fi	VDDIO_DIO1	U202, Pin B2	
P0_12	Wi-Fi	VDDIO_DIO1	U202, Pin B4	
P0_13	Wi-Fi	VDDIO_DIO1	U202, Pin B6	
P1_00	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A24	
P1_01	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A26	
P1_02	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A28	
P1_03	Wi-Fi	VDDIO_FDIO=1.8 V	U202, Pin A30	
P1_10	Wi-Fi	VDDIO_DIO2	U202, Pin A32	Connected to P_B0_0
P1_11	Wi-Fi	VDDIO_DIO2	U202, Pin A31	Connected to P_B0_1
P1_12	Wi-Fi	VDDIO_DIO2	U202, Pin A27	Connected to P_B0_3
P1_13	Wi-Fi	VDDIO_DIO2	U202, Pin A29	Connected to P_B0_4
P1_14	Wi-Fi	VDDIO_DIO2	U202, Pin B31	Connected to P_B0_2
P1_15	Wi-Fi	VDDIO_DIO2	U202, Pin B29	Connected to P_B0_5
P1_16	Wi-Fi	VDDIO_DIO2	U202, Pin B27	SWCLK
P1_17	Wi-Fi	VDDIO_DIO2	U202, Pin B30	SWDIO

8.2. Wi-Fi to Bluetooth LE Connectivity and Coexistence for RRQ61051

RRQ61051 Modules support Wi-Fi and Bluetooth LE technology. Wi-Fi and Bluetooth LE sections are two stand-alone systems which combine on RF side (an RF switch is located internally to the Module, but control signals are external) and connected on digital interface to each other for establishing communication and coexistence. The connections on digital interface are external to Module and they are implemented through headers J203 and J205.

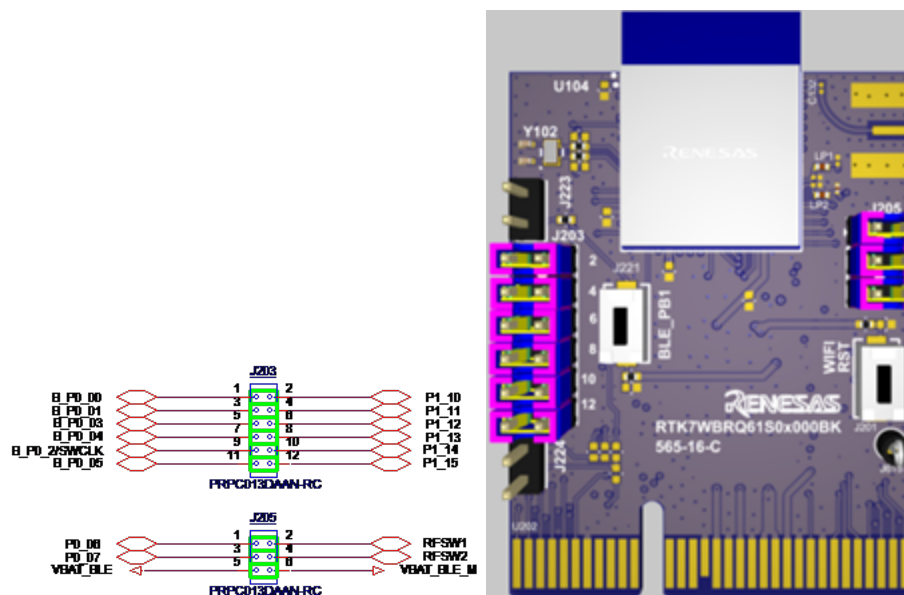


Figure 80. Wi-Fi and Bluetooth LE sections connections on Daughterboard for RRQ61051 Modules

The connections implement a full-UART interface and the coexistence between the two sections. Pin assignment and functions are shown in Table 23.

Table 23. Connectivity Wi-Fi and Bluetooth LE section of RRQ61051 Modules

Bluetooth LE pins		Apply jumper	Wi-Fi Pins	
Bluetooth LE Pins	Function	Function	Wi-Fi pins	
P_B0_0	UTX (Bluetooth LE)	J203. 1-2	URX (Wi-Fi)	P1_10
P_B0_1	URX (Bluetooth LE)	J203. 3-4	UTX (Wi-Fi)	P1_11
P_B0_2	BLE_RST/SWCLK	J203. 9-10	BLE_RST	P1_14
P_B0_3	URTS (Bluetooth LE)	J203. 5-6	UCTS (Wi-Fi)	P1_12
P_B0_4	UCTS (Bluetooth LE)	J203. 7-8	URTS (Wi-Fi)	P1_13
P_B0_5	iBtAct /SWDIO	J203. 11-12	Coex	P1_15

NOTE

Wi-Fi pins are supplied from VDD_DIO2 whereas Bluetooth LE pins are supplied from VBAT_BLE. Both voltage rails must have the same voltage level or leakages may occur.

Table 24. RF switch control

Pins	Apply jumper	Pins	Function
P0_06	J205. 1-2	RFSW1	Enable Bluetooth LE when RFSW1=High and RFSW2 = Low
P0_07	J205. 3-4	RFSW2	Enable Wi-Fi when RFSW1=Low and RFSW2 = High
VBAT_BLE_M	J205. 5-6	VBAT_BLE	Power Bluetooth LE Section

8.3. Jumper Settings for RRQ61001 Modules

As there is Bluetooth LE on RRQ61001 Modules, no jumpers required on daughterboards with RRQ61001.

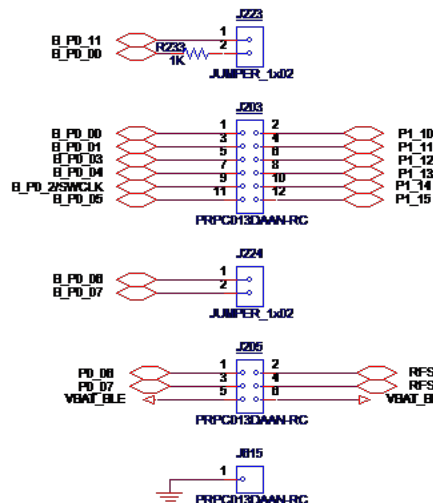


Figure 81. Jumper settings for RRQ61001 daughterboard

8.4. Reset and Push-buttons

Push-button **J201**, is used for resetting Wi-Fi section of RRQ610x1 Modules. Reset can be enabled also from button J607 on Motherboard, see [Section 5.8 Push-buttons](#).

Push-button **J202** connects B_P0_00 of Bluetooth LE with a strong pull-up to VBAT_BLE. Note that during Bluetooth LE booting, B_P0_00 is configured as Reset (Active High). Push-button J202 is enabled only with RRQ61051 modules.

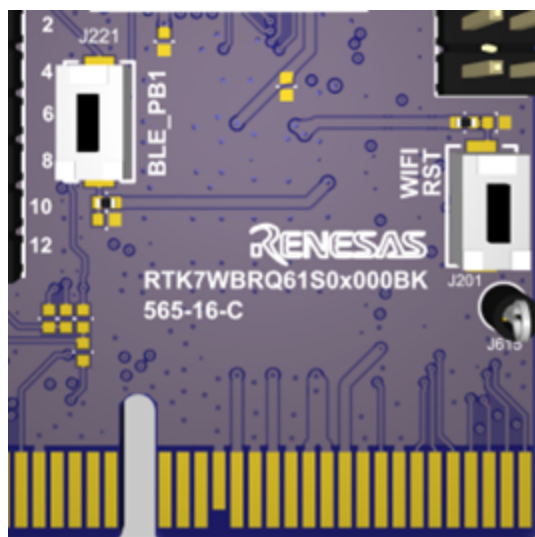
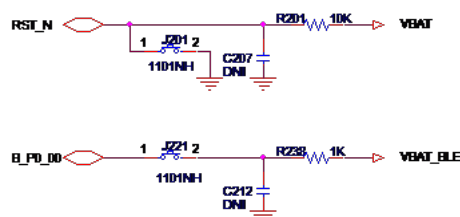


Figure 82. Push-buttons of RRQ610x1 daughterboard

8.5. The Crystal 32.768 kHz

32.768 kHz XTAL (Y102): is used for applications with demanding accuracy/drift characteristics, such as time-keeping. The selected crystal is the FC-12M 32.7680KA-A5 of EPSON timing. By default, the external 32.768 kHz crystal is assembled on RRQ610x1 Daughterboard. GPIOs P0_2 and P0_03 are not available either to U202, nor Motherboard.

X-tal

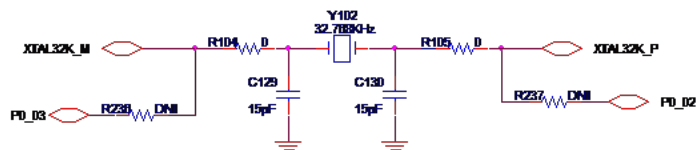


Figure 83. 32.768 kHz crystal

8.6. RF Section

- On RRQ610x1 Daughterboard, a place holder is applied for a SMA RF connector (J101). The RF SMA connector is not used.
- For performing conducted measurements with RRQ61051-009 Module, add an AC coupling capacitor if the equipment does not include it. This is not necessary for RRQ61001-009 Module.

Appendix A EK-RA6W1 Motherboard (565-11-E) – Assembly-Top

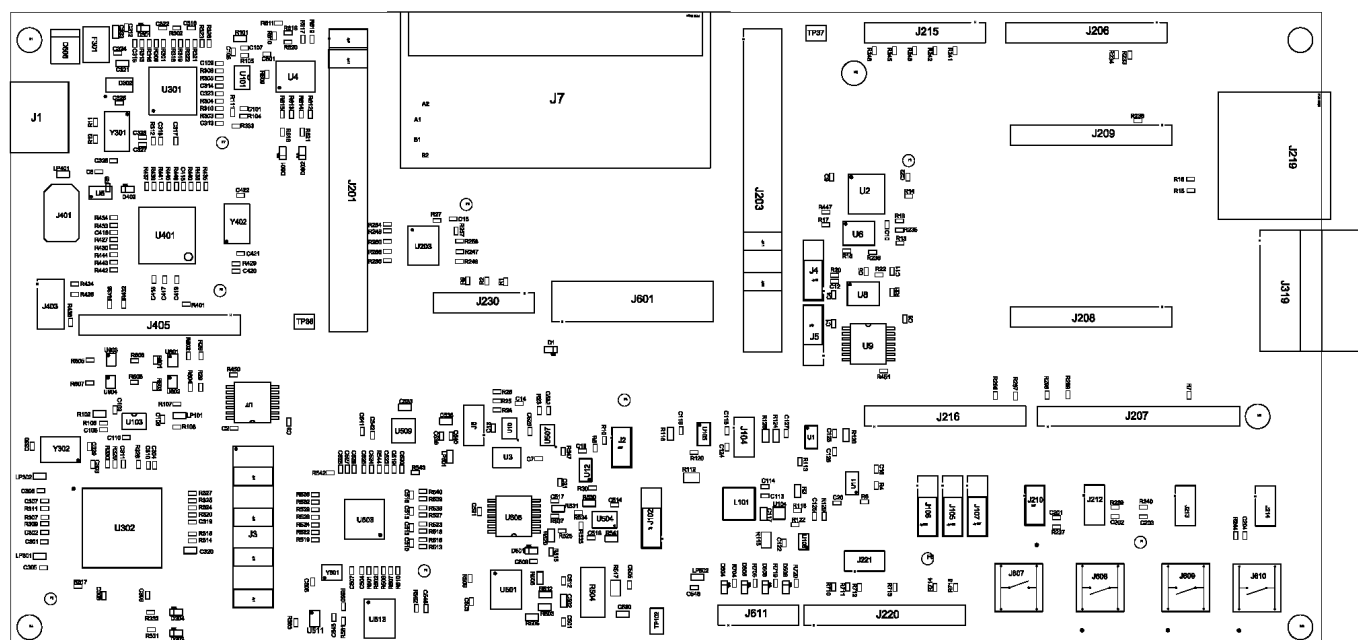


Figure 84. EK-RA6W1 Motherboard (565-11-E) – components location on top layer

9. Revision History

Revision	Date	Description
1.10	Nov 24, 2025	▪ Updated Figure 1 ▪ Modified Section 5.2.1 Power Measurements Setup ▪ Modified Section 5.10 SDIO Interface ▪ Updated Figure 78 ▪ Updated Figure 80 ▪ Updated Figure 81 ▪ Updated Figure 82
1.09	Oct 13, 2025	Added measurements setup Added note for J403
1.08	Sept 8, 2025	Updated figures
1.07	Aug 28, 2025	Updated figures
1.06	Aug 15, 2025	Updated figures
1.00	Mar 13, 2025	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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