

RH4Z250x-PMOD Evaluation Board

IO-Link Transceiver Extension Board

This document explains the hardware design of the RH4Z250x-PMOD (RH4Z2501-PMOD, RH4Z2502-PMOD), its main features and the necessary hardware setup to implement an IO-Link device.

Target device: RH4Z250x (RH4Z2501, RH4Z2502) single channel IO-Link physical layer transceiver with integrated protection.

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Terms and Definitions

C/Q	C/Q line of IO-Link interface. Connection for communication (C) or switching (Q) signal
DC	Direct Current
DC-DC	Direct Current - Direct Current
GND	Ground
IC	Integrated Circuit
IO	Input Output
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller Unit
NPN	Negative-Positive-Negative
OWI	One-Wire Interface
PCB	Printed Circuit Board
PHY	Physical Layer
PMOD	Digilent Pmod™ Connector

1. Overview

1.1 RH4Z250x Features

The RH4Z250x-PMOD is a PMOD module for the RH4Z250x Renesas silicon solution. The purpose of the module is to be used with a standard MCU evaluation board with a PMOD interface to implement an IO-Link device.

The RH4Z250x offers the following features:

- Voltage range from 9 V to 36 V
- Over-voltage peak robustness of ± 60 V
- Configurable driver output current 50 mA DC to 600 mA DC
- $R_{DS(on)}$ of less than 2.5Ω
- Adjustable driver slew rate
- Integrated wake-up detection
- MCU assisted wake-up generation (typically 600 mA)
- OWI digital communication and calibration interface
- Integrated linear voltage regulators: 3.3 V and 5 V
- Ambient temperature range -40°C to 125°C
- Glitch filter for receiver
- Integrated protection
 - ± 1.25 kV/2.5 A (peak) surge protection for VDD, CQ, GND (8/20- μs pulse according to IEC 61000-4-5)
- Reverse polarity protection for L+, CQ, GND/L-
- On-chip diagnostics:
 - Over-temperature detection
 - Supply voltage monitor
 - Broken chip detection

For more information, see *RH4Z250x Datasheet*.

1.2 RH4Z250x-PMOD Capabilities

The RH4Z250x-PMOD integrates an IO-Link PHY to equip MCU Evaluation Boards containing PMOD with the IO-Link interface.

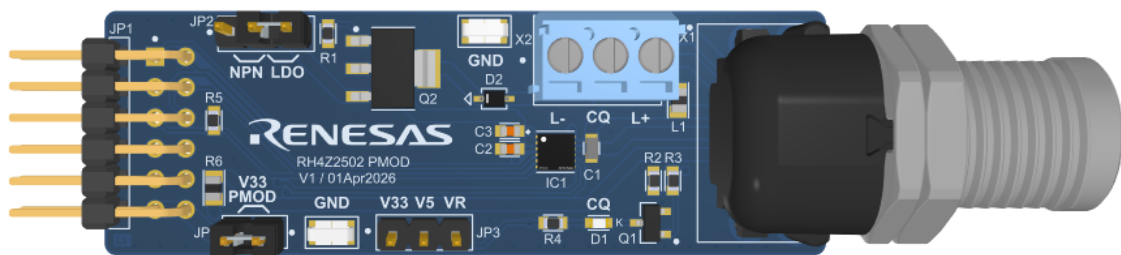


Figure 1. RH4Z2502-PMOD (default jumper setting)



CAUTION

Do not adjust any jumper settings on the RH4Z250x-PMOD during powered operation.

2. Getting Started

2.1 System Block Diagram

Figure 2 shows the system overview for the RH4Z250x-PMOD.

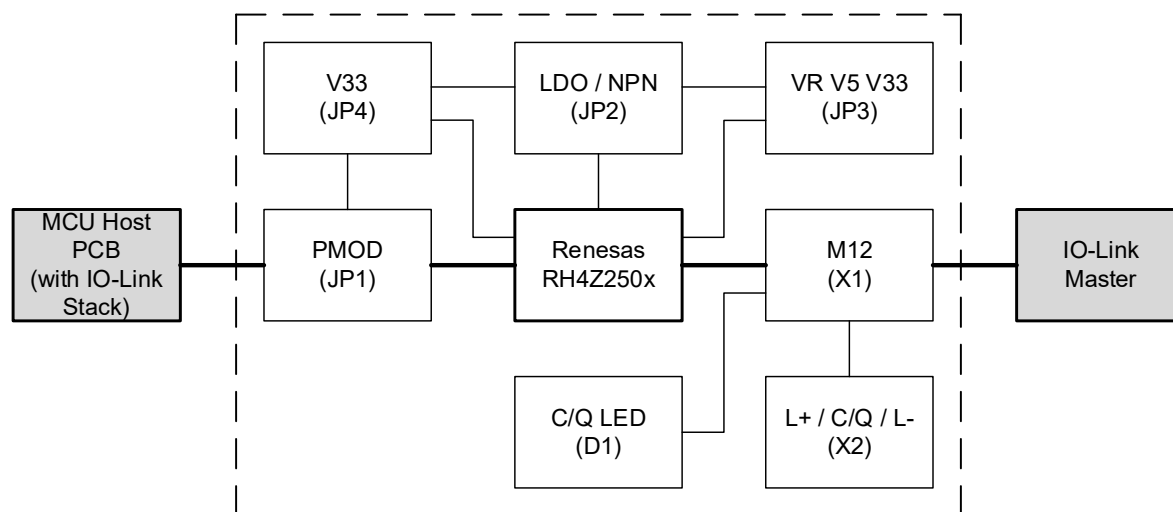


Figure 2. System block diagram

2.2 Default Board Configuration

Table 1 lists the default configuration for the RH4Z250x-PMOD.

Table 1. Default board configuration

Jumper/switch	Default position
JP2	LDO
JP3	Open
JP4	Closed

3. RH4Z250x-PMOD Components

3.1 X1: M12 Connector

X1 is a male 4-pin M12-A-coded connector. It enables an easy connection between the RH4Z250x-PMOD and an IO-Link Master. IO-Link is a serial, bidirectional point-to-point connection for signal transmission and power supply to sensors and actuators. The RH4Z250x-PMOD features a 4-pin Class A device port with the pin assignment, as shown in [Figure 3](#) and [Table 2](#). For usage of Pin 2, populate R6 with a 0-Ω resistor.

Table 2. X1: Pin assignment

Pin	Signal	Designation
1	L+	Power supply (+), 24 V
2	I/Q	NC/DI (OSSDe)/DO/AI/AO, routed to Pin 8 of JP1
3	L-	Power supply (-), 0 V/GND
4	C/Q	SIO (OSSDe)/SDCI, SIO (DI/DO) or SDCI (IO-Link-coded data)

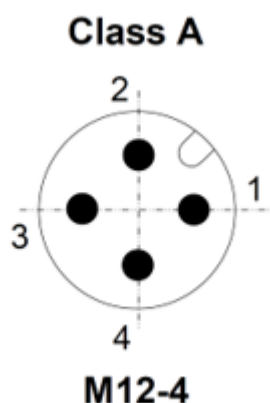


Figure 3. X1: Pin numbering (front view)

3.2 X2: Block Terminal

X2 offers direct access to L+, C/Q, and L- from the M12 connector.

NOTE

RH4Z2501-PMOD v1.1 boards offer access to L+ and L- only.

3.3 JP1: PMOD Connector

The RH4Z250x-PMOD is connected to Host MCU PCB (with the IO-Link device stack) through JP1 carrying a PMOD interface.

Table 3. JP1: Pin assignment

Pin	Function
1	OWI/DIAG
2	TxD
3	RxD
4	NC
5	GND
6	3V3
7	/WU
8	I/Q (connected to X1 Pin 2)
9	TxEN
10	NC
11	GND
12	3V3

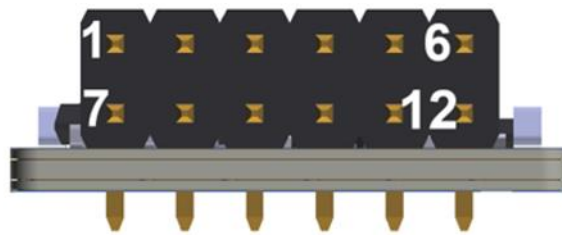


Figure 4. JP1: Pin numbering (front view)

3.4 JP2: Voltage Regulation Options (Onboard)

The RH4Z250x-PMOD enables the following methods to regulate the voltage supplied from the IO-Link Master:

- Set jumper to position LDO to use the internal LDO to regulate the voltage (maximum 50 mA).
- Set jumper to position NPN to use the external NPN transistor (Q2) to regulate the voltage. The heat from voltage drop between 24 V and 5 V is generated in the external transistor and not in the RH4Z250x IC. Current is limited by maximum supply current from Master and PCB thermal limits.

3.5 JP3: Voltage Regulation Options (External)

All voltage regulation pins are accessible on JP3 to implement external power options, for example, an external transistor or DC-DC converter. For more information, see *RH4Z250x Datasheet*.

3.6 JP4: 3.3 V PMOD Interface

When JP4 is closed, 3.3 V power supply on PMOD interface is enabled (maximum 50 mA if internal LDO is used).

3.7 D1: C/Q-LED

The RH4Z250x-PMOD has an LED that indicates the status of the C/Q line (IO-Link communication status). Its signal is regulated by NPN transistor Q1 and its voltage divider.

4. Revision History

Revision	Date	Description
1.01	Aug 17, 2026	▪ Changed RH4Z2501 to RH4Z250x ▪ Added the RH4Z2502-PMOD variant ▪ Section 1.1: Updated Figure 1 ▪ Section 3.2: Added a note on RH4Z2501-PMOD v1.1 boards.
1.00	Apr 15, 2024	Initial release.