User's Manual

32

RH850 Evaluation Platform

RH850/E2x 292pin

User's Manual: Piggyback Board T1-V2

Y-RH850-E2X-292PIN-PB-T1-V2

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Y-RH850-E2X-292PIN-PB-T1-V2 Documents

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   – The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/E2x 292pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/E2x 292pin microcontrollers. The piggyback board (Y-RH850-E2X-292PIN-PB-T1 -V2) can be used as a standalone board or can be mated with a mainboard (Y-RH850-X1X-MB-Tx-Vx, Y-RH850-X2X-MB-Tx-Vx) for extended functionality.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' to the pin or signal name. E.g. the reset pin is named RESETZ.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-E2X-292PIN-PB-T1-V2 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-E2X-292PIN-PB-T1-V2 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-E2X-292PIN-PB-T1-V2* shows the packing components of the Y-RH850-E2X-292PIN-PB-T1-V2 package.

Table 1.1 Package Components for the Y-RH850-E2X-292PIN-PB-T1-V2

Item	Description	Quantity
D017348	RH850/E2x 292pin piggyback board	1
D017409	Documentation CD	1
D010816-24	China RoHS document	1
D017408	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	42
Red Hirschmann 4 mm power lab sockets	In the bag	3
Black Hirschmann 4 mm power lab sockets	In the bag	1
20MHz Resonator	In the bag	1

Note

Please keep the Y-RH850-E2X-292PIN-PB-T1-V2 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-E2X-292PIN-PB-T1-V2. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-Tx-Vx
- Y-RH850-X2X-MB-Tx-Vx

1.3 Main Features

- Burn-in socket for mounting of the device
- Several options for power supply
  - Combined operation with powering from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.25 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.
- Debugging and programming interface:
  - 14-pin JTAG Debug Connector (e.g. for using E2 OCD Emulator or PG-FP6 Flash Programmer)
  - 34-pin AURORA Interface Connector
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with 20 MHz or 40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)
  - Renesas High speed Bus (RHSB)
  - High-speed SPI
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board. For a detail view of the socket, that is shown only as black square, please refer to chapter *1.6 Mounting of the Device.*

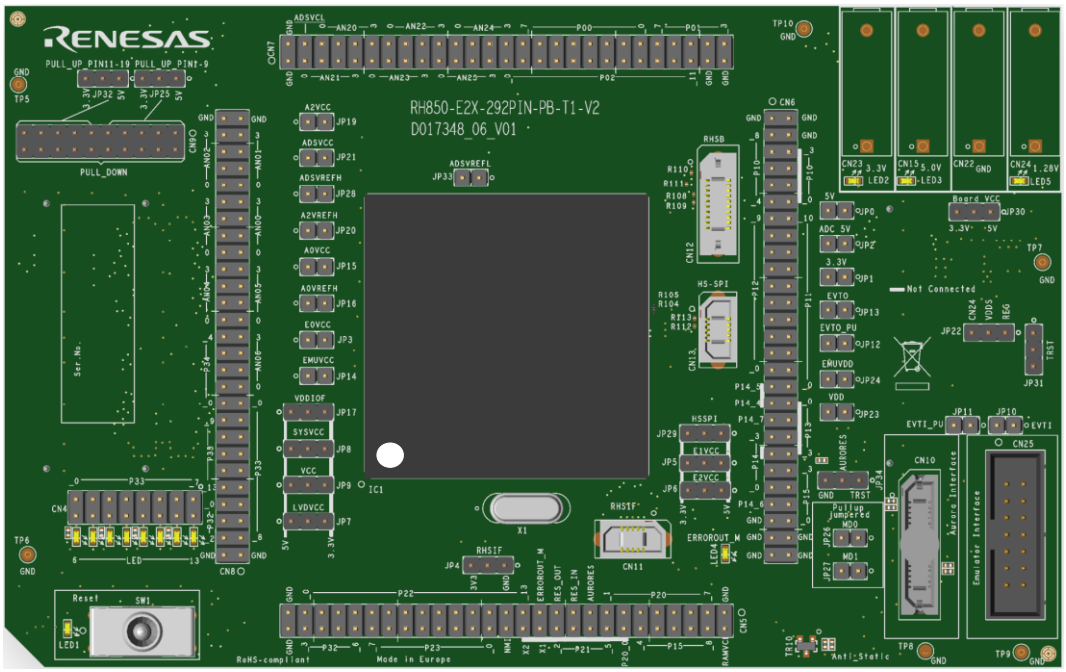


Figure 1.1 Piggyback board top view

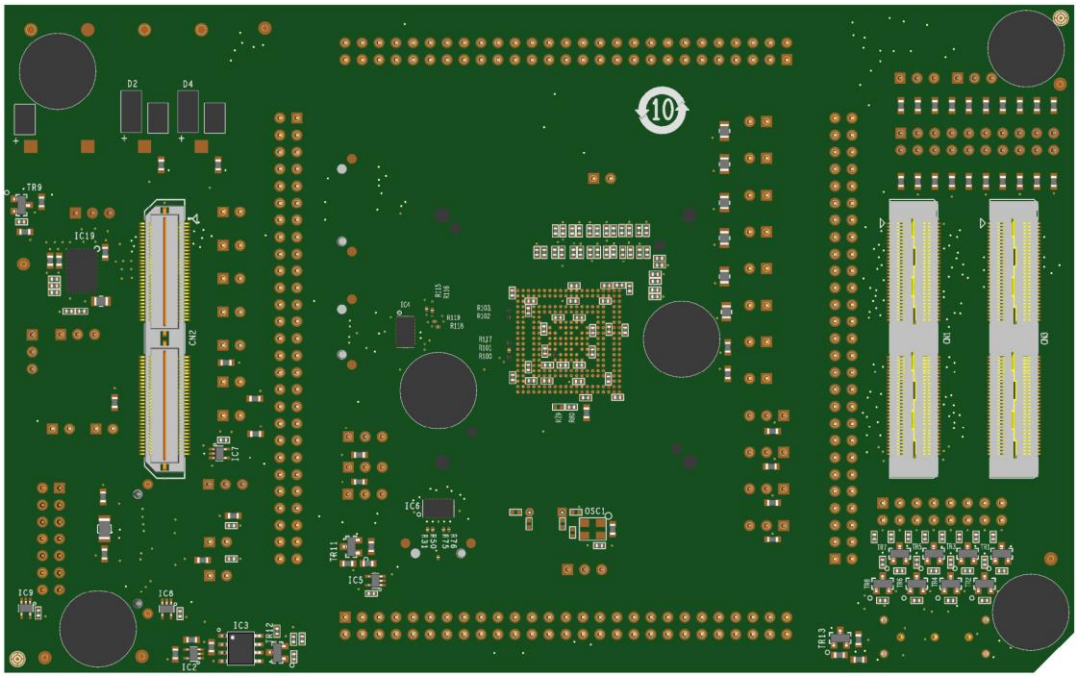


Figure 1.2 Piggyback board bottom view

1.5 Connection of Reset Switch SW1

On pcb revision D017348_06_V01 of Y-RH850-E2X-292PIN-PB-T1-V2 piggyback board the connection of the reset generator IC3 (pin 2) to the reset switch SW1 (pin 2) is missing. Below pictures show how the modification is done. Please make sure this modification has been applied to your pcb.

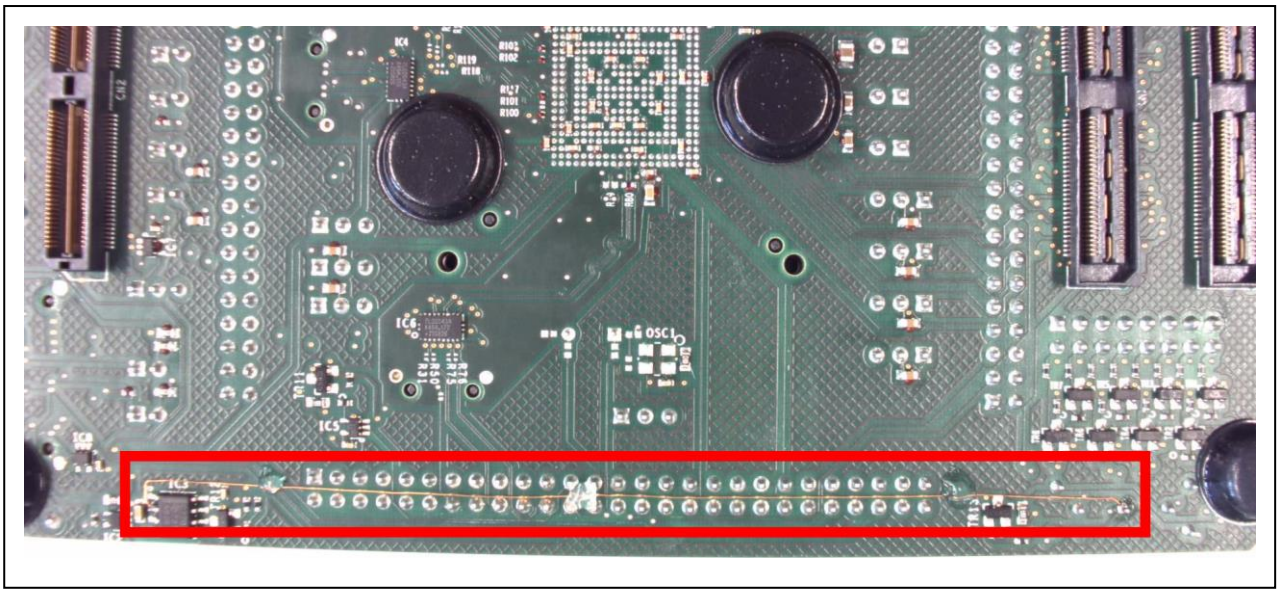


Figure 1.3 Connection of reset generator IC3 to reset switch SW1, total view

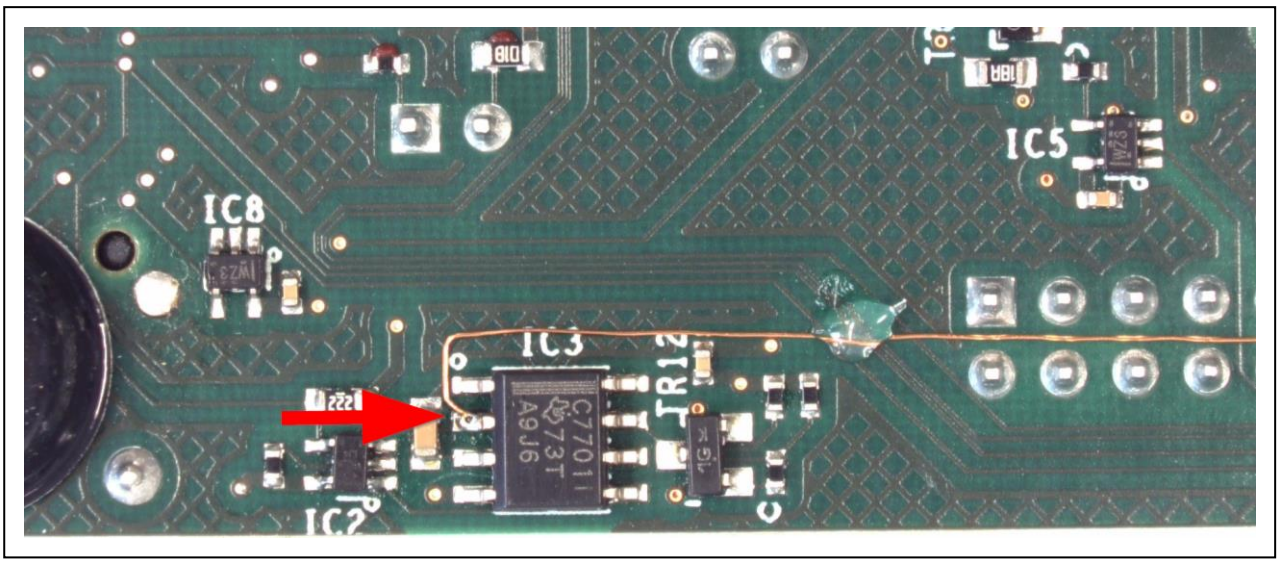


Figure 1.4 Detail view: connection to reset generator IC3

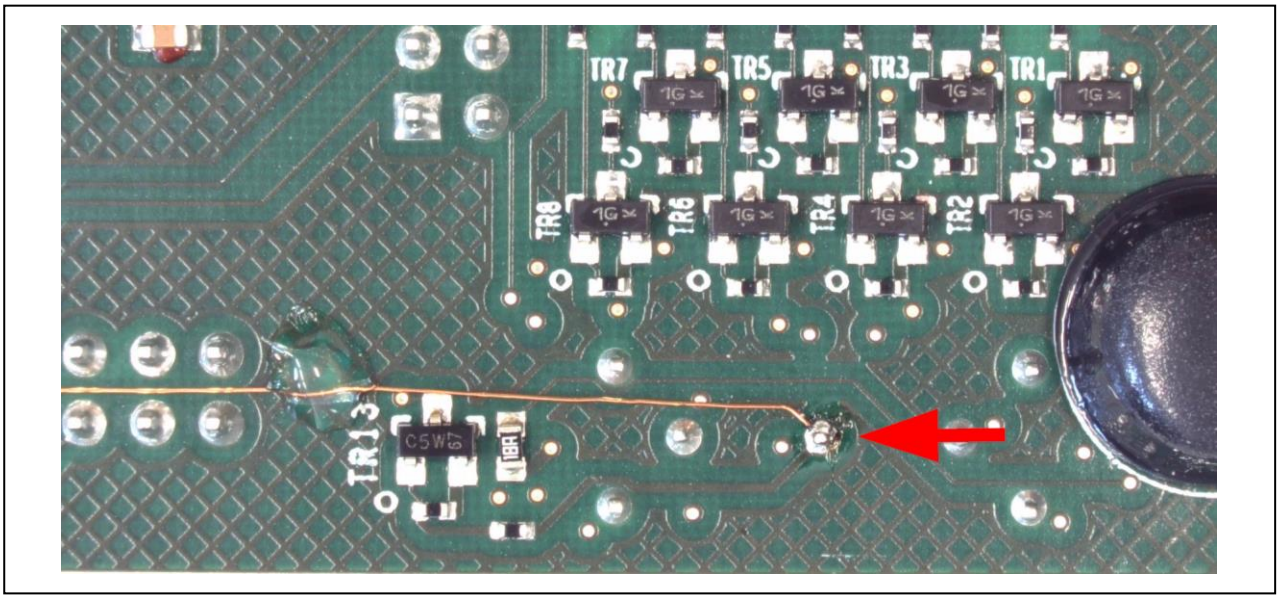


Figure 1.5 Detail view: connection to reset switch SW1

1.6 Mounting of the Device

The Y-RH850-E2X-292PIN-PB-T1-V2 piggyback board features a socket for mounting of the device. All E2x in BGA-292 package do fit into the available Enplas OTB-292(962RS)-0.8-019S-00 socket

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking of the socket.

The A1pin of the socket is marked with a circle near to the “IC1” label (see also white point in *Figure 1.1 Piggyback board top view*).
The A1 pin of the device is marked by a white triangle on the package (see white circle in the figure below).

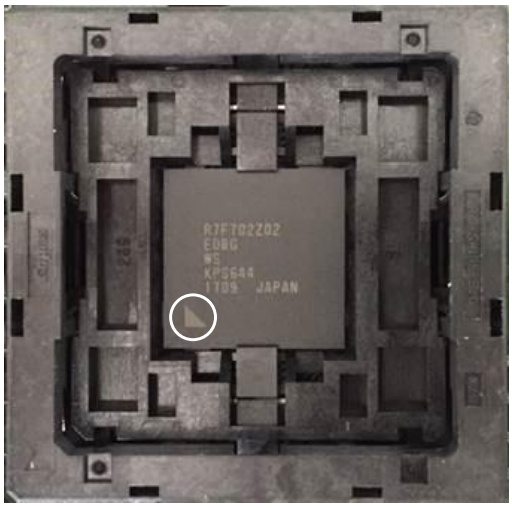


Figure 1.6 Enplas OTB-292(962R)-0.8-019S-00 socket with mounted device

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figure below.

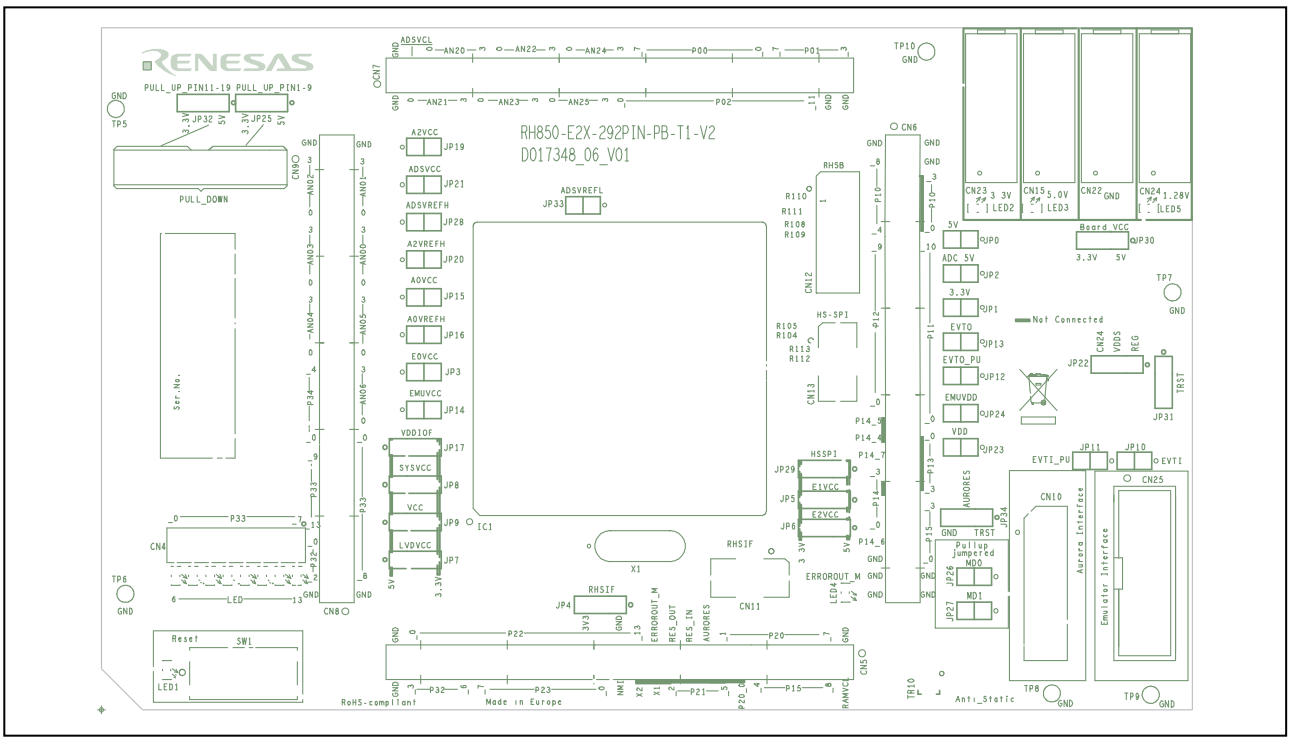


Figure 2.1 Placement of jumpers, connectors and LEDs

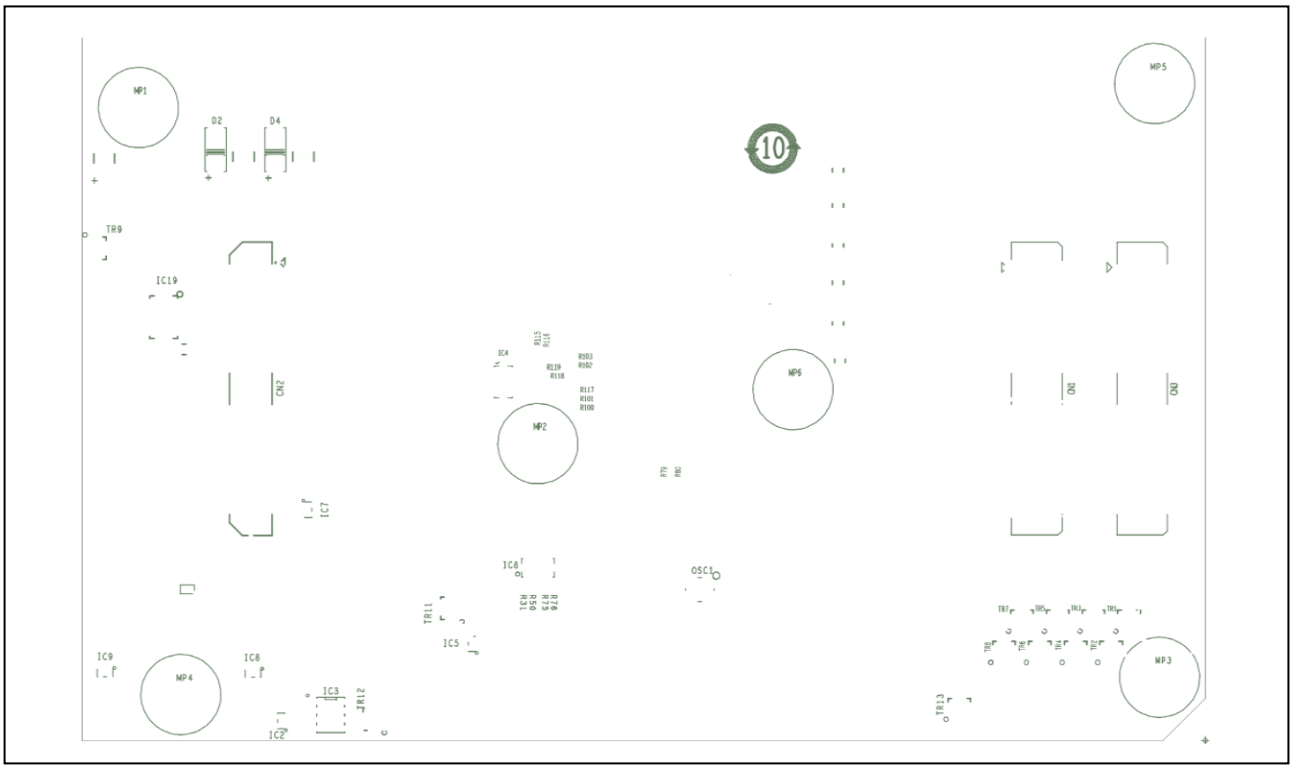


Figure 2.2 Placement of connectors on bottom side

2.1 Jumpers Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumpers overview

Jumper	Function	Remark
JP0	Current measurement bridge of 5.0 V power rail	refer to *3.4 Current Measurement Bridges*
JP1	Current measurement bridge of 3.3 V power rail	
JP2	Current measurement bridge of 5.0 V A/D Converter power supply	
JP3	Voltage selection for E0VCC • JP3[2-1]: 5.0 V	refer to *3.2 Voltage Distribution*
JP4	RHSIF I/F Rx/Tx signals swap • JP4[2-1]: RXDP/RXDN on pins 7 and 9 of CN11, TXDP/TXDN on pins 1 and 3 of CN11 • JP4[2-3]: TXDP/TXDN on pins 7 and 9 of CN11, RXDP/RXDN on pins 1 and 3 of CN11	refer to *5.56.3 Pull-Up/Pull-Down Pin Header CN9*
JP5	Voltage selection for E1VCC • JP5[2-1]: 5.0 V • JP5[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP6	Voltage selection for E2VCC • JP6[2-1]: 5.0 V • JP6[2-3]: 3.3 V	
JP7	Voltage selection for LVDVCC • JP7[2-1]: 5.0 V • JP7[2-3]: 3.3 V	
JP8	Voltage selection for SYSVCC • JP8[2-1]: 5.0 V • JP8[2-3]: 3.3 V	
JP9	Voltage selection for VCC • JP9[2-1]: 5.0 V • JP9[2-3]: 3.3 V	
JP10	Connect EVTI to P33_8	refer to *5.1 Debug and Flash Programming Interfaces*
JP11	Enable pull-up for EVTI • JP11[2-1]: E0VCC	
JP12	Enable pull-up for EVTO • JP12[2-1]: E0VCC	
JP13	Connect EVTO to P33_9	
JP14	Voltage selection for EMUVCC • JP14[2-1]: 3.3 V	refer to *3.2 Voltage Distribution*
JP15	Voltage selection for A0VCC • JP15[2-1]: 5.0 V	
JP16	Voltage selection for A0VREFH • JP16[2-1]: 5.0 V	

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP17	Voltage selection for VDDIOF • JP17[2-1]: 5.0 V • JP17[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP19	Voltage selection for A2VCC • JP19[2-1]: 5.0 V	
JP20	Voltage selection for A2VREFH • JP20[2-1]: 5.0 V	
JP21	Voltage selection for ADSVCC JP21[2-1]: 5.0 V	
JP22	Voltage selection for VDDs * • JP22[2-1]: regulated VDD • JP22[2-3]: external VDD	refer to *3.3 Device Core Voltage (VDD)*
JP23	VDDs enable for VDD * • JP23[2-1]: enable VDD	
JP24	VDDs enable for EMUVDD * • JP24[2-1]: enable EMUVDD	
JP25	Voltage selection for Pull-up/Pull-down pin header CN9 pins 1, 3, 5, 7, 9 • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V	refer to *5.8 Pull-Up/Pull-Down Pin* Header
JP26	MD0 connection • JP26[2-1]: SYSVCC	refer to *5.2 Operation Mode Selection*
JP27	MD1 selection • JP27[2-1]: SYSVCC • OPEN: GND	
JP28	Voltage selection for ADSVREFH JP28[2-1]: 5.0 V	refer to *3.2 Voltage Distribution*
JP29	HS-SPI I/F Rx/Tx signals swap • JP29[2-1]: RXDP/RXDN on pins 8 and 10 of CN13, TXDP/TXDN on pins 2 and 4 of CN13 • JP29[2-3]: TXDP/TXDN on pins 8 and 10 of CN13, RXDP/RXDN on pins 2 and 4 of CN13	refer to *5.7 High Speed SPI I/F (HS-SPI)*
JP30	Voltage selection for BOARD_VCC • JP30[2-1]: 5.0 V • JP30[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP31	TRST control on debug connector CN25 • JP31[2-1]: pull-up to SYSVCC • JP31[2-3]: control by emulator, pull-down to GND	refer to *5.1 Debug and Flash Programming Interfaces*
JP32	Voltage selection for Pull-up/Pull-down pin header CN9 pins 11, 13, 15, 17, 19 • JP32[2-1]: 5.0 V • JP32[2-3]: 3.3 V	refer to *5.8 Pull-Up/Pull-Down Pin Header*
JP33	GND connection for ADSVREFL	refer to *3.2 Voltage Distribution*

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP34	AURORES output • JP34[2-1]: TRST • JP34[2-3]: GND	refer to *5.1 Debug and Flash Programming Interfaces*

Note: * Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

2.2 Connectors Overview

The following table provides an overview of all connectors.

Table 2.2 Connectors overview

Connector	Function	Remark
CN1	Main Board connectors	refer to *6.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN4	Signaling LEDs pin header	refer to *5.4 Signaling LEDs*
CN5	Device ports connectors	refer to *6.2 Device Ports Connectors CN5 to CN8*
CN6		
CN7		
CN8		
CN9	Pull-up/Pull-down pin header	refer to *6.3 Pull-Up/Pull-Down Pin Header CN9*
CN10	Aurora I/F	refer to *6.4 Aurora Connector CN10*
CN11	RHSIF connector	refer to *6.5 RHSIF Connector CN11*
CN12	RHSB connector	refer to *6.6 RHSB Connector CN12*
CN13	HS-SPI connector	refer to *6.7 HS-SPI Connector CN13*
CN15	+5.0 V external power supply	refer to *3.1 Board Power Connection*, connectors are not assembled on the board
CN22	GND for external power supply	
CN23	+3.3 V external power supply	
CN24	+1.28 V external power supply *	
CN25	Debug connector	refer to *6.8 Debug Connector CN25*

Note: * Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

2.3 LED Overview

The following table provides an overview of all LED.

Table 2.3 LED overview

LED	Function	Color	Remark
LED1	Reset switch SW1 on	red	
LED2	3.3 V power supply P3V3	green	refer to *3.5 Power Supply LEDs*
LED3	5.0 V power supply P5V0	green	refer to *3.5 Power Supply LEDs*
LED4	Device ERROROUT signal	red	
LED5	1.28 V device core voltage VDD	green	refer to *3.5 Power Supply LEDs*
LED6	Signaling LED	yellow	connection via CN4, refer to *5.4 Signaling LEDs*
LED7	Signaling LED		
LED8	Signaling LED		
LED9	Signaling LED		
LED10	Signaling LED		
LED11	Signaling LED		
LED12	Signaling LED		
LED13	Signaling LED		

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5 V in case some ports shall be operated with 5 V I/O voltage
- 1.28 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm ‘banana-type’ connectors are used to connect external power supplies:
  - black connector CN22 for GND (VSS)
  - red connector CN15 for 5 V
  - red connector CN23 for 3.3 V
  - red connector CN24 for 1.28 V
    Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

These connectors are not assembled at delivery of the board, but separately supplied with the board package.

For each supply voltage (5.0 V, 3.3 V, 1.28 V) the board has a green LED (LED3, LED2, LED5) indicating the working power supply. The LED are placed directly beside the corresponding power supply connector.

In case the piggyback board is mounted on a Main Board, all voltages except for 1.28 V (VDD) are supplied by the Main Board.

CAUTION

Do not supply the 5 V (CN15) and 3.3 V (CN23) voltage directly to the piggyback board in case it is mounted on the Main Board.

Connecting external 1.28 V via CN24 (and GND via CN22) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in chapter *7. Jumper Configuration Examples*.

.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC	5 V	Power supply for I/O ports
E1VCC, E2VCC	3.3 V, 5 V	
LVDVCC	3.3 V, 5 V	Power supply for LVDS ports
SYSVCC	3.3 V, 5 V	Power supply for • System Logic and internal voltage regulator power • I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	Power supply for on-chip Switching Voltage Regulator (SVR)
EMUVCC	3.3 V	Emulation and Instrumentation RAM, Aurora
EMUVDD	1.28 V *	
A0VCC, A2VCC	5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH,	5 V	
VDD	1.28 V *	Core supply voltage

Note: * Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

Where indicated above voltages can be selected from 5.0 V or 3.3 V by a set of jumpers.

For details refer to the figure below and *Table 2.1 Jumpers overview*

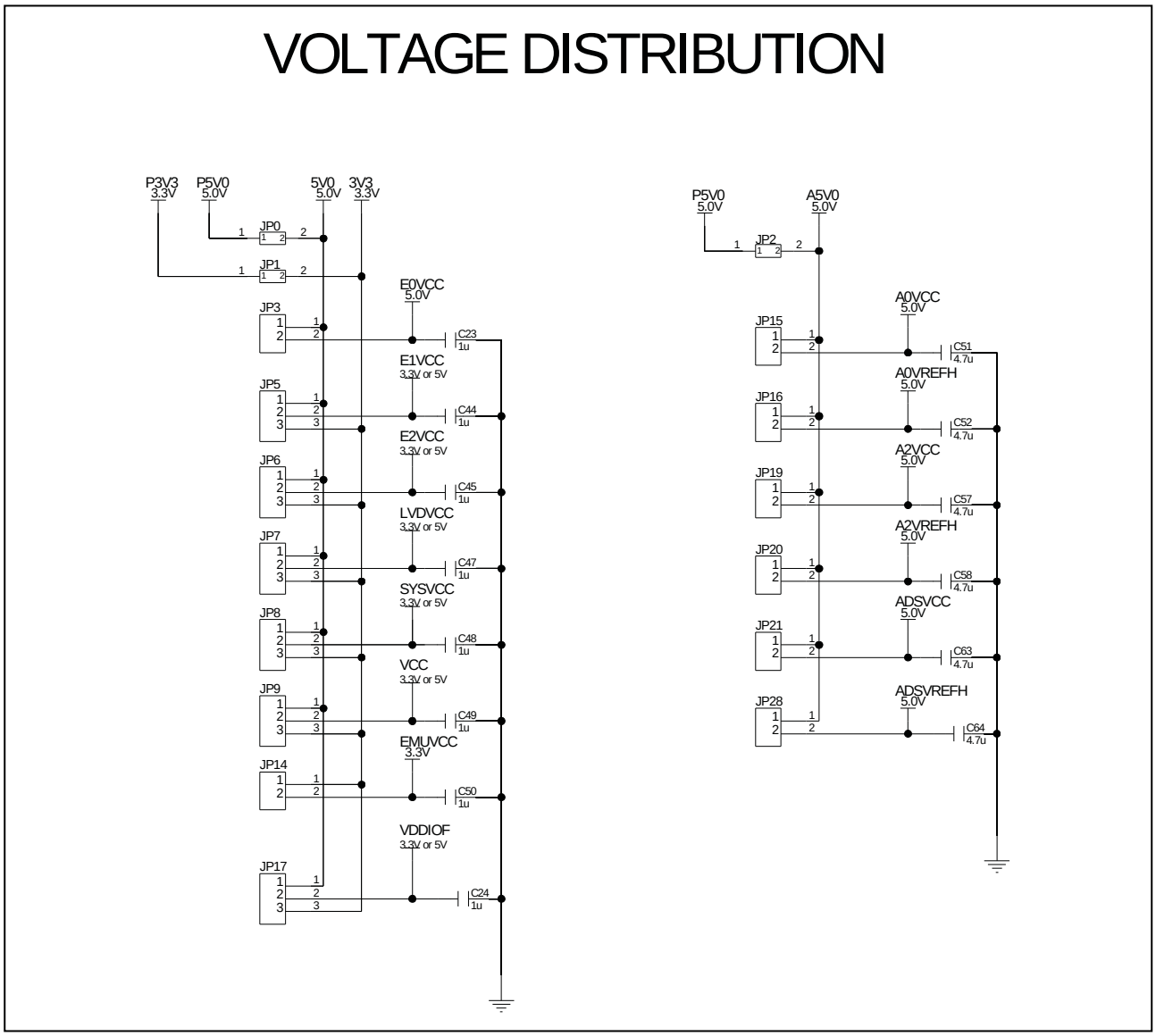


Figure 3.1 Voltage distribution

3.3 Device Core Voltage (VDD)

The piggyback board has an integrated voltage to generate the device core voltage

Note

The IN_1v2 and reg_vcc_VDD voltages have a level of typical 1.28 V, which is higher than the typical device core voltage VDD of 1.25 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

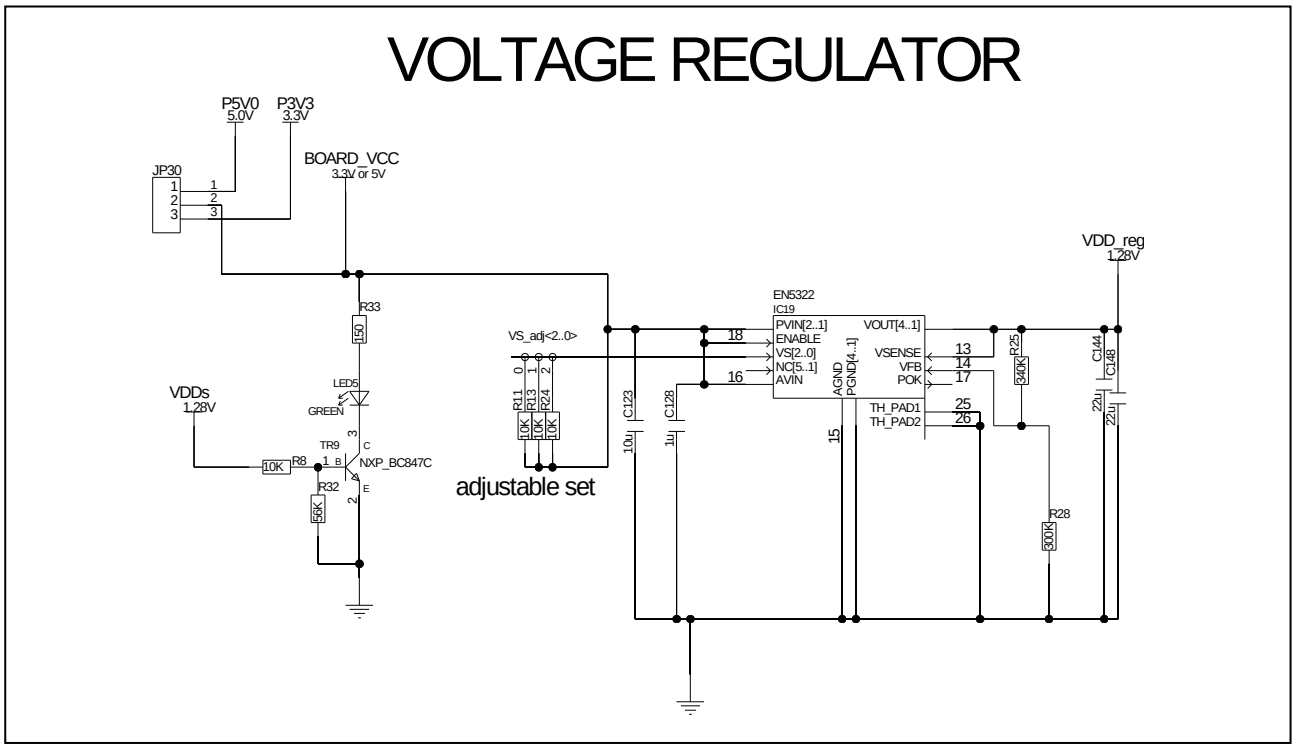


Figure 3.2 Device core voltage regulator

The device core voltage VDD (typ.1.28 V) can be

- supplied from external via CN24 (voltage IN_1v2)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC19 (voltage reg_vcc_VDD)

Selection of the VDD source is achieved by use of jumper JP22:

- JP22[2-1]: VDD = 1.28 V (VDDs) from
  - JP22[2-1]: VDDs = VDD_reg from on-board voltage regulator IC19
  - JP22[2-3]: VDDs = IN_1v2 from external supply CN24

The jumper JP23 and JP24 are used to enable power supply VDD and EMUVDD. Please refer to *Figure 3.3 Device core voltage selection*.

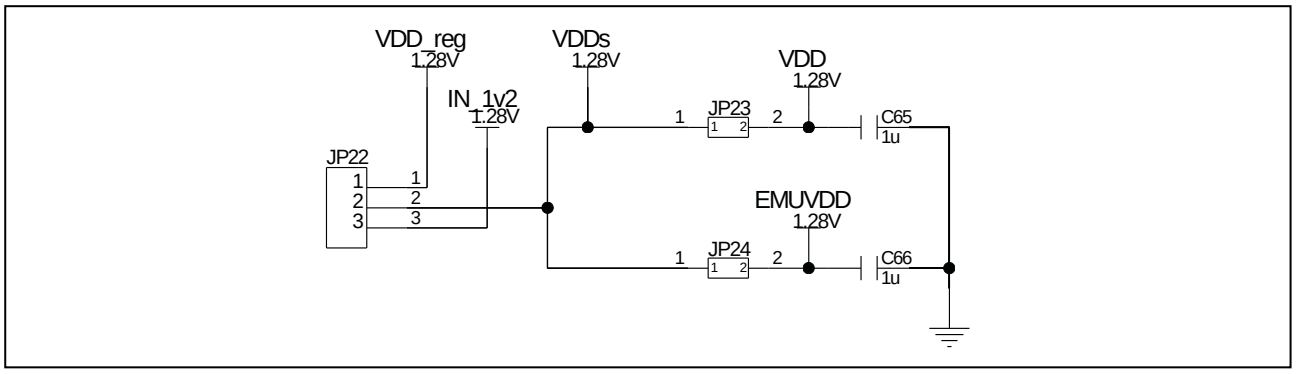


Figure 3.3 Device core voltage selection

3.4 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP0 and JP1 with a current meter.

Accordingly, the total current via the A/D Converter's supply voltage A5V0 can be measured via jumper JP2.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.1 Voltage distribution*.

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED3 for 5.0 V power rail P5V0
- LED2 for 3.3 V power rail P3V3
- LED5 for 1.28 V device core voltage VDD

4. Clock Supply

The device's operation clock can be generated by

- the on-chip oscillator main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals.
- an off-chip oscillator, the clock is fed into the X1 terminal.

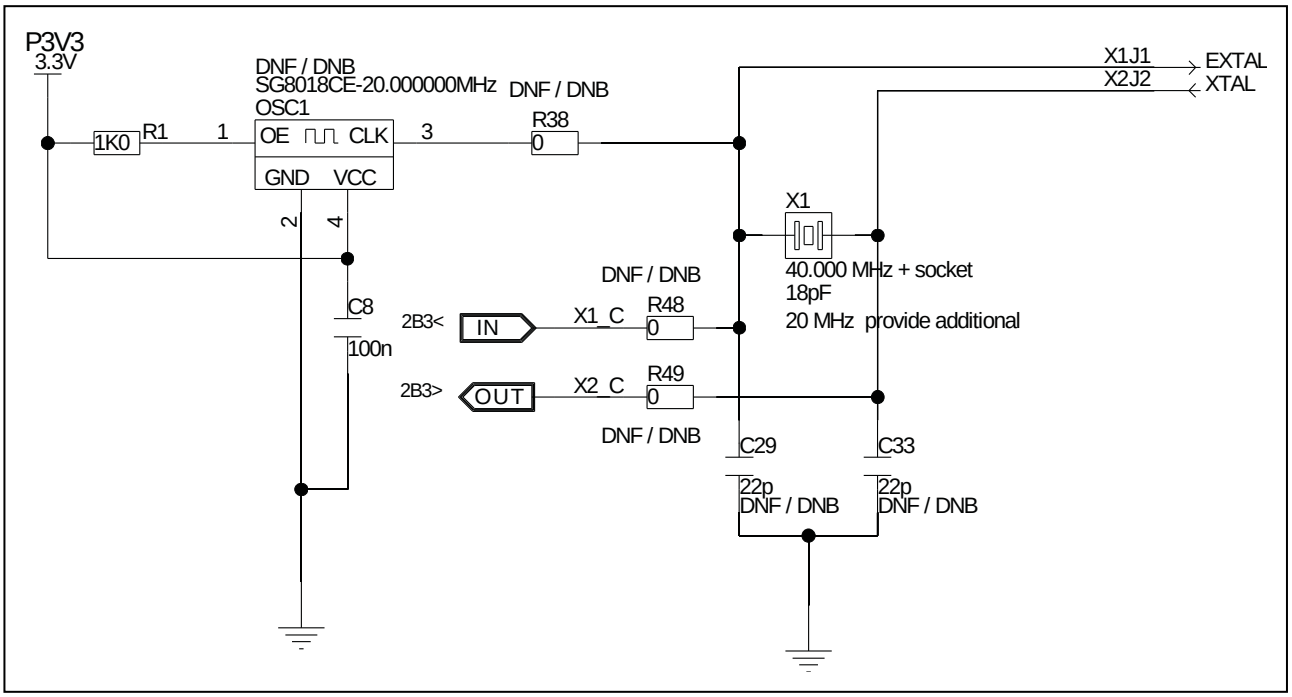


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

An alternative resonator for main oscillator frequency of 20 MHz is included in the board package.

The 40MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be soldered on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R38.

The SG-8018CE is neither mounted on nor provided with the board. For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN5

To minimize disturbance on the resonator signal, the signals X1 and X2 are by default not connected to a pin header. If needed the signals can be connected to CN5 via 0 Ω resistors:

- X1: Pin 24 of CN5 to supply an external clock to the device via R48
- X2: Pin 26 of CN5 for measurement purposes of the clock via R49

5. Other Circuits

5.1 Debug and Flash Programming Interfaces

The Renesas standard emulator for RH850/E2x is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

The piggyback board provides 2 connectors for an emulator.

- CN25: 14-pin connector that can be used for debugging and for programming on-chip flash.
- CN10: 34-pin connector for emulator that support Aurora interface (like Renesas IE850A, Lauterbach emulator, iSystem emulator, …)

5.1.1 Standard Debug and Flash Programming

Connector CN25 can be used for debugging and for programming the on-chip flash of RH850 using E2 emulator. Figure 5.1 shows the pin configuration of this interface.

The signal 'EVTO_TOOL' can be pulled up to 'E0VCC' via JP12. Please refer to the documentation of the used tool, whether this is needed.

The signal 'TRST' can be pulled up to 'SYSVCC' or to the 'TRST' line of the used tool via jumper JP31.

Refer to *6.8 Debug Connector CN25*

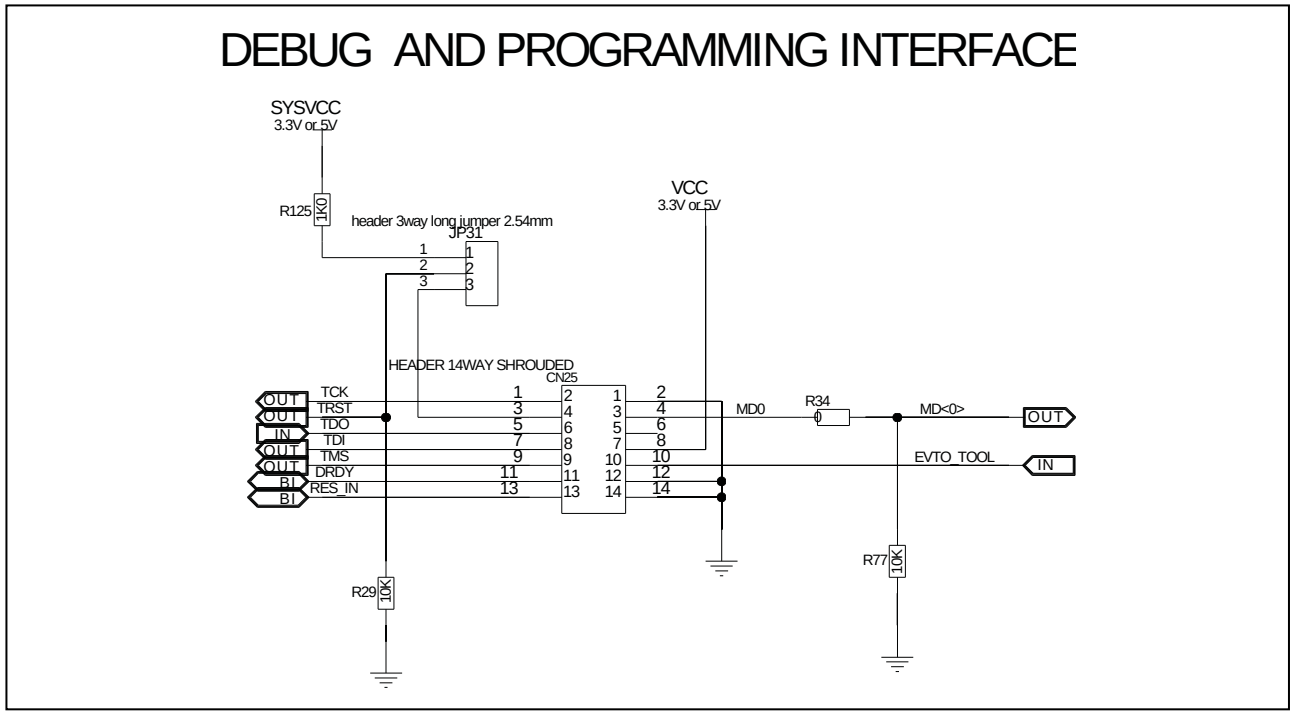


Figure 5.1 debug and flash programming connection

5.1.2 Aurora Trace I/F

CN10 is an Aurora trace interface for debugging. Debugging via Aurora interface is supported by Renesas IE850A emulator and various third-party emulators (e.g. Lauterbach, iSystem, …).

The signal 'EVTO_TOOL' can be pulled up to 'E0VCC' via JP12. Please refer to the documentation of the used tool, whether this is needed.

The signal 'TRST' can be pulled up to 'SYSVCC' or to the 'TRST' line of the used tool via jumper JP31.

Access to the signal AURORES is possible via jumper JP34. With this jumper, AURORES can also be connected to TRST or pulled down to GND.

Refer to *6.4 Aurora Connector CN10*

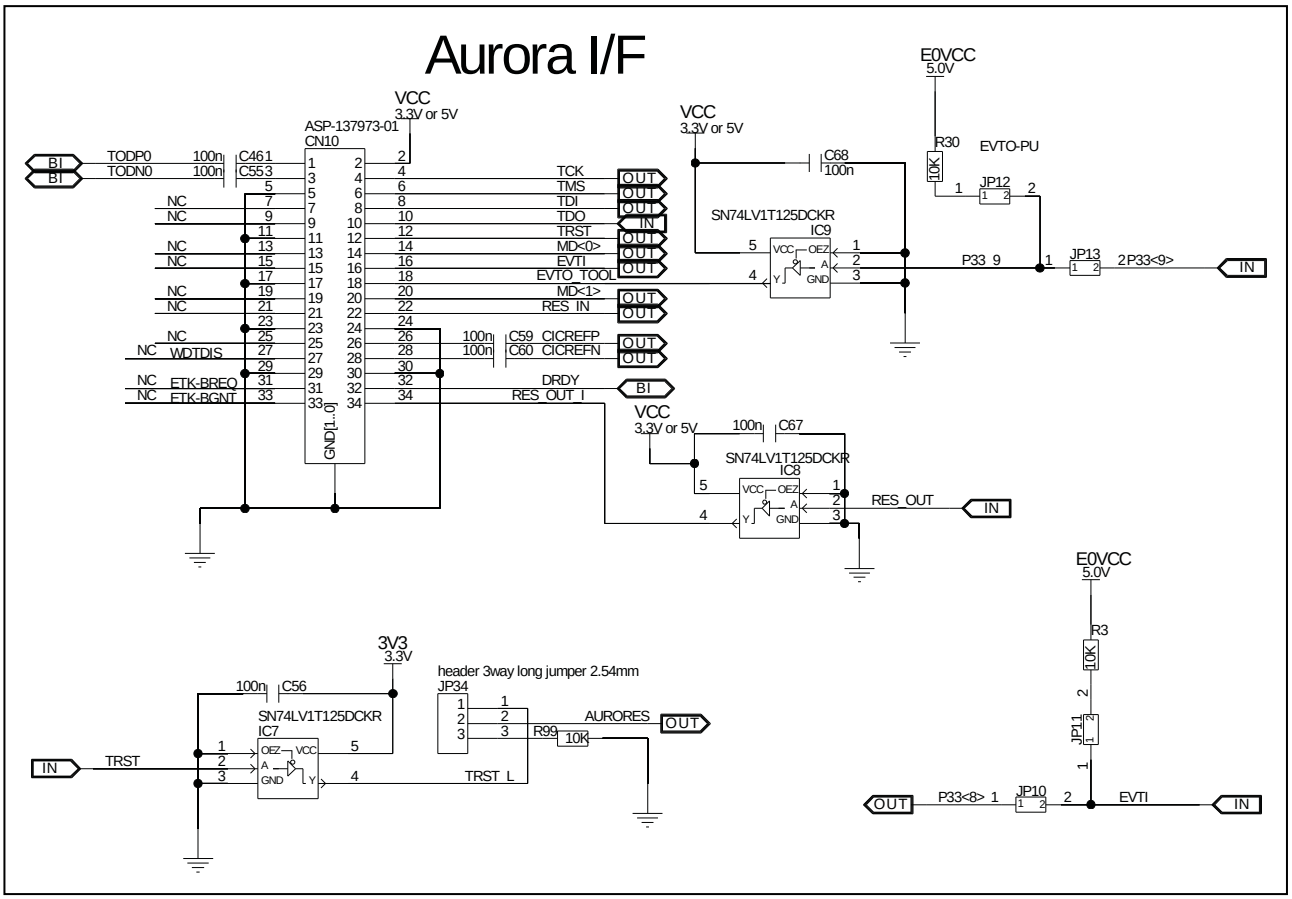


Figure 5.2 debug and flash programming connection

5.2 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode:

Table 5.1 Device operation mode selection jumpers

Jumper	Function
JP26	MD1 pin level • JP26[SHORT]: MD0 = H level • JP26[OPEN]: MD0 – controlled by debugger or programming tool, if a tool is connected via CN10 – GND if no tool connected
JP27	MD1 pin level • JP27[SHORT]: MD1 = H level • JP27[OPEN]: MD1 – controlled by debugger or programming tool if a tool is connected via CN10 or CN25 – GND if no tool connected

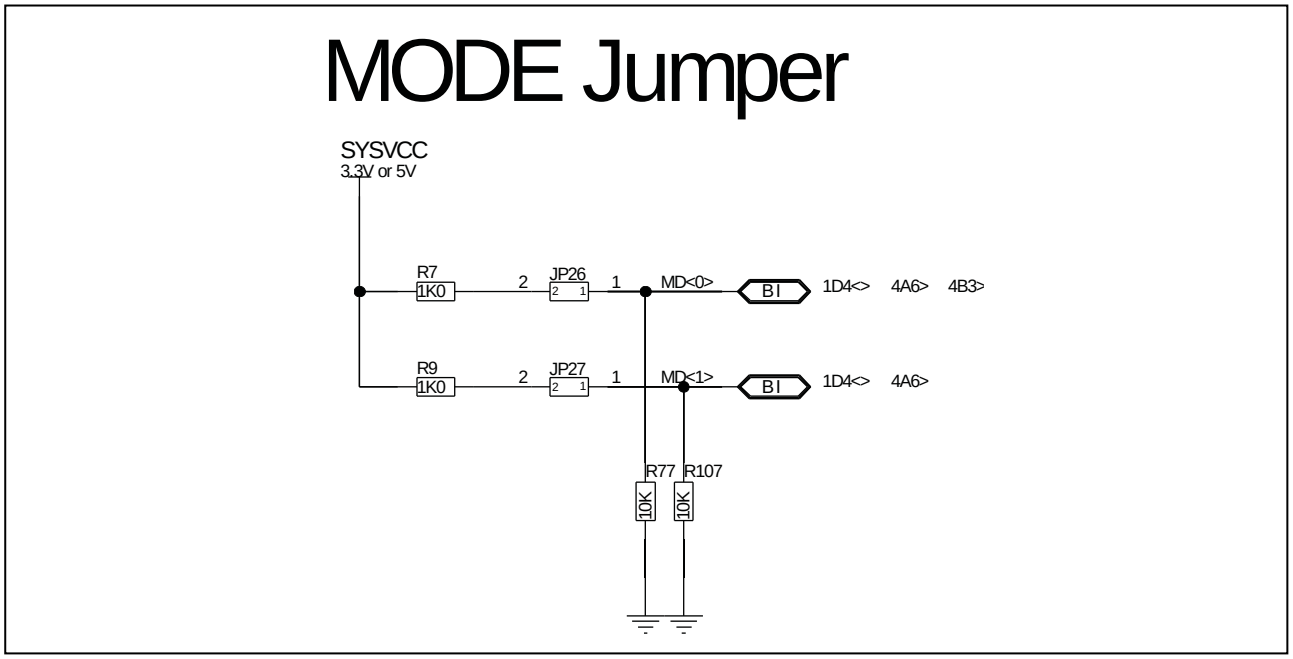


Figure 5.3 Mode signals

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

All jumpers related to the mode selection can be left open.

5.3 RESET Switch

The SW1 is used to issue a RESET to the device.

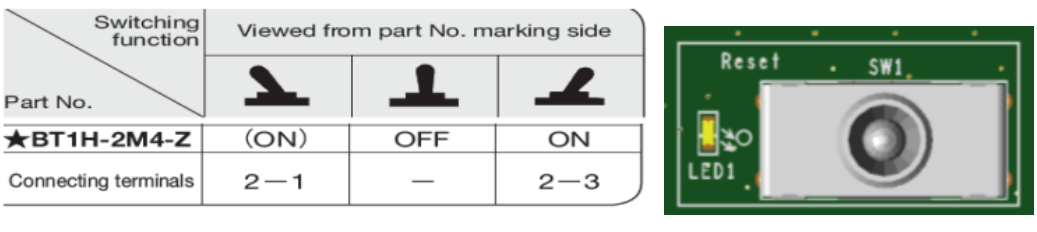


Figure 5.4 Reset switch

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '2-1(ON)' position: temporary reset

Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.

- SW1 in right '2-3 ON' position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The lighted red LED1 indicates that SW1 is "on", i.e. in position '2-1 (ON)' or '2-3 ON'.

Note

LED1 does not light up when RESET is asserted by any other means than SW1.

5.4 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

Device pins P33_0 to P33_7 are connected to the odd pins of the pin header CN4, while the LEDs LED6 to LED13 are connected to the even CN4 pins.

Thus, the LEDs can be either connected to

- the device port pins P33_0 to P33_7 by closing the connection on CN4 using a jumper, or
- any device pin by connecting directly with the even CN4 pins using a separate cable.

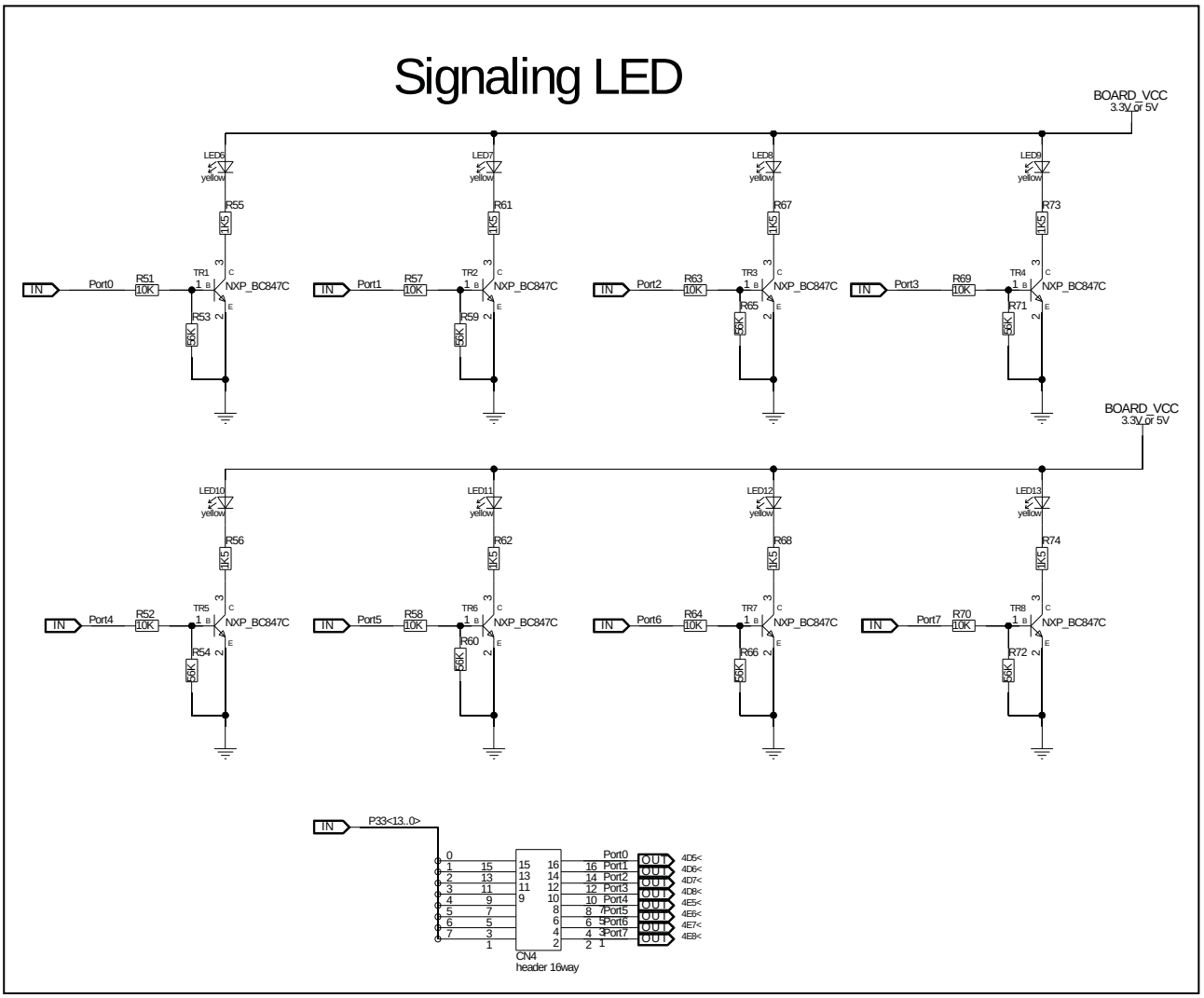


Figure 5.5 Signaling LED

5.5 Renesas High-Speed Serial I/F (RHSIF)

The CN11 connector can be used to connect to the device's RHSIF interface. The connector is a Samtec ‘ERF8-005-05.0-L-DV-L-TR’ type connector

Refer to *6.5 RHSIF Connector CN11* for the CN11 pin assignment.

RHSIF and MSPI0 interface at CN11 are operated in LVDS mode.

Rx and Tx signals available at CN11 can be swapped by setting the jumper JP4:

- JP4[2-1]:
  - RXDP/RXDN at CN11 pins 7 and 9
  - TXDP/TXDN at CN11 pins 1 and 3
- JP4[2-3]:
  - RXDP/RXDN at CN11 pins 1 and 3
  - TXDP/TXDN at CN11 pins 7 and 9

By default, the interface signals are not connected to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN5 (pins #14, 16, 18, 20 and 22) via connecting with 0Ohm resistances R31, R50, R75, R76 and R78. For details, please refer to *10 Schematics*

Notes

1. In order to minimize signal interference no signals from CN5 are connected to CN11. If required they can be connected via 0 Ω resistors R31, R50, R75, R76 and R78.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

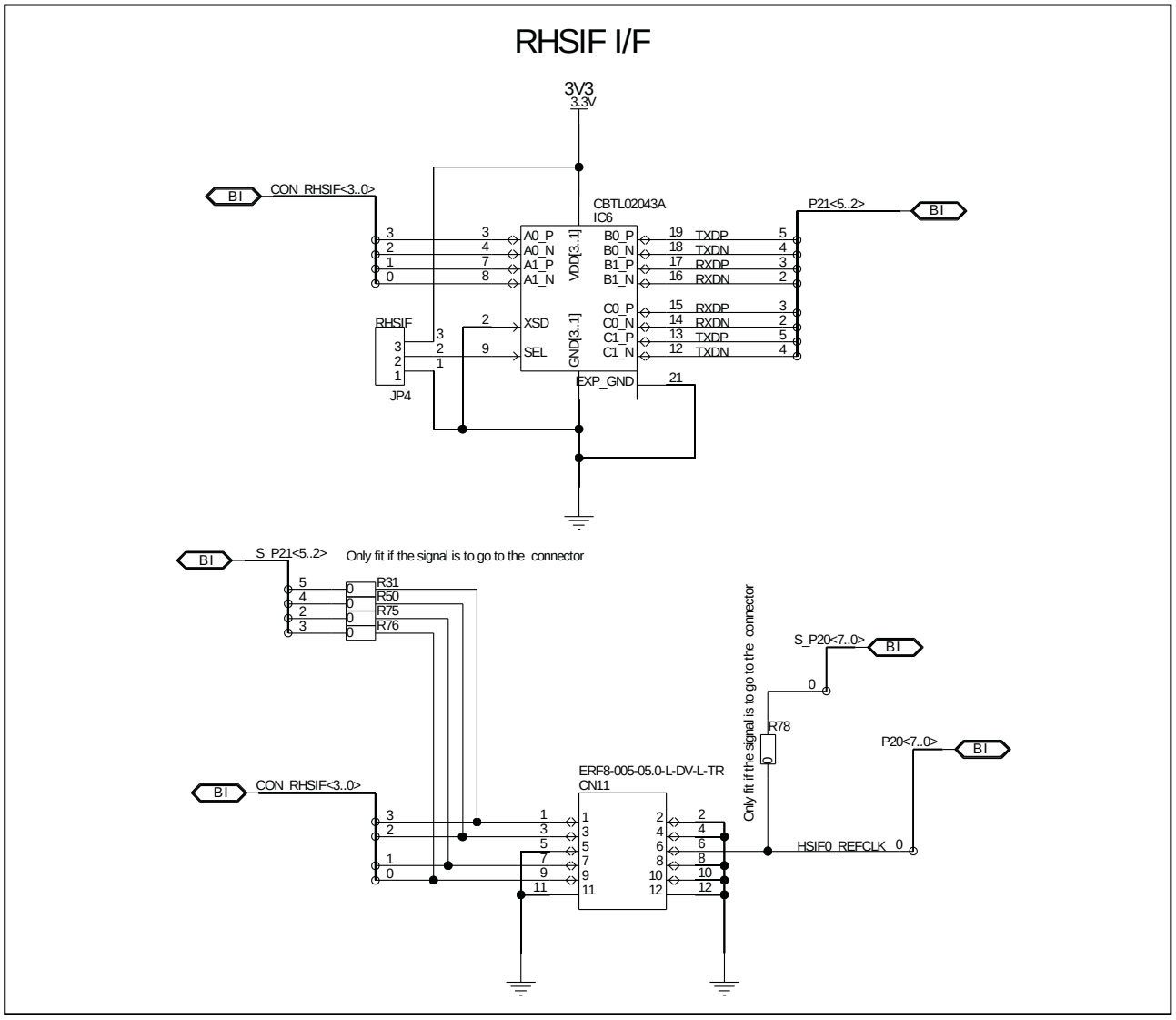


Figure 5.6 RHSIF interface

5.6 Renesas High speed Bus (RHSB)

CN12 is available to connect to the HS-SPI I/F signals of the device. The connector is a Samtec 'ERF8-010-05.0-L-DV-L-TR' type connector.

Refer to *6.6 RHSB Connector CN12* for the CN12 pin assignment.

In order to use RHSB I/F it is necessary to disable LVDS mode.

The signals RHSB0SON and RHSB0SOP on connector CN12 (pins 17 and 19) are by default not directly connected to the corresponding device pins. In order to use these signals for the RHSB I/F CN12 pins #17 and #19 must be connected to the device via 0Ohm resistances R104 and R105. In case of using the HS-SPI I/F (refer to *5.7 High Speed SPI I/F (HS-SPI)*), it is recommended to not apply the latter resistances. This it to minimize signal disturbance.

The signals assigned to CN12 pins #1, 3, 7, 9, 17 and 19 are by default not connected to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN6 (pins #6, 8, 10, 12, 40 and 42) via connecting with 0Ohm resistances R108 – R111 and R115 and R116. Please also consider above note 1. For details, please refer to *10 Schematics*

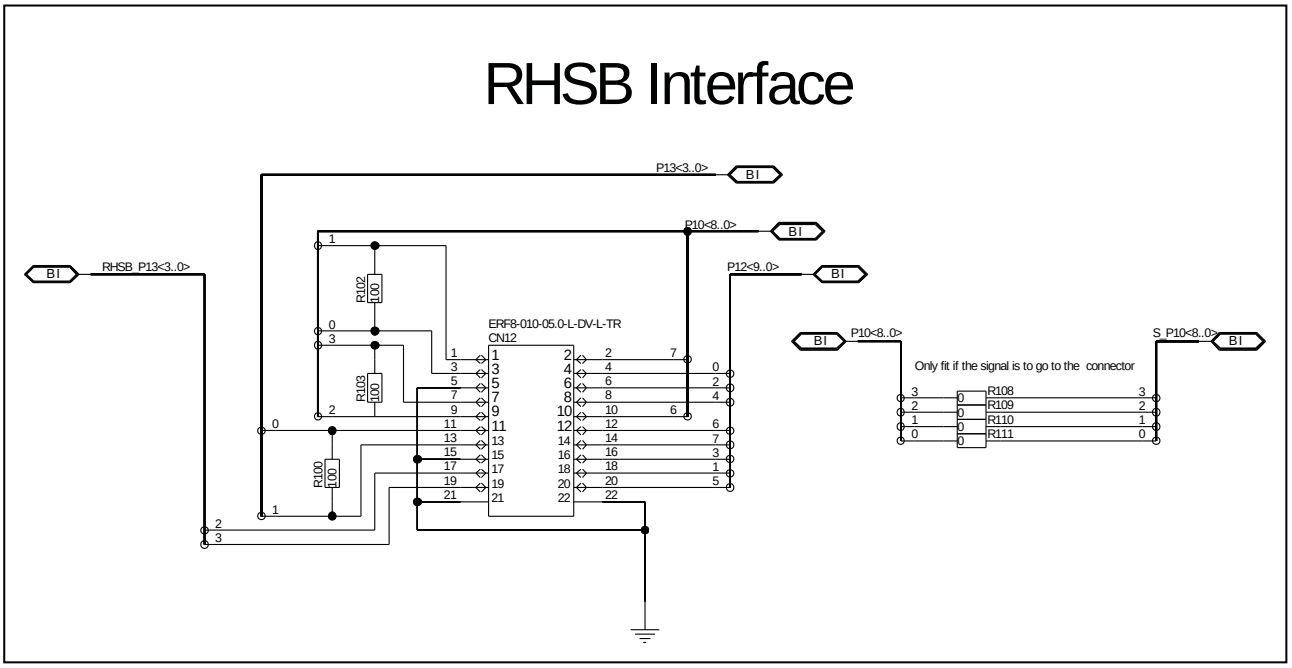


Figure 5.7 RHSB interface

5.7 High Speed SPI I/F (HS-SPI)

CN13 is available to connect to the HS-SPI I/F signals of the device. The connector is a Samtec 'ERF8-005-05.0-L-DV-L-TR' type connector.

Refer to *6.7 HS-SPI Connector CN13* the CN13 pin assignment.

Rx and Tx signals available at CN13 can be swapped by setting the jumper JP29:

- JP29[2-1]:
  - RXDP/RXDN at CN13 pins 8 and 10
  - TXDP/TXDN at CN13 pins 2 and 4
- JP29[2-3]:
  - RXDP/RXDN at CN13 pins 2 and 4
  - TXDP/TXDN at CN13 pins 8 and 10

By default, the interface signals are not connected ted to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN6 (pins #33, 35, 36, 38, and 40 – 42) via connecting with 0Ohm resistances R112, R113, R115, R116, R118 and R119. For details, please refer to *10 Schematics*.

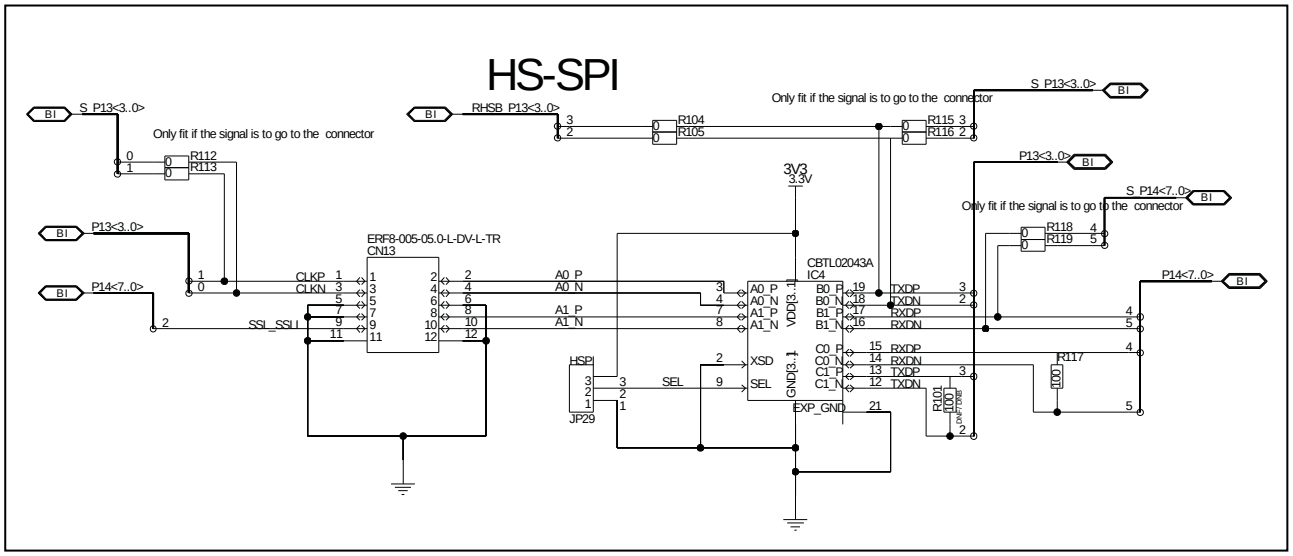


Figure 5.8 HS-SPI interface

5.8 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN9 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN9 pin to the signal via a separate cable.

The CN9 pins have following pull-up or pull-down voltage levels:

- all even numbered pins are connected to L level, i.e. to GND
- odd numbered pins 1, 3, 5, 7, 9 can be connected to
  - 5.0 V, if JP25[2-1] is set
  - 3.3 V, if JP25[2-3] is set
- odd numbered pins 11, 13, 15, 17, 19 can be connected to
  - 5.0 V, if JP32[2-1] is set
  - 3.3 V, if JP32[2-3] is set

Refer to *6.3 Pull-Up/Pull-Down Pin Header CN9*

6. Connectors

6.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a Main Board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the Main Board, please refer to the User's Manual of any supported Main Board.

Refer to *1.2 Supported Main Boards* for a list of supported Main Boards.

6.1.1 Main Board Connector CN1

Table 6.1 Main board connector CN1

Pin	Main Board function	Piggyback board device port	Pin	Main Board function	Piggyback board device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RES_IN	6	NMI	NMI
7	WAKE	–	8	–	–
9	INT0	P15_3	10	INT1	P15_6
11	INT2	P10_4	12	INT3	P10_8 (IRQ4)
13	–	–	14	–	–
15	UART0TX	P22_11	16	UART1TX	P02_1
17	UART0RX	P22_12	18	UART1RX	P02_4
19	LIN0TX	P34_0	20	LIN1TX	P33_12
21	LIN0RX	P34_2	22	LIN1RX	P33_10
23	IIC0SCL	–	24	IIC1SCL	–
25	IIC0SDA	–	26	IIC1SDA	–
27	CAN0TX	P32_1 (CTX2)	28	CAN1TX	P15_2
29	CAN0RX	P32_0 (CRX2)	30	CAN1RX	P15_1
31	SENT0IN	P00_2 (RSENT1RX)	32	SENT1IN	P01_4 (RSENT2RX)
33	SENT0OUT	P02_9 (RSENT1SPCO)	34	SENT1OUT	P02_05 (RSENT2SPCO)
35	PSI50RX	P00_3	36	PSI51RX	–
37	PSI50TX	P00_4	38	PSI51TX	–
39	PSI50Sync	–	40	PSI51Sync	–
41	FLX0TX	P22_9	42	FLX0EN	P22_6
43	FLX0RX	P22_4	44	FLXSTPWT	–
45	FLX1TX	P22_1	46	FLX1EN	P22_5
47	FLX1RX	P22_2	48	FLX	–
49	–	–	50	–	–
51	ETH0MDIO	P12_3	52	ETH0MDC	P12_0

Table 6.1 Main board connector CN1 (cont'd)

Pin	Main Board function	Piggyback board device port
53	ETH0RXD0	P12_7
55	ETH0RXD1	P12_5
57	ETH0RXD2	P11_6
59	ETH0RXD3	P11_10
61	ETH0RXCLK	P12_2
63	ETH0RXER	P12_6
65	ETH0CRSDV	P11_8
67	ETH0RXDV	P12_9
69	ETH0RESET	P12_1
71	–	–
73	USB0UDMF	–
75	USB0UDPF	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P00_7
87	DIGIO_2	P01_5
89	DIGIO_4	P01_7
91	DIGIO_6	P02_6
93	DIGIO_8	P02_8
95	DIGIO_10	P02_11
97	DIGIO_12	P14_0
99	DIGIO_14	P14_3
101	–	–
103	MUX0	P34_0
105	MUX2	P34_1
107	ADC0	AN03_1
109	ADC2	AN04_2
111	ADC4	AN05_1
113	ADC6	AN06_0
115	VDDIOF	VDDIOF
117	VDDB	P3V3
119	VDDB	P3V3
121	–	GND
123	–	GND
125	–	GND
127	–	GND

Pin	Main Board function	Piggyback board device port
54	ETH0TXD0	P11_7
56	ETH0TXD1	P11_9
58	ETH0TXD2	P11_3
60	ETH0TXD3	P11_1
62	ETH0TXCLK	P11_4
64	ETH0TXER	P11_2
66	ETH0TXEN	P11_0
68	ETH0COL	P12_4
70	ETH0LINK	P12_8
72	–	–
74	USB0UDMH	–
76	USB0UDPH	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P01_3
88	DIGIO_3	P01_6
90	DIGIO_5	P02_3
92	DIGIO_7	P02_7
94	DIGIO_9	P02_10
96	DIGIO_11	P11_5
98	DIGIO_13	P14_1
100	DIGIO_15	P14_7
102	–	–
104	MUX1	P34_2
106	–	–
108	ADC1	AN04_0
110	ADC3	AN05_0
112	ADC5	AN05_3
114	ADC7	AN06_1
116	VDDIOF	VDDIOF
118	VDDB	P3V3
120	VDDB	P3V3
122	–	GND
124	–	GND
126	–	GND
128	–	GND

6.1.2 Main Board Connector CN2

Table 6.2 Main board connector CN2

Pin	Function	Device port
1	CAN2TX	P02_0
3	CAN2RX	P02_2
5	CAN4TX	P15_7
7	CAN4RX	P15_8
9	LIN2TX	P10_5
11	LIN2RX	P10_6
13	LIN4TX	P00_4
15	LIN4RX	P00_5
17	LIN6TX	–
19	LIN6RX	–
21	LIN8TX	–
23	LIN8RX	–
25	LIN10TX	–
27	LIN10RX	–
29	LIN12TX	–
31	LIN12RX	–
33	LIN14TX	–
35	LIN14RX	–
37	–	–
39	–	–
41	–	–
43	–	–
45	–	–
47	CAN6TX	–
49	CAN6RX	–
51	–	–
53	–	–
55	–	–
57	–	–
59	–	–
61	–	–
63	–	–
65	–	–
67	–	–
69	–	–
71	–	–
73	–	–
75	–	–

Pin	Function	Device port
2	CAN3TX	P32_6
4	CAN3RX	P32_4
6	CAN5TX	–
8	CAN5RX	–
10	LIN3TX	P00_0
12	LIN3RX	P00_1
14	LIN5TX	P33_9
16	LIN5RX	P33_8
18	LIN7TX	–
20	LIN7RX	–
22	LIN9TX	–
24	LIN9RX	–
26	LIN11TX	–
28	LIN11RX	–
30	LIN13TX	–
32	LIN13RX	–
34	LIN15TX	–
36	LIN15RX	–
38	–	–
40	–	–
42	–	–
44	–	–
46	–	–
48	CAN7TX	–
50	CAN7RX	–
52	–	–
54	–	–
56	–	–
58	–	–
60	–	–
62	–	–
64	–	–
66	–	–
68	–	–
70	–	–
72	–	–
74	–	–
76	–	–

Table 6.2 Main board connector CN2 (cont'd)

Pin	Function	Device port	Pin	Function	Device port
77	–	–	78	–	–
79	–	–	80	–	–
81	–	–	82	–	–
83	–	–	84	–	–
85	–	–	86	–	–
87	–	–	88	–	–
89	–	–	90	–	–
91	–	–	92	–	–
93	–	–	94	–	–
95	–	–	96	–	–
97	–	–	98	–	–
99	–	–	100	–	–
101	–	–	102	–	–
103	–	–	104	–	–
105	–	–	106	–	–
107	–	–	108	–	–
109	–	–	110	–	–
111	–	–	112	–	–
113	–	–	114	–	–
115	–	–	116	–	–
117	–	–	118	–	–
119	–	–	120	–	–
121	–	GND	122	–	GND
123	–	GND	124	–	GND
125	–	GND	126	–	GND
127	–	GND	128	–	GND

6.1.3 Main Board Connector CN3

Table 6.3 Main board connector CN3

Pin	Function	Device port	Pin	Function	Device port
1	–	–	2	–	–
3	–	–	4	–	–
5	–	–	6	–	–
7	–	–	8	–	–
9	–	–	10	CSI1CS1	P20_2
11	–	–	12	–	–
13	–	–	14	–	–
15	–	–	16	–	–

Table 6.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
17	–	–
19	–	–
21	CSI1CS2	P20_4
23	–	–
25	–	–
27	–	–
29	CSI1SCLK	P20_3
31	–	–
33	–	–
35	–	–
37	–	–
39	–	P22_3
41	–	–
43	–	–
45	–	–
47	–	–
49	–	–
51	–	–
53	–	–
55	–	–
57	–	–
59	–	–
61	–	–
63	–	–
65	–	–
67	–	–
69	–	–
71	–	–
73	–	–
75	–	–
77	–	–
79	–	–
81	–	–
83	–	–
85	–	–
87	–	–
89	–	–
91	–	–
93	–	–

Pin	Function	Device port
18	–	–
20	–	–
22	CSI1CS3	P20_5
24	–	–
26	DIGIO_24	P22_0
28	CSI1SO	P20_6
30	CSI1SI	P20_7
32	–	–
34	–	–
36	–	–
38	–	–
40	–	–
42	–	–
44	–	–
46	–	–
48	–	–
50	–	–
52	–	–
54	–	–
56	–	–
58	–	–
60	–	–
62	–	–
64	–	–
66	–	–
68	–	–
70	–	–
72	–	–
74	–	–
76	–	–
78	–	–
80	–	–
82	–	–
84	–	–
86	–	–
88	–	–
90	–	–
92	–	–
94	–	–

Table 6.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
95	–	–
97	–	–
99	–	–
101	–	–
103	–	–
105	–	–
107	–	–
109	–	–
111	–	–
113	–	–
115	–	–
117	–	–
119	–	–
121	–	GND
123	–	GND
125	–	GND
127	–	GND

Pin	Function	Device port
96	–	–
98	–	–
100	–	–
102	–	–
104	–	–
106	–	–
108	–	–
110	–	–
112	–	–
114	–	–
116	–	–
118	–	–
120	–	–
122	–	GND
124	–	GND
126	–	GND
128	–	GND

6.2 Device Ports Connectors CN5 to CN8

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

6.2.1 Device Ports Connector CN5

Table 6.4 Device ports connector CN5

Pin	Device port	Pin	Device port
1	GND	2	RAMSVCL
3	P20_7	4	P15_8
5	P20_6	6	P15_7
7	P20_5	8	P15_6
9	P20_4	10	P15_5
11	P20_3	12	P15_4
13	P20_2	14	S_P20_0 *
15	P20_1	16	S_P21_5 *
17	AURORES	18	S_P21_4 *
19	RES_IN	20	S_P21_3 *
21	RES_OUT	22	S_P21_2 *
23	ERROROUT_M	24	X1_C **
25	P22_13	26	X2_C **
27	P22_12	28	NMI
29	P22_11	30	P23_0
31	P22_10	32	P23_1
33	P22_9	34	P23_2
35	P22_8	36	P23_3
37	P22_7	38	P23_4
39	P22_6	40	P23_5
41	P22_5	42	P23_6
43	P22_4	44	P23_7
45	P22_3	46	P32_6
47	P22_2	48	P32_5
49	P22_1	50	P32_4
51	P22_0	52	P32_3
53	GND	54	GND

Note * By default these signals are not connected to CN11 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R31, R50, R75, R76 and R78.

** By default, these signals are not connected to CN5 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R48 and R49.

6.2.2 Device Ports Connector CN6

Table 6.5 Device ports connector CN6

Pin	Device port	Pin	Device port
1	GND	2	GND
3	P10_8	4	GND
5	P10_7	6	S_P10_3 *
7	P10_6	8	S_P10_2 *
9	P10_5	10	S_P10_1 *
11	P10_4	12	S_P10_0 *
13	P12_9	14	P11_10
15	P12_8	16	P11_9
17	P12_7	18	P11_8
19	P12_6	20	P11_7
21	P12_5	22	P11_6
23	P12_4	24	P11_5
25	P12_3	26	P11_4
27	P12_2	28	P11_3
29	P12_1	30	P11_2
31	P12_0	32	P11_1
33	S_P14_5 **	34	P11_0
35	S_P14_4 **	36	S_P13_0 **
37	P14_7	38	S_P13_1 **
39	P14_3	40	S_P13_2 **
41	P14_2	42	S_P13_3 **
43	P14_1	44	P15_3
45	P14_0	46	P15_2
47	P14_6	48	P15_1
49	GND	50	P15_0
51	GND	52	GND
53	GND	54	GND

Note * By default these signals are not connected to CN12 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R108-R111.

** By default, these signals are not connected to CN13 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R112, R113, R115, R116, R118, R119.

6.2.3 Device Ports Connector CN7

Table 6.6 Device ports connector CN7

Pin	Device port
1	GND
3	AN21_0
5	AN21_1
7	AN21_2
9	AN21_3
11	AN23_0
13	AN23_1
15	AN23_2
17	AN23_3
19	AN25_0
21	AN25_1
23	AN25_2
25	AN25_3
27	P02_0
29	P02_1
31	P02_2
33	P02_3
35	P02_4
37	P02_5
39	P02_6
41	P02_7
43	P02_8
45	P02_9
47	P02_10
49	P02_11
51	GND
53	GND

Pin	Device port
2	GND
4	ADSVCL
6	AN20_0
8	AN20_1
10	AN20_2
12	AN20_3
14	AN22_0
16	AN22_1
18	AN22_2
20	AN22_3
22	AN24_0
24	AN24_1
26	AN24_2
28	AN24_3
30	P00_7
32	P00_6
34	P00_5
36	P00_4
38	P00_3
40	P00_2
42	P00_1
44	P00_0
46	P01_7
48	P01_6
50	P01_5
52	P01_4
54	P01_3

6.2.4 Device Ports Connector CN8

Table 6.7 Device ports connector CN8

Pin	Device port
1	GND
3	P33_8
5	P33_7
7	P33_6
9	P33_5
11	P33_4
13	P33_3
15	P33_2
17	P33_1
19	P33_0
21	AN06_0
23	AN06_1
25	AN06_2
27	AN06_3
29	AN05_0
31	AN05_1
33	AN05_2
35	AN05_3
37	AN00_0
39	AN00_1
41	AN00_2
43	AN00_3
45	AN01_0
47	AN01_1
49	AN01_2
51	AN01_3
53	GND

Pin	Device port
2	GND
4	P32_2
6	P32_1
8	P32_0
10	P33_13
12	P33_12
14	P33_11
16	P33_10
18	P33_9
20	P34_0
22	P34_1
24	P34_2
26	P34_3
28	P34_4
30	AN04_0
32	AN04_1
34	AN04_2
36	AN04_3
38	AN03_0
40	AN03_1
42	AN03_2
44	AN03_3
46	AN02_0
48	AN02_1
50	AN02_2
52	AN02_3
54	GND

6.3 Pull-Up/Pull-Down Pin Header CN9

Table 6.8 Pull-up/pull-down pin header CN9

Pin	Function
1	fixed H level, depends on JP25: • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V
3	
5	
7	
9	
11	fixed H level, depends on JP32: • JP32[2-1]: 5.0 V • JP32[2-3]: 3.3 V
13	
15	
17	
19	

Pin	Function
2	fixed L level
4	
6	
8	
10	
12	
14	
16	
18	
20	

6.4 Aurora Connector CN10

Table 6.9 Aurora connector CN10

Pin	Function	Pin	Function
1	TODP0	2	VCC
3	TODN0	4	TCK
5	GND	6	TMS
7	–	8	TDI
9	–	10	TDO
11	GND	12	TRST
13	–	14	MD0
15	–	16	EVTI
17	GND	18	EVTO
19	–	20	MD1
21	–	22	RES_IN
23	GND	24	GND
25	–	26	CICREFP
27	–	28	CICREFN
29	GND	30	GND
31	–	32	DRDY
33	–	34	RES_OUT

6.5 RHSIF Connector CN11

Table 6.10 RHSIF connector CN11

Pin	JP4[2-1]		JP4[2-3]	
	Device port	Function	Device port	Function
1	P21_5	HSIF0_TXDP	P21_3	HSIF0_RXDP
2	–	GND	–	GND
3	P21_4	HSIF0_TXDN	P21_2	HSIF0_RXDN
4	–	GND	–	GND
5	–	GND	–	GND
6	P20_0	HSIF0_REFCLK	P20_0	HSIF0_REFCLK
7	S_P21_3	HSIF0_RXDP	S_P21_5	HSIF0_TXDP
8	–	GND	–	GND
9	S_P21_2	HSIF0_RXDN	S_P21_4	HSIF0_TXDN
10	–	GND	–	GND

Table 6.10 RHSIF connector CN11 (cont'd)

Pin	JP4[2-1]		JP4[2-3]	
	Device port	Function	Device port	Function
11	–	GND	–	GND
12	–	GND	–	GND

Note

In order to minimize signal interference no signals from CN11 are not connected to CN5. If required they can be connected via 0 Ω resistors R31, R50, R75, R76 and R78.

6.6 RHSB Connector CN12

Table 6.11 RHSB connector CN12

Pin	Device port	Function
1	P10_1 *	RHSB1FCLN
3	P10_0 *	RHSB1FCLP
5	-	GND
7	P10_3 *	RHSB1SON
9	P10_2 *	RHSB1SOP
11	P13_0	RHSB0FCLN
13	P13_1	RHSB0FCLP
15	-	GND
17	P13_2 *	RHSB0SON
19	P13_3 *	RHSB0SOP
21	-	GND

Pin	Device port	Function
2	P10_7	RHSB1CSD0
4	P12_0	RHSB1EMRG
6	P12_2	RHSB1SI0
8	P12_4	RHSB1SI1
10	P10_6	RHSB1CSD1
12	P12_6	RHSB0CSD0
14	P12_7	RHSB0EMRG
16	P12_3	RHSB0SI0
18	P12_1	RHSB0SI1
20	P12_5	RHSB0CSD1
22	-	GND

Note

* In order to minimize signal interference these signals are not connected to CN6. If required they can be connected via 0 Ω resistors R108 to R111, R115 and R116.

6.7 HS-SPI Connector CN13

Table 6.12 HS-SPI connector CN13

Pin	JP29[2-1]		JP29[2-3]	
	Device port	Function	Device port	Function
1	P13_1 *	CLKP	P13_1 *	CLKP
2	P13_3 *	TXDP	P14_4 *	RXDP
3	P13_0 *	CLKN	P13_0 *	CLKN
4	P13_2 *	TXDN	P14_5 *	RXDN

Table 6.12 HS-SPI connector CN13 cont'd

Pin	JP29[2-1]		JP29[2-3]	
	Device port	Function	Device port	Function
5	–	GND	–	GND
6	–	GND	–	GND
7	–	GND	–	GND
8	P14_4 *	RXDP	P13_3 *	TXDP
9	P14_2	SSL/SSLI	P14_2	SSL/SSLI
10	P14_5 *	RXDN	P13_2 *	TXDN
11	–	GND	–	GND
12	–	GND	–	GND

Note

* In order to minimize signal interference these signals are not connected to CN6. If required they can be connected via 0 Ω resistors R112, R113, R115, R116, R118 and R119.

6.8 Debug Connector CN25

Table 6.13 Debug connector CN25

Pin	Function
1	TCK/LPDCLKI
3	Jumper JP31 #3 (TRST)
5	TDO/LPDO
7	TDI/LPDIO
9	TMS
11	DRDY/LPDCLKO
13	RES_IN/RESET

Pin	Function
2	GND
4	MD0/FPMD0
6	–
8	VCC/TVDD
10	EVTO
12	GND
14	GND

7. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumpers Overview*.

For jumper settings related to the device operation mode, refer to *5.2 Operation Mode Selection*.

The following sections show some jumper settings, that allow to operate the piggyback board in different power supply configurations.

7.1 General Settings

All of the following board configurations are based on these conditions:

- All voltages for all functions are activated.
- Current measurements are not carried out, hence JP0, JP1 and JP2 are set.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 to CN11 must be assembled on the board.

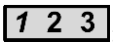
- The blue jumper are debug jumper and setting depend on the operating mode of the piggyback board.

Processor operation	JP31 [TRST]	JP34 [AURORARES]
Debug mode	2-3 (TRST connected to CN25)	1-2 (AURORARES from TRST)
Stand-alone operation	2-3 (TRST connected to CN25)	2-3 (AURORARES = GND)

- The red jumpers are related to the power supply configuration.
- The green jumpers have to be set when using RH850/E2x-FCC1 processor. They must not be set when using RH850/E2M processor.

Following jumper symbols are used:

-  : open jumper
- 

: jumper must be set in the indicated position.
- 

: jumper must be set; position can be defined by user.

Note

The pin 1 of a jumper can be identified by a

- small circle near the jumper
- square soldering pad.

7.2 Difference between RH850/E2x-FCC1 and RH850/E2M

The piggyback board can be used with RH850/E2x-FCC1 and RH850/E2M processor. For these 2 processors the jumper settings are slightly different. Below table shows the difference in the jumper settings.

Table 7.1 Jumper settings for E2X-FCC and E2M

Purpose	Jumper #	RH850/E2M in BGA292	
		FCC1 for E2M	E2M
5.0V Main	0	O	O
3.3V Main *1	1	O (opt.)	- (opt.)
5.0V Analog Main	2	O	O
E0VCC Config	3	O	O
E1VCC Config	5	#1 - #2	#1 - #2
E2VCC Config	6	#1 - #2	#1 - #2
LVDVCC Config	7	#1 - #2	#1 - #2
SYSVCC Config	8	#1 - #2	#1 - #2
VCC Config	9	#1 - #2	#1 - #2
EVTI	10	- (opt.)	- (opt.)
EVTI Pull-Up	11	- (opt.)	- (opt.)
EVTO Pull-Up	12	- (opt.)	- (opt.)
EVTO	13	- (opt.)	- (opt.)
EMUVCC	14	O (opt.)	-
A0VCC Config	15	O	O
A0VREFH Config	16	O	O
VDDIOF	17	#1 - #2	#1 - #2
A2VCC	19	O	O
A2VREFH Config	20	O	O
ADSVCC	21	O	O
1.28V Source	22	#1 - #2	#1 - #2
VDD	23	O	O
EMUVDD *1	24	O	-
CN9 Pull-Up 1-9	25	- (opt.)	- (opt.)
MD0 Pull-Up	26	- (opt.)	- (opt.)
MD1 Pull-Up	27	- (opt.)	- (opt.)
ADSVREFH	28	O	O
HS-SPI IC4 Config	29	- (opt.)	- (opt.)
Board_VCC Config	30	#1 - #2	#1 - #2
TRST Config	31	#2 - #3	#2 - #3
CN9 Pull-Up 11-19	32	- (opt.)	- (opt.)
ADSVREFL Pull-Down	33	O	O
AURORES Config *2	34	#1 - #2	#2 - #3 only

*1: Optionally for the FCC1 device only. If any of the FCC1 specific features are used (e.g. ERAM, Aurora Trace …) these jumpers need to be set.

*2: Optionally for the FCC1 device only if Aurora Trace is used. Please refer to the user's documentation of the used tool for dedicated requirement.

The table has the following meaning:

O: Jumper must be connected.

O (opt): Recommended to be connected. Can be left open if not necessary for use case

-: Jumper must be left open

- (opt): Not mandatory to connect. Can be connected if needed for use case

#x - #y: Connect the pins #x and #y for the standard configuration. Possible to configure depending on the use case and on the allowed specification of the used device.

7.3 Stand-Alone Operation with Single External Power Supply

This example enables to operate the board with only the 5.0 V external power supply.

Note

If the piggyback board is powered with 3.3V only the analog part of the RH850/E2x does not have a power supply. Thus, operation cannot be guaranteed.

Usage of power supply connections:

- CN15: 5.0 V
- CN22: GND connection
- CN23: not connected, no 3.3 V supply
- CN24: not connected, no IN_1v12 supply
  - JP22[2-1]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage

Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

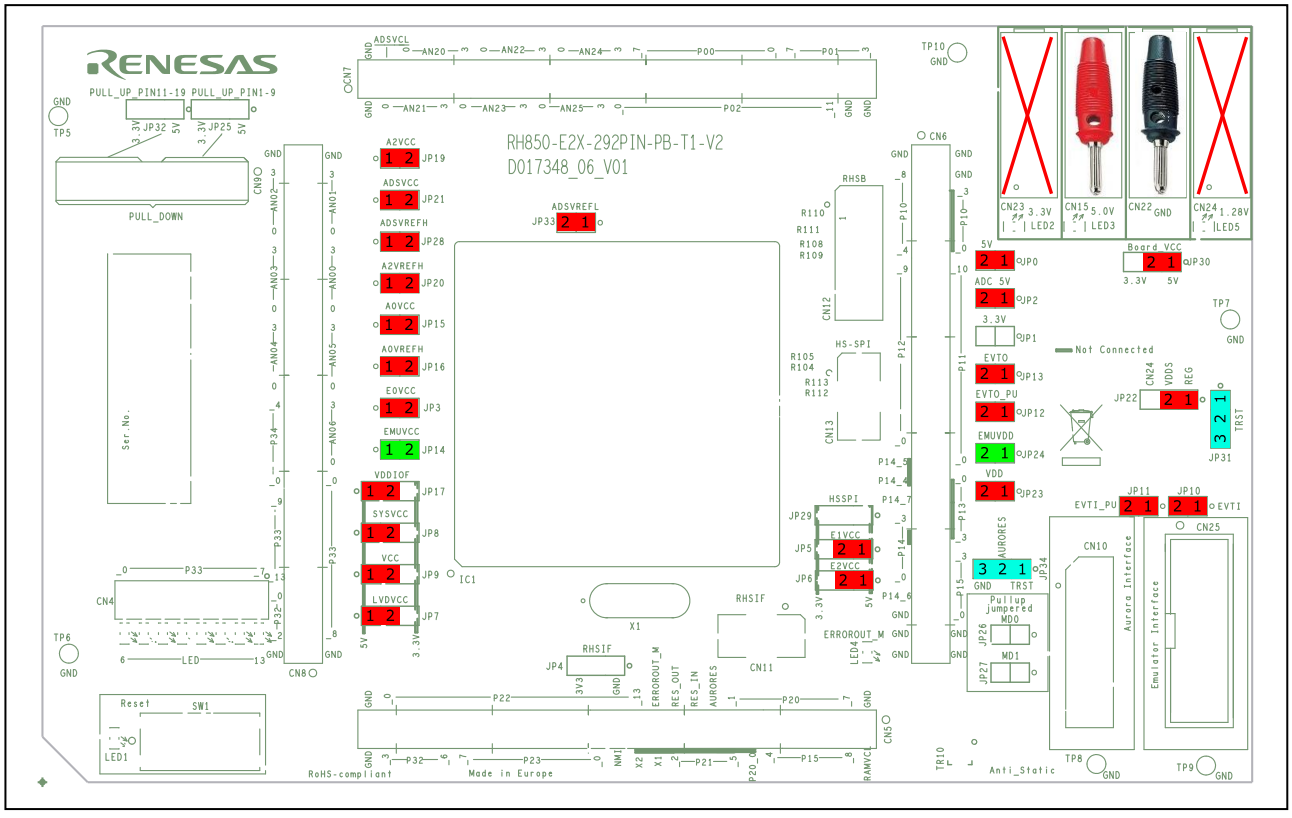


Figure 7.1 Stand-alone operation with single external power supply

7.4 Stand-Alone Operation with All External Power Supplies

This example assumes all external power supplies are connected and used.

Usage of power supply connections:

- CN15: 5.0 V
- CN22: GND connection
- CN23: 3.3 V
- CN24: 1.28V (IN_1v12)
  - JP22[3-2]: use voltage from external supply for VDD voltage

  Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

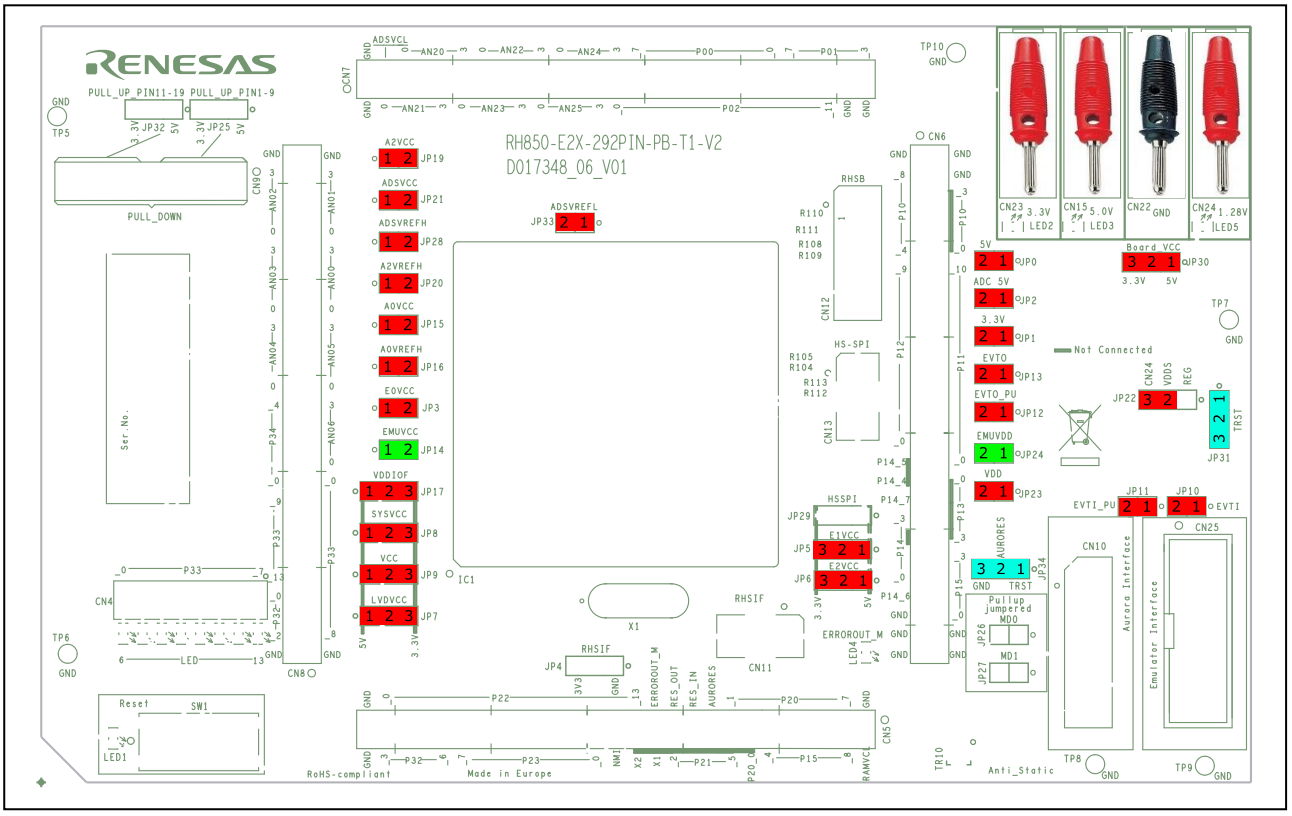


Figure 7.2 Stand-alone operation with maximum external power supply

7.5 Plug-In Operation with Power Supply from Main Board

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

Do not supply the 5V (CN15) and 3.3V (CN23) voltage directly to the piggyback board

Usage of power supply connections:

- CN15: not connected, no 5.0 V supply
- CN22: not connected
- CN23: not connected, no 3.3 V supply
- CN24: not connected, no IN_1v12 supply
  - JP22[2-1]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage

  Refer to *3.3 Device Core Voltage (VDD)* for further details about VDD voltage.

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN24) as the source for VDD voltage. In this case set JP22[2-3].

CAUTION

Do not supply 5V (CN15) and 3.3V (CN23) directly to the piggyback board as these voltages are already supplied by the main board.

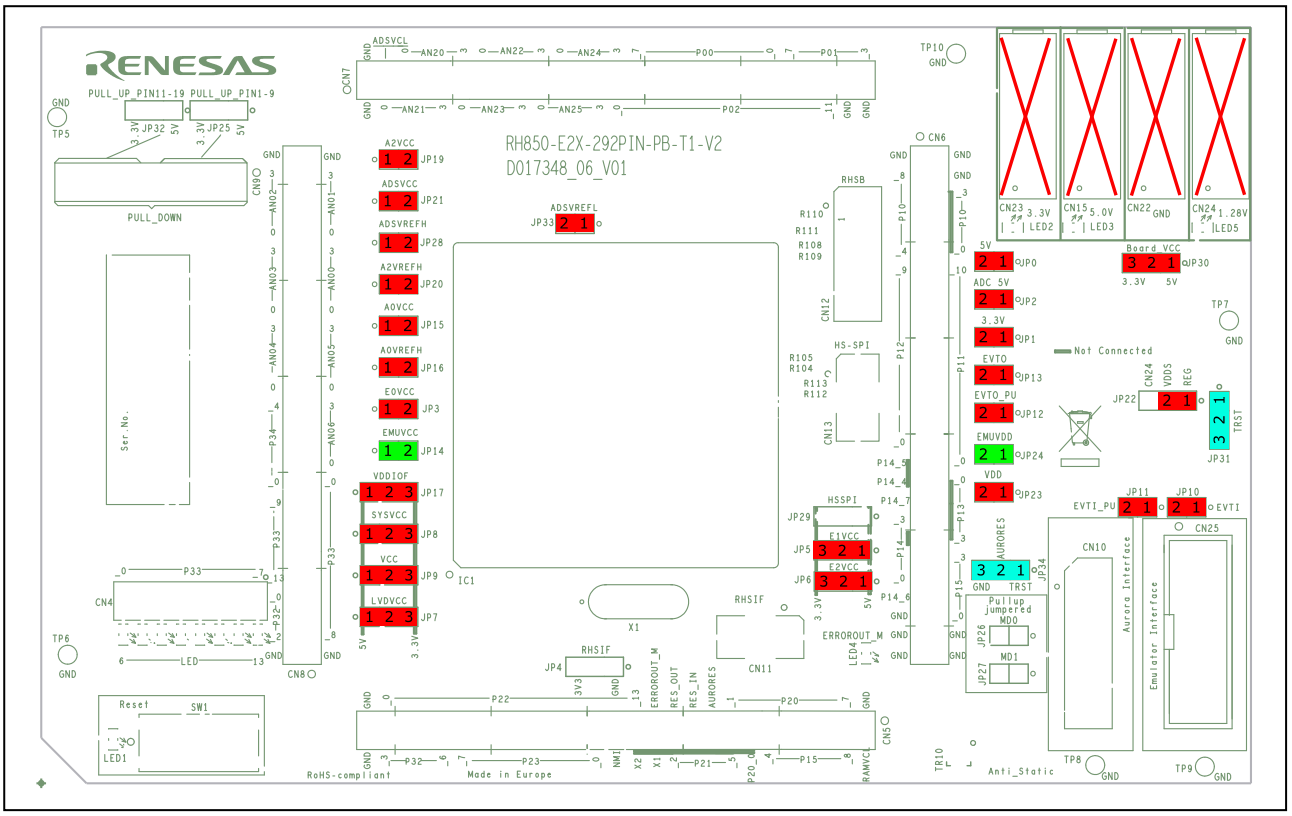


Figure 7.3 Main board operation without external power supply

8. Precautions

8.1 Power-Off Sequence

A dedicated sequence needs to be applied, when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '2-3 ON' position, so that RESET is permanently asserted. Alternatively keep SW1 manually in' 2-1 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to section *5.3 RESET Switch*.

9. Mechanical Dimensions

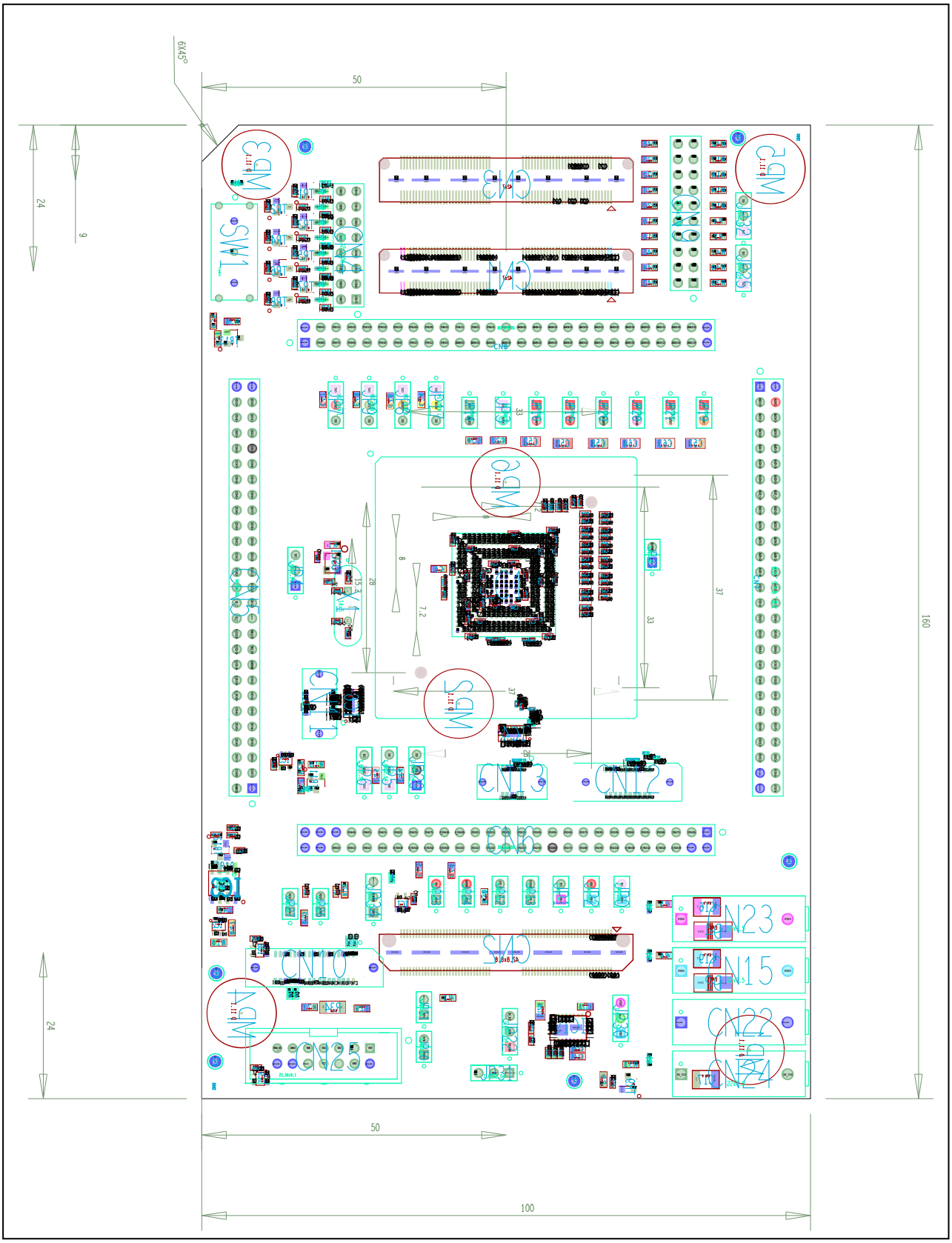


Figure 9.1 Mechanical dimensions

10. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Oscillators and resonators: OSC1
- Capacitors: C29, C33
- Resistors: R38, R48, R49, R79, R101

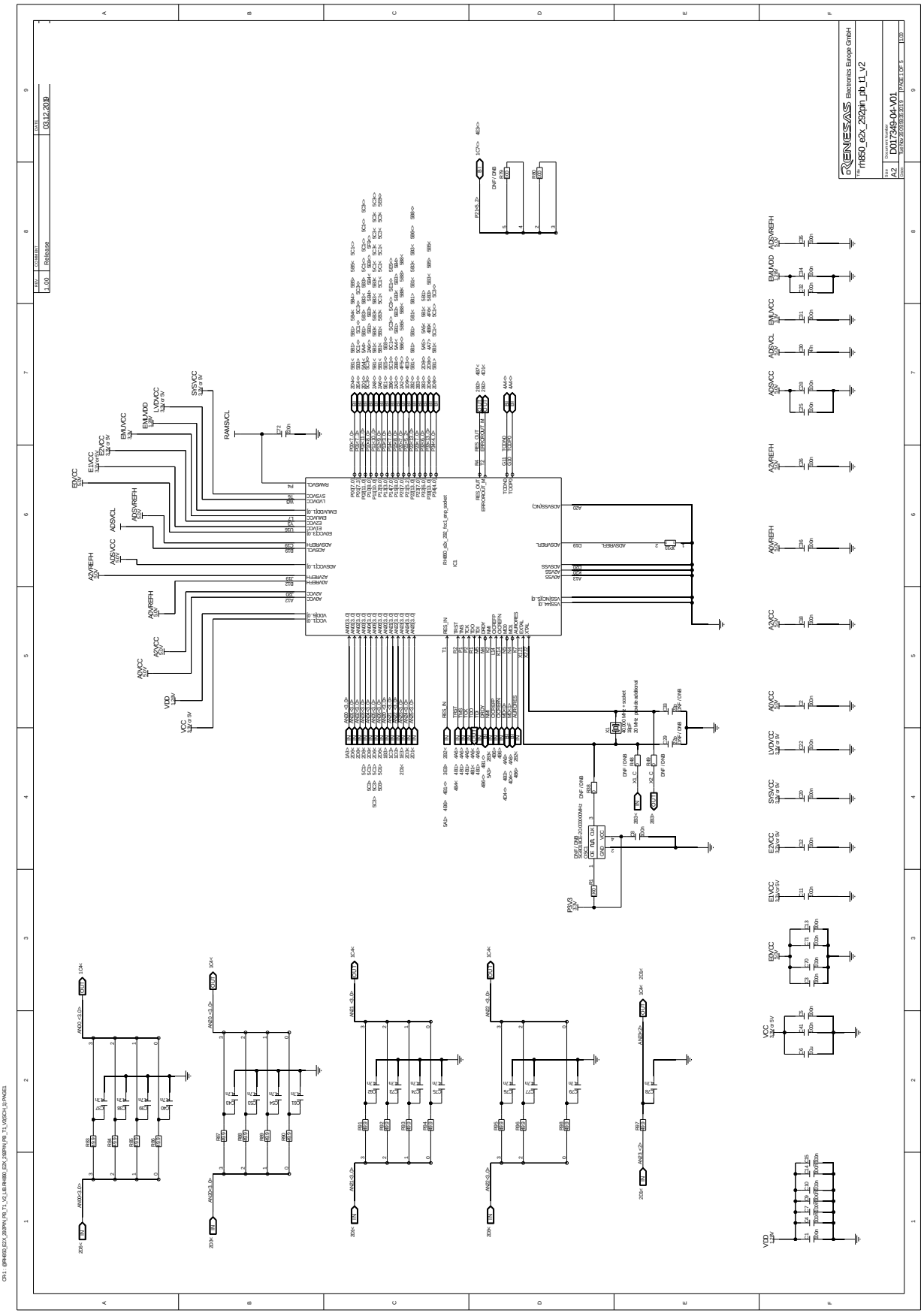
The above components are indicated with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

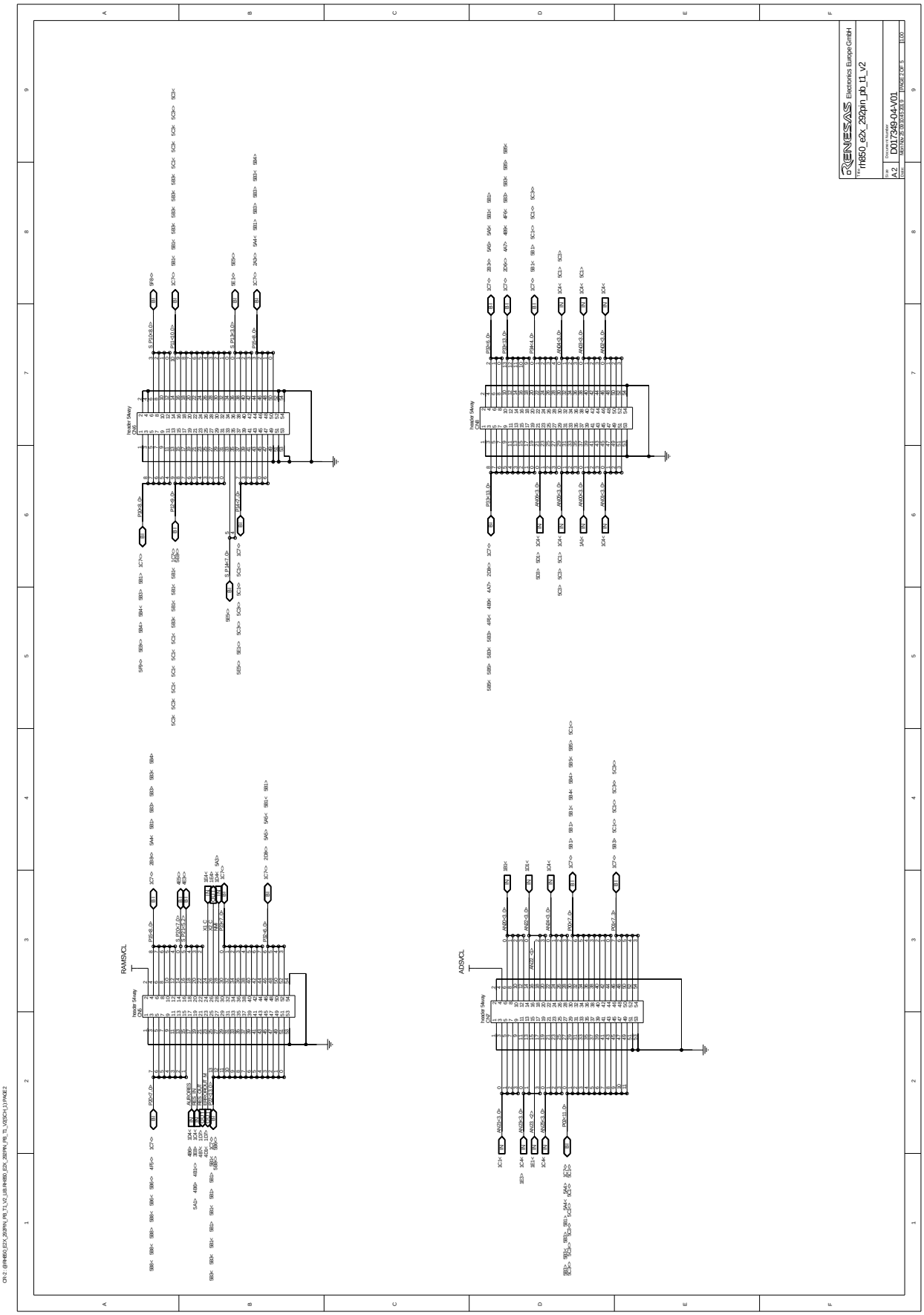
- 3 Hirschmann 4 mm power lab sockets, red for CN15, CN23, CN24
- 1 Hirschmann 4 mm power lab sockets, black for CN22
- one resonator HC49 (20 MHz)
- 42 jumpers, 2.54 mm, black

The above components are indicated with "DO NOT FIT / TO DELIVER WITH THE BOARD" in the schematics.

10.1 Page 1



10.2 Page 2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rh850_e2x_292pin_pb_t1_v2
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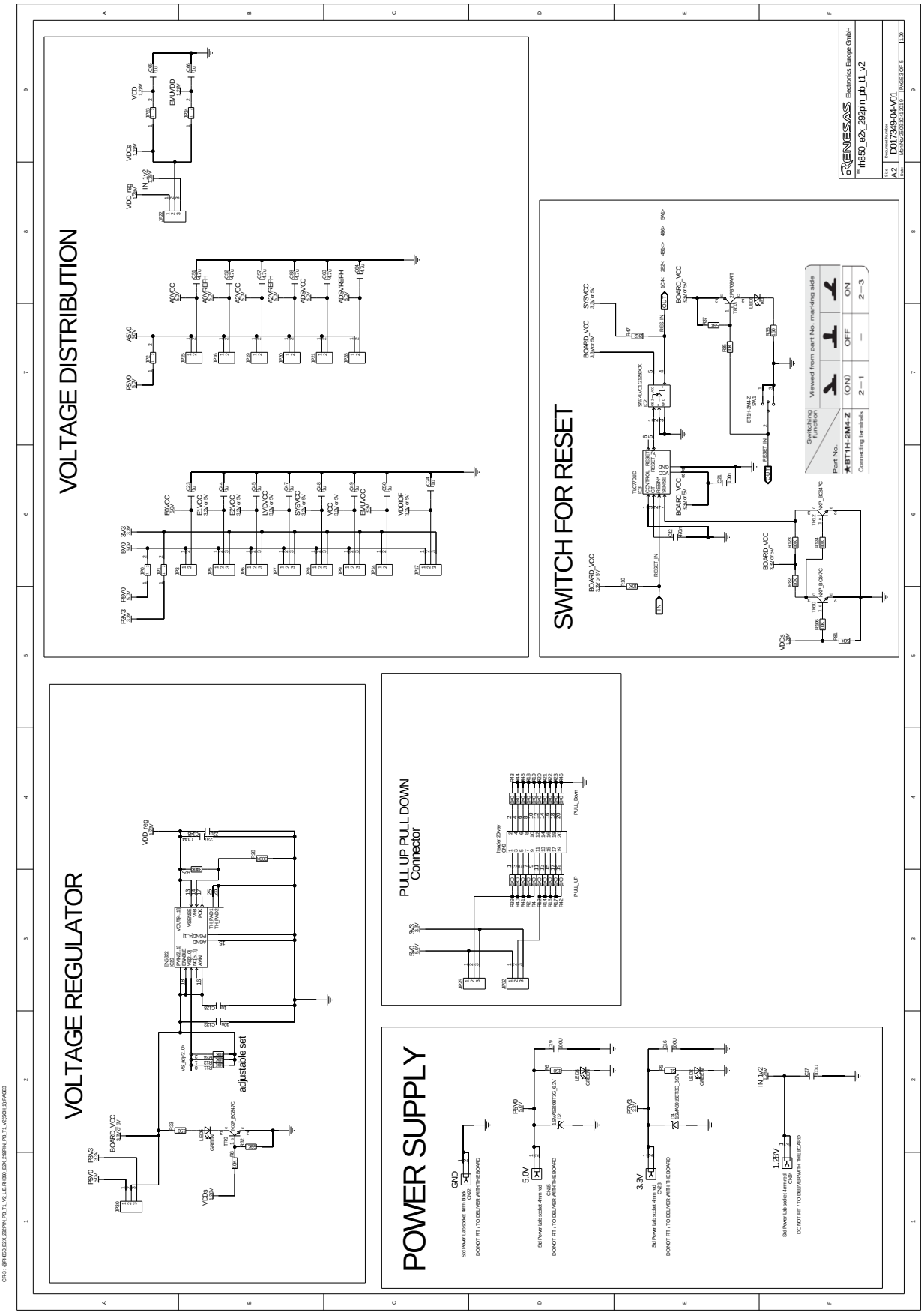
RAMSCL
ADSCL
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

10.3 Page 3


VOLTAGE DISTRIBUTION
SWITCH FOR RESET
VOLTAGE REGULATOR
adjustable set
PULL UP PULL DOWN
Connector
POWER SUPPLY
GND
5.0V
3.3V
1.28V
RENESAS Electronics Europe GmbH
rh850_e2x_292pin_pb_t1_v2
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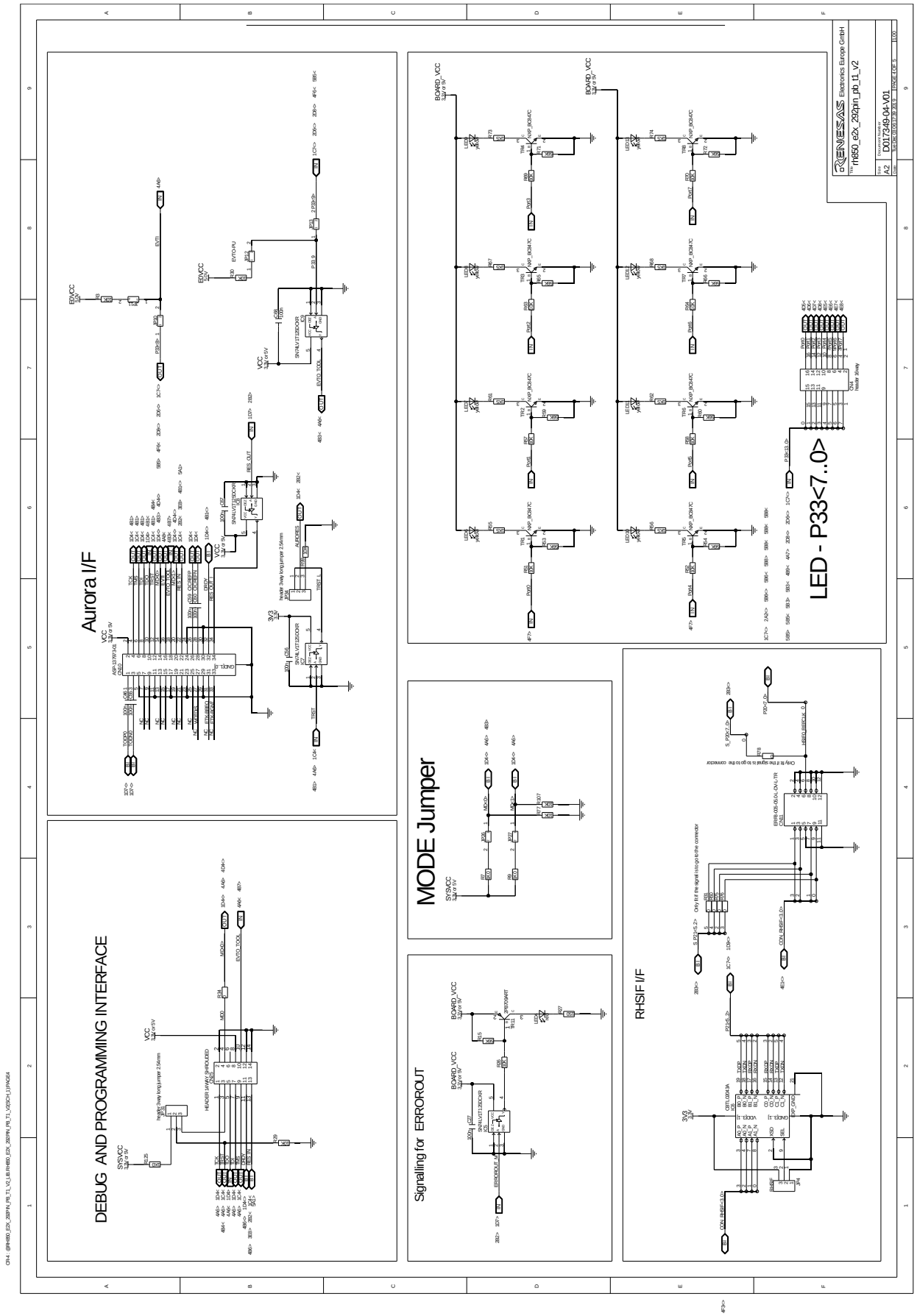
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

10.4 Page 4


Aurora I/F
DEBUG AND PROGRAMMING INTERFACE
MODE Jumper
Signalling for ERRROUT
RHSIF I/F
LED - P33<7..0>
RENESAS Electronics Europe GmbH
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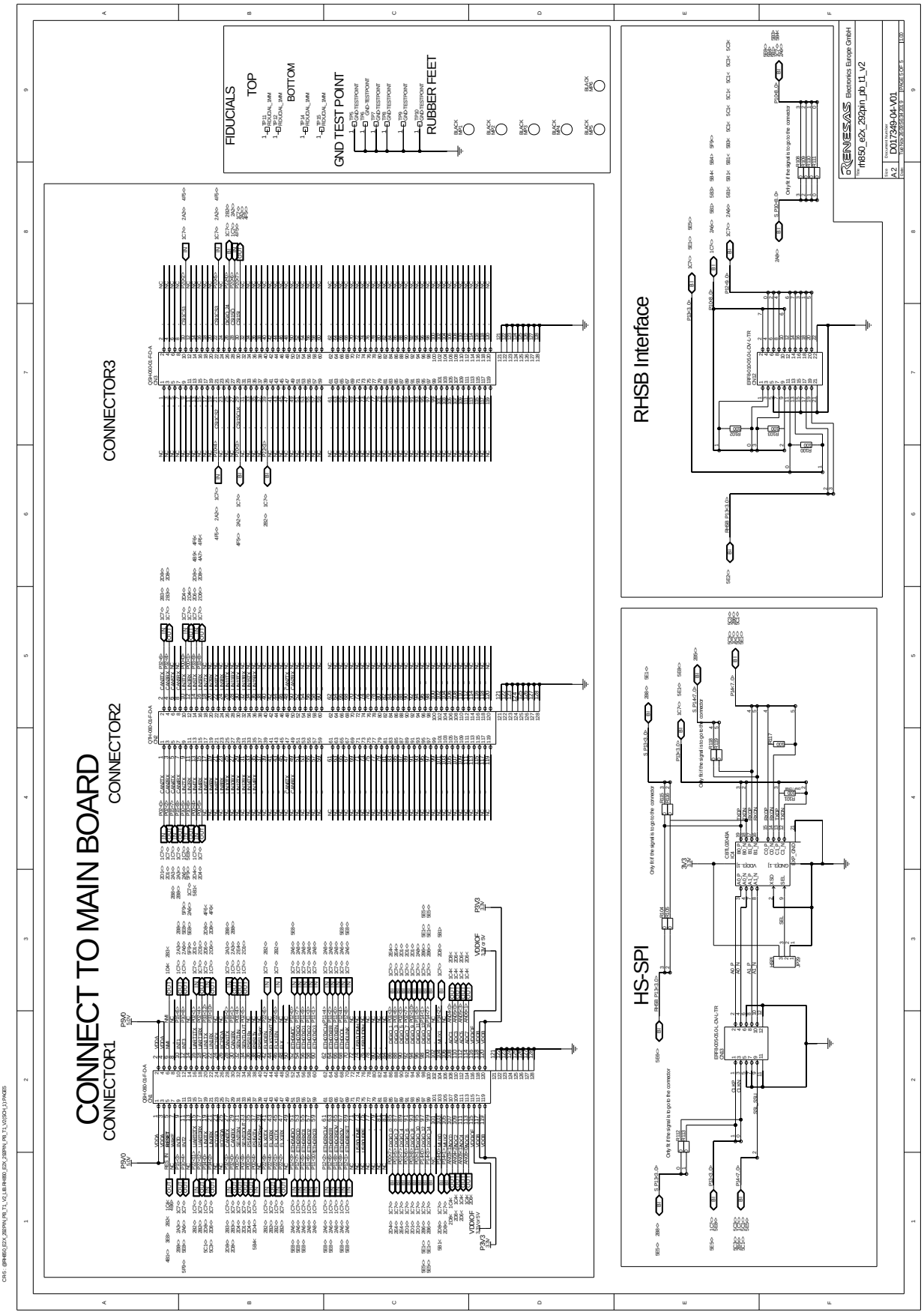
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

10.5 Page 5


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
HS-SPI
RHSB Interface
FIDUCIALS
TOP
BOTTOM
GND TEST POINT
RUBBER FEET
RENESAS Electronics Europe GmbH
rh850_e2x_292pin_pb_t1_v2
D0017349-04-V01
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2020-06-03	–	Initial release

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Colophon 6.0

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