User's Manual

32

RH850 Evaluation Platform

RH850/F1x 144-pin
RH850/R1x 144-pin

User's Manual: Piggyback board V3

Y-RH850-F1X-144PIN-PB-T1-V3

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has **s**tabilized.
   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   – The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

Chapter 1 Introduction

The RH850/F1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/F1x microcontrollers. The piggyback board (Y-RH850-F1X-144PIN-PB-T1-V3) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V-5.0V)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each device pin
- Reset switch
- MainOSC and SubOSC circuitry
- Signal LEDs
- Connectors to mainboard

This document describes the functionality provided by the piggyback board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the User's Manual of the applicable devices:

- RH850/F1L
- RH850/R1L
- RH850/F1M
- RH850/F1K
- RH850/F1KM-S2
- RH850/F1KM-S4

This manual describes the following board revision:

- Y-RH850-F1X-144PIN-PB-T1-V3

For differences to the Y-RH850-F1X-144PIN-PB-T1-V2 see the Revision History.

1.1 Package Components

The Y-RH850-F1X-144PIN-PB-T1-V3 product package consists of the items included in below table. After you have unpacked the box, check if your Y-RH850-F1X-144PIN-PB-T1-V3 package contains all these items.

Item	Description	Quantity
D15371#01	RH850/F1x 144pin piggyback board	1
D15373	Documentation CD	1
D010816-24	China RoHS document	1
D15370-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	37
Red Hirschmann 4 mm power lab sockets	In the bag	2
Black Hirschmann 4 mm power lab sockets	In the bag	1
Crystal, TC38, 32.768 kHz	In the bag	1
Crystal, HC49, 8 MHz	In the bag	1
Crystal, HC49, 20 MHz	In the bag	1

Note: Please keep the Y-RH850-F1X-144PIN-PB-T1-V3 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-F1X-144PIN-PB-T1-V3. If packing of your product is not complete, it may be damaged during transportation.

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide the views of the piggyback board.

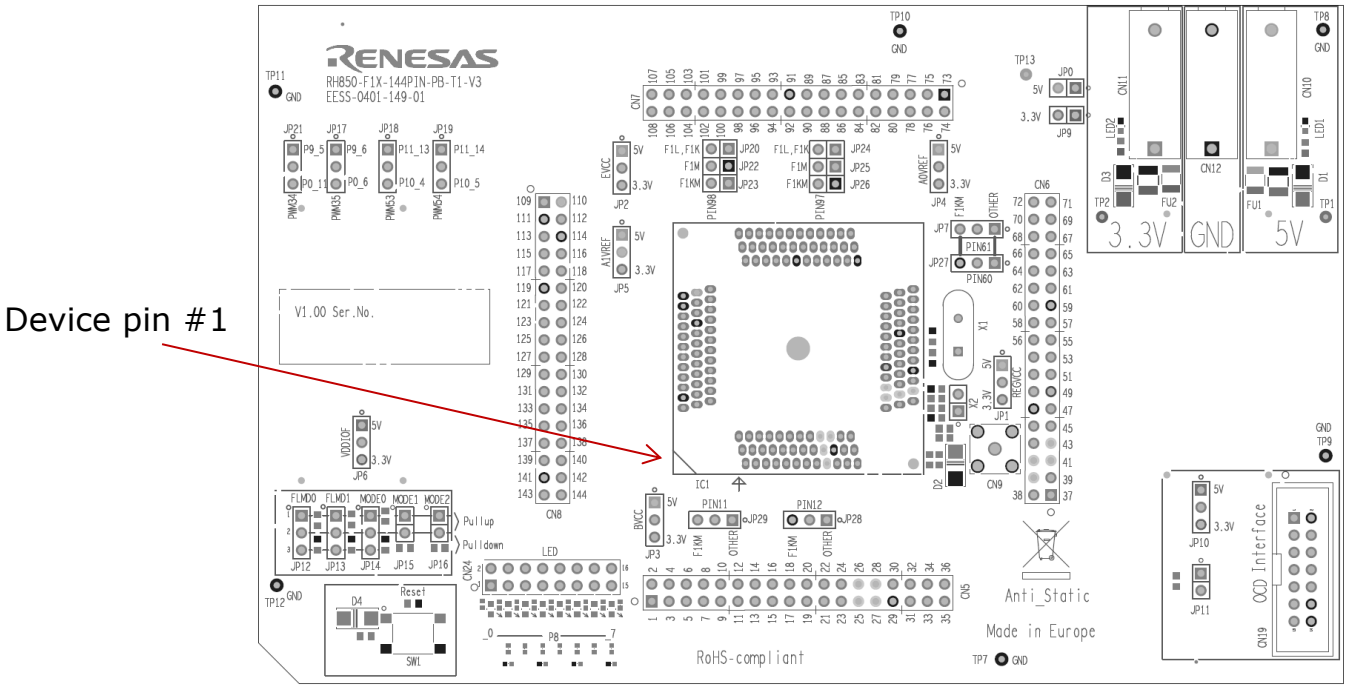

Figure 1 – Piggyback board top view

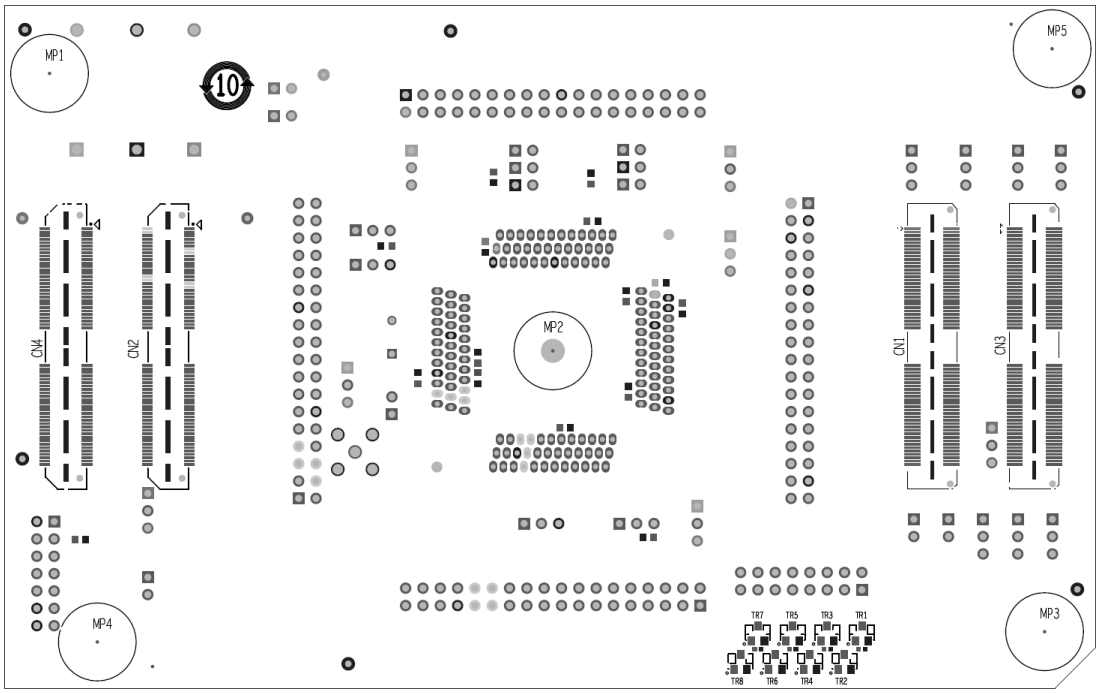

Figure 2 – Piggyback board bottom view

2.2 Mounting of the device

The board is designed for use with the following devices, all in their 144 pin package:

- RH850/F1L
- RH850/F1M
- RH850/F1K
- RH850/F1KM-S2
- RH850/F1KM-S4
- RH850/R1L

The device must be placed inside the socket IC1. To insert the device, press down the lid, align the #1 pin of the device to the #1pin of the socket, insert the device inside the socket and release the lid.

Chapter 3 Jumper Configuration

The function of the board can be configured via jumpers. This chapter describes the standard configuration, i.e. jumper setting for the intended devices. For the supported function of the used device, please refer to the corresponding HW user's manual.

The table has the following meaning:

- x-y: Connect the pins x and y; valid for 3-pin jumpers (e.g. JP19)

The pin #1 can be identified by a small circle in the vicinity of the jumper

Depending on the used device a configuration of several jumpers is required. The detailed configuration is shown below. The applicable setting for each device / jumper is highlighted in blue:

	F1L	F1M	F1H	F1K	F1KM-S2 F1KM-S4	Function
JP7 1-2	closed	closed	closed	closed	open	Selection of Pin 61: P1_6 or ISOVCL
JP7 2-3	open	open	open	open	closed	
JP20	closed	open	open	closed	open	Selection of pin 98: P9_6, VSS or REGVCC
JP22	open	closed	open	open	open	
JP23	open	open	open	open	closed	
JP24	closed	open	open	closed	open	Selection of pin 97: P9_5, ISOVCL or VSS
JP25	open	closed	open	open	open	
JP26	open	open	open	open	closed	
JP27 1-2	closed	closed	closed	closed	open	Selection of Pin 60: P1_7 or VSS
JP27 2-3	open	open	open	open	closed	
JP28 1-2	closed	closed	closed	closed	open	Selection of Pin 14: P11_14 or VSS
JP28 2-3	open	open	open	open	closed	
JP29 1-2	closed	closed	closed	closed	open	Selection of Pin 73: P11_13 or ISOVCL
JP29 2-3	open	open	open	open	closed	
JP21 1-2	closed	open	open	Either	open	Selection of PWGA34: Either from P9_5 or P0_11
JP21 2-3	open	closed	closed	Or	closed	
JP17 1-2	closed	open	open	Either	open	Selection of PWGA35: Either P9_6 or P0_6
JP17 2-3	open	closed	closed	Or	closed	
JP18 1-2	closed	closed	closed	closed	open	Selection of PWGA53: Either P11_13 or P10_4
JP18 2-3	open	open	open	open	closed	
JP19 1-2	closed	closed	closed	closed	open	Selection of PWGA54: Either P11_14 or P10_5
JP19 2-3	open	open	open	open	closed	

The jumper setting also are shown in this picture:

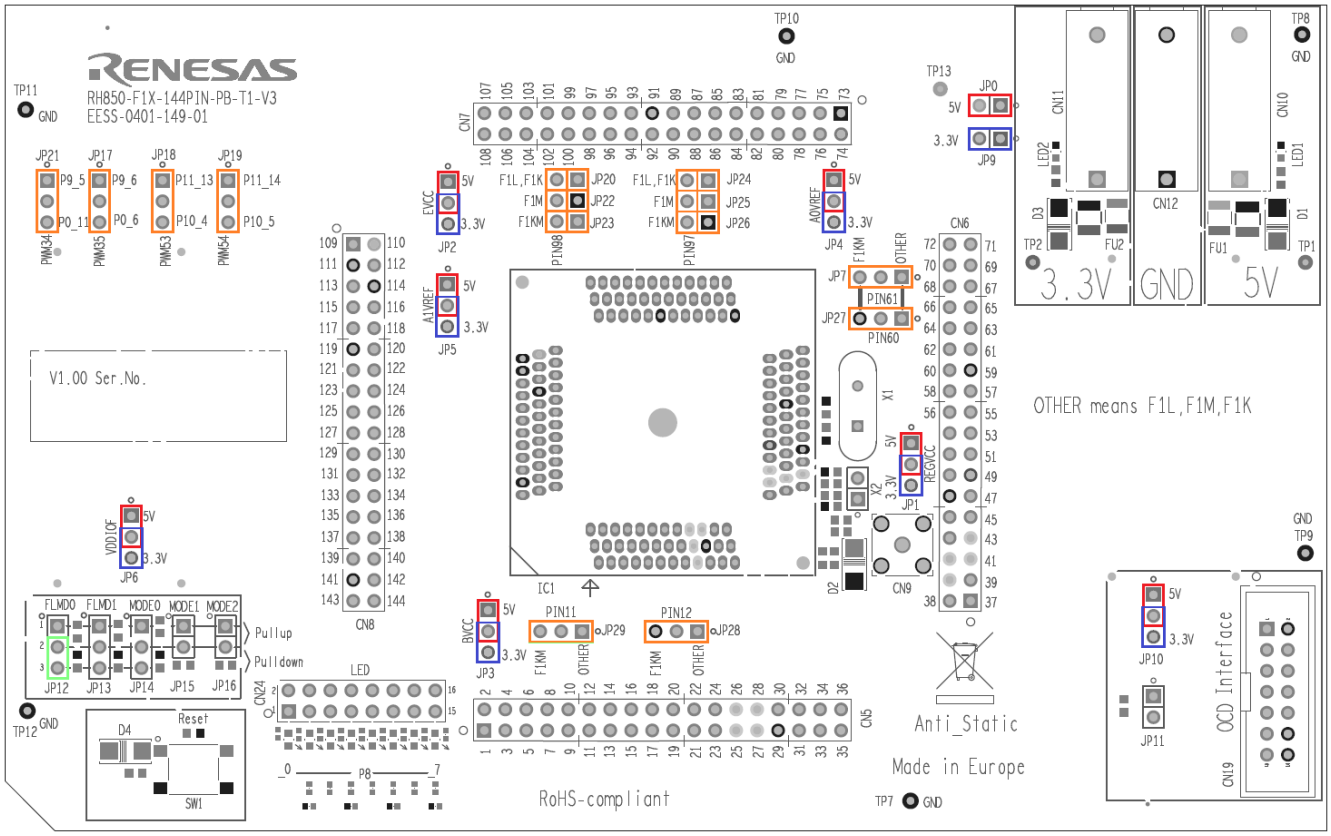

Figure 3 – Jumper setting overview

- The green jumper JP12 for FLMDO0 always must be closed for a 'normal' (user mode and debug) operation of the device.
- The red jumpers must be set for a single "Voltage 1" (typ +5.0V) operation of the device.
- The blue jumper must be set for a single "Voltage 2" (typ +3.3V) operation of the device.
- The orange jumpers must be selected depending on the used device. See the printing on the board for the applicable setting.

For jumper settings related to the device operation mode, refer to the chapter 8.2.

Chapter 4 Power supply

4.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. Though a single supply voltage is sufficient for the operation of the device, two (different) voltages can be supplied to the board.

Within this document the following voltages are considered as 'typical' connections:

Voltage1 = 5.0V

Voltage2 = 3.3V

The following connectors are available to supply those voltages:

- Three 4mm 'banana-type' connectors:
  - Two red connectors for voltages *Voltage1* (CN10) and *Voltage2* (CN11).
  - A black connector for VSS connection (CN12).

  Note: The three connectors are supplied with the board but not assembled.
- The E1 emulator, that is used for debug purposes and flash programming, can also supply a single operating voltage ('Dbg_Voltage').
  The voltage is programmable via the E1 GUI as 3.3 or 5.0V (typ).
  See the documentation of the E1 and chapter 5 'Debug and Programming interface' for details.
- In case the piggyback board is mounted on a mainboard, the voltages *Voltage1* and *Voltage2* are supplied by the on-board regulators of the mainboard.

NOTE: *Do not supply any voltage directly to the piggyback board in case it is mounted on the mainboard.*

For each of the two voltages, 'Voltage 1 ' and 'Voltage 2', a green LED (LED1 and LED2) is available to signal that the related voltage is available on the piggyback board.

4.2 Voltage distribution

The table shows the required device power supply pins and their function:

Device supply pin	Function
REGVCC	Supply for the device internal regulators for the digital logic.
EVCC	Supply for ports of AWO and ISO area.
BVCC	Supply for ports of AWO and ISO area.
A0VREF	Supply for ports and analog functions of ADC0.
A1VREF	Supply for ports and analog functions of ADC1.

Additional one power supply for mainboard can be selected:

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.

- For each of the above voltages, the voltage source can be selected from *Voltage1* (typ. 5.0V) or *Voltage2* (typ. 3.3V) by the jumpers JP1 to JP6.

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Chapter 5 Clock sources

Four external crystal oscillators for the device clock supply are provided with the board.

5.1.1 MainOsc

A crystal or ceramic resonator in the range of 8MHz to 24MHz can be mounted on socket X1.

A 8MHz, 16Mhz and 20MHz oscillator is supplied with the board.

5.1.2 SubOSC

An oscillator with a frequency of 32.768kHz is supplied with the board and can be soldered into the connector X2.

Chapter 6 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN19 is provided.

The signal connection of the connector CN19 is shown in the picture below:

CN19 pin	Device Port	Device signal
1	JP0_2	DCUTCK / LPDCLK
2	GND	GND
3	JP0_4	DCUTRST
4	FLMD0	FLMD0
5	JP0_1	DCUTDO / LPDO
6	P10_8*	FLMD1
7	JP0_0	DCUTDI / LPDI
8	'Dbg_Voltage'	-
9	JP0_3	DCUTMS
10	JP0_6	EVTO
11	JP0_5	DCURDY / LPDCLKOUT
12	GND	-
13	RESET	-
14	GND	-

* In case of connecting a debug/programming tool to CN19, the pin header JP11 must be closed.

The 'Dbg_Voltage' (on CN19 pin 8) is monitored or supplied by the debug and flash programming tools. Therefore, it is necessary to select either Voltage1 (5V) or the Voltage2 (3.3V) by pin header JP10:

JP10 pin	Selection for Dbg_Voltage
1-2	5V is selected
2-3	3.3V is selected

If the EVTO signal is used, a pull-up can be applied to that signal. To do so, close the JP11.

JP11 pin	Pull-up for EVTO
Open	No pull-up is applied
Closed	Pull-up is selected

Chapter 7 Connectors for ports of device

Connection to each pin of the device is possible via the connectors CN5 to CN8.

Note :The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

7.2 Connectors to Mainboard

Three connectors (CN1 to CN3) are available to connect the piggyback board to a mainboard.

The signal connection of each connector is described in the following tables:

7.2.1 Connector CN1

Pin	Function	Device Port		Pin	Function	Device Port
1	VOLTAGE1	-		2	VOLTAGE1	-
3	VOLTAGE1	-		4	VOLTAGE1	-
5	RESET	_RESET		6	NMI	P9_0
7	WAKE	-		8	-	-
9	INT0	P9_1		10	INT1	P0_6
11	INT2	P9_2		12	INT3	P9_3
13	-	-		14	-	-
15	UART0TX	P10_10		16	UART1TX	P0_5
17	UART0RX	P10_9		18	UART1RX	P0_4
19	LIN0TX	P10_10		20	LIN1TX	P0_8
21	LIN0RX	P10_9		22	LIN1RX	P0_7
23	IIC0SDL	P10_3		24	IIC1SDL	P9_1
25	IIC0SDA	P10_2		26	IIC1SDA	P9_0
27	CAN0TX	P10_1		28	CAN1TX (*)	P0_3
29	CAN0RX	P10_0		30	CAN1RX (*)	P0_2
31	SENTIN0	P8_0		32	SENTIN1	P9_0
33	SENTOUT0	P8_1		34	SENTOUT1	P9_1
35	PSI50Rx	-		36	PSI51Rx	-
37	PSI50Tx	-		38	PSI51Tx	-
39	PSI50Snyc	-		40	PSI51Sync	-
41	FLX0TX	P11_1		42	FLX0EN	P10_11
43	FLX0RX	P10_14		44	FLX0STPWT	P10_12
45	FLX1TX	P10_8		46	FX1EN	P10_13
47	FLX1RX	P10_9		48	FLXCLK	P10_10
49	-	-		50	-	-
51	ETH0MDIO	-		52	ETH0MDC	-
53	ETH0RXD0	-		54	EH0TXD0	-
55	ETH0RXD1	-		56	EH0TXD1	-
57	ETH0RXD2	-		58	EH0TXD2	-
59	ETH0RXD3	-		60	EH0TXD3	-
61	ETH0RXDCLK	-		62	ETH0TXCLK	-
63	ETH0RXER	-		64	ETH0TXER	-
65	ETH0CRSDV	-		66	ETH0TXEN	-
67	ETH0RXDV	-		68	ETH0COL	-
69	ETH0RESET	-		70	-	-
71	-	-		72	-	-

73	USB0UDMF	-		74	USB0UDMH	-
75	USB0UDPF	-		76	USB0UDPH	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	DIGIO_0	P8_0		86	DIGIO_1	P8_1
87	DIGIO_2	P8_2		88	DIGIO_3	P8_3
89	DIGIO_4	P8_4		90	DIGIO_5	P8_5
91	DIGIO_6	P8_6		92	DIGIO_7	P11_0
93	DIGIO_8	P10_0		94	DIGIO_9	P10_7
95	DIGIO_10	P10_8		96	DIGIO_11	P10_15
97	DIGIO_12	P0_9		98	DIGIO_13	P0_10
99	DIGIO_14	P0_11		100	DIGIO_15	P0_12
101	-	-		102	-	-
103	MUX0	P10_4		104	MUX1	P10_5
105	MUX2	P10_6		106	-	-
107	ADC0	AP0_0		108	ADC1	AP0_1
109	ADC2	AP0_2		110	ADC3	AP0_3
111	ADC4	AP0_4		112	ADC5	AP0_5
113	ADC6	AP0_6		114	ADC7	AP0_7
115	VDDIOF	-		116	VDDIOF	-
117	VOLTAGE2	-		118	VOLTAGE2	-
119	VOLTAGE2	-		120	VOLTAGE2	-

(*) CAN1 signals for R1L

When using this piggyback board in conjunction of R1L 144-pin device and the Y-RH850-X1X-MB-T1-Vx mainboard the following details must be noted:

On the Piggyback board the signals of P0_2 and P0_3 are connected the CN1 pins 30 and 28 for usage as CAN1Rx and CAN1Tx signals.

The ports P0_2 and P0_3 on the R1L 144-pin device do not carry those CAN1 signals, they are available (only) at ports P10_6 (CAN1RX) and P10_7 (CAN1TX).

Applicable workaround / solutions:

In order to use the CAN1 instance of the R1L device on the mainboard a manual wire connection must be made between the related pins of the device and pin headers on the mainboard. See the connection below for details:

CAN1 signals	Piggyback board	Mainboard
CAN1Tx	Pin 121 (P10_7)	CN5 pin 1
CAN1Rx	Pin 120 (P10_6)	CN5 pin 2

7.2.2 Connector CN2

Pin	Function	Device Port	Pin	Function	Device Port
1	CAN2Tx	P12_0	2	CAN3Tx	P1_3
3	CAN2Rx	P11_15	4	CAN3Rx	P1_2
5	CAN4Tx	P0_10	6	CAN5Tx	P11_6
7	CAN4Rx	P0_9	8	CAN5Rx	P11_5
9	LIN2Tx	P0_10	10	LIN3Tx	P20_5
11	LIN2Rx	P0_9	12	LIN3Rx	P20_4
13	LIN4Tx	P1_11	14	LIN5Tx	P11_11
15	LIN4Rx	P1_10	16	LIN5Rx	P11_12
17	LIN6Tx	-	18	LIN7Tx	-
Q	LIN6Rx	-	20	LIN7Rx	-
21	LIN8Tx	-	22	LIN9Tx	-
23	LIN8Rx	-	24	LIN9Rx	-
25	LIN10Tx	P10_10	26	LIN11Tx	P0_5
27	LIN10Rx	P10_9	28	LIN11Rx	P0_4
29	LIN12Tx	P10_14	30	LIN13Tx	P1_1
31	LIN12Rx	P10_13	32	LIN13Rx	P1_0
33	LIN14Tx	P1_9	34	LIN15Tx	P1_5
35	LIN14Rx	P1_8	36	LIN15Rx	P1_4
37	-	-	38	-	-
39	-	-	40	-	-
41	MLBCLK	-	42	MLBRESET	-
43	MLBSIG	-	44	MLBDAT	-
45	-	-	46	-	-
47	-	P10_4	48	-	P10_13
49	-	P10_6	50	-	P10_14
51	-	-	52	-	-
53	-	-	54	-	-
55	-	-	56	-	-
57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
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107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

7.2.3 Connector CN3

Pin	Function	Device Port	Pin	Function	Device Port
1	PWM00	P10_0	2	PWM01	P10_1
3	PWM02	P10_2	4	PWM03	P10_3
5	PWM04	P10_7	6	PWM05	P10_8
7	PWM06	P10_9	8	PWM07	P10_10
9	PWM08	P9_0	10	PWM09	P9_1
11	PWM10	P0_4	12	PWM11	P0_1
13	PWM12	P0_2	14	PWM13	P0_3
15	PWM14	P8_0	16	PWM15	P8_1
17	PWM16	P10_11	18	PWM17	P10_12
Q	PWM18	P10_13	20	PWM19	P10_14
21	PWM20	P9_2	22	PWM21	P9_3
23	PWM22	P8_2	24	PWM23	P8_3
25	PWM24	P10_15	26	PWM25	P11_0
27	PWM26	P11_1	28	PWM27	P11_2
29	PWM28	P11_3	30	PWM29	P11_4
31	PWM30	P11_5	32	PWM31	P11_6
33	PWM32	P11_7	34	PWM33	P9_4
35	PWM34	P9_5 or P0_11	36	PWM35	P9_6 or P0_6
37	PWM36	P8_4	38	PWM37	P8_5
39	PWM38	P8_6	40	PWM39	P8_7
41	PWM40	P8_8	42	PWM41	P8_9
43	PWM42	P8_10	44	PWM43	P8_11
45	PWM44	P8_12	46	PWM45	P0_12
47	PWM46	P0_13	48	PWM47	P0_14
49	PWM48	P11_8	50	PWM49	P11_9
51	PWM50	P11_10	52	PWM51	P11_11
53	PWM52	P11_12	54	PWM53	P11_13 or P10_4
55	PWM54	P11_14 or P10_5	56	PWM55	P11_15
57	PWM56	P12_0	58	PWM57	P12_1
59	PWM58	P12_2	60	PWM59	P20_4
61	PWM60	P20_5	62	PWM61	P18_0
63	PWM62	P18_1	64	PWM63	P18_2
65	PWM64	-	66	PWM65	-
67	PWM66	-	68	PWM67	-
69	PWM68	-	70	PWM69	-
71	PWM70	-	72	PWM71	P18_3
73	PWM72	-	74	PWM73	-
75	PWM74	-	76	PWM75	-
77	PWM76	-	78	PWM77	-
79	PWM78	-	80	PWM79	-
81	PWMADC00	AP0_8	82	PWMADC0	AP0_9
83	PWMADC02	AP0_10	84	PWMADC0	AP0_11
85	PWMADC04	AP0_12	86	PWMADC0	AP0_13
87	PWMADC06	AP0_14	88	PWMADC0	AP0_15
89	PWMADC08	AP1_0	90	PWMADC0	AP1_1

91	PWMADC10	AP1_2	92	PWMADC1	AP1_3
93	PWMADC12	AP1_4	94	PWMADC1	AP1_5
95	PWMADC14	AP1_6	96	PWMADC1	AP1_7
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

Chapter 8 Other circuitry

8.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

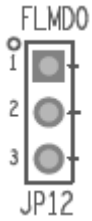
8.2 Mode Selection

The piggyback board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP12
- FLMD1 via jumper JP13
- MODE0 via jumper JP14
- MODE1 via jumper JP15
- MODE2 via jumper JP16

To apply "High" or "Low" to the mode pins, the pins 1 and 2, or the pins 2 and 3 (if available) of the corresponding jumper must be closed, respectively.

Note: Pin 1 of all jumpers is marked by a small circle.



CAUTION: Be careful in configuration of mode related pins. Wrong configuration and operation of the device outside of its specification can cause irregular behaviour of the device and long term damage cannot be excluded. Be sure to check the corresponding User's Manual for details, which modes are specified for the used device

Note:
In the very most cases the 'Normal operating mode' of the device will be used. This mode is for execution of the user program. The on-chip debug functions also use this mode.
To select the 'Normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, close the pins 2-3 on the jumper JP25:

All other jumper related to the mode selection can be left open.

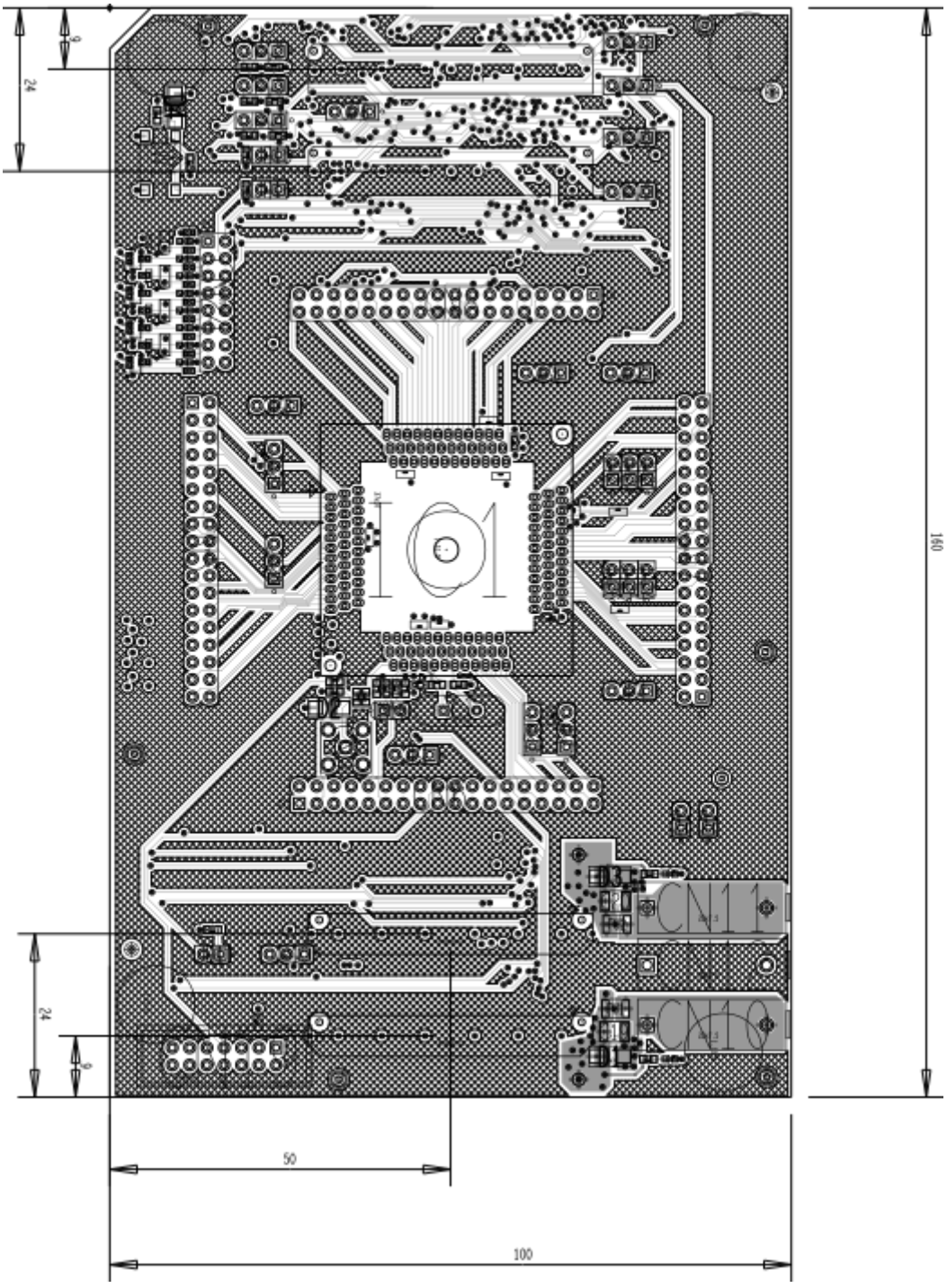
8.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins. Device pins P8_0 to P8_7 are connected to the even pins 2 to 16 of the pin header CN24, while the LEDs 1 to 8 are connected to the odd pins 1 to 15, respectively.

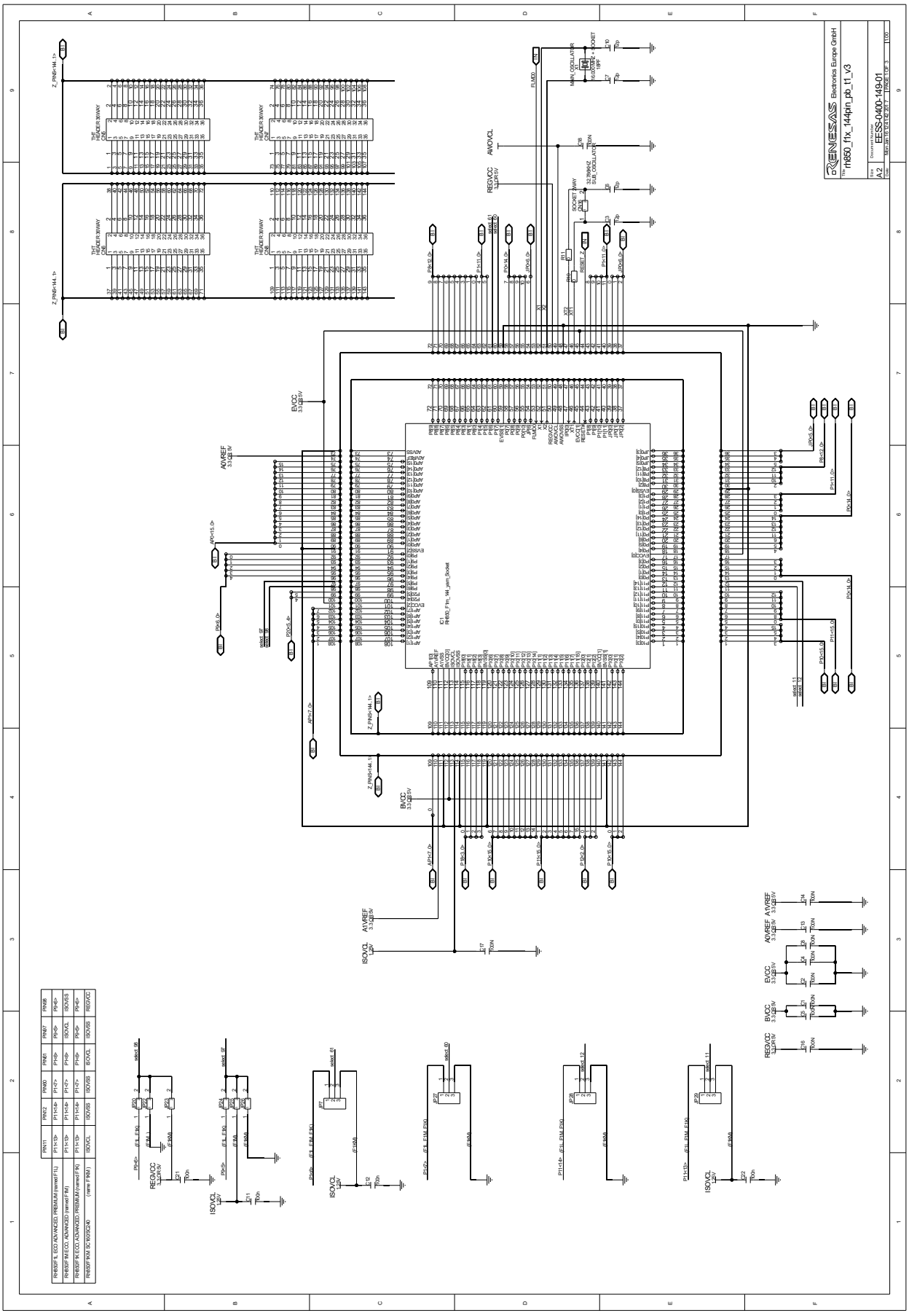
Thus the LEDs can be either connected to

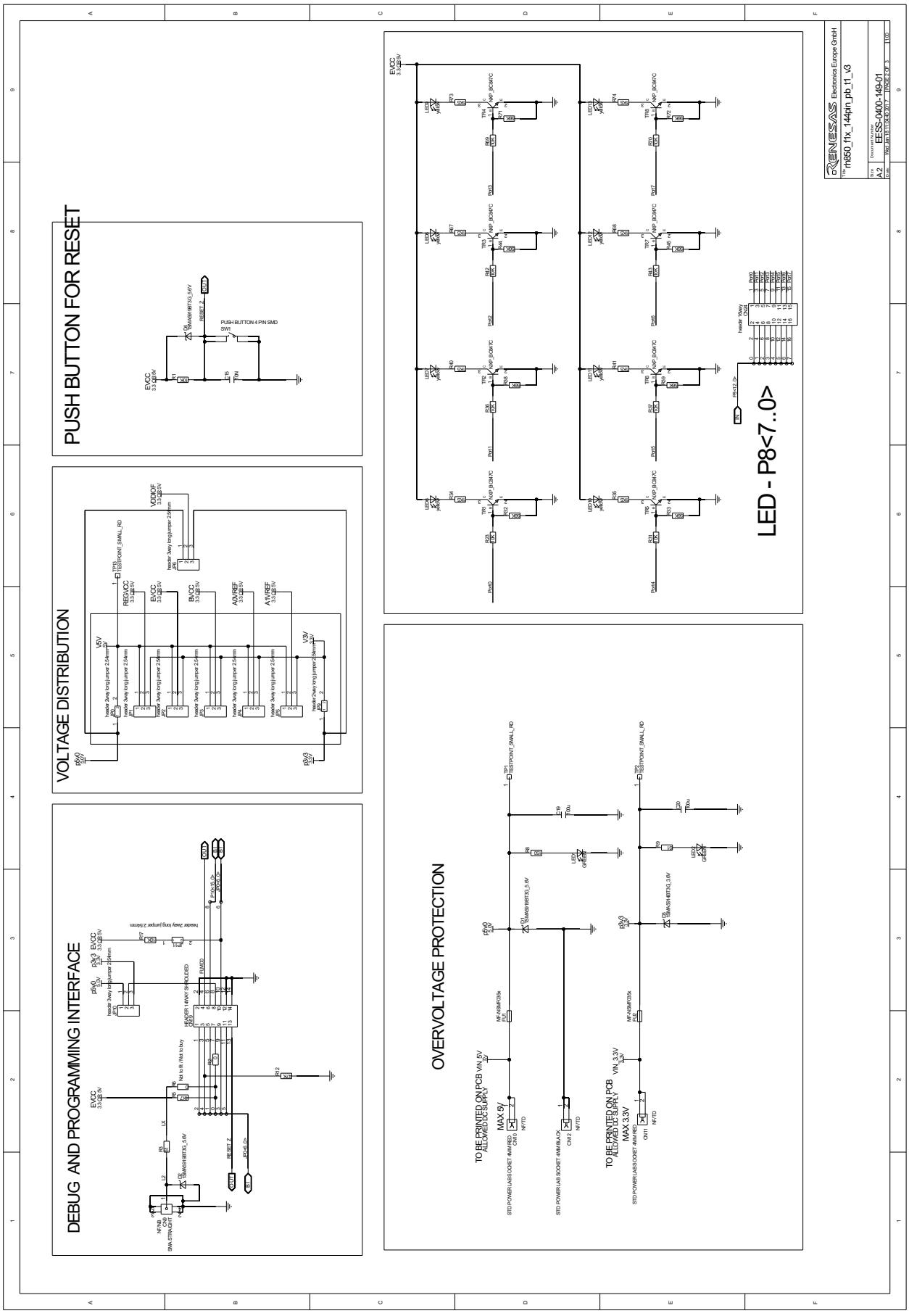
- the device port pins P8_0 to P8_7 by closing the connection on CN24 using a jumper, or
- any device port pin by using the provided wire connections.

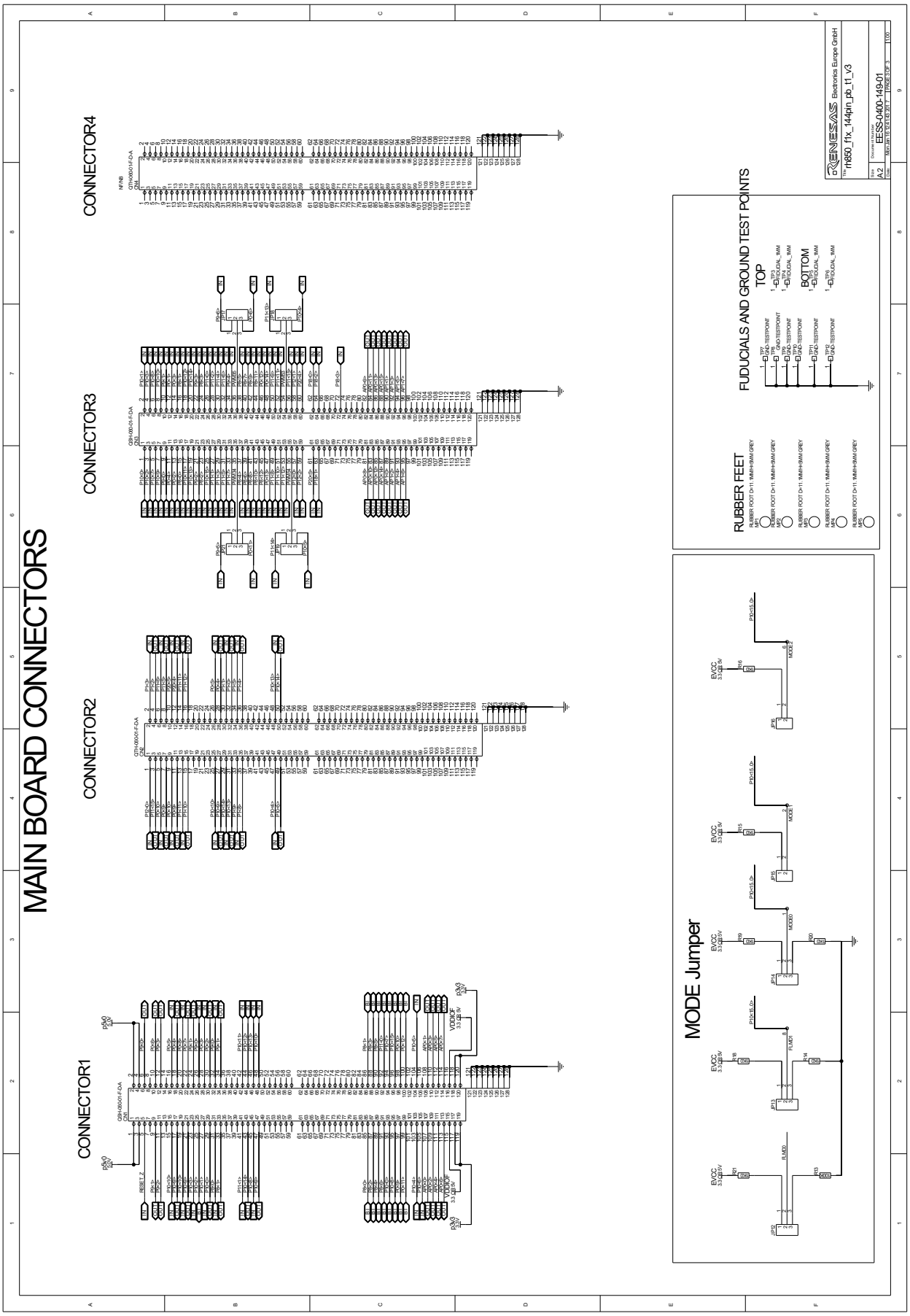
Chapter 9 Mechanical dimensions



Chapter 10 Schematic




PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
OVERVOLTAGE PROTECTION
LED - P8<7..0>
RENESAS Electronics Europe GmbH
rh850_f1x_144pin_pb_t1_v3
EESS-0400-149-01


MAIN BOARD CONNECTORS
CONNECTOR1
CONNECTOR2
CONNECTOR3
CONNECTOR4
MODE Jumper
FUDUCIALS AND GROUND TEST POINTS
TOP
BOTTOM
RUBBER FEET
RENESAS Electronics Europe GmbH
rh850_f1x_144pin_pb_t1_v3
ECS-0400-149-01

Chapter 11 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2017-06-21	1.00	Initial release
2018-05-17	1.10	Corrected table for the jumper configuration in chapter 3
2021-08-12	1.20	Added RH850/F1KM-S2 to the list of supported devices

Differences to the Y-RH850-F1X-144PIN-PB-T1-V2:

- Support for RH850/F1K, F1KM-S2 and F1KM-S4 devices.
- Added jumpers for mode selection.
- Added signal LEDs.
- EVTO signal added to the debug interface.
- Updated signal assignment of main board connectors CN1 to CN4.

RH850/F1x, R1x 144pin Piggyback Board T1-V3 User's Manual: Piggyback Board T1-V3

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