RSSKRX23E-B

User's Manual

Renesas Electronics
www.renesas.com

Rev.1.10   Apr. 2024

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(Rev.5.0-1   October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

CAUTION

This is a 'Class A' (EN55032:2015+A11:2020) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

CAUTION

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

European Union Regulatory Notices:

The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the European Union only. This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner. Renesas Electronics Europe GmbH can take back end of life equipment, register for this service at http://www.renesas.eu/weee

Disclaimer

By using this Renesas Solution Starter Kit (RSSK), the user accepts the following terms:

Precautions

The following precautions should be observed when operating this RSSK:

How to Use This Manual

1. Purpose and Target Readers

This manual is provided to help the users understand the outline and electrical characteristics of the board of Renesas Solution Starter Kit for RX23E-B (called "RSSKRX23E-B board" or "the board" below).

Although this manual contains an overview of the RSSKRX23E-B board functions, it is not written as a built-in programming or hardware design guide.

> Particular attention should be paid to the precautionary notes when using RSSKRX23E-B board. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

> The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

For Renesas Solution Starter Kit for RX23E-B the following documents are available. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Explanation of the RSSKRX23E-B board hardware specifications	RSSKRX23E-B User's Manual	R12UZ0108 (this document)
Quick Start Guide	Provides simple instructions to setup the RSSKRX23E-B board and example of use	RSSKRX23E-B Quick Start Guide	R20QS0044
Application Note	Explanation of the control program for RSSKRX23E-B board and its binary file.	RX23E-B Group RSSKRX23E-B Board Control Program	R01AN6364

For specifications of the device (RX23E-B: R5F523E6LDFP, or R5F523E6LGFP) mounted on the board, the following documents are available. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual: Hardware	Explanation of RX23E-B hardware specifications (pin layout, memory map, peripheral function specifications, electrical characteristics, and timing) and operation * For details on how to use peripheral functions, refer to "Application Notes".	RX23E-B Group User's Manual: Hardware	R01UH0972

2. For Your Safety

Do not fail to read this manual before using the board

- Follow the indications in this manual when using the board
- Keep this manual near the board so you can refer to it whenever necessary.
- Transfer or sale of the board to third parties is prohibited without written approval.
- The purchaser or importer of the board is responsible for ensuring compliance with local regulations.

In addition, the customer is responsible for ensuring that the board is handled correctly and safely, in accordance with the laws of the customer's country (region).

- The manual for the board, and specification (the documents) are the tool that was developed for

the function and performance evaluation of Renesas Electronics semiconductor device (Renesas Electronics device) mounted on the board, and not guarantee the same quality, function and performance.

- By purchasing the board or downloading the documents from Renesas Electronics website, the support

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- All information contained in this manual represents information on products at the time of publication

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Meaning of Notations

In this manual, items related to the safe use of the product are indicated as described below.
The degree of injury to persons or damage to property that could result if the designated content in this manual is not followed is indicated as follows.

⚠ **Warning**	Indicates content that, if not followed, could result in death or serious injury to the user.
⚠ **Caution**	Indicates content that, if not followed, could result in injury*1 to persons or physical damage.*2

Note 1.   Injury refers to conditions for which treatment would necessitate hospitalization or regular hospital visits.
Note 2.   Physical damage refers to damage affecting the wider surroundings, such as the user's home or property.

Requirements related to the handling of the product are classified into the following categories.

- Marks indicating that an action is prohibited.

🚫	General Prohibition The indicated action is prohibited.

- Marks indicating that an action is alerted

⚠	General Caution Indicates a general need for caution that is not specified.	⚠	Example: Caution - Static Electricity! Indicates the possibility of injury due to static electricity

- Marks directing that the specified action is required.

❗	General Instruction The specified action is required.		Example: Turn Off (Disconnect) Power Supply! Instructs the user to turn off (disconnect) the power supply to the product.

■ Danger Items

	⚠ **Warning**
🛈	Always insert plugs, connectors, and cables securely, and confirm that they are fully inserted. ● Incomplete connections could cause fire, burns, electric shock, or injury.
🛈 ⊶	Use the power supply apparatus specified in the manual. ● Failure to do so could cause fire, burns, electric shock, injury, or malfunction.
	Disconnect the power supply and unplug all cables when the system will not be used for a period of time or when moving the system. ● Failure to do so could cause fire, burns, electric shock, or malfunction. ● This will protect the system against damage due to lightning.
	Use a mechanism (switch, outlet, etc.) located within reach to turn off (disconnect) the power supply. ● In case of emergency, it may be necessary to cut off the power supply quickly.
	Turn off the power supply immediately if you notice abnormal odor, smoke, abnormal sound, or overheating. ● Continuing to use the system in an abnormal condition could cause fire, burns, or electric shock.
🚫	Do not integrate the product or any part of it into other equipment. Do not insert or remove cables or connectors when the product is powered on. ● The product has no safety case. ● Failure to observe the above could cause fire, electric shock, burns, or malfunction. ● The product may not perform as expected if used for other than its intended purpose.

■ Caution Items

	⚠ **Caution**
⚠	Before modifying any part of this product, carefully check the manual. ● Incorrect modification or retrofitting may cause heat generation and device failures.
🛈	Follow the procedure specified in the manual when powering the system on or off. ● Failure to do so could cause overheating or malfunction.
	Use the cable that is less than 3m in length to be connected to the product. ● Failure to do so could cause device failures or malfunction by external noise.
⚠	Caution – Static Electricity ● Use the antistatic band. Failure to do so could cause malfunction or unstable motion.

3.List of Abbreviations and Acronyms

Abbreviation	Full Form / Description
ADC	Analog to Digital Converter
AFE	Analog Front End
AMUX	Analog Multiplexer
BUF	Buffer Amplifier
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DSAD	Delta-Sigma Analog-to-Digital Converter
E2 Lite	Renesas On-chip Debugging Emulator
FW	Firmware
GUI	Graphical User Interface
I2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
I/F	Interface
LCDC	Liquid Crystal Display Controller
LDO	Low Dropout regulator
LED	Light Emitting Diode
LSW	Low Side Switch
MCU	Micro Controller Unit
NM	Not Mounted
PC	Personal Computer
PGA	Programmable Gain Amplifier
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RS-485	Recommended Standard 485
RTD	Resistance Temperature Detector
S12AD	12-Bit Successive-Approximation-Register Analog-to-Digital Converter
SCI	Serial Communication Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus

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Table of Contents

RSSKRX23E-B
Renesas Solution Starter Kit for RX23E-B

1. Overview

1.1 Purpose

The board of Renesas Solution Starter Kit for RX23E-B (called "RSSKRX23E-B board" or "the board" below) is an evaluation tool for the Renesas microcontroller RX23E-B. This manual describes the hardware aspect of the RSSKRX23E-B board in detail. The manual also describes how to connect the board to a PC and sensors for evaluation.

1.2 Mounted MCU

Table 1-1 lists the specifications of the MCU mounted on the board.

Table 1-1 Mounted MCU

Product group	RX23E-B
MCU model name	R5F523E6LDFP (Note)
Maximum CPU operating frequency	32 MHz
Number of bits	32 bit
Package/number of pins	PLQP0100KB-B / 100-pin
24-bit delta-sigma A/D converter (DSAD)	• One circuit (DSAD0) • Fourth-order sinc filter, fourth-order sinc filter + fourth order sinc filter, fifth-order sinc filter, or fifth-order sinc filter + first-order sinc filter • Internal programmable gain instrumentation amplifier (PGA) • Operating mode: single scan, continuous scan, or one-shot • High-speed conversion: 125 kSPS (max.) • Oversampling ratio: First stage: 32 to 256 (only multiples of 32) Second stage: 1 to 4096
16-bit D/A converter (R16DA)	• 16-bit resolution • Low impedance output (equipped with output buffer)
ROM	256 KB
RAM	32 KB
Operating temperature range	-40 to +85℃ (R5F523E6LDFP)
Storage temperature range	-55 to +125℃

Note: R5F523E6LGFP (operating temperature range: -40 to +105℃) may be mounted. The mounted MCU cannot be specified.

1.3   Functions and Features

The board has the following functions and features.

(1)   Functions and features for hardware and system design engineers

- Power supply selection circuit
- A/D converter evaluation circuit
- Thermocouple measurement circuit
- Resistance temperature detector (RTD) measurement circuit
- Strain gage measurement circuit
- FW controlling DSAD, AFE, and DAC operation
- Transmission of measurement results and reception of AFE settings using USB communication

(2)   Functions and features for software design engineers

- RX23E-B programming and debugging
- Switches, LEDs, an LCD, and other user interfaces

The board has all circuits required for microcontroller operation.

1.4 Specifications

1.4.1 Board Specification

Table 1-2 lists the board specifications.

Table 1-2 Specifications of the RSSKRX23E-B board

Item	Specification
Board model name	RTK0ES1001C00001BJ
Applicable emulator	E2 Emulator, E2 Emulator Lite
Board outline	140 mm × 135 mm
Board thickness	1.6 mm
Layer construction	4-layer (Signal – GND - Power supply - Signal)
Component mounting	One side
Operating temperature	Room temperature
Operating humidity	No condensation allowed

1.4.2   Main Components, Communication I/F and User I/F

Table 1-3 lists the main components, communication I/F and user I/F.

Table 1-3 Main Components, Communication I/F, User I/F

Item	Reference	Model name / Description
MCU	U1	R5F523E6LDFP or R5F523E6LGFP (Note)
Main clock	Y1	ECS-80-12-33-JEN: External quartz crystal unit 8 MHz
Sub clock	Y2	SSP-T7-FL: External quartz crystal unit 32.768 kHz
LDO	U2	ISL80410IBEZ: High-accuracy LDO, Variable output (set to 5V)
5VREF	U3	ISL21090BFB850Z: Ultra-low noise, Precision voltage reference, 5 V output
2.5VREF	U8	ISL21090BFB825Z: Ultra-low Noise, Precision voltage reference, 2.5 V output
RS-485 transceiver	U5	RAA7881582GSU: 20 Mbps, RS-485/RS-422 transceiver
CAN transceiver	U6	MAX13053: ±80 V Fault protection, Silent mode
USB serial converter	U10	FT232HL: USB Hi-Speed
On-board RTD	RTD1	PTS060301B100RP100: Pt100 Class F0.3 (Class B)
LED	LED0	User LED, Color: Red, Connected to P70
	LED1	User LED, Color: Yellow, Connected to P71
	LED2	User LED, Color: Red, Connected to P72
	LED3	User LED, Color: Yellow, Connected to P73
	LED4	Power LED, Color: Green, Turned on when power ON
Switch	SW1	Tactile switch, 1-pin, Connected to PE1 (IRQ4)
	SW2	Tactile switch, 1-pin, Connected to PE2 (IRQ5)
	SW3	Slide switch, 2-pin, Connected to PE3 (IRQ6), PE4 (IRQ7)
	SW4	Reset switch, Tactile switch, 1-pin, Connected to RES#

Note: Either one is mounted. The mounted MCU cannot be specified.

1.4.3 Connectors

Table 1-4 lists the connectors on the board.

Table 1-4 Mounted Connectors

Item	Reference	Overview
Power supply terminal block	CN1	System power input terminal block (2-pin)
	CN2	Analog power input terminal block (2-pin)
	CN4	Analog power output terminal block (2-pin)
Signal terminal block	CN3	D/A converter I/O terminal block (4-pin)
	CN5	Analog input terminal block 1 (4-pin)
	CN6	±10 V Analog input terminal block (4-pin)
	CN7	Analog input terminal block 2 (15-pin)
Thermocouple connector	CN8	Miniature thermocouple socket (2-pin), Material: copper
Emulator connector	CN9	14-pin interface connector, straight
USB connector	CN10	USB mini-B
RS-485 connector	J1	Pin header (3-pin 2.54 mm pitch)
CAN connector	J2	Pin header (3-pin 2.54 mm pitch)
PMOD type 3A connector	PMOD1	Pin socket (12-pin, 2-line, right angle)
PMOD type 6A connector	PMOD2	Pin socket (12-pin, 2-line, right angle)
MCU pin header	JA1	No component mounted (24-pin, 2.54 mm pitch)
	JA2	No component mounted (30-pin, 2.54 mm pitch)
	JA3	No component mounted (24-pin, 2.54 mm pitch)
LCD connector	JA4	No component mounted (50-pin, 2.54 mm pitch)

1.4.4   Jumper Pins

Table 1-5 lists the jumper pins on this board.
<u>Do not switch the jumper pins while the power is on as this may cause malfunction, degradation, or unexpected operation.</u> JP2 consists of two components, JP2_1 and JP2_2. JP2_2 is not mounted. for JP7~JP10 settings and factory default settings, refer to "Table 2-4 Functions of the Analog Input Circuit and Corresponding Jumper Settings"

Table 1-5 Jumper Pins

Reference	Function	Explanation
JP1	Selecting a digital power supply	Selects Vd, VLDO, Vbus, or Vp as VCC. Factory default setting is VLDO.
JP2	Selecting an analog power supply	Selects VCC, Va, or 5VREF as AVCC0. Factory default setting is VCC.
JP3	Selecting the direction of PMOD TYPE-3A power supply	Selects the direction of PMOD TYPE-3A connector (PMOD1) power supply. Factory default setting is to output power to the PMOD1 connector.
JP4	Selecting VREFH	Selects AVCC0 or external input as VREFH. Factory default setting is AVCC0.
JP5, JP6	Selecting an external reference input	Selects AVCC0 (AVSS0) or external reference input as REF1P and REF1N. Factory default setting is external reference input.
JP7, JP9, JP10	Selecting on-board RTD	Connects AIN9 (IEXC1), AIN5, AIN4, and REF0P to the on-board RTD (RTD1).
JP8	Selecting 3-wire RTD	Switches AIN9 (IEXC1), AIN8 (IEXC0), AIN5, and AIN4 for connection to 3-wire RTD.
JP11	Selecting the MCU operating mode	Selects the single-chip mode or boot mode as the MCU operating mode. Factory default setting is single-chip mode.
JP12	Selecting whether to use the CAN bus termination resistor	Selects whether to use the termination resistor in CAN communication line. Factory default setting is termination resistor enabled.

1.4.5   System Block Diagram

System Block Diagram
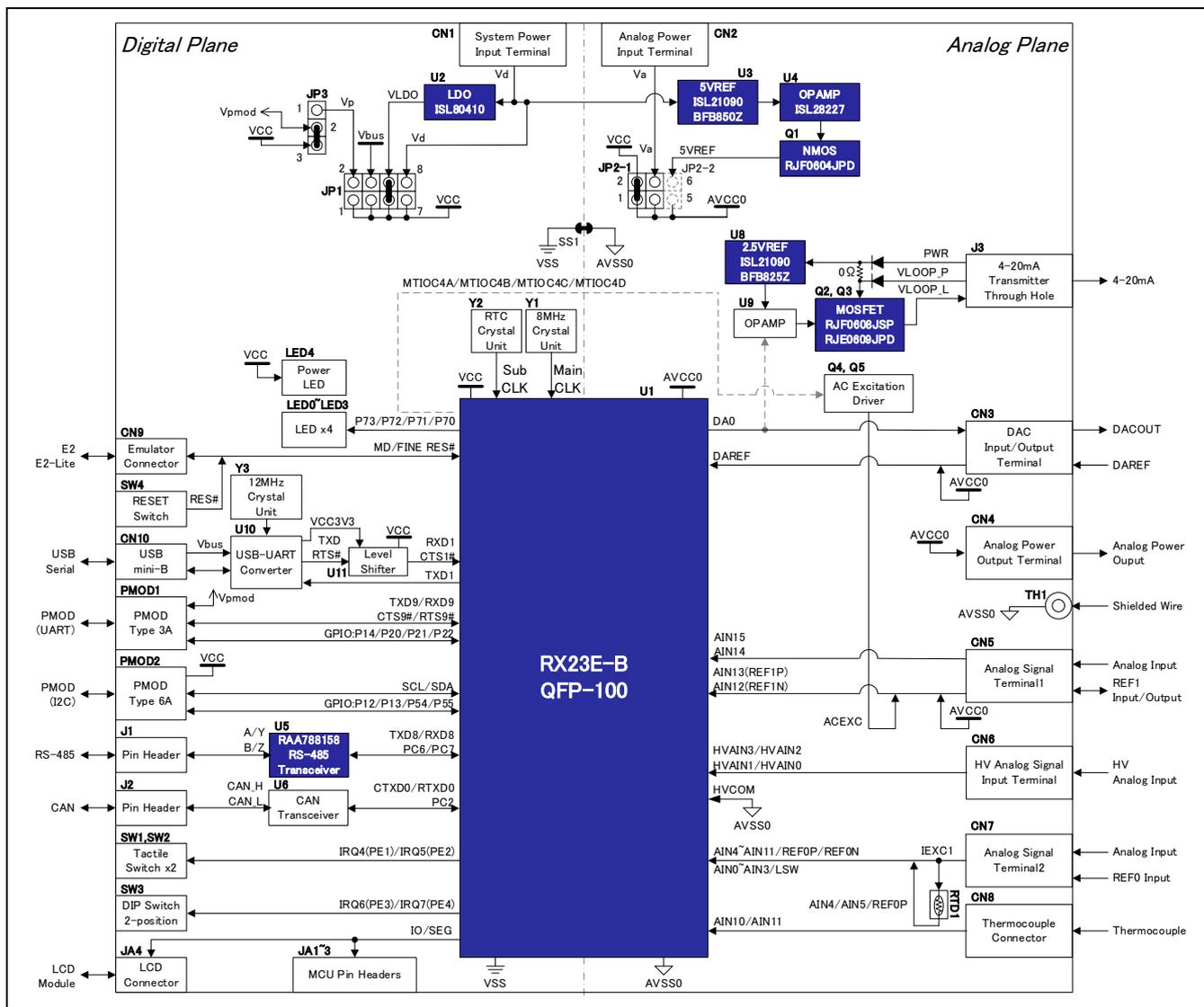
Figure 1.1 RSSKRX23E-B Board System Block Diagram

1.4.6   Board Appearance
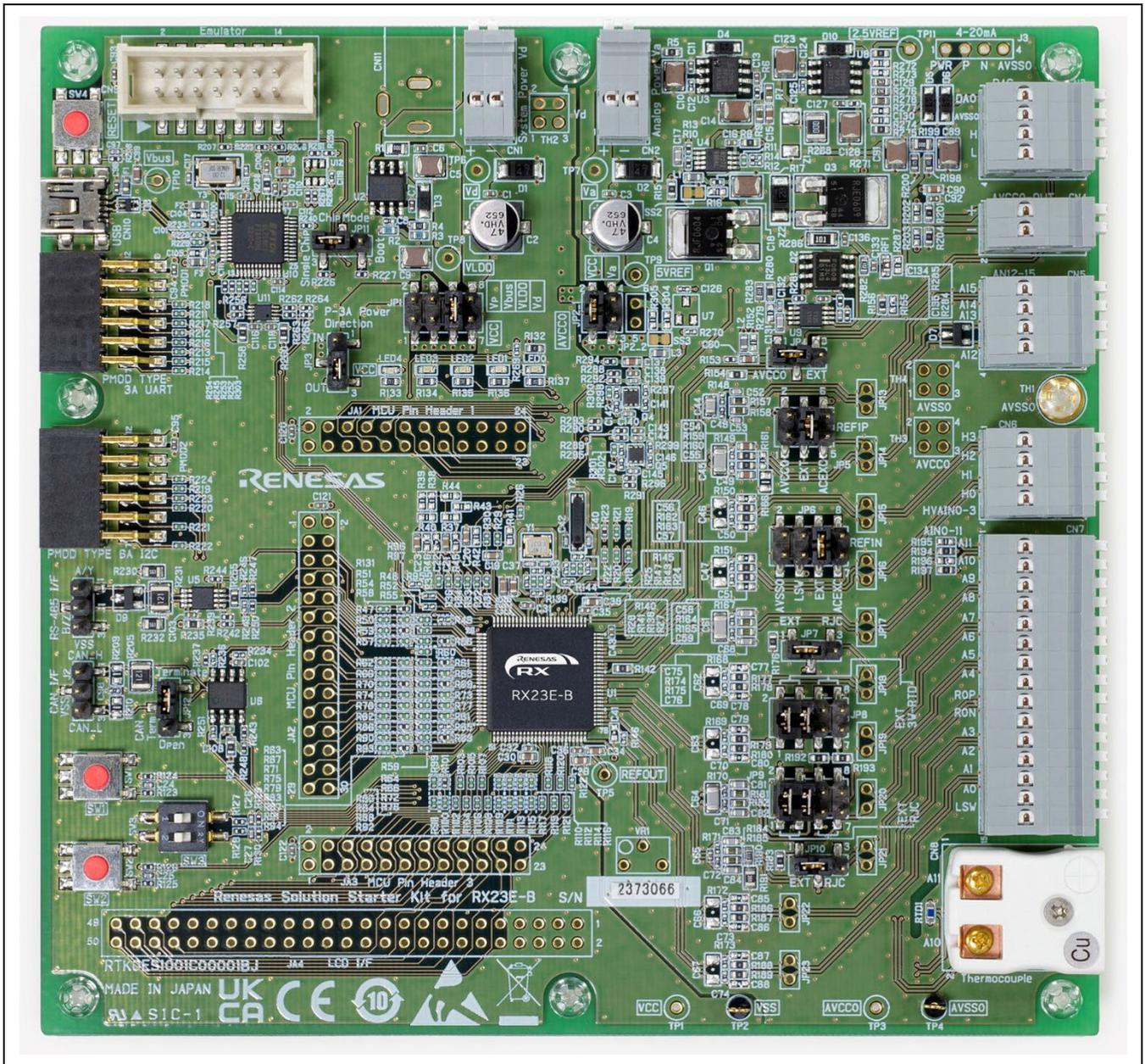
Figure 1.2 RSSKRX23E-B Board Appearance (Front side)
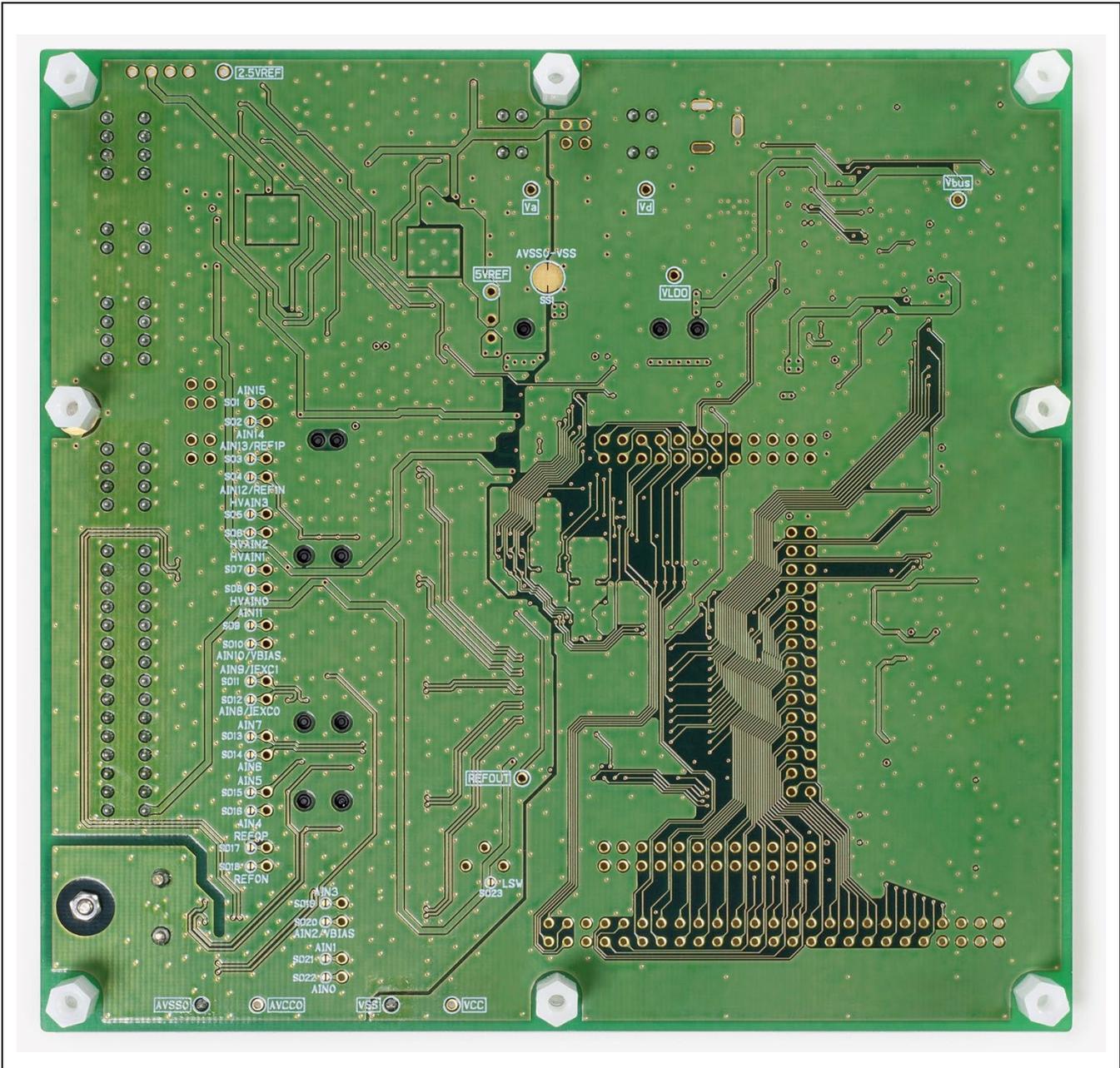
Figure 1.3 RSSKRX23E-B Board Appearance (Back side)

2.   Using the RSSKRX23E-B Board

2.1   Operating Conditions

Table 2-1 lists the recommended operating conditions of the board.

When using the board, please observe the recommended operating conditions and maximum ratings.
Failure to observe the recommended operating conditions may cause unexpected operation. Failure
to observe the maximum ratings may cause malfunction or degradation.

Table 2-1 Recommended Operating Conditions
Condition: VSS = AVSS0 = 0V

Item	Symbol	Connector (Pin No.)	Recommended operating range	Maximum rating	Condition
System power supply	Vd (VCC)	CN1	4.5 to 5.25 V (Note 1)	5.8 V (Note 2)	When pins 7-8 of JP1 are connected (When Vd is connected to VCC)
	Vd		7 to 18 V (Note 3)	20 V	When pin 5-6 of JP1 are connected (When the LDO is used)
USB power supply	Vbus (VCC)	CN10	4.5 to 5.25 V (Note 1)	5.5 V	When pins 3-4 of JP1 are connected (When Vbus is connected to VCC)
	Vbus		3.6 to 5.25 V	5.5 V	When pins 1-2, 5-6, or 7-8 of JP1 are connected (Note 4)
PMOD3A Power supply	Vp (VCC)	PMOD1	4.5 to 5.25 V (Note 1)	5.8 V	When pins 1-2 of JP1 AND pins 1-2 of JP3 are connected (Power suppy from PMOD type 3A)
Analog power supply	AVCC0	CN2	4.5 to 5.5 V (Note 5)	6.5 V	When pins 3-4 of JP2 are connected AND VCC > 2.4 V (When analog/digital power supplies are separated)
Digital pin	V_{IN}	JA1, JA2, JA3, JA4 PMOD1, PMOD2	-0.3 to VCC+0.3		RX23E-B absolute maximum rating
Analog pin	V_{AIN}	CN5, CN7 (R0P, R0N, A0to11)	-0.3 to AVCC0 +0.3		RX23E-B absolute maximum rating
HV analog pin	V_{HVAIN}	CN6	±10 V	±15 V	RX23E-B absolute maximum rating
LSW pin	I_{LSW}	CN7 (LSW, R1N (A12)[*6])	-	30 mA	When the LSW is switched ON

(Note 1) Operation of USB serial communication, CAN communication, and RS-485 communication are
guaranteed only in condition of inside recommended operating range (4.75 to 5.25 V). The
recommended operating voltage range of the digital side of the RX23E-B is 1.8 to 5.5 V.

(Note 2) Although the absolute maximum rating of the digital side of the RX23E-B is 6.5 V, the absolute
maximum rated I/O voltage of the USB serial converter IC, FT232HL (U10), is 5.8 V.

(Note 3) The operating voltage of the LDO (ISL80410) is 6 to 40 V, and that of high precision reference voltage source of 5 V output (ISL21090BFB850Z) is 7 to 36 V. The recommended operating range and the maximum ratings on the board are specified, considering the capacitor rated voltage, power line voltage drop, and heat generation of the LDO.

(Note 4) Use Vbus for supplying power to U10 (FT232HL) regardless of the connection status of J1.

(Note 5) Supply the power to VCC and AVCC0 simultaneously or sequentially in this order.

(Note 6) The R1N (REF1N) pin is connected to the LSW pin when pins 3 and 4 of JP6 are connected.

2.2 Selecting Power Supplies

Figure 2.1 shows the power supply configuration of the board. Table 2-2 shows how to select each power supply on the board. Before using a combination of power supplies not listed in Table 2-2, carefully check the recommended operating conditions in Table 2-1.
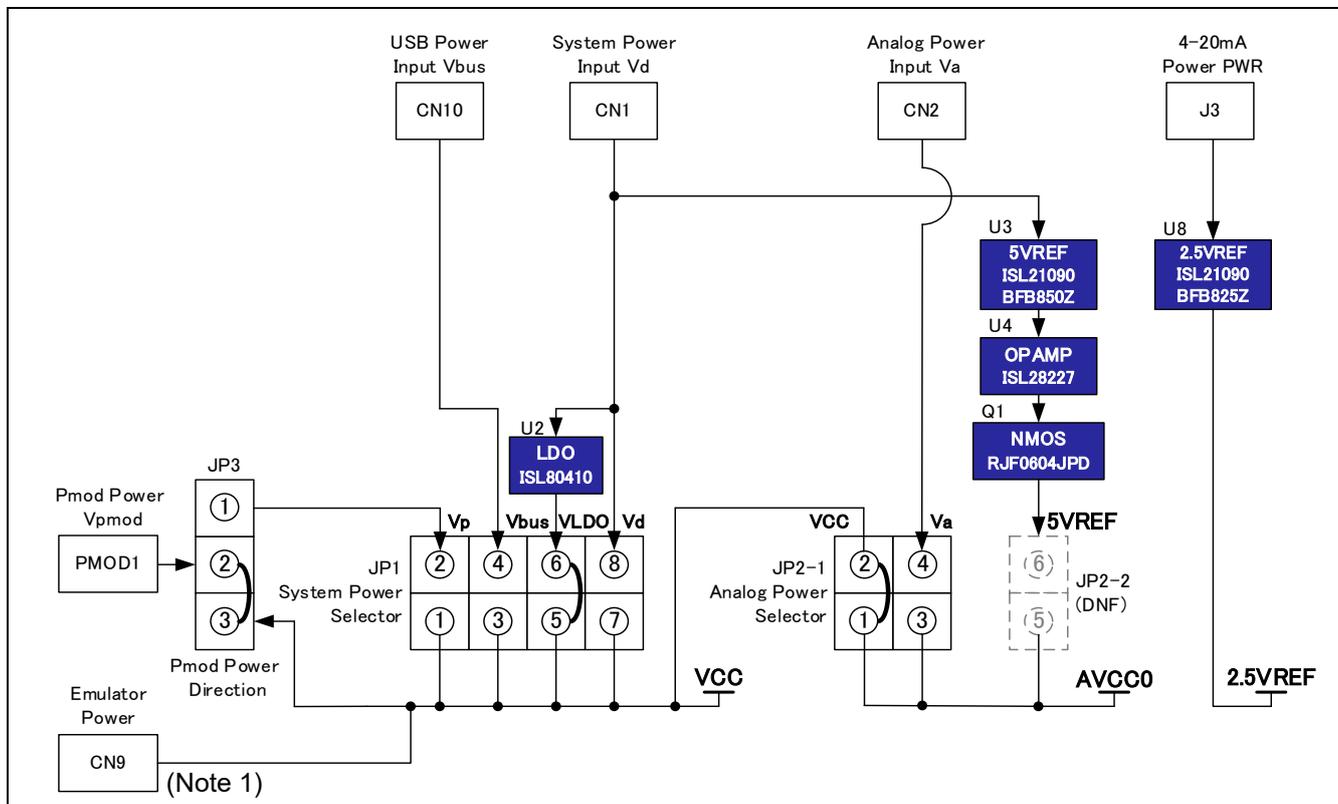
Figure 2.1 Power Supply Configuration of the RSSKRX23E-B Board

Table 2-2 Power Selection Example

Input power supply	Digital power supply VCC	Analog power supply AVCC0	JP1 connection	JP2 connection	Remarks
Vd	Vd	Vd	Pins 7-8	Pins 1-2	Common power supply
	Vd	Va	Pins 7-8	Pins 3-4	Separate power supplies
	VLDO	VLDO	Pins 5-6	Pins 1-2	Factory default setting
Vbus	Vbus	Vbus	Pins 3-4	Pins 1-2	USB operation
Vp	Vp	Vp	Pins 1-2	Pins 1-2	Connect pins 1-2 of JP3
Emulator	Emulator	Emulator	Pins 7-8 (Note 1)	Pins 1-2	Do not supply the power from Vd, VLDO, Vbus, or Vp. (Note 2)

(Note 1) **When supplying the power from the emulator, do NOT connect pins 5 and 6 of JP1. If they are connected, the emulator power supply is connected to the U2 output pin, and U2 may be damaged.**

(Note 2) **The emulator power supply is directly connected to VCC. Never supply the power from the emulator while the power is supplied from Vd, VLDO, Vbus, or Vp. It may cause the damage of the power supply, emulator, and/or U2.**

2.3   Connecting a PC to the Board

Figure 2.2 shows a configuration used when a PC is connected to the board. Table 2-3 lists functions available when a PC is connected to the board.

When connecting a PC to the board, supply the power to the board as described in " 2.2 Selecting Power Supplies".

The board can be connected to the Renesas on-chip debugging emulator to debug user code. When using the emulator, connect the 14-pin interface cable attached with the emulator to CN9. **Before supplying the power from the emulator, check that the following conditions are satisfied. If any of the conditions is not satisfied, a failure may occur in the board, power supply, and/or emulator.**

- **The power is not supplied to VCC from any source other than the emulator.**
- **Pins 5 and 6 of JP1 are not connected.**

3.3-V power is supplied from E2 emulator Lite. Note that USB serial communication, RS-485 communication, and CAN communication do not operate. When using the emulator, refer to the user's manual of the emulator. The board contains a USB serial conversion IC. SCI1 interface of the MCU and USB serial conversion IC are connected and communication with a PC is available by USB serial communication. To use USB serial communication, connect a USB cable to CN10 (USB mini-B connector).

For details on the circuits around CN9 and CN10, see "3.1 USB Serial Communication Circuit" and "3.2 Emulator Peripheral Circuit".
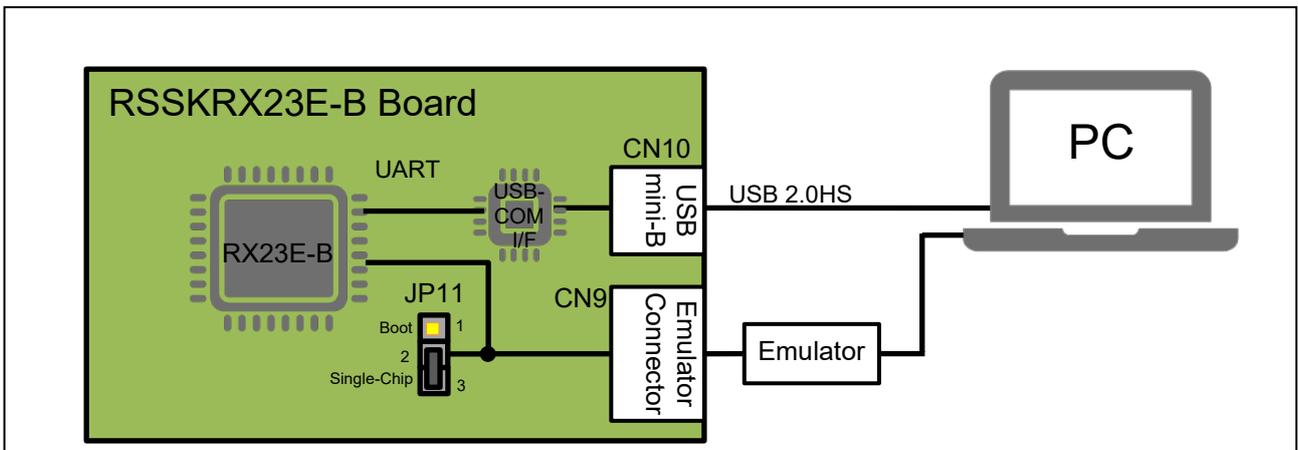
Figure 2.2 Connecting to a PC

Table 2-3 Function Available When a PC Is Connected

Item	Connected to	JP11 connection and function	
		When pins 1-2 are connected	When pins 2-3 are connected
Emulator	CN9	Disabled	Code debugging FW write via the FINE interface
USB serial communication	CN10	FW write via the SCI interface	Communication with a PC

2.4   Using the Analog Input Circuit

Overview of the Analog Input Circuit

The analog input circuit on the board has the following functions.

- DSAD measurement circuit
- Thermocouple measurement circuit
- Reference junction compensation circuit using the on-board RTD
- Four-wire RTD measurement circuit
- Three-wire RTD measurement circuit
- Strain gage measurement circuit

This manual covers the circuit configuration required for implementing each function and the relationship between the DSAD measurement result in two's complement format and input signal. For details on processing for converting the DSAD measurement result to a physical quantity, refer to the application notes related to sensor measurement.

To switch the function, it is necessary to change the jumper pin connection and AFE settings. The jumper pin connection and built-in FW are factory-set for the DSAD measurement circuit using AIN1 and AIN0. Table 2-4 lists each function of the analog input circuit, corresponding jumper pin connection, and AFE settings.

Table 2-4 Functions of the Analog Input Circuit and Corresponding Jumper Settings

Connection / Function	Jumper pin connection						Used pins of the MCU (pin function)		
	JP5	JP6	JP7	JP8	JP9	JP10	Positive side	Negative side	Others
Factory settings	1-2	1-2	1-2	1-2 and 3-4	1-2 and 3-4	1-2	N/A	N/A	N/A
DSAD measurement circuit	X	X	X	X	X	X	AIN1	AIN0	N/A
	X	X	X	X	X	X	AIN3	AIN2	N/A
	X	X	X	X	X	X	AIN7	AIN6	N/A
HV input evaluation circuit	X	X	X	X	X	X	HVAIN3	HVAIN2	N/A
	X	X	X	X	X	X	HVAIN1	HVAIN0	N/A
Thermocouple measurement circuit	X	X	X	X	X	X	AIN11	AIN10 (VBIAS)	N/A
Reference junction compensation circuit	X	X	2-3	1-2 and 3-4	5-6 and 7-8	2-3	AIN5	AIN4	REF0P REF0N AIN9(IEXC1)
Four-wire RTD measurement circuit	X	X	1-2	1-2 and 3-4	1-2 and 3-4	1-2	AIN5	AIN4	REF0P REF0N AIN9(IEXC1)
Three-wire RTD measurement circuit	X	X	1-2	5-6 and 7-8	1-2 and 3-4	1-2	AIN5	AIN4	REF0P REF0N AIN9(IEXC1) AIN8(IEXC0)
Strain gauge measurement circuit	1-2	1-2 or 3-4	X	X	X	X	AIN15	AIN14	AIN13(REF1P) AIN12(REF1N)

X: Don't care   N/A: Not applicable

(Note) Since the thermocouple measurement circuit is independent of the connection of JP5 to JP10, it can be used simultaneously with other functions.

(Note) Since the strain gauge measurement circuit is independent of the connection of JP7 to JP10, it can be used simultaneously with other functions.

Table 2-5 Factory Settings of the DSAD and AFE

Item	Symbol	Setting value		Remarks
		Polarity	DSAD0	
Measurement pin	-	Positive side	AIN1	-
		Negative side	AIN0	
Reference voltage	VREF	Positive side	REFOUT	-
		Negative side	AVSS0	
Gain	GAIN	-	1x	PGA enabled
Data rate	DR	-	976.553SPS	OSR1:256, OSR2:16, SINC4+SINC4

(Note) The bias voltage generator and excitation current source are not used in the factory setting.

2.4.1   DSAD Measurement Circuit

Figure 2.3 shows an example usage of the DSAD measurement circuit on the board.
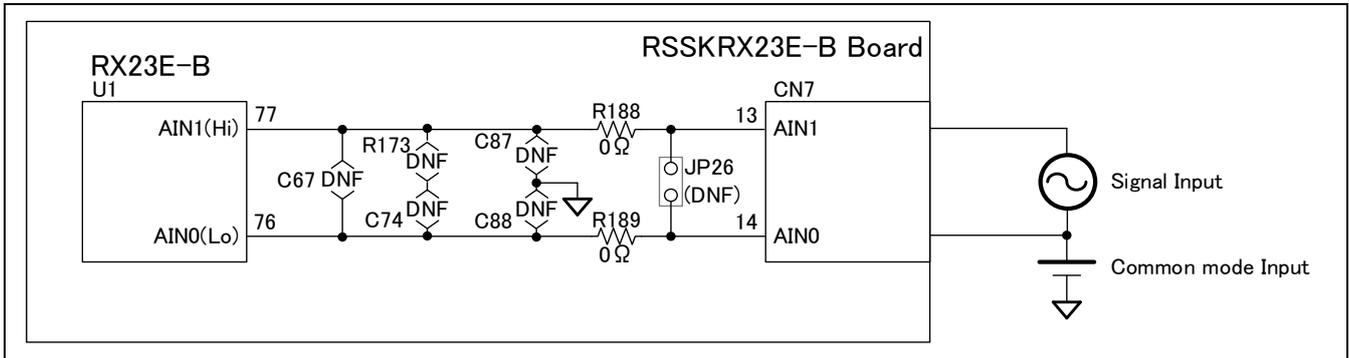
Figure 2.3 Example Usage of DSAD Measurement Circuit

The FW built onto the board at shipment is set to measure the differential voltage between AIN1 and AIN0. When using the measurement circuit, input voltage to pins 13 and 14 of CN7. The differential input voltage V_{ID} can be obtained from the DSAD conversion result in two's complement format AD_{DATA} using the following expression.

$$V_{ID} = \frac{VREF \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} \, [V]$$

Before applying voltage to the analog pins of the RX23E-B, check the following conditions. If either condition is not satisfied, measurement cannot be performed correctly.

(1)   The voltage between each AIN and AVSS0 is within the absolute input voltage range for the analog pins of RX23E-B.
(2)   The voltage between AIN pins is within the differential voltage input range.

The absolute input voltage range and differential voltage input range depend on the analog power supply voltage (AVCC0), the reference voltage (VREF), and the DSAD settings. For details, refer to "RX23E-B Group User's Manual: Hardware".

During evaluation, self-noise of the DSAD and AFE can be measured by short-circuiting input pins. To short-circuit input pins, fix the input pin potential to satisfy condition (1). Without fixing, the input bias current may cause the input pin potential to be outside the absolute input voltage range. Sample methods for fixing the input pin potential are listed below.

(a)   Connect an external stable potential to one measurement pin.
(b)   Connect one measurement pin to GND via a resistor.
(c)   Apply bias voltage to one measurement pin using the AFE bias voltage generator (VBIAS).

When using method (a) or (b) for measurement, check that the input pin potential is within the range of condition (1). The bias voltage generation circuit in (c) can output only AIN2 and AIN10 pins. Depending on connection, the differential input impedance becomes imbalanced, and the circuit may be susceptible to common mode noise.

2.4.2   Thermocouple Measurement Circuit

Figure 2.4 shows the thermocouple measurement circuit on the board.
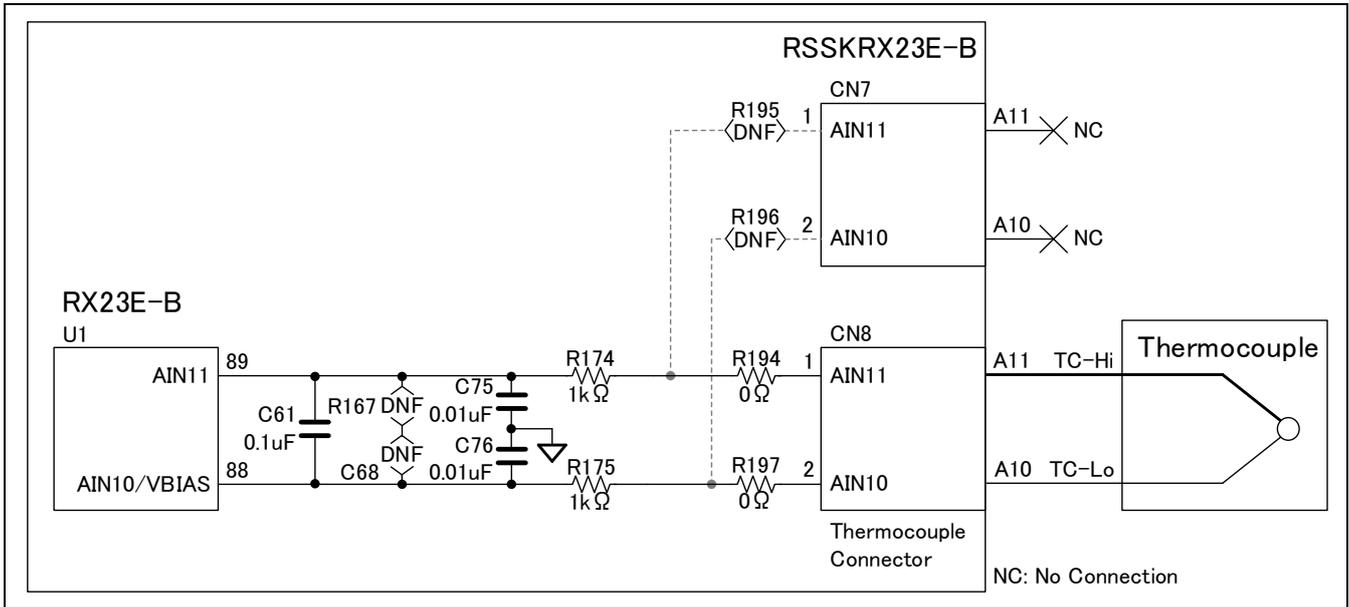
Figure 2.4 Thermocouple Measurement Circuit

CN8 is a miniature connector socket on the board used for the thermocouple input pins (material: copper-copper). Thermocouple attached with the board can be connected to CN8 for measurement.

Connect the positive side of the thermocouple to AIN11 pin of CN8 and the negative side to AIN10 pin. The output from the thermocouple (thermoelectromotive force) is input to AIN11 and AIN10, and the differential voltage is measured with the DSAD. The thermoelectromotive force V_{TEMP} can be obtained from the DSAD conversion result in two's complement format AD_{DATA} using the following expression.

$$V_{TEMP} = \frac{VREF \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [V]$$

For thermocouple measurement, fix the input pin potential. Without fixing, the PGA input bias current may cause the input pin potential to be outside the absolute input voltage range. It is possible to fix the input pin potential by applying VBIAS to AIN10 pin from the MCU.

Measuring a temperature with the thermocouple requires cold junction compensation or reference junction compensation. The board enables reference junction compensation using the on-board RTD. For details on the reference junction compensation circuit using the on-board RTD, see 2.4.4 "Reference Junction Compensation Circuit Using the On-Board RTD".

The pins 1 (AIN11) and 2 (AIN10) of CN7 are not connected to the MCU. When using AIN11 and AIN10 from CN7, remove R194 and R197 and implement R195 and R196.

2.4.3   Reference Junction Compensation Circuit Using the On-Board RTD

Figure 2.5 shows the reference junction compensation circuit on the board.
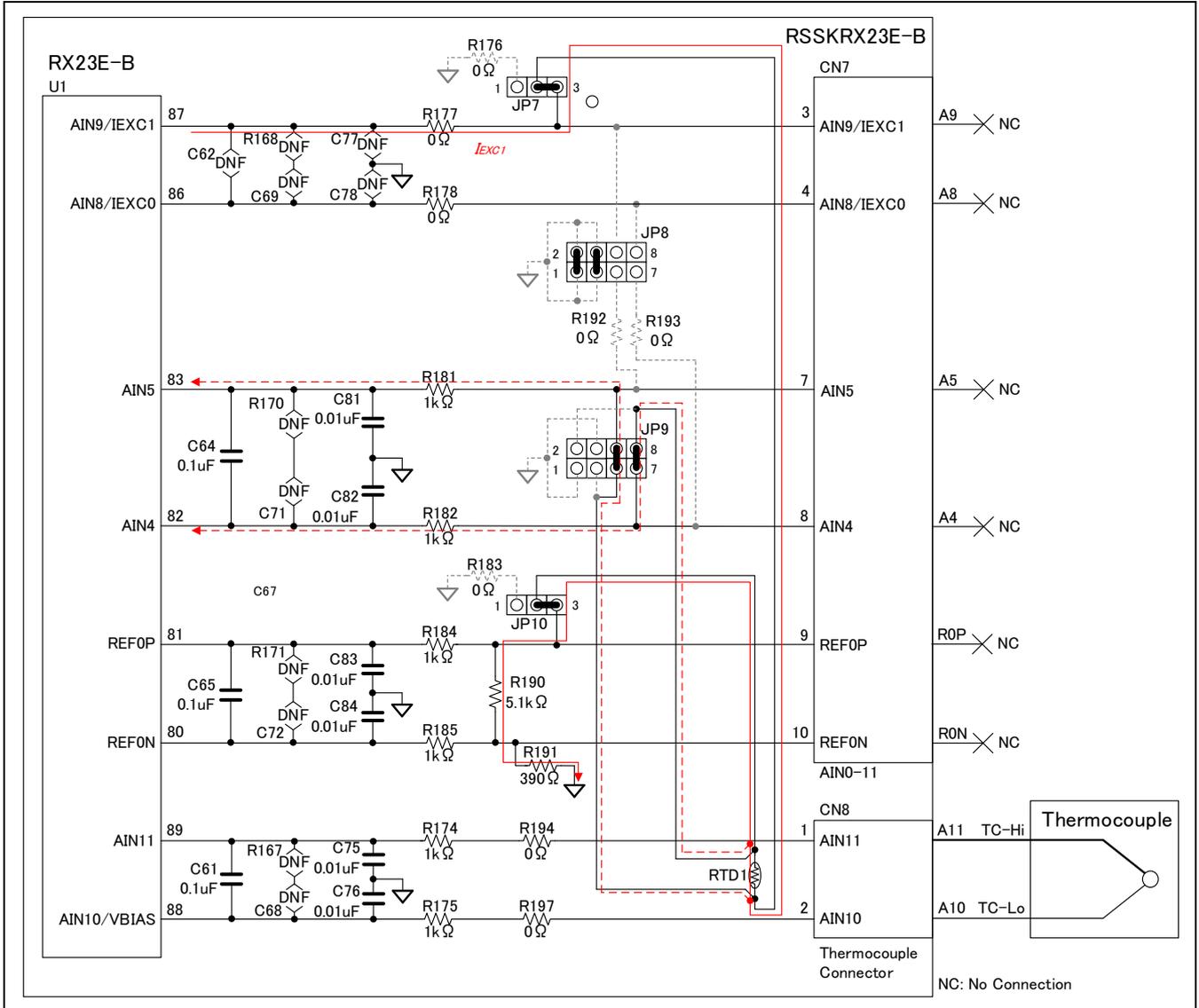
Figure 2.5 Reference Junction Compensation Circuit

On the board, the temperature near CN8 is detected with the on-chip resistance temperature detector, RTD1, for reference junction compensation for thermocouple measurement. For RTD1 measurement, a four-wire ratiometric measurement method is used. The excitation current I_{EXC1} is output from AIN9 and is made to flow in the path shown by the arrow. The voltages at both ends of RTD1 are input to AIN5 and AIN4, and they are measured with the DSAD. The voltages at both ends of the reference resistor R190 are input to REF0P and REF0N and used as DSAD external reference voltages. The RTD1 resistance can be indicated using the DSAD conversion result in two's complement format AD_{DATA} as shown below.

$$I_{EXC1} \times RTD_1 = \frac{I_{EXC1} \times R_{190} \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [V]$$

When I_{EXC1} is deleted from both sides,

$$RTD_1 = \frac{R_{190} \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} \, [\Omega]$$

With the above expression, the RTD1 resistance can be obtained independently of the excitation current I_{EXC1}. Use a built-in reference buffer (RBUF) with AFE for external reference input REF0N and REF0P. The use of the RBUF can reduce the current input to the external reference input pins. Note that the use of the RBUF narrows the absolute input voltage range for external reference. R191 is provided to make the voltages at the external reference input pin within the absolute input voltage range when the RBUF is used.

2.4.4   Four-Wire RTD Measurement Circuit

Figure 2.6 shows the four-wire RTD measurement circuit on the board.
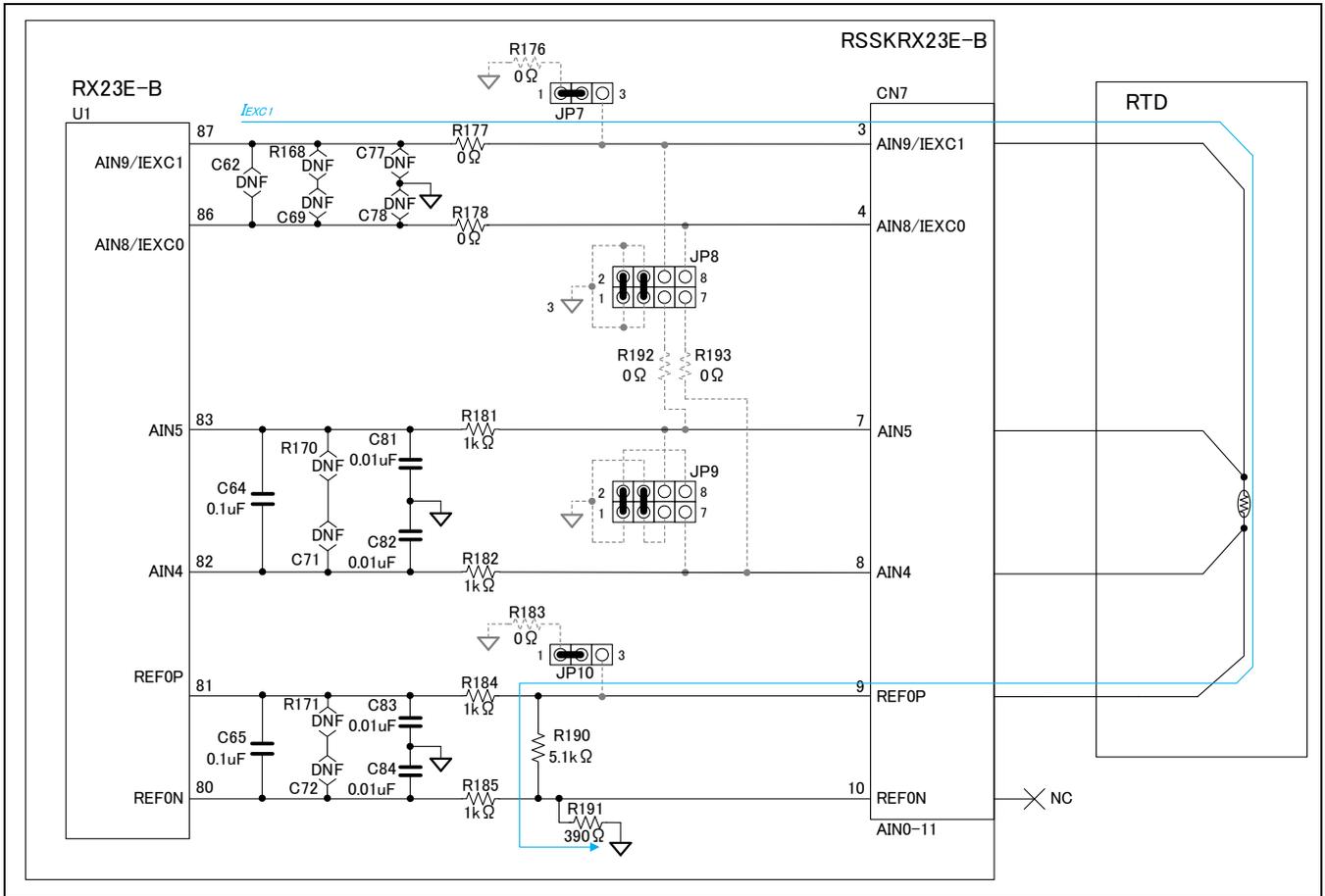
Figure 2.6 Four-Wire RTD Measurement Circuit

A configuration for four-wire RTD measurement is similar to that for on-board RTD measurement. Connect two pins of same polarity of a four-wire RTD to pins 3 (AIN9/IEXC1) and 7 (AIN5) of CN7 and two pins of the other polarity to pins 8 (AIN4) and 9 (REF0P). The excitation current I_{EXC1} is output from AIN9 and is made to flow in the path shown by the arrow. The voltages at both ends of the RTD are input to AIN5 and AIN4 as detection signals, and they are measured with the DSAD. The voltages at both ends of the reference resistor R190 are input to REF0P and REF0N and used as DSAD external reference voltages.

The RTD resistance RTD_{4-wire} can be indicated using the DSAD conversion result in two's complement format AD_{DATA} as shown below.

$$I_{EXC1} \times RTD_{4-wire} = \frac{I_{EXC1} \times R_{190} \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [V]$$

When I_{EXC1} is deleted from both sides,

$$RTD_{4-wire} = \frac{R_{190} \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [\Omega]$$

With the above expression, the RTD resistance RTD_{4-wire} can be obtained independently of the excitation current I_{EXC1}.

In the same way as for on-board RTD measurement, use RBUF for external reference input.

2.4.5   Three-Wire RTD Measurement Circuit

Figure 2.7 shows the three-wire RTD measurement circuit on the board.
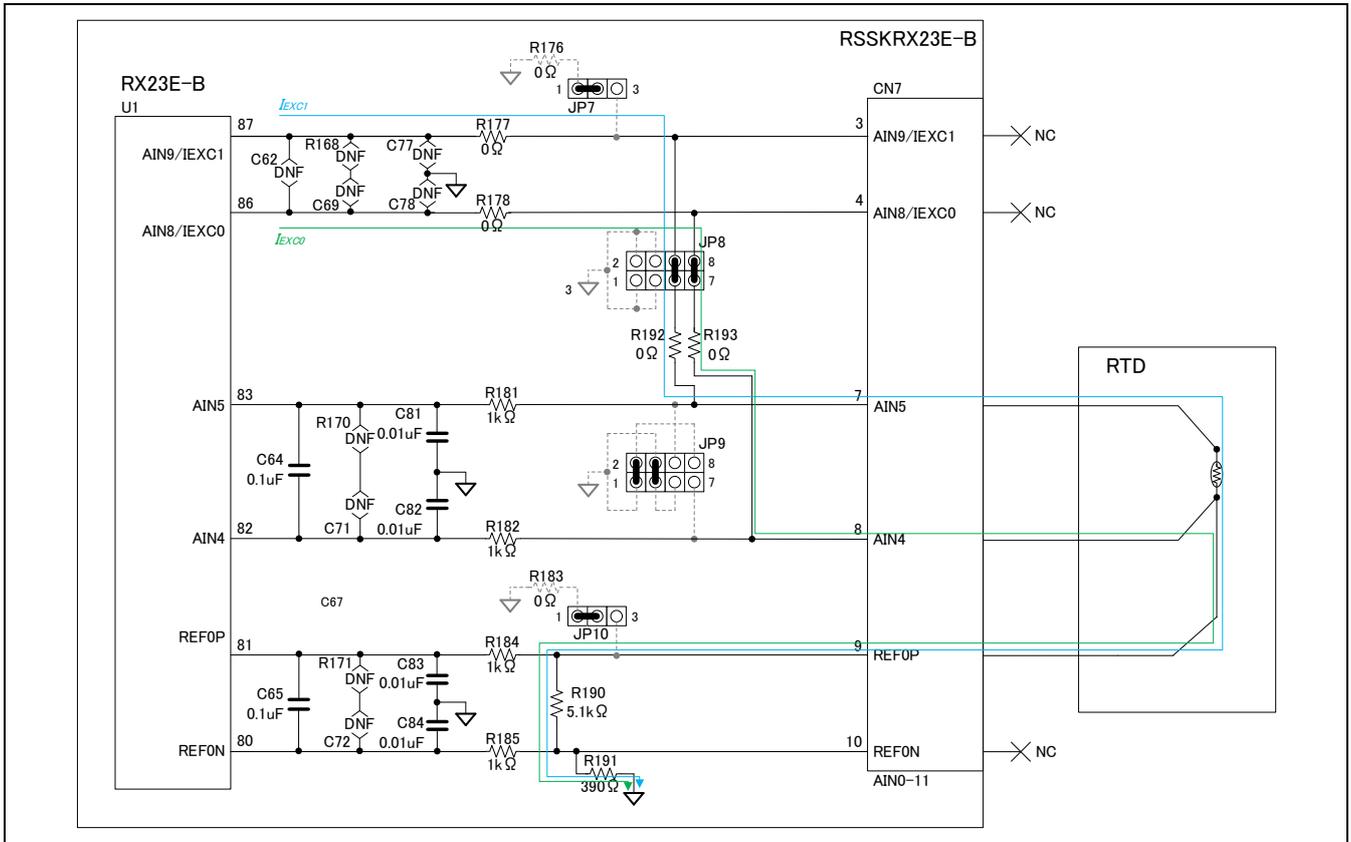
Figure 2.7 Three-Wire RTD Measurement Circuit

Connect one pin at one side of a three-wire RTD to pin 7 (AIN5) of CN7 and two pins of the other polarity to pins 8 (AIN4) and 9 (REF0P) of CN7. The excitation currents I_{EXC1} and I_{EXC0} are output from AIN8 and AIN9 and are made to flow in the path shown by the arrow. The voltages at both ends of the RTD are input to AIN5 and AIN4 as detection signals, and they are measured with the DSAD. The voltages at both ends of the reference resistor R190 are input to REF0P and REF0N and used as DSAD external reference voltages. The RTD resistance RTD_{3-wire} can be indicated using the DSAD conversion result in two's complement format AD_{DATA} as shown below.

$$I_{EXC1} \times RTD_{3-wire} = \frac{(I_{EXC0} + I_{EXC1}) \times R_{190} \times 2}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [V]$$

When $I_{EXC1} = I_{EXC0}$, $I_{EXC0} + I_{EXC1} = 2 \times I_{EXC1}$. When I_{EXC1} is deleted from both sides,

$$RTD_{3-wire} = \frac{R_{187} \times 4}{GAIN} \times \frac{AD_{DATA}}{2^{24}} [\Omega]$$

With the above expression, when the excitation currents I_{EXC0} and I_{EXC1} are equal, the RTD resistance RTD_{3-wire} can be obtained independently of the excitation currents. The excitation current source of the RX23E-B is matched with high precision, and it can be used for three-wire RTD measurement.
In the same way as for on-board RTD and four-wire RTD measurement, use RBUF for external reference input.

2.4.6 Load Cell Measurement Circuit

Figure 2.8 shows the load cell measurement circuit on the board.
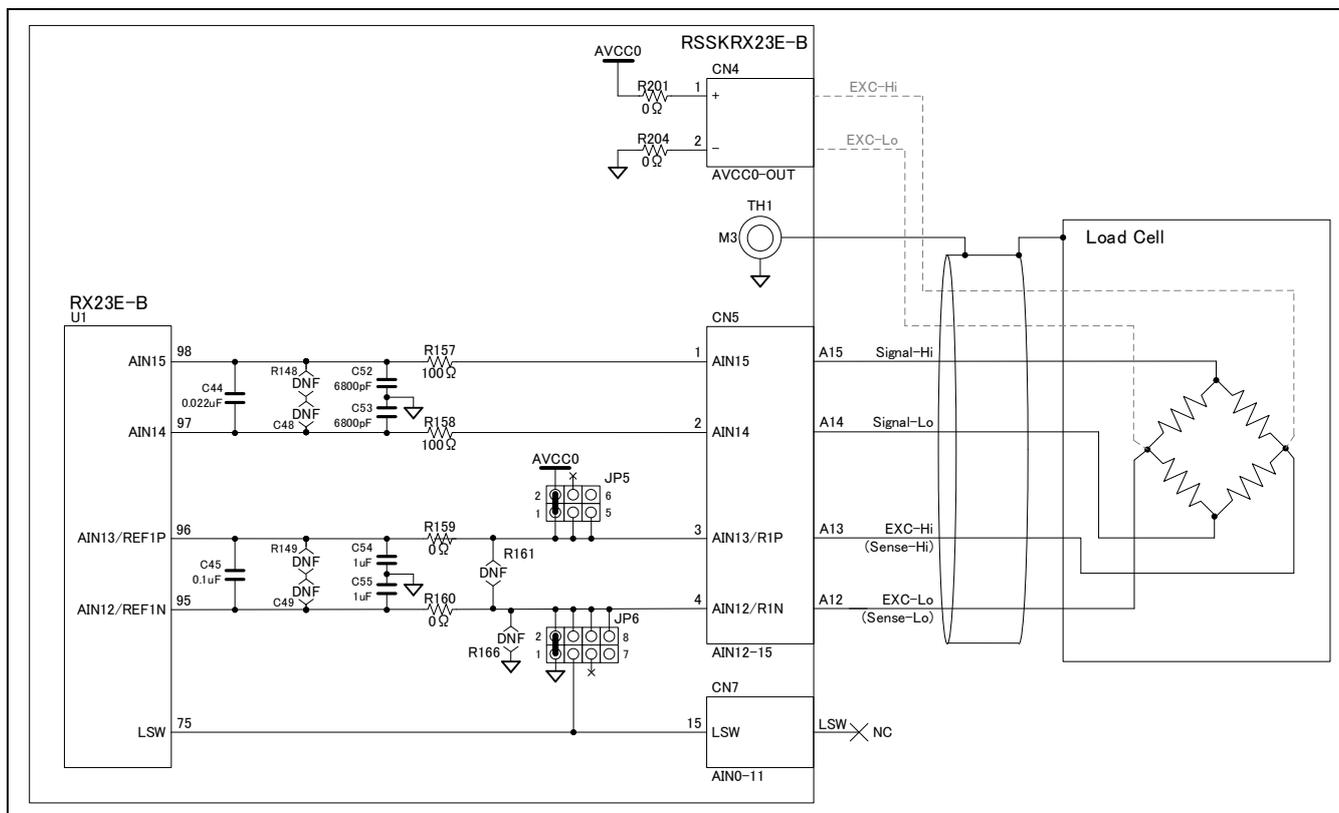
Figure 2.8 Load Cell Measurement Circuit

Connect Signal-Hi of the load cell to pin 1 (AIN15) of CN5, Signal-Lo to pin 2 (AIN14), EXC-Hi to pin 3 (AIN13/REF1P), and EXC-Lo to pin 4 (AIN12/REF1N). The signal voltages of the load cell are input to AIN15 and AIN14, and the differential voltage is measured with the DSAD. Use AVCC0 and AVSS0 as the excitation voltage source and external reference inputs. When the load cell has a shielded wire, it can be connected to TH1 or the negative pin of CN4.

LSW can be used as external reference inputs instead of AVSS0 by switching JP6 connection to short-circuit pins 3 and 4. The LSW pin is connected to AVSS0 via an analog switch in the MCU. This switch can be changed according to the MCU register setting. Power can be supplied to the load cell by turning on the switch, and can be stopped by turning off the switch. Supplying the power to the load cell only during measurement can reduce power consumption. **The allowable current to the LSW pin is 30 mA. When using the LSW pin, consider the allowable current.**

When connecting a load cell, be careful about the maximum output current of the analog power supply. When using LDO (U2) for analog power supply (connecting pins 5 and 6 of JP1), be careful about the maximum output current of the LDO. **The maximum output current of the LDO mounted on the board, ISL80410, is 150 mA. If current exceeding the maximum output current is required, do not use the LDO.**

In this circuit, the relationship between the differential voltage between AIN15 and AIN14 V_{LC} and the weight loaded on the load cell M can be indicated using the rated output of the load cell RO and the rated capacity M_{max} as shown below.

$$V_{LC} = RO \times (AVCC0 - AVSS0) \times \frac{M}{M_{max}} [V]$$

The differential voltage V_{LC} can be indicated using the DSAD conversion result in two's complement format AD_{DATA} with the following expression.

$$V_{LC} = \frac{2 \times (AVCC0 - AVSS0)}{GAIN} \times \frac{AD_{DATA}}{2^{24}}$$

When V_{LC}, AVCC0, and AVSS0 are deleted from the above two expressions, the loaded weight M can be indicated with the following expression.

$$M = \frac{M_{max} \times 2}{RO \cdot GAIN} \times \frac{AD_{DATA}}{2^{24}}$$

2.4.7   Handling Unused Pins in the Analog Input Circuit

If there is an unused pin in the analog input circuit, handle the unused pin according to Table 2-6. If the unused pin is not handled accordingly, the circuit becomes susceptible to external noise and static electricity, which may deteriorate performance and cause a failure.

Table 2-6 Handling Unused Pins in the Analog Input Circuit

Pin name	Device specification	Handling method
AIN0~AIN15	Connected to AVSS0 directly or via a resistor.	Use SO1 to SO4, SO9 to SO16 and SO19 to SO22 to connect to AVSS0.
REF0P	Connected to AVCC0 directly or via a resistor.	Use SO17 to connect to AVCC0.
REF0N	Connected to AVSS0 directly or via a resistor.	Use SO18 to connect to AVSS0
LSW	Connected to AVSS0 directly or via a resistor.	Use SO23 to connect to AVSS0
VREFH	Left open	Connect pins 2-3 of JP4.
VREFL	Connected to AVSS0 directly or via a resistor.	No handling required. Factory default setting is to be connected to AVSS0 via R156 (0Ω).
HVAIN0~HVAIN3	Left open	No handling required.
HVCOM	Left open	Remove R142 (0Ω).
DA0	Left open	No handling required.

3.   Microcontroller Peripheral Circuits

3.1   USB Serial Communication Circuit

Figure 3.1 shows the USB serial communication circuit on this board.
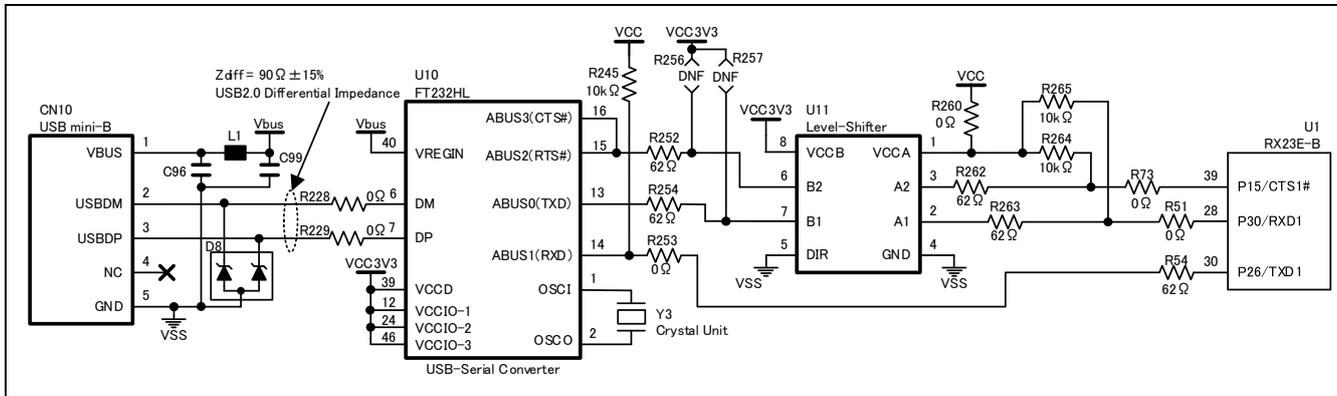
Figure 3.1 USB Serial Communication Circuit

The board has a USB serial communication conversion IC, FT232HL (U10). The FT232HL operating voltage range is 3.6 to 5.5 V, and it operates with power VBUS supplied from USB-miniB connector (CN10).

3.2 Emulator Peripheral Circuit

Figure 3.2 shows the emulator peripheral circuit on the board, and Table 3-1 lists the JP11 connections and corresponding functions.
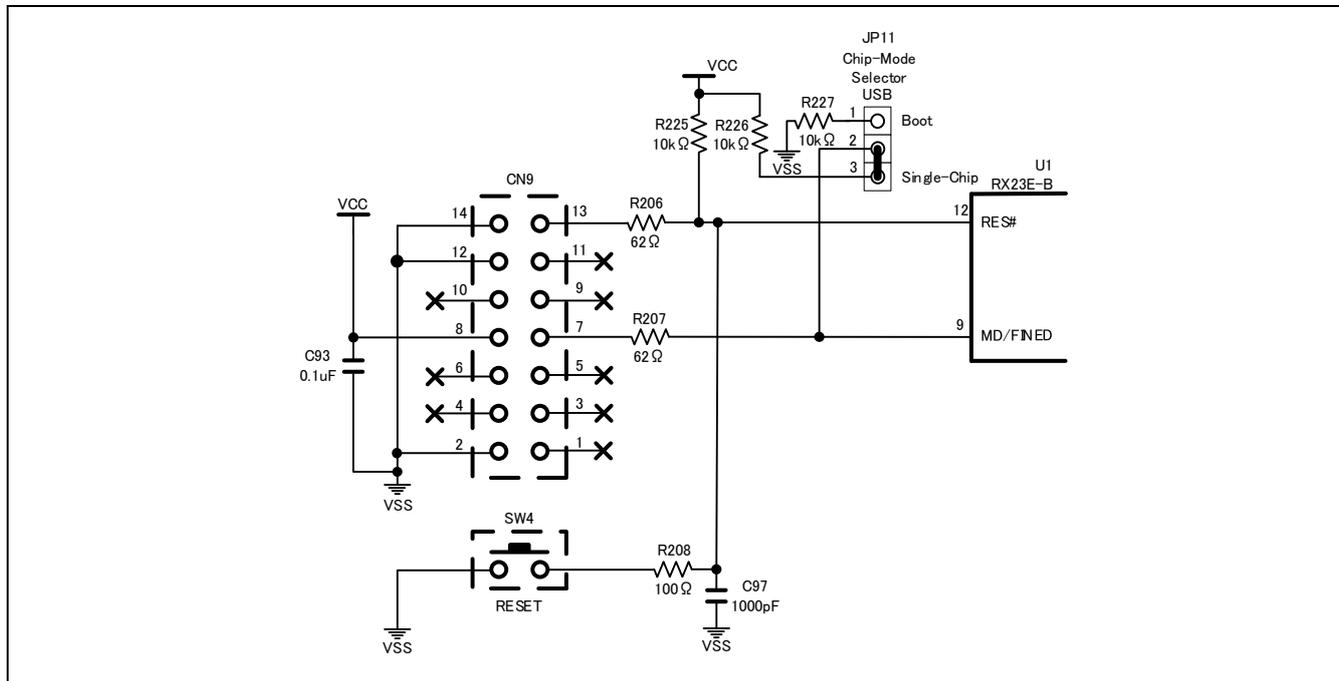
Figure 3.2 Emulator Peripheral Circuit

Table 3-1 JP11 Connections and Corresponding Functions

JP11 connection	Operating mode	Function	Remarks
Pins 1-2	Boot mode (SCI interface)	Writes the FW using the SCI interface.	Allows you to write the FW using USB serial communication (CN10).
Pins 2-3	Single-chip mode	Debugs and writes the FW using the emulator.	Applicable emulator: E2 emulator, E2 emulator Lite

When using the emulator, connect it to CN9. **Before supplying power from the emulator, carefully check that the power does not collide with the input power supply or LDO output.**
By pressing the RESET button (SW4), MCU RES# pin can be reset.
The MCU operating mode can be selected from the boot mode (SCI interface) or single-chip mode by changing the JP11 setting. **During power on, never change the JP11 setting. The MCU may perform unpredictable operation.**

For details on the reset operation, and boot mode operation and functions, refer to "RX23E-B Group User's Manual: Hardware".
For details on how to use the emulator, refer to the user's manual of the emulator.

3.3   RS-485 Communication Circuit

Figure 3.3 shows the RS-485 communication circuit on the board.

The RS-485 communication circuit of this board is equipped with a PROFIBUS DP-compliant, half-duplex communication RS-485 driver RAA788158. 120-Ω termination resistors and 560-Ω fail-safe bias resistors are provided at R230, R231 and R232.

Figure 3.3 RS-485 Communication Circuit

3.4   CAN Communication Circuit

Figure 3.4 shows the CAN communication circuit on the board. The CAN communication circuit on the board has a CAN transceiver. The CAN bus can be connected directly from J2. As a termination resistor, a 120-Ω resistor is connected between CAN-H and CAN-L. When the termination resistor is required, connect pins 1 and 2 of JP12. When it is not required, connect pins 2 and 3 of JP12.

Figure 3.4 CAN Communication Circuit

3.5   LED Circuit

Figure 3.5 shows the LED drive circuit on the board. ON/OFF of LED0 to LED0 can be controlled by ports of MCU (P70 to P73). LED4 is a VCC power indicator.
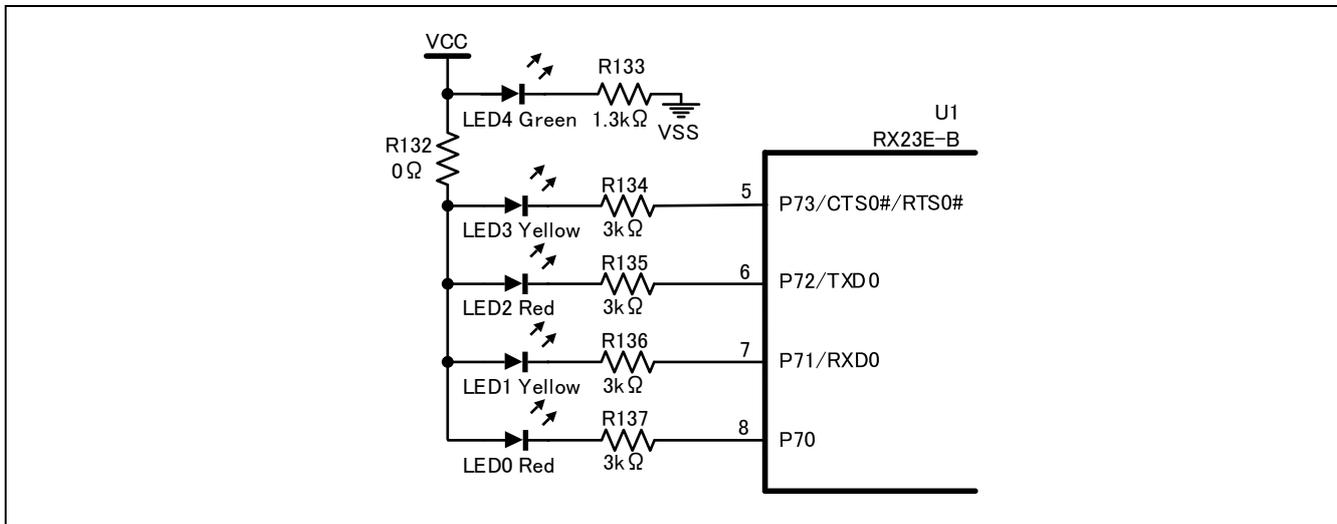
Figure 3.5 LED Drive Circuit

3.6   Switch Input Circuit

Figure 3.6 shows the switch input circuit on the board.

For details on the RESET switch (SW4), see "3.2 Emulator Peripheral Circuit".
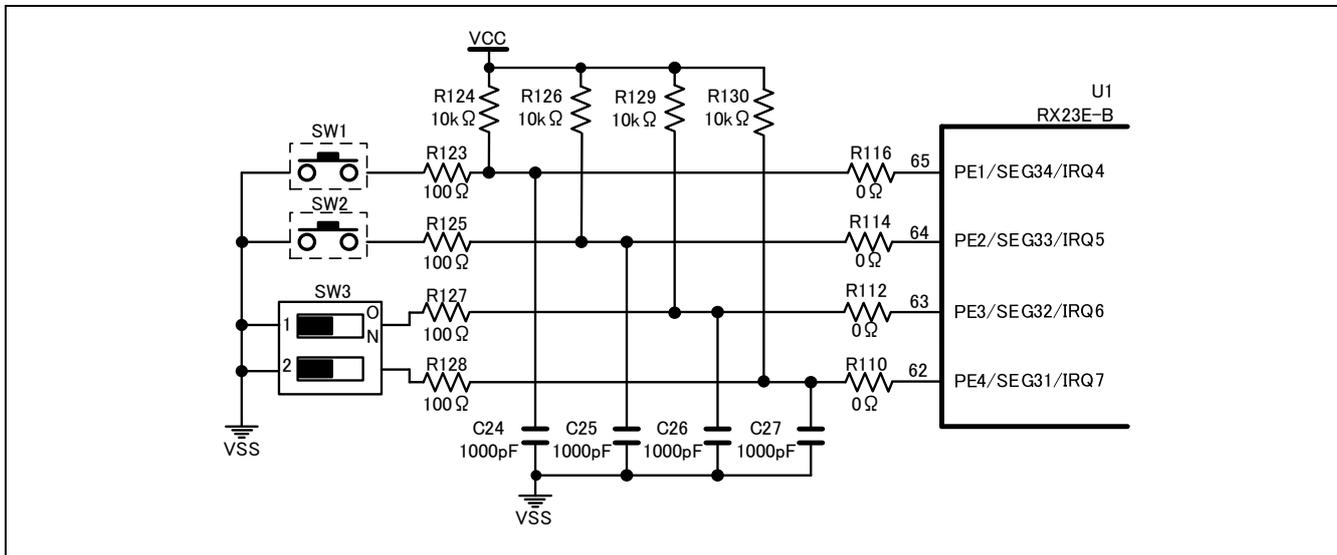
Figure 3.6 Switch Input Circuit

3.7   External Clock Input Circuit

Figure 3.7 shows the external clock input circuit on the board.

The board has an 8-MHz external quartz crystal unit as an external clock input source.
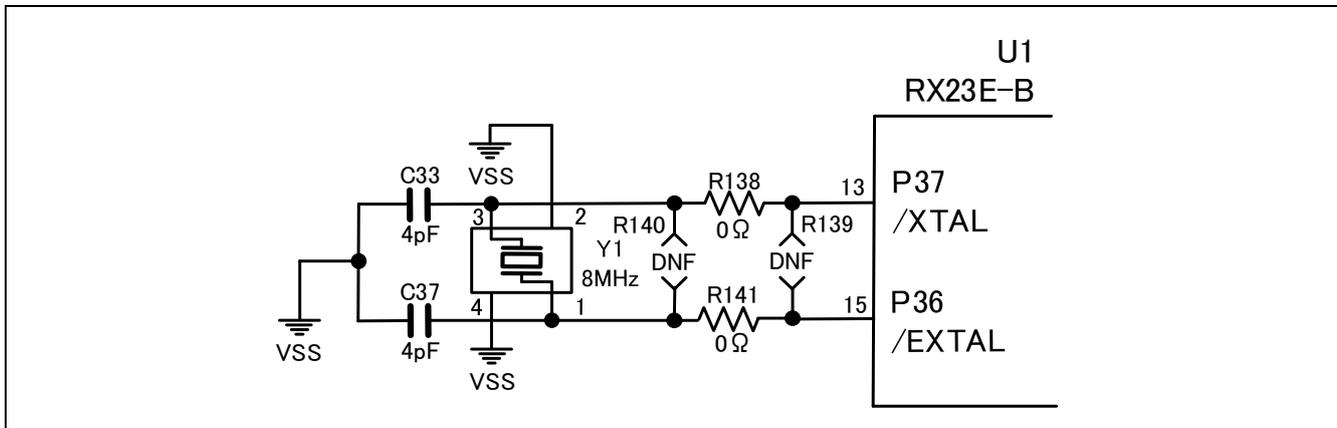
Figure 3.7 External Clock Input Circuit

3.8   Sub Clock Input Circuit

Figure 3.8 shows the sub clock input circuit on the board.

The board has a 32.768 kHz external quartz crystal unit as a sub clock input source.
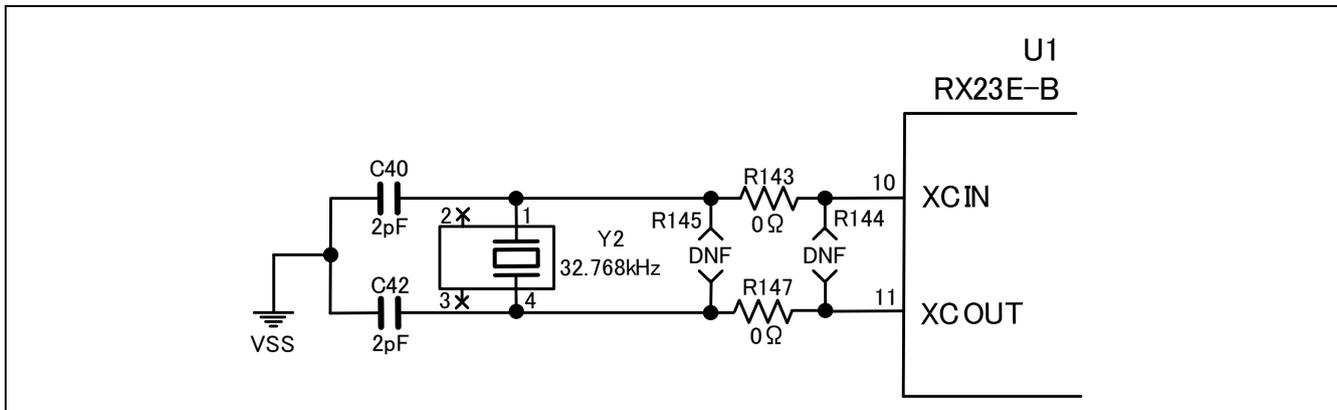
Figure 3.8 Sub Clock Input Circuit

4.   Board Information

4.1   Using Terminal Blocks

Table 4-1 lists the model name used for terminal blocks CN1 to CN7 and the applicable wires.

Table 4-1 Terminal Blocks and Applicable Crimp terminal

Item	Specification
Terminal block model name	ML-700-NH (SATO PARTS CO.,LTD.)
Nominal applicable wire diameter	Single core：Φ0.65mm (AWG22) Stranded wire：0.32mm² (AWG22) Strand wire diameter 0.12mm or more
Applicable wire diameter range	Single core：Φ0.32mm~Φ0.65mm (AWG28~AWG22) Stranded wire：0.08mm²~0.32mm² (AWG28~AWG22) Strand wire diameter 0.12mm or more
Standard stripping line length	9~10mm

If you want to use a ferrule terminal, you can push in the ferrule terminal to connect it to a connector (push-in type). If a ferrule terminal or crimping tool is unavailable, you can connect a stripped wire. To use a stripped wire, follow the procedure below.

i)   Push and hold the white button into the board.

ii)   Insert a stripped wire into the pin insertion hole.

iii)   Release the white button slowly.

iv)   Lightly pull the wire to confirm that it is fixed.

To remove the ferrule terminal or the wire, follow the procedure below.

i)   Push and hold the white button into the board.

ii)   Remove the ferrule terminal or the wire from the pin insertion hole.

iii)   Release the white button slowly.

4.2   Connectors

Table 4-2 to Table 4-19 detail each connector.

Table 4-2 CN1: System Power Input Terminal Block

Silk printing	Function	Direction	Explanation
+	Power supply input (Vd)	Input	System power supply input. Connected to Vd. Vd can be connected to VCC by changing JP1 setting.
−	GND input (VSS)	Input	GND input. Connected to VSS.

Table 4-3 CN2: Analog Power Input Terminal Block

Silk printing	Function	Direction	Explanation
+	Power supply input (Va)	Input	System power supply input pin. Connected to Va. Va can be connected to AVCC0 by changing JP2 setting.
−	GND input (AVSS0)	Input	GND input pin. Connected to AVSS0.

Table 4-4 CN3: D/A Converter I/O Terminal Block

Silk printing	Function	Direction	Explanation
DA0	DA0 output	Output	D/A output pin for an external device. Directly connected to DA0 (pin 1) of the RX23E-B.
AVSS0	GND output (AVSS0)	Output	Analog GND output pin for an external device. Connected to AVSS0.
H	VREFH input	Input	Positive reference input pin of D/A converter. Factory default setting is that pins 1 and 2 of JP4 are connected, so the H pin of CN3 is open. (AVCC0 is applied to the VREFH pin of the MCU.) When using an external input, connect pins 2 and 3 of JP4.
L	VREFL input	Input	Negative reference input pin of D/A converter. Connected to AVSS0 inside the board. Disconnected from CN3 with R155 (not mounted). To use this, mount R155. The VREFL pin of the MCU is connected to AVSS0 via R156.

Table 4-5 CN4: Analog Power Output Terminal Block

Silk printing	Function	Direction	Explanation
+	Power supply output (AVCC0)	Output	Analog power supply output pin for an external device. Connected to AVCC0. Carefully observe the current limitation and heat generation of the power supply and LDO (U2).
−	GND output (AVSS0)	Output	Analog GND output pin for an external device. Connected to AVSS0.

Table 4-6 CN5: Analog Input Terminal Block 1

Silk printing	Connected MCU pin	Direction	Explanation
A15	AIN15	Input	Analog signal input pin
A14	AIN14	Input	Analog signal input pin
A13	AIN13 REF1P	I/O	Analog signal input pin. Can be connected to AVCC0 by changing the JP5 setting. When inputting from an external device, connect pins 3 and 4 of JP5.
A12	AIN12 REF1N	I/O	Analog signal input pin. Can be connected to AVSS0 and LSW by changing the JP6 setting. When inputting from an external device, connect pins 5 and 6 of JP6.

Table 4-7 CN6: ±10V Analog Input Terminal Block

Silk printing	Connected MCU pin	Direction	Explanation
H3	HVAIN3	Input	±10V Analog signal input pin
H2	HVAIN2	Input	±10V Analog signal input pin
H1	HVAIN1	Input	±10V Analog signal input pin
H0	HVAIN0	Input	±10V Analog signal input pin

Table 4-8 CN7: Analog Input Terminal Block 2

Silk printing	Connected MCU pin	Direction	Explanation
A11	AIN11	Input	Analog signal input pin Disconnected from CN7 with R195 (not mounted). To use this, mount R195.
A10	AIN10 VBIAS	I/O	Analog signal input pin. Disconnected from CN7 with R196 (not mounted). To use this, mount R196. Can output bias voltage of (AVCC0 + AVSS0) / 2 using the bias voltage generator (VBIAS) by setting.
A9	AIN9 IEXC1	I/O	Analog signal input pin. Can be connected to RTD1 by changing the JP7 setting. Can be connected to AIN5 by changing the JP8 setting. Can output current using the excitation current source (IEXC) by setting.
A8	AIN8 IEXC0	I/O	Analog signal input pin. Can be connected to AIN4 by changing the JP8 setting. Can output current using the excitation current source (IEXC) by setting.
A7	AIN7	Input	Analog signal input pin
A6	AIN6	Input	Analog signal input pin
A5	AIN5	Input	Analog signal input pin. Can be connected to RTD1 by changing the JP9 setting.
A4	AIN4	Input	Analog signal input pin. Can be connected to RTD1 by changing the JP9 setting.
R0P	REF0P	Input	Positive reference voltage input pin. Can be connected to RTD1 by changing the JP10 setting.
R0N	REF0N	Input	Negative reference voltage input pin. Connected to AVSS0 with R191 (390 Ω).
A3	AIN3	Input	Analog signal input pin.
A2	AIN2 VBIAS	I/O	Analog signal input pin. Can output bias voltage of (AVCC0 + AVSS0) /2 using the bias voltage generator (VBIAS) by setting.
A1	AIN1	Input	Analog signal input pin
A0	AIN0	Input	Analog signal input pin
LSW	LSW	Output	LSW output pin. Connected to AVSS0 via the switch (on-resistance 10-Ω max.) by setting. Be careful not to exceed the allowable current 30 mA max.

Table 4-9 CN8: Thermocouple Connector

Silk printing	Connected MCU pin	Direction	Explanation
A11	AIN11	Input	Analog signal input pin
A10	AIN10 VBIAS	I/O	Analog signal input pin. Can output bias voltage of (AVCC0 + AVSS0) / 2 using the bias voltage generator (VBIAS) by setting.

Table 4-10   CN9: Emulator Connector

Pin No.	Function	Direction	Explanation
1	(Not used)	-	-
2	VSS	Output	GND pin. Connected to VSS.
3	(Not used)	-	-
4	(Not used)	-	-
5	(Not used)	-	-
6	(Not used)	-	-
7	MD/FINED	I/O	MD/FINED pin. JP11 can be used to switch between the single-chip mode (pull-up) and the boot mode (pull-down).
8	VCC	Output	Digital power output pin. Connected to VCC.
9	(Not used)	-	-
10	(Not used)	-	-
11	(Not used)	-	-
12	VSS	Output	GND pin. Connected to VSS.
13	RES#	Input	RES# pin
14	VSS	Output	GND pin. Connected to VSS.

Table 4-11 CN10: USB Connector

Pin No.	Function	Direction	Explanation
1	Vbus	Input	USB power supply pin. Connected to Vbus. Vbus can be connected to VCC by changing the JP1 setting.
2	USBDM	I/O	USB data line D- pin.
3	USBDP	I/O	USB data line D+ pin.
4	NC	-	Unconnected pin.
5	GND	Input	GND pin for an external USB power supply. Connected to VSS.

Table 4-12 J1: Pin Header for RS-485 Communication

Pin No.	Function	Direction	Explanation
1	A/Y	I/O	RS-485 driver non-inverting I/O pin. Connected to the A/Y pin of the driver.
2	B/Z	I/O	RS-485 driver inverting I/O pin. Connected to the B/Z pin of the driver.
3	VSS	Output	GND pin. Connected to VSS.

Table 4-13 J2: Pin Header for CAN Communication

Pin No.	Function	I/O	Explanation
1	CAN_H	I/O	CAN_H pin. Connected to CAN_L via the termination resistor (R205, 120 Ω) by changing the JP12 setting
2	VSS	Output	GND pin. Connected to VSS.
3	CAN_L	I/O	CAN_L pin. Connected to CAN_H via the termination resistor (R205, 120 Ω) by changing the JP12 setting.

Table 4-14 PMOD1: PMOD Type 3A Connector

Pin No.	Function	I/O	Explanation
1	CTS	Output	CTS pin. Connected to P23/CTS9#/RTS9# via R60.
2	TXD	Input	TXD pin. Connected to P25/TXD9 via R56.
3	RXD	Output	RXD pin. Connected to P24/RXD9 via R58.
4	RTS	Input	RTS pin. Connected to P23/CTS9#/RTS9# via R61.
5	VSS	I/O	GND pin. Connected to VSS.
6	Vpmod	I/O	Power output and input pin for PMOD1. Connected to Vpmod. When pins 1 and 2 of JP3 are connected, power can be supplied from the PMOD1 connector by connecting pins 1 and 2 of JP1. Connected to VCC when pins 2 and 3 of JP3 are connected.
7	GPIO4	I/O	GPIO pin. Connected to P22 via R63.
8	GPIO3	I/O	GPIO pin. Connected to P21 via R65.
9	GPIO2	I/O	GPIO pin. Connected to P20 via R67.
10	GPIO1	I/O	GPIO pin. Connected to P14 via R75.
11	VSS	I/O	GND pin. Connected to VSS.
12	Vpmod	I/O	Power output and input pin for PMOD1. Connected to Vpmod.

Table 4-15 PMOD2: PMOD Type 6A Connector

Pin No.	Function	I/O	Explanation
1	NC	-	Unconnected pin.
2	NC	-	Unconnected pin.
3	SCL	I/O	SCL pin. Connected to P16/SCL via R71.
4	SDA	I/O	SDA pin. Connected to P17/SDA via R69.
5	VSS	Output	GND pin. Connected to VSS.
6	VCC	Output	Digital power output pin. Connected to VCC.
7	GPIO4	I/O	GPIO pin. Connected to P13 via R77.
8	GPIO3	I/O	GPIO pin. Connected to P12 via R79.
9	GPIO2	I/O	GPIO pin. Connected to P55 via R81.
10	GPIO1	I/O	GPIO pin. Connected to P54 via R83.
11	VSS	Output	GND pin. Connected to VSS.
12	VCC	Output	Digital power output pin. Connected to VCC.

Table 4-16 JA1: MCU Through-hole 1

Pin No.	MCU Pin No	Function	I/O	Explanation
1	-	VSS	Output	GND pin. Connected to VSS.
2	-	VCC	Output	Digital power output pin. Connected to VCC.
3,4,5	-	NC	-	Unconnected pin.
6	4	P74	I/O	Connected to P74 via R18.
7	5	P73/CTS0#/RTS0#	I/O	Connected to P73 via R19. P73 is connected to LED3.
8	6	P72/TXD0	I/O	Connected to P72 via R20. P72 is connected to LED2.
9	7	P71/RXD0	I/O	Connected to P71 via R21. P71 is connected to LED1.
10	8	P70	I/O	Connected to P70 via R22. P70 is connected to LED0.
11	9	MD/FINED	I/O	Connected to MD/FINED via R23. Pull-up and pull-down can be selected with JP11.
12	10	XCIN	Input	Input/output pins for sub-clock oscillator. Not connected to MCU. When connecting to MCU, mount R24 and R25.
13	11	XCOUT	Output	
14	12	RES#	Input	Reset pin of MCU. Connected to RES# via R26.
15	13	P37/XTAL	I/O	Quartz crystal unit connection pin. Can also be used as a general-purpose IO. Not connected to MCU. When connecting to MCU, mount R27 and R28.
16	15	P36/EXTAL	I/O	
17	18	P67/CAPH/MTIOC4A	I/O	Connected to P67 via R29. C19 is placed between P66 and P67.
18	19	P66/CAPL/MTIOC4C	I/O	Connected to P66 via R30. C19 is placed between P66 and P67.
19	20	P65/VL1/MTIOC4B	I/O	Connected to P65 via R31. C20 is placed between P65 and VSS.
20	21	P64/VL2/MTIOC4D	I/O	Connected to P64 via R32. C21 is placed between P64 and VSS.
21	22	P63/VL3	I/O	Connected to P63 via R33.
22	23	P62/VL4	I/O	Connected to P62 via R34. C23 is placed between P62 and VSS.
23	24	P61/SEG00	I/O	Connected to P61 via R35.
24	25	P60/SEG01	I/O	Connected to P60 via R36.

Table 4-17 JA2: MCU Through-hole 2 (1/2)

Pin No.	MCU Pin No	Function	I/O	Explanation
1	-	VSS	Output	GND pin. Connected to VSS.
2	-	VCC	Output	Digital power output pin. Connected to VCC.
3,4,5	-	NC	-	Unconnected pin.
6	26	P35/NMI	Input	Connected to P35 via R47. Pulled up to VCC by R131.
7	27	P31/SEG02	I/O	Connected to P31 via R48.
8	28	P30/SEG03/RXD1	I/O	Connected to P30 via R50. P30 is connected to A1 pin of U11 via R51.
9	29	P27/SEG04	I/O	Connected to P27 via R52.
10	30	P26/SEG05/TXD1	I/O	Connected to P26 via R53. P26 is connected to RXD pin of U10 via R54.
11	31	P25/SEG06/TXD9	I/O	Connected to P25 via R55. P25 is connected to PMOD1 connector via R56.
12	32	P24/SEG07/RXD9	I/O	Connected to P24 via R57. P24 is connected to PMOD1 connector via R58.
13	33	P23/SEG08/CTS9#/ RTS9#	I/O	Connected to P23 via R59. P23 is connected to PMOD1 connector via R60 and R61.
14	34	P22/SEG09	I/O	Connected to P22 via R62. P22 is connected to PMOD1 connector via R63.
15	35	P21/SEG10	I/O	Connected to P21 via R64. P21 is connected to PMOD1 connector via R65.

Table 4-18 JA2: MCU Through-hole 2 (2/2)

Pin No.	MCU Pin No	Function	I/O	Explanation
16	36	P20/SEG11	I/O	Connected to P20 via R66. P20 is connected to PMOD1 connector via R67.
17	37	P17/SEG12/SDA	I/O	Connected to P17 via R68. P17 is connected to PMOD2 connector via R69.
18	38	P16/SEG13/SCL	I/O	Connected to P16 via R70. P16 is connected to PMOD2 connector via R71.
19	39	P15/SEG14/CTS1#/RTS1#	I/O	Connected to P15 via R72. P15 is connected to A2 pin of U11 via R73.
20	40	P14/SEG15	I/O	Connected to P14 via R74. P14 is connected to PMOD1 connector via R75.
21	41	P13/SEG16	I/O	Connected to P13 via R76. P13 is connected to PMOD2 connector via R77.
22	42	P12/SEG17	I/O	Connected to P12 via R78. P12 is connected to PMOD2 connector via R79.
23	43	P55/SEG18	I/O	Connected to P55 via R80. P55 is connected to PMOD2 connector via R81.
24	44	P54/SEG19	I/O	Connected to P54 via R82. P54 is connected to PMOD2 connector via R83.
25	45	PC7/SEG20	I/O	Connected to PC7 via R84. PC7 can be connected to RE# pin of U5 via R85 (not mounted).
26	46	PC6/SEG21	I/O	Connected to PC6 via R86. PC6 is connected to DE pin of U5 via R87.
27	47	PC5/SEG22/TXD8	I/O	Connected to PC5 via R88. PC5 is connected to DI terminal of U5 via R89.
28	48	PC4/SEG23/RXD8	I/O	Connected to PC4 via R90. PC4 is connected to RO terminal of U5 via R91.
29	49	PC3/SEG24	I/O	Connected to PC3 via R92.
30	50	PC2/SEG25	I/O	Connected to PC2 via R93. PC2 is connected to S terminal of U6 via R94.

Table 4-19 JA3: MCU Through-hole 3

Pin No.	MCU Pin No	Function	I/O	Explanation
1	-	VSS	Output	GND pin. Connected to VSS.
2	-	VCC	Output	Digital power output pin. Connected to VCC.
3,4	-	NC	-	Unconnected pin.
5	51	PC1/COM0/CRXD0	I/O	Connected to PC1 via R98. PC1 is connected to RXD pin of U6 via R99.
6	52	PC0/COM1/CTXD0	I/O	Connected to PC0 via R100. PC0 is connected to pin of U6 via R101.
7	53	PA4/COM2	I/O	Connected to PA4 via R102.
8	54	PA3/COM3	I/O	Connected to PA3 via R103.
9	55	PA2/SEG26	I/O	Connected to PA2 via R104.
10	56	PA1/SEG27	I/O	Connected to PA1 via R105.
11	57	PA0/SEG28	I/O	Connected to PA0 via R106.
12	58	PB1/SEG29	I/O	Connected to PB1 via R107.
13	60	PB0/SEG30	I/O	Connected to PB0 via R108.
14	62	PE4/SEG31/IRQ7	I/O	Connected to PE4 via R109. PE4 is connected to pole 2 of SW3 via R110.
15	63	PE3/SEG32/IRQ6	I/O	Connected to PE3 via R111. PE3 is connected to pole 1 of SW3 via R112.
16	64	PE2/SEG33/IRQ5	I/O	Connected to PE2 via R113. PE2 is connected to SW2 via R114.
17	65	PE1/SEG34/IRQ4	I/O	Connected to PE1 via R115. PE1 is connected to SW1 via R116.
18	66	PE0/SEG35	I/O	Connected to PE0 via R117.
19	67	PD4/SEG36	I/O	Connected to PD4 via R118.
20	68	PD3/SEG37	I/O	Connected to PD3 via R119.
21	69	PD2/SEG38	I/O	Connected to PD2 via R120.
22	70	PD1/SEG39	I/O	Connected to PD1 via R121.
23	71	PD0	I/O	Connected to PD0 via R122.
24	-	NC	-	Unconnected pin.

4.3   Jumper Pins

Table 4-20 to Table 4-28 detail each jumper pin.

Table 4-20 JP4: Jumper Pins for Selecting DACREF-H

JP4 connection	Connection	Explanation
Pins 1-2	AVCC0 -> VREFH	Connects AVCC0 to VREFH.
Pins 2-3	-	Select this setting to input an external reference from CN3.

Table 4-21 JP5: Jumper Pins for Selecting External Reference REF1P

JP5 connection	Connection	Explanation
Pins 1-2	AVCC0 -> REF1P	Connects AVCC0 to REF1P.
Pins 3-4	-	Select this setting to input an external reference to REF1P from CN5.
Pins 5-6	-	Extension for AC excitation measurement of a load cell. See the application note for details.

Table 4-22 JP6: Jumper Pins for Selecting External Reference REF1N

JP6 connection	Connection	Explanation
Pins 1-2	AVSS0 -> REF1N	Connects AVSS0 to REF1N.
Pins 3-4	LSW -> REF1N	Connects LSW to REF1N.
Pins 5-6	-	Select this setting to input an external reference to REF1N from CN5.
Pins 7-8	-	Extension for AC excitation measurement of a load cell. See the application note for details.

Table 4-23 JP7: Jumper Pins for Connecting AIN9/IEXC1 to On-Board RTD

JP7 connection	Connection	Explanation
Pins 1-2	-	Select this setting to use AIN9/IEXC1 from CN7.
Pins 2-3	AIN9/IEXC1 -> RTD1	Connects AIN9/IEXC1 to the on-board RTD (RTD1).

Table 4-24 JP8: Jumper Pins for Selecting Three-Wire RTD Connection

JP8 connection	Connection	Explanation
Pins 1-2 Pins 3-4	-	Select this setting to use AIN9/IEXC1 and AIN8/IECV0 from CN7.
Pins 5-6 Pins 7-8	AIN9/IEXC1 -> AIN5 AIN8/IEXC0 -> AIN4	Connects AIN9/IEXC1 and AIN8/IEXC0 to AIN5 and AIN4 respectively. Can supply excitation current to the 3-wire RTD via AIN5 and AIN4.

Table 4-25 JP9: Jumper Pins for Connecting AIN5/AIN4 to On-Board RTD

JP9 connection	Connection	Explanation
Pins 1-2 Pins 3-4	-	Select this setting to use AIN5 and AIN4 from CN7.
Pins 5-6 Pins 7-8	RTD1 - > AIN5 RTD1 - > AIN4	Connects AIN5 and AIN4 to the on-board RTD (RTD1).

Table 4-26 JP10: Jumper Pins for Connecting REF0P to On-Board RTD

JP10 connection	Connection	Explanation
Pins 1-2	-	Select this setting to use REF0P from CN7.
Pins 2-3	RTD1 - > REF0P	Connects REF0P to the on-board RTD (RTD1).

Table 4-27 JP11: Jumper Pins for Selecting the MCU Operating Mode

JP11 connection	Connection	Explanation
Pins 1-2	MD/FINED pull-down	Sets the MCU operating mode to the boot mode (SCI interface). You can write the FW with USB serial communication (CN10).
Pins 2-3	MD/FINED pull-up	Sets the MCU operating mode to the single-chip mode. Use this setting to operate the FW written in the MCU. You can debug and write the FW using the emulator (CN9).

Table 4-28 JP12: Jumper Pins for Selecting Whether to Use the CAN Bus Termination Resistor

JP12 connection	Connection	Explanation
Pins 1-2	-	Connects the termination resistor (120Ω).
Pins 2-3	-	Disconnects the termination resistor (120Ω).

4.4 Initial Settings of MCU Pins

Table 4-29 Initial Settings of MCU Pins (1/3)

MCU pin No.	MCU pin name in the circuit diagram	Pin function	I/O setting	Connected destination on the board
4	P74	P74	Input Pull-up	JA1
5	P73/CTS0#/RTS0#	P73	Output	JA1, LED3
6	P72/TXD0	P72	Output	JA1, LED2
7	P71/RXD0	P71	Output	JA1, LED1
8	P70	P70	Output	JA1, LED0
9	MD/FINED	MD/FINED	－	JA1, CN9, JP11, (VCC)
10	XCIN	XCIN	－	JA1, Y2
11	XCOUT	XCOUT	－	JA1, Y2
12	RES#	RES#	－	JA1, CN9, SW4, pull-up (VCC)
13	P37/XTAL	XTAL	－	JA1, Y1
15	P36/EXTAL	EXTAL	－	JA1, Y1
18	P67/CAPH/MTIOC4A	P67	Input Pull-up	JA1
19	P66/CAPL/MTIOC4C	P66	Input Pull-up	JA1
20	P65/VL1/MTIOC4B	P65	Input Pull-up	JA1
21	P64/VL2/MTIOC4D	P64	Input Pull-up	JA1
22	P63/VL3	P63	Input Pull-up	JA1
23	P62/VL4	P62	Input Pull-up	JA1
24	P61/SEG00	P61	Input Pull-up	JA1
25	P60/SEG01	P60	Input Pull-up	JA1
26	P35/NMI	NMI	Input	JA2, pull-up (VCC)
27	P31/SEG02	P31	Input Pull-up	JA2
28	P30/SEG03/RXD1	RXD1	－	JA2, U11, pull-up (VCC)
29	P27/SEG04	P27	Input Pull-up	JA2
30	P26/SEG05/TXD1	TXD1	－	JA2, U10, pull-up (VCC)

Table 4-30 Initial Settings of MCU Pins (2/3)

MCU pin No.	MCU pin name in the circuit diagram	Pin function	I/O setting	Connected destination on the board
31	P25/SEG06/TXD9	P25	Input Pull-up	JA2, PMOD1
32	P24/SEG07/RXD9	P24	Input Pull-up	JA2, PMOD1
33	P23/SEG08/CTS9#/RTS9#	P23	Input Pull-up	JA2, PMOD1
34	P22/SEG09	P22	Input Pull-up	JA2, PMOD1
35	P21/SEG10	P21	Input Pull-up	JA2, PMOD1
36	P20/SEG11	P20	Input Pull-up	JA2, PMOD1
37	P17/SEG12/SDA	P17	Input Pull-up	JA2, PMOD2
38	P16/SEG13/SCL	P16	Input Pull-up	JA2, PMOD2
39	P15/SEG14/CTS1#/RTS1#	CTS1#	−	JA2, U11, pull-up (VCC)
40	P14/SEG15	P14	Input Pull-up	JA2, PMOD1
41	P13/SEG16	P13	Input Pull-up	JA2, PMOD2
42	P12/SEG17	P12	Input Pull-up	JA2, PMOD2
43	P55/SEG18	P55	Input Pull-up	JA2, PMOD2
44	P54/SEG19	P54	Input Pull-up	JA2, PMOD2
45	PC7/SEG20	PC7	Input Pull-up	JA2
46	PC6/SEG21	PC6	Input	JA2, U5, pull-down (VSS)
47	PC5/SEG22/TXD8	PC5	Input	JA2, U5, pull-up (VCC)
48	PC4/SEG23/RXD8	PC4	Input	JA2, U5, pull-up (VCC)
49	PC3/SEG24	PC3	Input Pull-up	JA2
50	PC2/SEG25	PC2	Input	JA2, U6, pull-down (VSS)
51	PC1/COM0/CRXD0	PC1	Input	JA3, U6, pull-up (VCC)
52	PC0/COM1/CTXD0	PC0	Input Pull-up	JA3, U6
53	PA4/COM2	PA4	Input Pull-up	JA3
54	PA3/COM3	PA3	Input Pull-up	JA3
55	PA2/SEG26	PA2	Input Pull-up	JA3
56	PA1/SEG27	PA1	Input Pull-up	JA3
57	PA0/SEG28	PA0	Input Pull-up	JA3
58	PB1/SEG29	PB1	Input Pull-up	JA3
60	PB0/SEG30	PB0	Input Pull-up	JA3

Table 4-31 Initial Settings of MCU Pins (3/3)

MCU pin No.	MCU pin name in the circuit diagram	Pin function	I/O setting	Connected destination on the board
62	PE4/SEG31/IRQ7	PE4	Input	SW3, pull-up (VCC)
63	PE3/SEG32/IRQ6	PE3	Input	SW3, pull-up (VCC)
64	PE2/SEG33/IRQ5	PE2	Input	SW2, pull-up (VCC)
65	PE1/SEG34/IRQ4	PE1	Input	SW1, pull-up (VCC)
66	PE0/SEG35	PE0	Input Pull-up	JA3
67	PD4/SEG36	PD4	Input Pull-up	JA3
68	PD3/SEG37	PD3	Input Pull-up	JA3
69	PD2/SEG38	PD2	Input Pull-up	JA3
70	PD1/SEG39	PD1	Input Pull-up	JA3
71	PD0	PD0	Input Pull-up	JA3

Rev.	Date	Description	
		Page	**Summary**
1.00	Nov.10.23	—	First Edition issued
1.10	Apr.12.24	28	Figure 3.4 CAN communication circuit: CAN communication pin header Reference number correction of errors J7 → J2

RSSKRX23E-B