RTKA214290DE0010BU

The RTKA214290DE0010BU evaluation board provides a simple platform to evaluate the 3×3mm 8 Ld DFN and SOIC version of the RAA214290 on the same board.

The RAA214290 is a low-dropout linear voltage regulator that operates from 2.5V to 20V and provides up to 1A of output current with a typical dropout of 540mV. The output voltage is adjustable with external feedback resistors anywhere from 1.224V to 18V.

Features

- Wide input voltage range: 2.5V to 20V
- Adjustable output voltage range: 1.224 to 18V with ±2% accuracy
- Excellent line and load regulation
- Stable with MLCC output capacitor as low as 2.2µF
- Integrated Fault protections including thermal shutdown and short-circuit current limit with foldback
- 3mm×3mm DFN and SOIC can be evaluated on the same board

Specifications

This board is specified for the following operating conditions:

- V_{IN} supply: 2.5V to 20V
- V_{OUT} adjustable by changing the feedback resistor divider.
- Low Dropout of 540mV at 1A
- Short Circuit Current Limit Protection with fold-back at higher input voltages

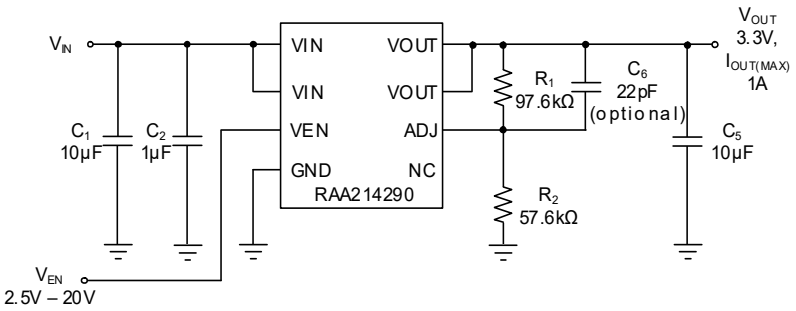

Figure 1. Block Diagram - SOIC

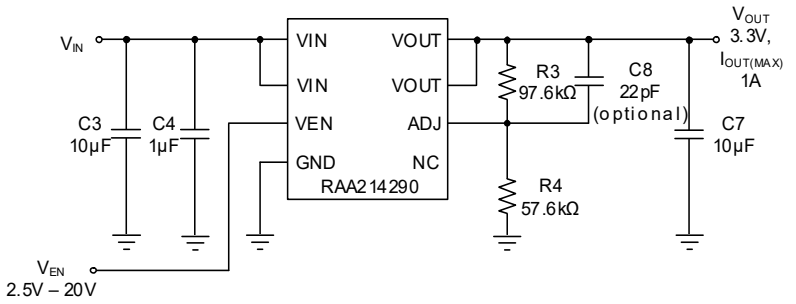

Figure 2. Block Diagram - DFN

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1. Functional Description

The RTKA214290DE0010BU evaluation board provides a simple platform to evaluate the features of the RAA214290 LDO and help characterize important critical performance parameters. The evaluation board is functionally optimized to allow efficient operation up to the maximum output current of 1A.

1.1 Adjusting The Output Voltage

The RAA214290 output voltage (V_{OUT}) can be programmed down to 1.224V and up to 18V using the feedback (FB) resistors, R_1 and R_2 for the SOIC package (Figure 3) or R_3 and R_4 for the DFN package (Figure 4).

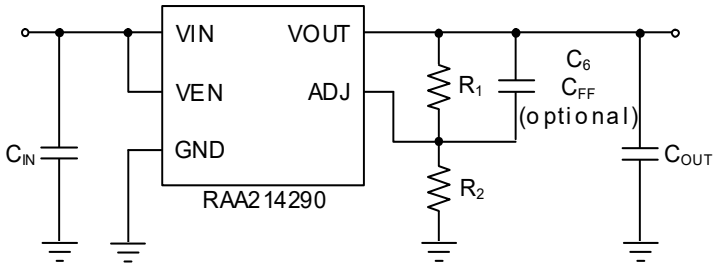

Figure 3. RAA214290 SOIC Simplified Application Schematic

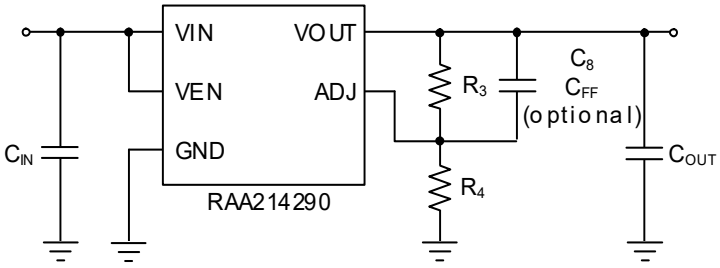

Figure 4. RAA214290 DFN Simplified Application Schematic

To simplify the explanation for how to change the output voltage R_1 and R_2 is referred to as R_F, and R_2 and R_3 is referred to as R_G as shown in Figure 5.

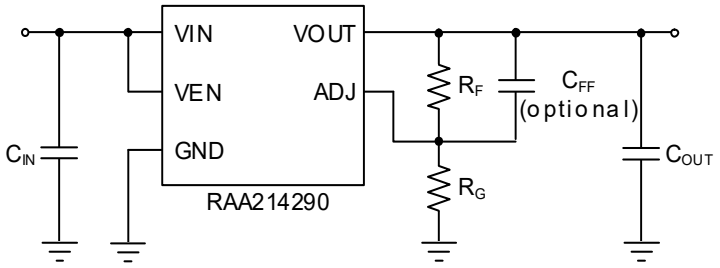

Figure 5. RAA214290 Simplified Application Schematic

V_{OUT} is calculated using Equation 1.

(EQ. 1) $$V_{OUT} = 1.224V \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 1 to get Equation 2 and solving for RF.

(EQ. 2) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{1.224V} - 1\right)$$

Table 1 suggests the FB resistor values to get some common voltage rails with 0.1% error. These resistors are commercially available in 0.1% tolerances. This table is not exhaustive and there may be other R_F and R_G resistor combinations that can provide better accuracy. These resistor values also only require the user to change the R_G resistor instead of both resistors.

Table 1. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	Error (%)
1.224	0	None	0.0
1.5	100	442	-0.1
1.8	100	210	-0.4
1.9	100	180	-0.2
2.5	100	95.3	-0.3
3	100	68.1	-0.7
3.3	100	59	0.0
4.2	100	41.2	0.1
4.5	100	37.4	0.1
5	100	32.4	0.0
9	100	15.8	0.3
12	100	11.3	-0.5
18	100	7.32	0.3

1.2 Using the Feed-Forward Capacitor

A Feed-Forward Capacitor (CFF) in parallel with the R_F resistor as shown in Figure 5 can be used to improve the transient, noise, start-up, and PSRR performance. However, it is not necessary to use one to achieve stability.

Table 2 lists some recommended R_F and R_G resistors and feed-forward capacitor combinations for typical voltage rails. Keep in mind that the R_F and R_G resistor values listed can be used without a feed-forward capacitor as well. When using the feed-forward capacitor it is generally better to keep R_G constant which is why Table 2 shows different R_F and R_G values than Table 1.

Table 2. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	C_{FF} (pF)	Error (%)
1.224	None	0	47	0.0
1.5	13	57.6	43	0.0
1.8	27	57.6	39	0.1
1.9	31.6	57.6	37	0.2
2.5	60.4	57.6	30	-0.3
3	84.5	57.6	25	-0.7
3.3	97.6	57.6	22	0.1

Table 2. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails (Cont.)

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	C_{FF} (pF)	Error (%)
4.2	140	57.6	17	0.0
4.5	154	57.6	16	0.1
5	178	57.6	15	-0.1
9	365	57.6	DNP	0.2
12	511	57.6	DNP	-0.7
18	787	57.6	DNP	0.3

1.3 Enabling and Disabling the Device

The evaluation board has a test point connected to the device EN pin for both the SOIC and DFN package options, which means this pin is floating. Do not let this pin float. Instead, to ENABLE the device, connect the same power supply powering VIN to the EN_U1 or EN_U2 test points depending on the package option. This sets the part to automatically ENABLE when the VIN supply is powered up. To DISABLE the device, connect the EN_U1 or EN_U2 test points to Ground somewhere on the board such as GND_U1_IN1 or GND_U2_IN2.

To control the EN pin independent of VIN, a separate power supply or signal generator can be connected between EN_U1 and GND_U1_IN1 for the DFN package or EN_U2 and GND_U2_IN1 for the SOIC package.

1.4 Quick Start Guide

Complete the following steps if using the 3x3mm 8-Ld DFN package.

1. Connect the input supply to the terminals marked VIN_U1 and GND_U1_IN1.
2. For automatic enabling, connect the same input supply's positive terminal to EN_U1. If powering EN with a separate power supply or signal generator connect the leads to EN_U1 and GND_U1_IN1.
3. Connect the load to the output terminals VOUT_U1 and GND_U1_OUT1
4. After setting the input voltage and load conditions turn on the input supply followed by the load if applicable.
5. Observe the output voltage.

Complete the following steps if using the 8-Ld SOIC package.

1. Connect the input supply to the terminals marked VIN_U2 and GND_U2_IN1.
2. For automatic enabling, connect the same input supply's positive terminal to EN_U2. If powering EN with a separate power supply or signal generator connect the leads to EN_U2 and GND_U2_IN1.
3. Connect the load to the output terminals VOUT_U1 and GND_U1_OUT2
4. After setting the input voltage and load conditions turn on the input supply followed by the load if applicable.
5. Observe the output voltage.

2. Board Design

Figure 6. RTKA214290DE0010BU Evaluation Board

2.1 Layout Guidelines

A proper PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance, and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The feedback resistors should be placed as close to the IC as possible. If using a feed-forward capacitor make sure it is also close to the RF resistor. The trace for FB must be away from noisy planes and traces.

2.2 Schematic Diagrams

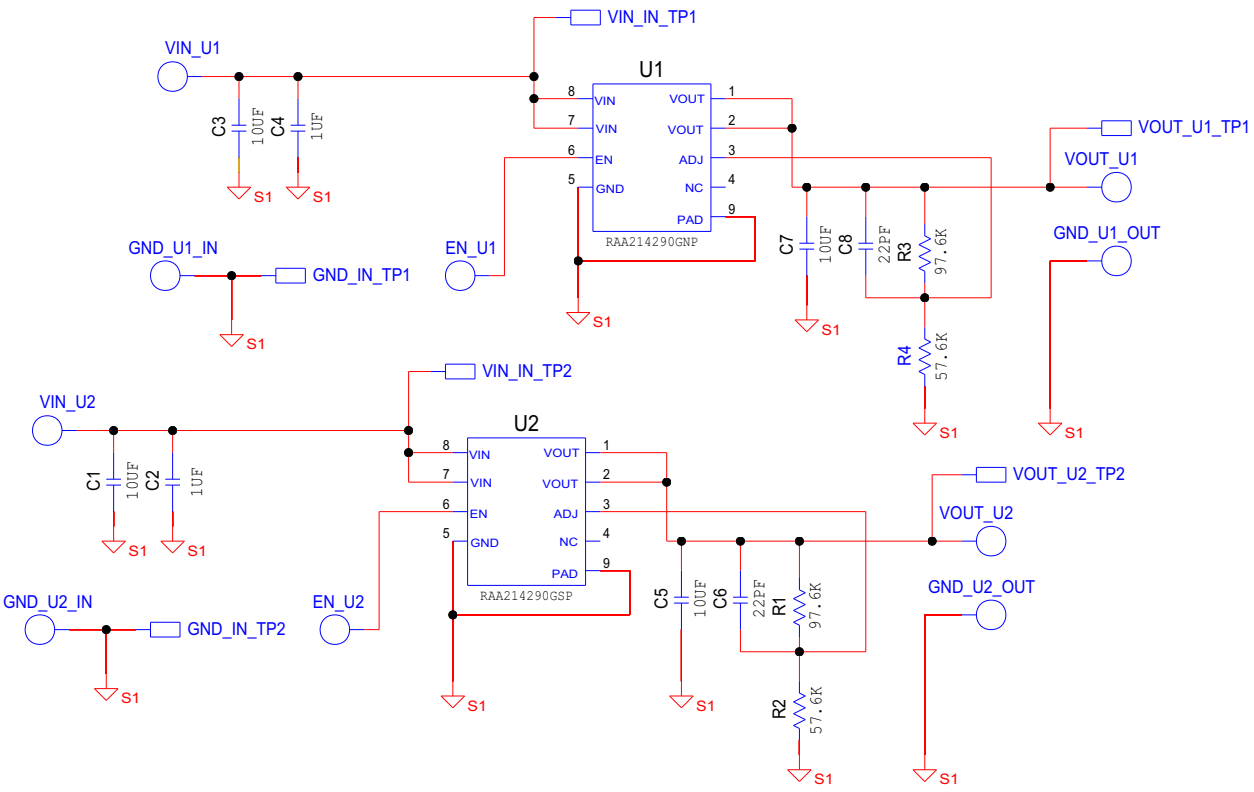

Figure 7. RTKA214290DE0010BU Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	-	PWB-PCB, RTKA214290DE0010BU, REVA, ROHS	Imagineering Inc	RTKA214290DE0010BUREVAPCB
2	C6, C8	CAP, SMD, 0603, 22pF, 50V, 10%, X7R, ROHS	Various	Generic
2	C2, C4	CAP, SMD, 0805, 1.0µF, 50V, 10%, X7R, ROHS	Murata	GRM21BR71H105KA12L
2	C1, C3	CAP, SMD, 1210, 10µF, 50V, 10%, X5R, ROHS	Murata	GRM32ER71H106KA12L
2	C5, C7	CAP, SMD, 1210, 10µF, 50V, 10%, X5R, ROHS	Murata	GRM32ER71H106KA12L
10	EN_U1, EN_U2, VIN_U1, VIN_U2, VOUT_U1, VOUT_U2, GND_U1_IN, GND_U2_IN, GND_U1_OUT, GND_U2_OUT	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
2	VOUT_U1_TP1, VOUT_U2_TP2	CONN-MINI TEST PT, VERTICAL, RED, ROHS	Keystone	5000
2	GND_IN_TP1, GND_IN_TP2	CONN-MINI TEST PT, VERTICAL, BLK, ROHS	Keystone	5001
2	VIN_IN_TP1, VIN_IN_TP2	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
1	U1	IC-20V, 1A LDO REGULATOR, 8P, DFN, ROHS	Renesas Electronics	RAA214290GNP#AA0
1	U2	IC-20V, 1A LDO REGULATOR, 8P, SOIC, ROHS	Renesas Electronics	RAA214290GSP#HA0
2	R1, R3	RES, SMD, 0603, 97.6k, 1/10W, 1%, TF, ROHS	Various	Generic
2	R2, R4	RES, SMD, 0603, 57.6k, 1/10W, 1%, TF, ROHS	Various	Generic
4	Bottom four corners	BUMPONS,0.44inWx0.20inH, CYLINDRICAL DOME, BLK, ROHS	3M	SJ-5003 (BLACK)

2.4 Board Layout

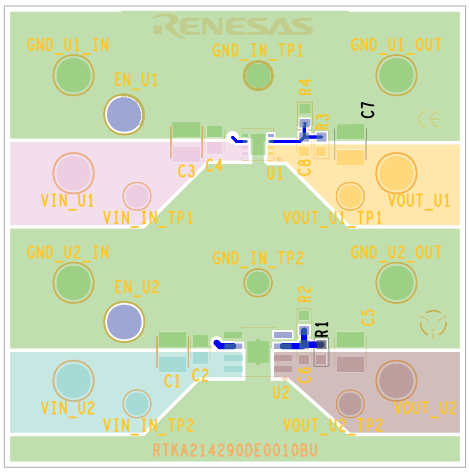

Figure 8. Top Layer

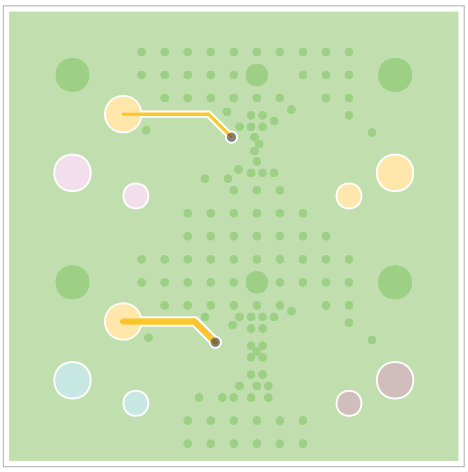

Figure 9. Bottom Layer

3. Typical Performance Graphs

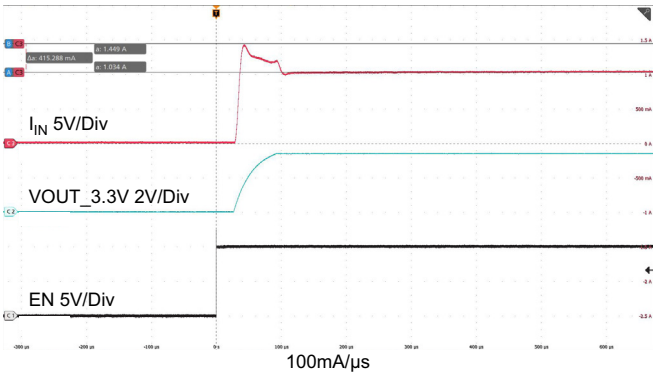

Figure 10. Start-up and In-Rush Current for 25°C (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, CFF = 22pF, I_{OUT} = 1A)

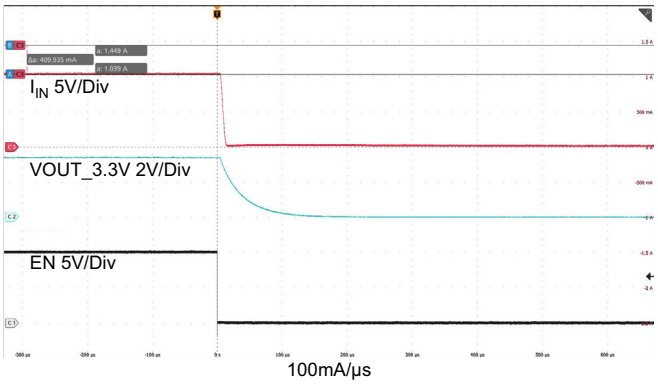

Figure 11. Shut-down for 25°C (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, CFF = 22pF, I_{OUT} = 1A)

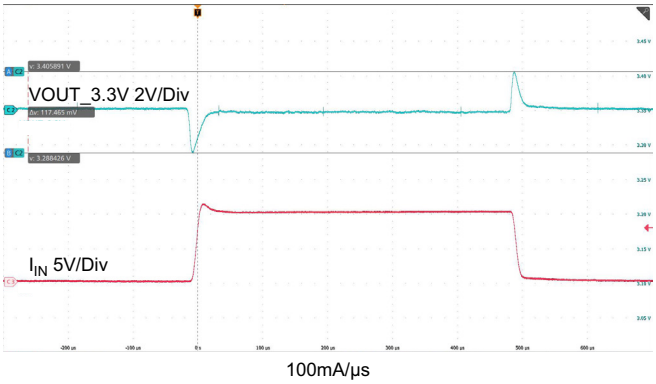

Figure 12. Load Transient Response for 25°C (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, CFF = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µS)

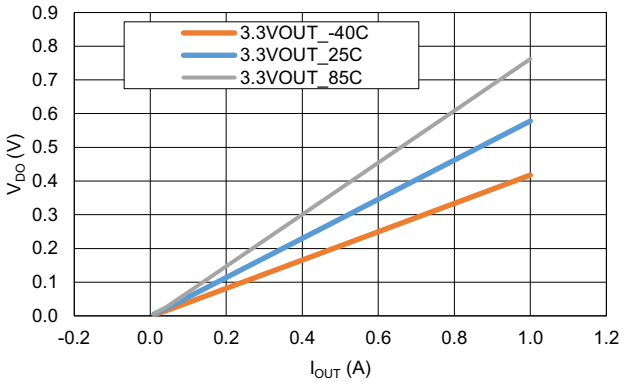

Figure 13. Dropout Voltage vs Output Current for Various Junction Temperature (V_{OUT} = 3.3V)

4. Ordering Information

Part Number	Description
RTKA214290DE0010BU	RAA214290 DFN and SOIC package evaluation board

5. Revision History

Revision	Date	Description
1.00	Nov 2, 2023	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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