RTKA489300DE0000BU

High-Efficiency 3-Level Voltage Regulator Evaluation Board

Description

The RAA489300 is a 3-level buck voltage regulator that provides voltage regulation and protection, offering a wide range of adjustable output voltages. It delivers higher efficiency and significantly reduces inductor size compared to 2-level designs at the same power level. Additionally, the advanced Renesas R3™ technology ensures fast transient response and smooth transitions between DCM and CCM modes.

The RTKA489300DE0000BU safely converts input power from a wide DC range of up to 57.6V (for example, from an AC/DC adapter or USB EPR PD port) to a regulated voltage, covering both USB SPR PPS and USB EPR AVS with a maximum output of 48V.

The RTKA489300DE0000BU includes various system operation functions such as the Forward PTM, Low Power PTM, Reverse PTM, and adjustable output voltage. It also has programmable switching frequency, and a power-good indicator. The protection functionalities include OCP, OVP, UVP, and OTP.

The RTKA489300DE0000BU has serial communication through SMBus/I^{2}C that allows programming of many critical parameters to deliver a customized solution. These programming parameters include but are not limited to output current limit, input current limit, and output voltage setting.

Features

- Single inductor 3-level buck
- Proprietary modulator for flying capacitor balancing and smooth mode transition
- EXT5V pin to generate 5V or 10V gate drive voltage through internal charge pump
- Pass through mode (PTM) in both directions
- Support pre-biased output with soft-start
- Input and output current monitor
- MOSFET drivers with adaptive shoot-through protection
- Complete protection: OCP, OVP, UVP, and OTP
- SMBus and I^{2}C compatible

Specifications

- Wide input voltage range: 4.5V to 57.6V
- Wide output voltage range: 3V to 48V
- Programmable switching frequency: up to 400kHz

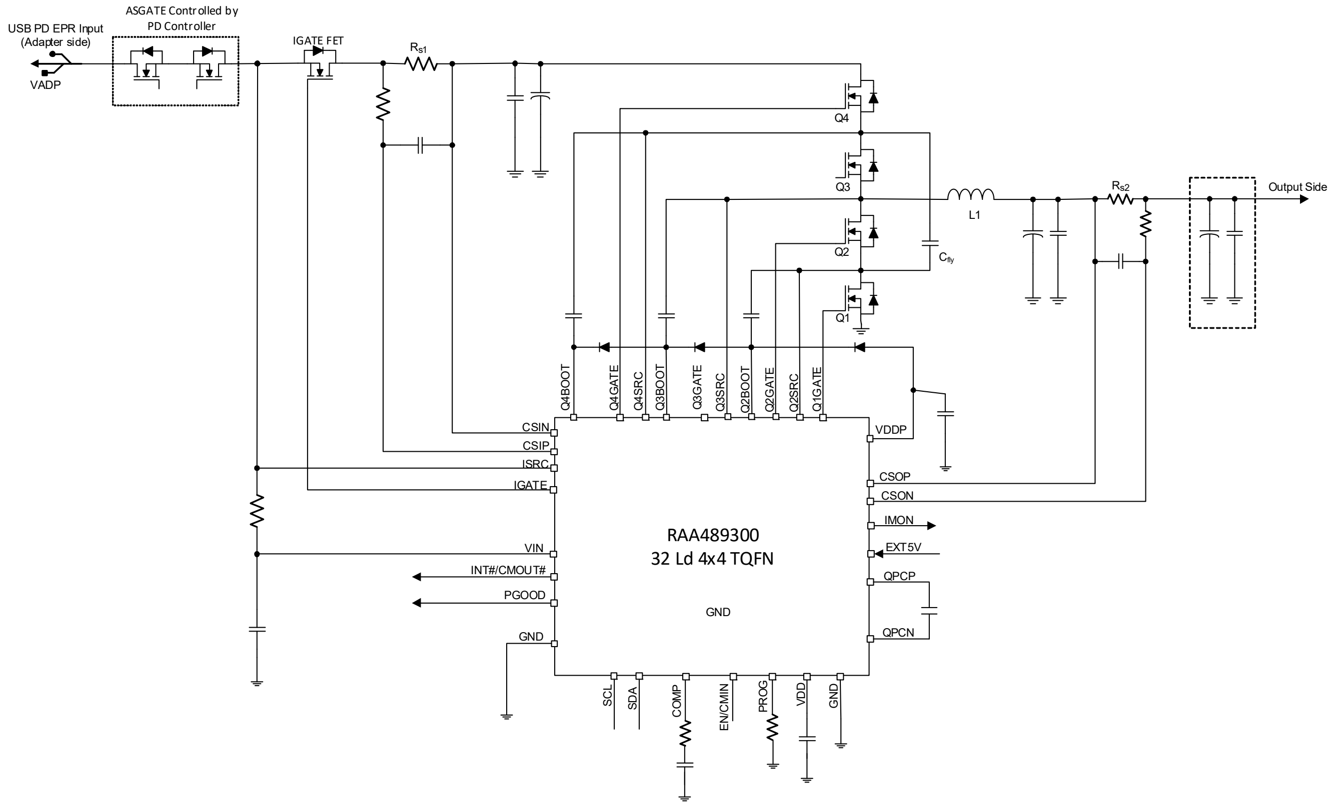


Figure 1. Typical 3-Level Application Circuit – with Isolation FET at Input

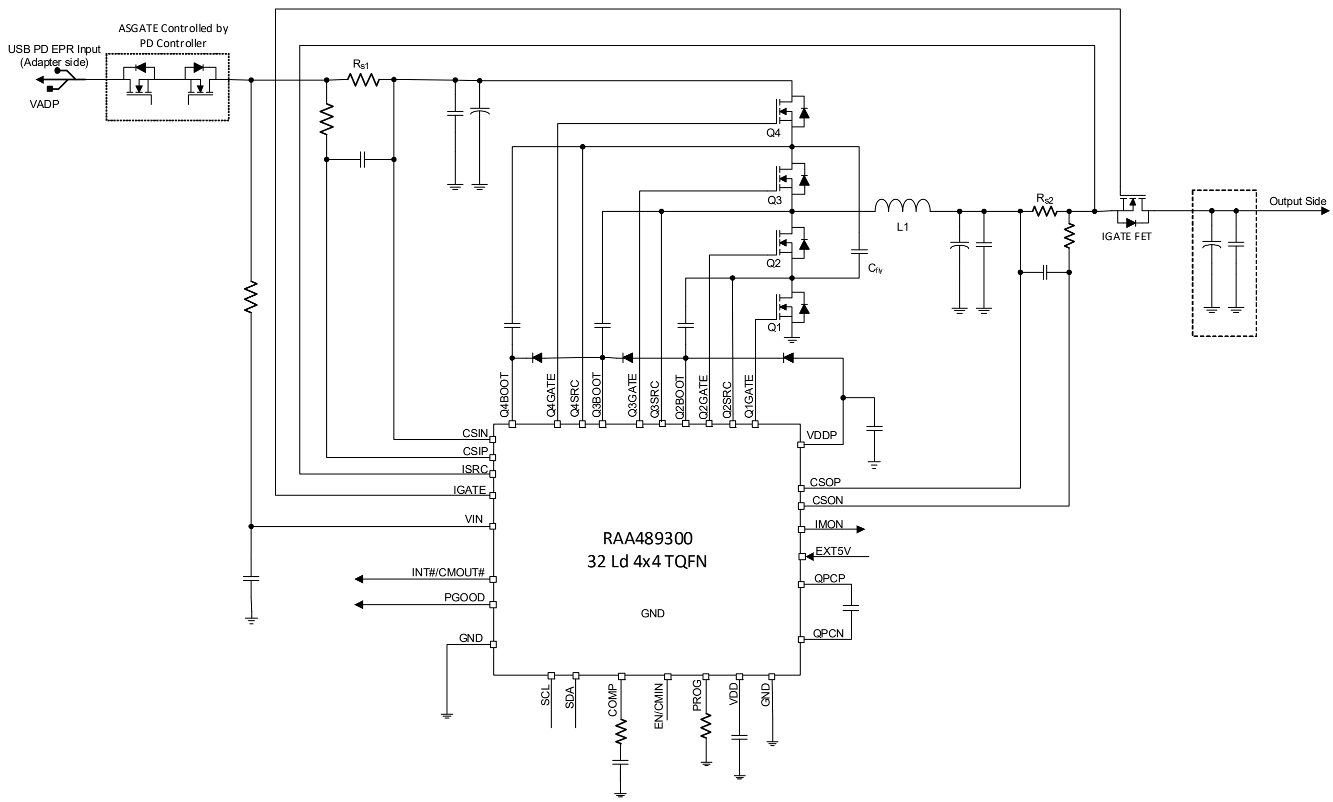


Figure 2. Typical 3-Level Application Circuit – without Isolation FET at Output

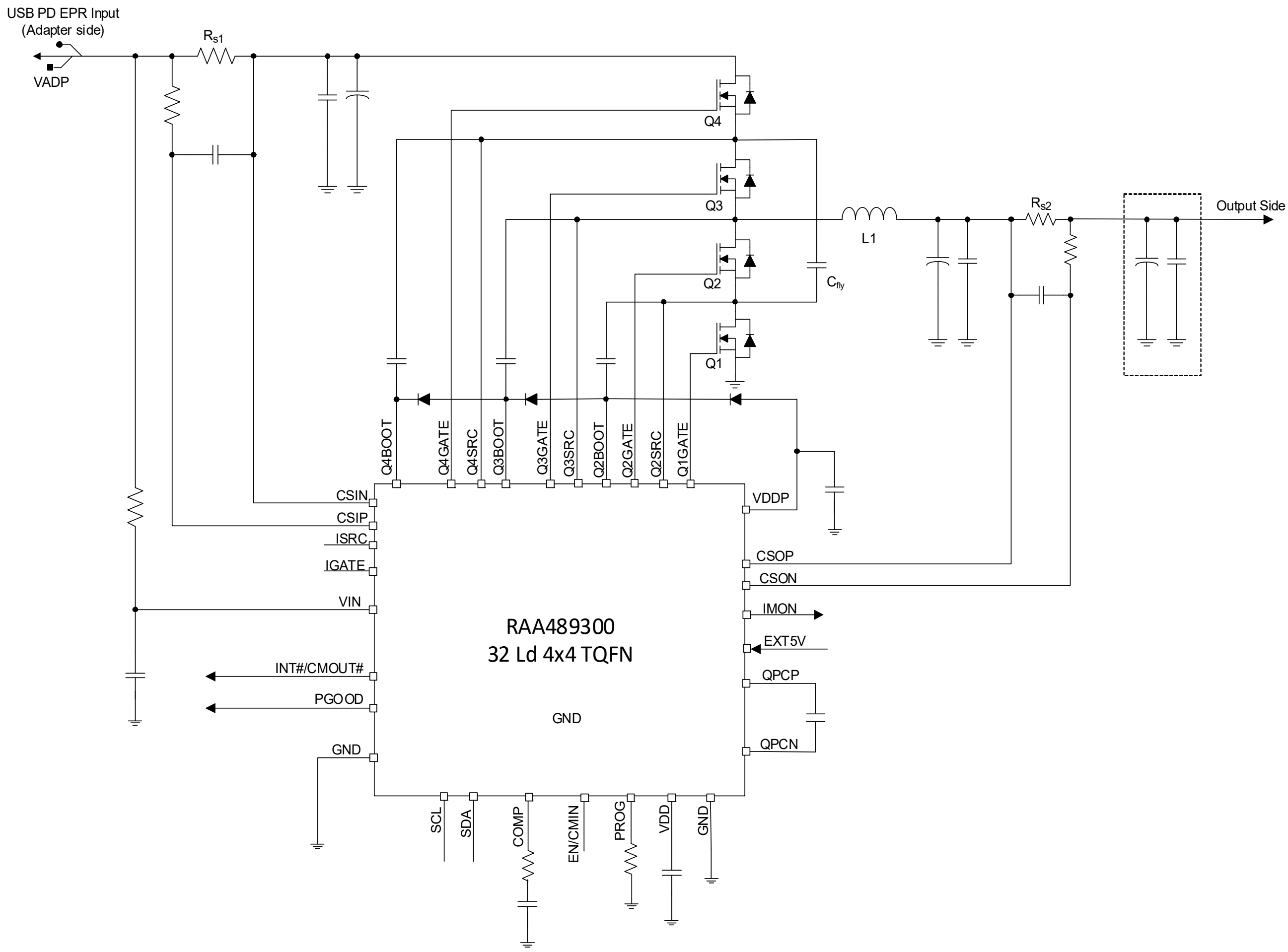


Figure 3. Typical 3-Level Application Circuit – without Isolation FET

Contents

1. Software Installation Guide

The RAA489300 HID I2C Control Tool communicates with the RAA489300 controller through the HID USB-I2C interface board (ISLUSBADAPT-EVZ). The graphical user interface (GUI) facilitates access to the RAA489300 registers.

The following section describes how to install, start, and use the GUI software.

1.1 Required Hardware

- RTKA489300DE00000BU RAA489300 Evaluation Board
- HID USB-I2C interface board (ISLUSBADAPT-EVZ)
- USB 2.0 A/B cable

1.2 Required Software

The software Installation Wizard package includes the following two components:

- RAA489300 HID I2C Control Tool
- National Instruments Runtime VISA Engine

1.3 GUI Installation

Both the RAA489300 Control Software and the National Instruments Runtime Engine are installed automatically from the installation wizard.

Note: Renesas recommends closing all other applications before this installation and to reboot the computer when the installation is completed.

1. Extract the zip file to the local drive and not the network drive. Network security can prohibit the .inf file from being copied to the network.
2. Run **AutoRun.exe**. An installation menu appears (see Figure 4).

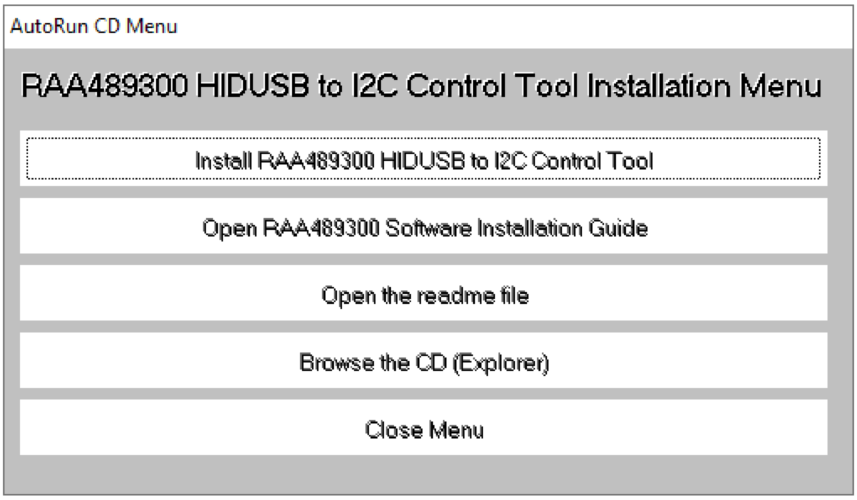


Figure 4. Installation Menu

3. Click **Install RAA489300 USBHID Control Tool** and the **Destination Directory** dialog box appears (see Figure 5).

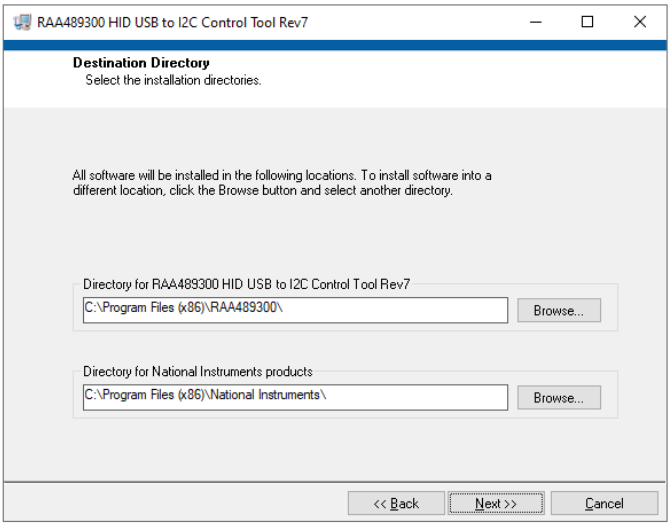


Figure 5. Destination Directory

4. Click **Next** to continue with the selected directory.
5. To complete the software installation, follow the instructions to accept two End User License Agreements.
6. Click **Close Menu** from the installation wizard after the installation is complete.

2. Using the GUI

To use the evaluation system, the RAA489300 USBHID to I2C Control Tool Software must first be installed.

- Do not connect the evaluation board to the USB port until installation is completed.
- The RAA489300 evaluation board must be set up before using the graphical user interface (GUI).

2.1 Setting a USB Connection with the Hardware

This section describes how to setup RAA489300 EVB with USBHID I2C Interface board to communicate with GUI.

1. Connect USB-HID I2C interface board to USB port on the computer using USB A/B cable.
2. Connect SCL, SDA, GND of interface board to the evaluation board, respectively.
3. Provide 5V to 5V_EXT on the EVB.

2.2 Getting Started

1. Select **Microsoft Start** > **All Programs** > **Renesas** > **RAA489300 USBHID-I2C Control Tool**. The GUI appears (see Figure 6).

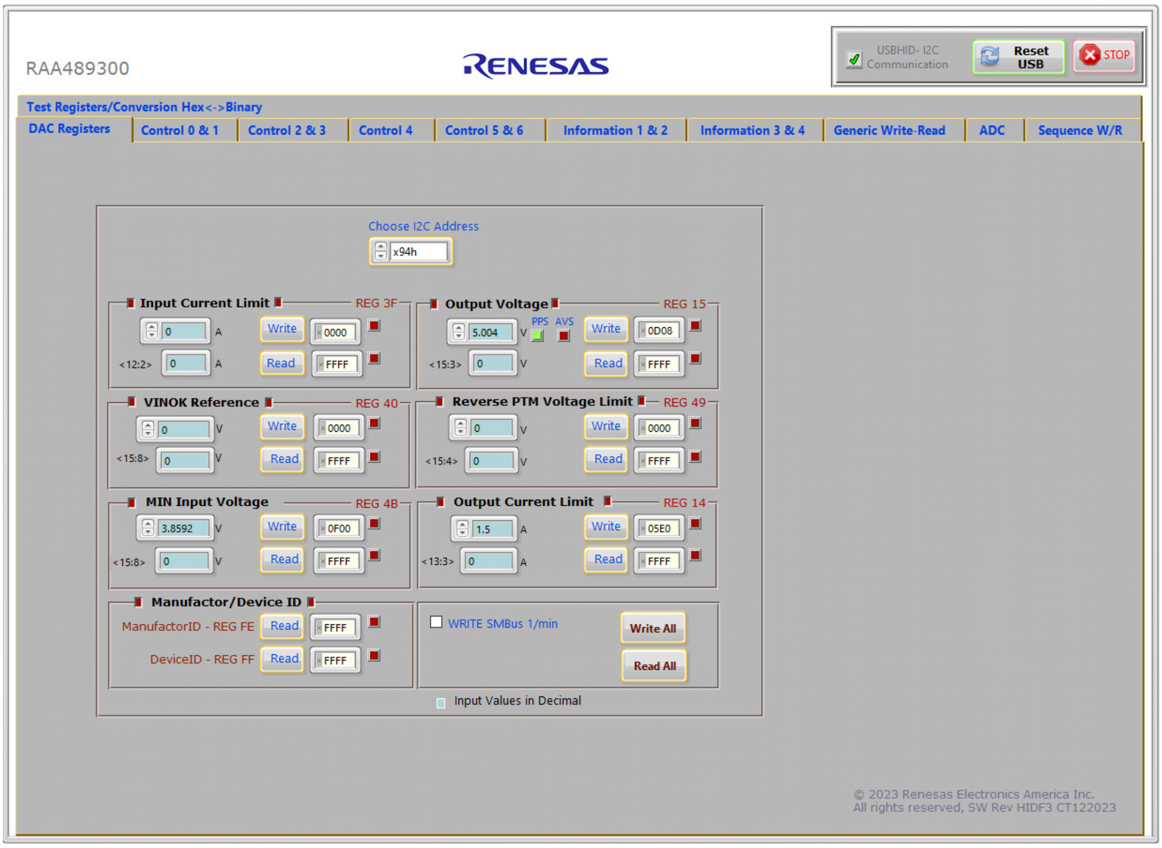


Figure 6. RAA489300 Graphical Interface

2. Check the status of the USB HID-I2C Communication at the top-right of the GUI. If the communication is OK, the USB HID-I2C Communication status shows a green checkmark (see Figure 6).
   - A green LED turns on in the HID USB-I2C interface board when communication between the computer and the HID USB-I2C interface board is established (see Figure 7).

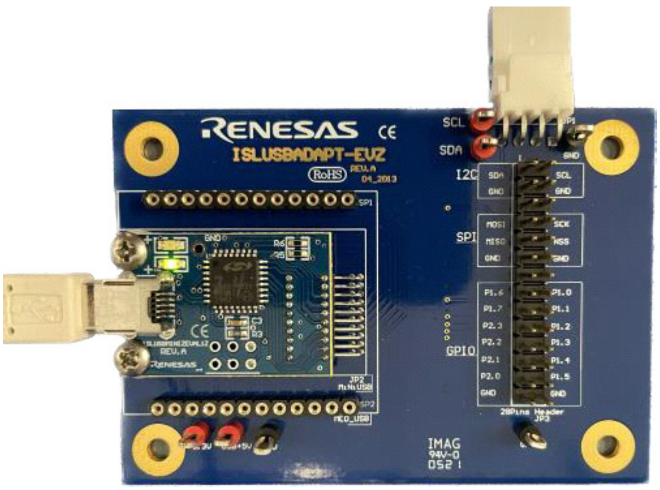


Figure 7. HID USB-I2C Interface Board

If the status in the GUI shows a red crossing mark, it indicates that the computer cannot establish the connection.

The following describes two communication issues:

- Issue 1 – Computer to HID USB-I2C Interface Board Communication

When there is communication failure between the computer and HID USB-I2C interface board, a GUI message appears (see Figure 8), and on the HID USB-I2C interface board, a green LED turns off.

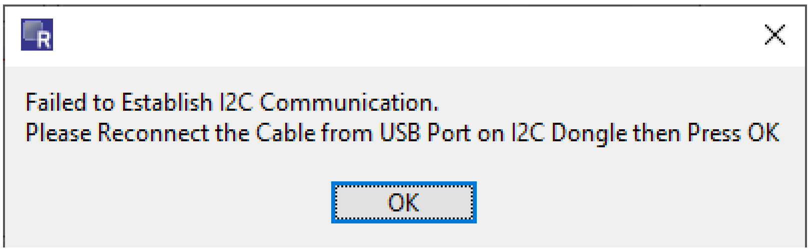


Figure 8. Failed to Establish Message

To troubleshoot, follow these steps:

1. When the Failed to Establish message appears, reconnect the USB connection.
2. Click the **OK** button.
3. The green LED is on when the interface board is connected to the computer.
4. Read any register to check the communication.

- Issue 2 – HID USB-I2C Interface Board to EVB Communication

When there is a communication issue between the HID USB-I2C interface board and the EVB, the following message appears.

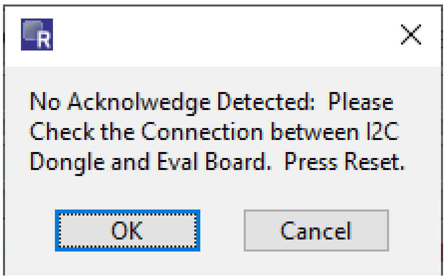


Figure 9. Failed to Establish Message

Note: A green LED in the interface board can remain on when communication is established between the computer and the HID USB-I2C interface board.

To troubleshoot, follow these steps:

1. When the message above appears, reconnect SDA, SCL, and GND to the EVB.
2. Click the **OK** button.
3. Read any register to check communication.

Note: If the problem continues, power off and on the evaluation board and reconnect the USB to the interface board.

3. Functional Description

The RTKA489300DE0000BU provides all the circuits required to evaluate the features of the RAA489300. Many of the features of the RAA489300, such as a 3-level buck and conventional 2-level buck, PTM in both directions, input and output current monitoring, and pre-biased output with soft-start are available on this evaluation board.

3.1 Recommended Equipment

- Power supply capable of up to 57.6V and at least 6A source current
- Electronic load capable of sinking current up to 12A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

3.2 Setup and Configuration

The default topology, address, operation, and input current limit are set by R43 that is tied to the PROG pin. The PROG Pin Programming Options table in the *RAA489300 Datasheet* shows the programming options. These values can also be changed through the SMBus control registers in the Renesas GUI (see Figure 10).

The two LEDs indicate the PGOOD and INT/CMOut status, respectively. For more details about the functions of these two pins, refer to the *RAA489300 Datasheet*. Figure 10 shows the top view of the evaluation board and highlights the key testing points and connection terminals. For more information about the RAA489300, including other modes of operation, refer to the *RAA489300 Datasheet*.

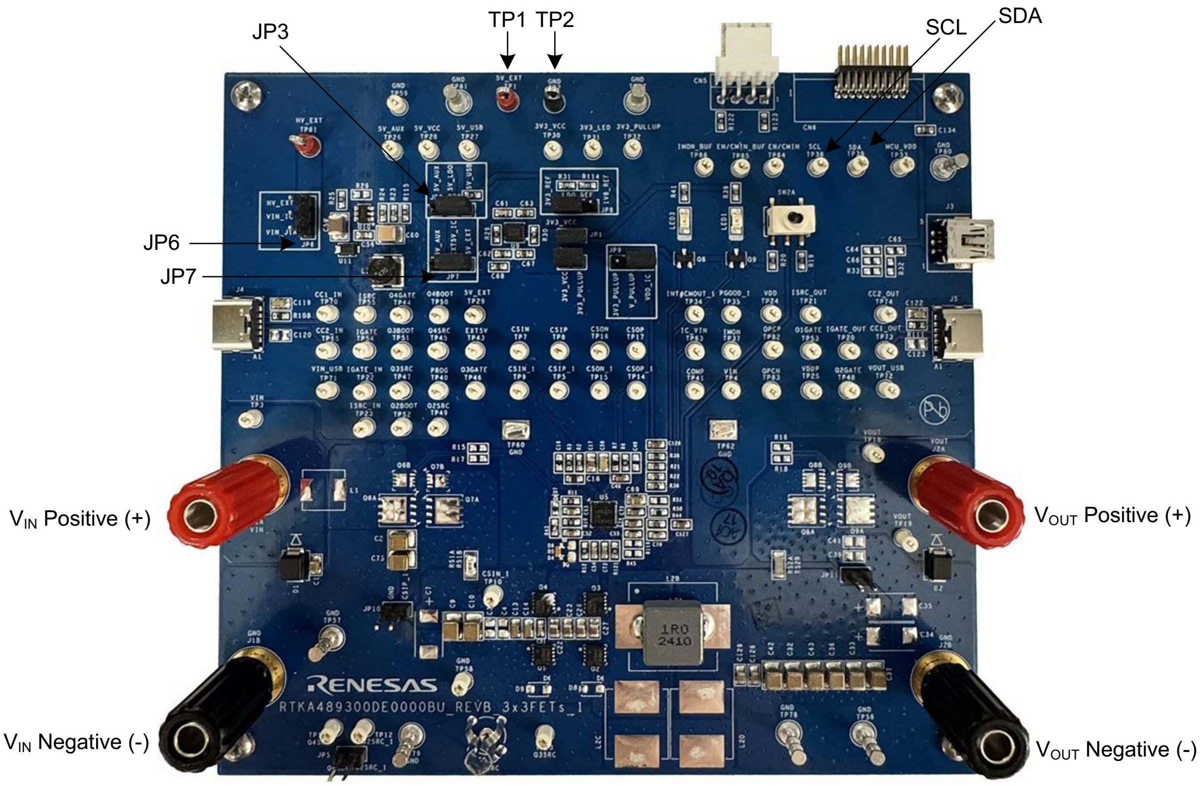


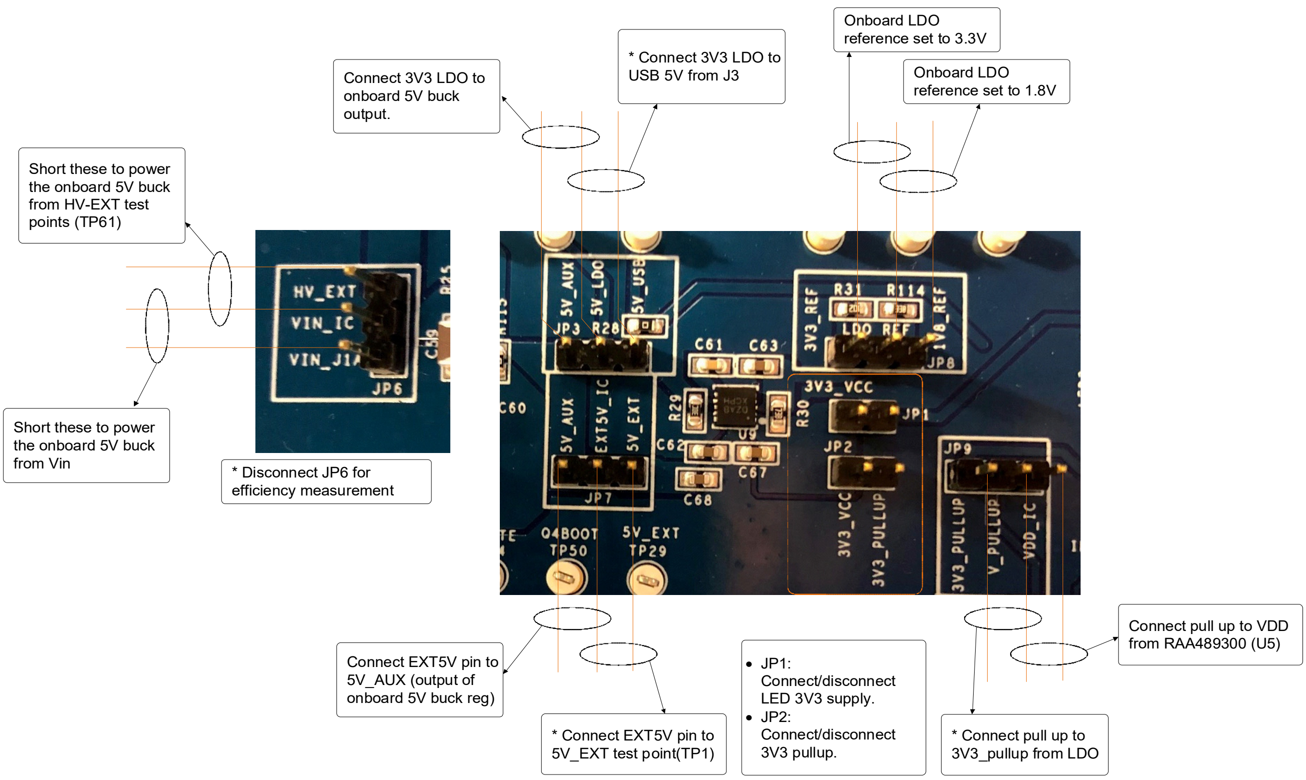
Figure 10. RTKA489300DE0000BU Board Connection Guideline

3.2.1 Check Jumpers and I2C/SMBus Connection

The RAA489300 can be powered either by an internal LDO or using an external 5V input. The RTKA489300DE0000BU board has 3 jumpers so that the user can select whether to use the internal LDO or external 5V power supply. Figure 11 shows the locations of the jumpers related to the selection of driving power for the RAA489300 on the RTKA489300DE0000BU board. The RTKA489300DE0000BU board is equipped with a buck converter to generate external 5V voltage (EXT5V) from the input voltage through J1A and J1B (GND). JP6 is a jumper that selects whether to receive the input of the buck converter to generate EXT5V from J1A and J1B(GND) or from TP61. By default, pin 1 (VIN) and pin 2 are connected, and J1A and J1B are used as inputs of the buck converter. JP3 is a jumper that sets whether to use the 5V generated by the buck converter or the 5V of the USB input as the EXT5V of the RAA489300. JP7 is a jumper that can select whether to directly receive 5V from TP1 and TP2 or use 5V generated from a buck converter. Review these two examples on the use of EXT5V:

- Example 1 – In the case of receiving 5V of driving power from the RAA489300 through an external power supply, pin 2 and pin 3 (5V_EXT) of JP7 must be connected.
- Example 2 – When using the internal LDO of RAA489300 without using EXT5V, leave all pins of JP6 unconnected, or the 5V power is not supplied from the external power supply while pin 2 and pin 3 (5V_EXT) of JP7 are connected.

See Figure 11 for a detailed description of the RAA489300 driving power according to each jumper connection.



Note: The asterisk (*) marks the configuration to follow for the efficiency test.

Figure 11. Jumper Configuration Guide

3.2.2 Apply Input Voltage and Setup

Complete the following steps for the startup. The register settings of the RAA489300 can be changed using the RAA489300 GUI software. A brief description of the RAA489300 GUI software can be found in Using the GUI.

1. If driving the RAA489300 using 5V of an external power supply, supply 5V of the external power supply through TP1 and TP2 with the main power of the 3-Level Buck converter. Set the current limit of the power supply for 5V of an external power supply to 300mA.
2. Before enabling switching, the control registers must be set up as follows:
   a. Control4 (0x4E) Bit[5:7] = b111 → Set the Low Side ZCD Filter bandwidth to 3.2MHz.
   b. Control4 (0x4E) Bit[8:9] = b01 → Set the low voltage range phase comparator blanking time to 80ns.

3. After confirming that the current limit of the power supply that provides main power is sufficient, main power is supplied through J1A and J1B (GND) with no load. Ensure the main input voltage does not exceed 57.6V.
4. Check the V_{CFLY} voltage is close to half the input voltage.
5. Set the output voltage using the output voltage register (0x15) to a value lower than the input voltage. Because the default absolute OV threshold for the output voltage (Control1 Bits[3:2]) is 24V, Renesas recommends setting the output voltage below 24V.
6. In a no-load condition, set Control0 (0x39) Bit[0] to 1 to enable switching. The default pre-charge wait time is set to 200ms. If switching is activated while there is a load, it might not transition to the switching state because of the short-circuit detection feature on the output side of the RAA489300.
7. If the input voltage requires a change at no load or at a low load (20mA or less), Renesas recommends that the input voltage change slew rate is lower than 1mV/µsec. Change the input voltage under load.

3.2.3 Apply Load

When driving the RAA489300 with an internal LDO, the maximum output should be less than 50W. If setting the output voltage above 23V, change the absolute overvoltage threshold setting for the output voltage in Control1 Bits[2:3] to above 23V. Before applying the load, set the input current limit (0x3F) and the output current limit (0x14). The default value for the input current limit is 0.476A, and the default value for the output current limit is 1.504A.

3.2.4 Entering Forward PTM

Complete the following steps to enter Pass-Through Mode:

1. Set the Forward/Reverse Operation bit to Forward (Control0 Bit[2] = 0)
2. Set the Low Power PTM mode bit to disable (Control2 Bit[12] = 0)
3. Set the PGOOD Window bits to 20% (Control2 Bits[9:8] = b11)
4. Set the Output Voltage register(0x15) to the value obtained from Equation 1.

(EQ. 1)
$$\text{OutputVoltage} = \text{InputVoltage} \times \text{Input Voltage Tolerance Ratio} - 0.5\text{V}$$

5. Set the Enable PTM bit to enable (Control1 Bit[1] = 1) to enter the Forward PTM mode.

3.2.5 Exiting Forward PTM

Complete the following steps to exit Pass-Through Mode:

1. Set the Relative Output OV Protection to disable (Control5 Bit[8] = 1).
2. Set the CFLY UV/OV Fault to disable (Control5 Bit[11] = 1).
3. Set the CFLY Pre-Charge Function to enable (Control2 Bit[7] = 1).
4. Set the CSOP Discharge bit to enable (Control2 Bit[14] = 1).
5. Set the Enable PTM bit to disable (Control1 Bit[1] = 0) to exit the Forward PTM mode.

3.2.6 ADC Register

RAA489300 provides four ADC registers. Table 1 shows the ADC register information that the RAA489300 provides. When a 5mΩ sense resistor is used with the RAA489300, the ADC output current measurements value is clamped at 11.32A.

Table 1. RAA489300 ADC Channel Overview

Channel	Register Address	LSB	Sensing resistor	Valid Bits	Maximum Value
Input Voltage (V)	0x83	0.192V	-	[7:0]	48.96 V
Output Voltage (V)	0x85	0.192V	-	[7:0]	48.96V
Input Current (A)	0x86	22.2mA	10mΩ	[7:0]	5.661A
Output Current (A)	0x87	44.4 mA	5mΩ	[7:0]	11.322A

3.2.7 Setting for Lowest Bias Current Consumption

To achieve the lowest bias current in Sleep state, Bit[7] of the Control2 register can be set to 1. This bit disables the CFLY Pre-Charge Function. Set this bit to 0 again before sending the command to exit sleep state.

4. Board Design

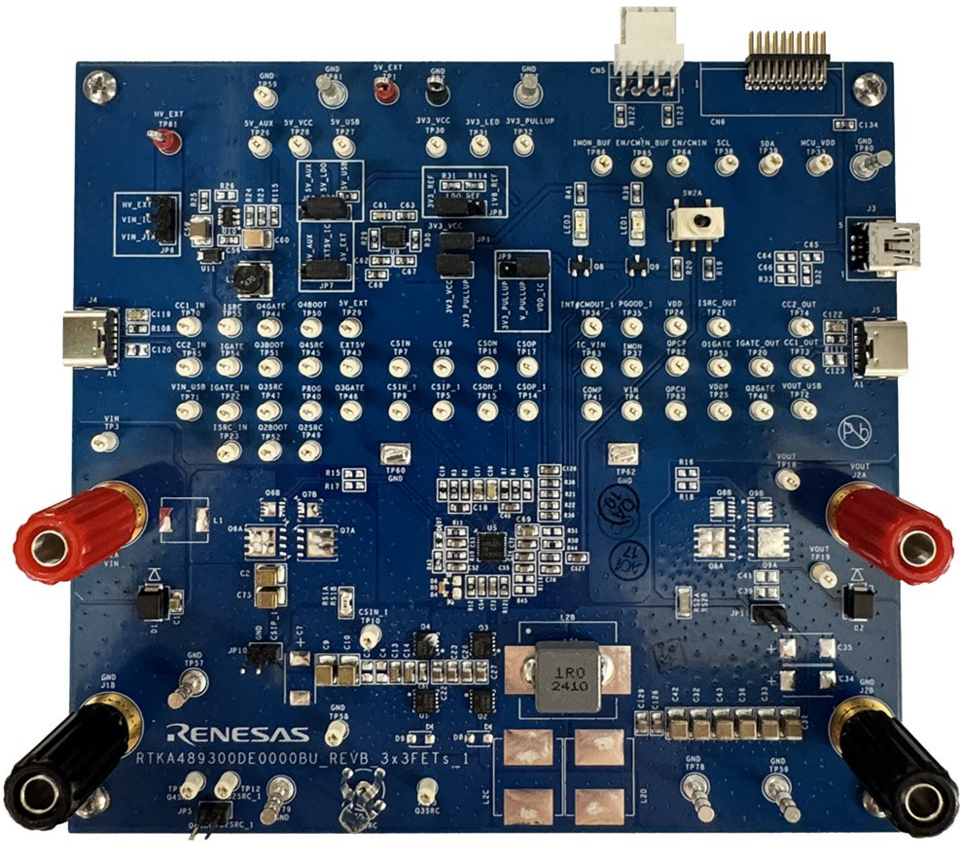


Figure 12. RTKA489300DE0000BU Evaluation Board (Top)

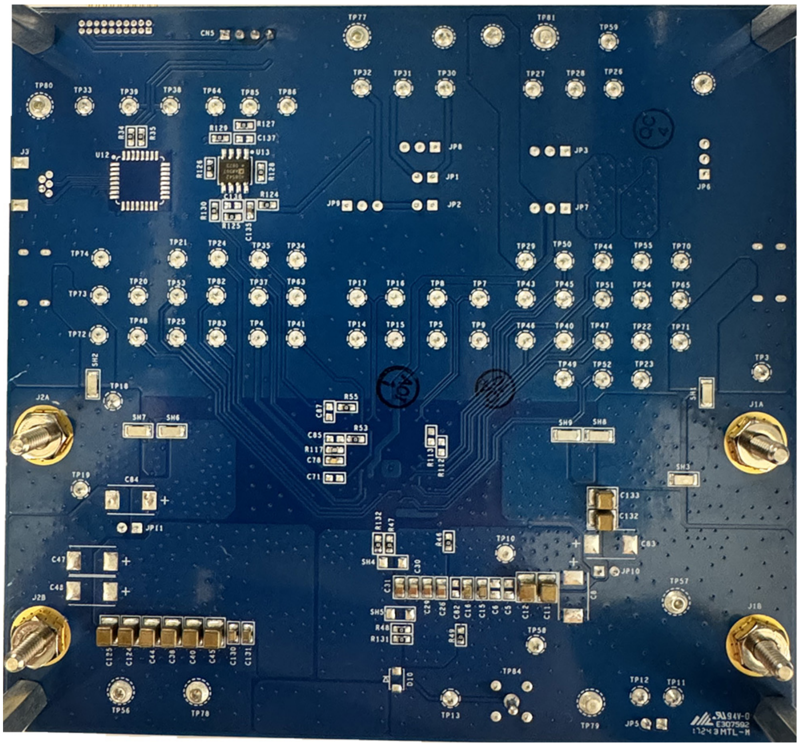


Figure 13. RTKA489300DE0000BU Evaluation Board (Bottom)

4.1 Layout Guidelines

Layout example of RAA489300 and the power stage:

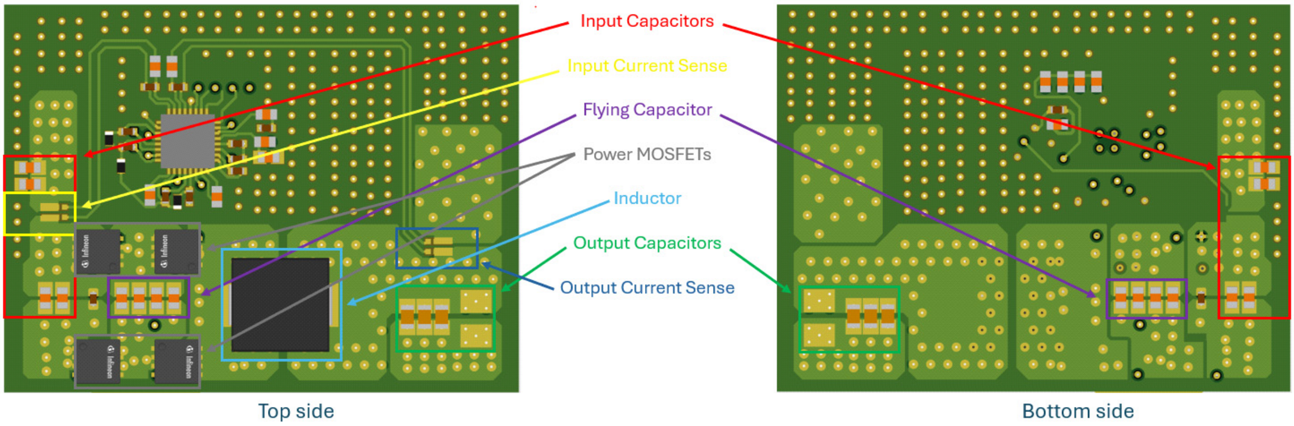


Figure 14. Example Layout of the RAA48900

An an example layout of the power stage components along with the IC is shown in Figure 14. The input, flying, and the output capacitors are split on both layers and are placed in a super-imposed fashion. The example layout shows a 6-layer PCB design with the following stack-up as shown in Table 2.

Table 2. Layer Stack-up of the Example PCB Layout

Layer	Stack
Top Layer	Components + Power planes + Signal Routing
Layer 2	Gnd Planes only
Layer 3	Signal Routing
Layer 4	Power Planes
Layer 5	GND Planes only
Bottom Layer	Components + Power planes + Signal Routing

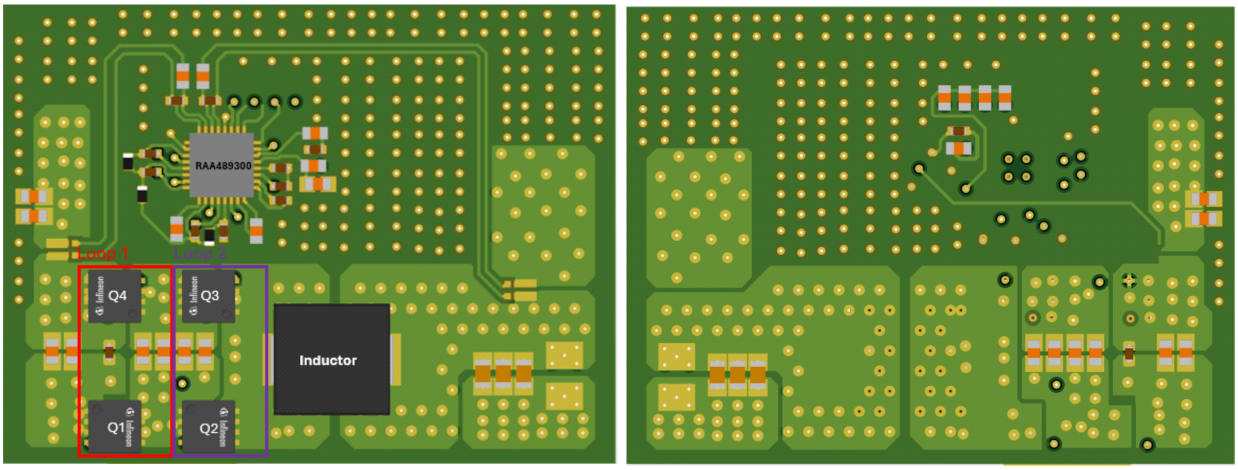


Figure 15. Top Side (left) and Bottom Side (right) of the Example Layout

The two main commutation loops that must be minimized are highlighted in the example power stage layout in Figure 15.

- Loop 1 encompasses the input capacitors, the highest side MOSFET (Q4), the flying capacitor, and the lowest side MOSFET (Q1). The impedance on this loop can be minimized by arranging the components in Figure 15. The impedance can further be lowered by placing low ESR and ESL capacitors close to the drain terminal of Q4 and the source terminal of Q1.
- Loop 2 consists of the flying capacitors, Q3 MOSFET, and Q2 MOSFET. This loop can be minimized when arranged as shown in Figure 15. Generous use of stitching vias is recommended along with power planes when connecting the flying capacitors to the MOSFETs.

Renesas recommends routing the corresponding gate and source traces from the IC to the MOSFETs close to each other and in the same layer as shown in Figure 16 from the example layout. In this example, the gate and source traces are routed in Layer 4 of the PCB.

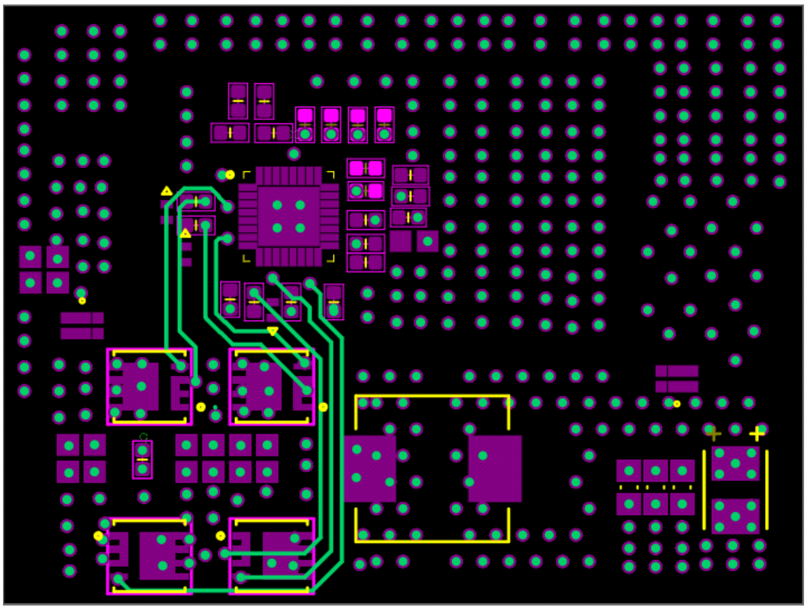


Figure 16. Gate and Source Traces from the IC to the FETs

4.1.1 General Guidelines for Routing the Traces to Current-Sense Resistors:

The CSIP and CSIN pins connect to the input current sense resistor along with he CSOP and CSON pins connecting to the output current sense resistor. The traces from the pins to the respective resistors must be routed in a parallel fashion to minimize any offset voltage resulting from input bias currents to the current sense amplifiers.

As a general rule of thumb, route the current-sensing traces through vias to connect the center of the pads, or route the traces into the pads from the inside of the current-sensing resistor. Figure 17 shows the two preferred ways of routing current-sensing traces.

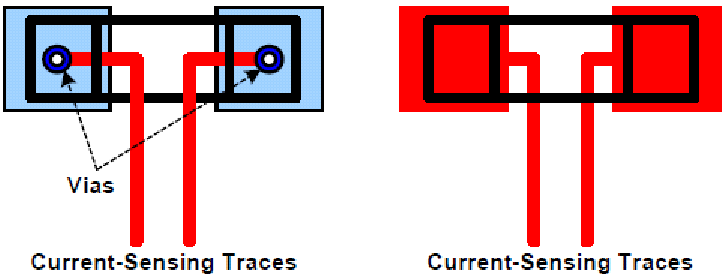


Figure 17. Recommended Routing Style for the Current Sense Traces from the Resistor Placed On: The Other Side as Controller (Left), the Same Side as Controller (Right)

Table 3. Pin-wise Layout Recommendations

Pin Number	Pin Name	Guidelines
1	IGATE	When an isolation FET is used in the application, the trace connecting the IGATE pin to the gate terminal of the isolation FET must be routed parallel to the trace connecting the ISRC pin to the source of the isolation FET. When the Isolation FET is not used, leave this pin floating.
2	ISRC	When an isolation FET is used in the application, the trace connecting the IGATE pin to the gate terminal of the isolation FET must be routed parallel to the trace connecting the ISRC pin to the source of the isolation FET. When the Isolation FET is not used, connect ISRC to GND or VDD.

Table 3. Pin-wise Layout Recommendations (Cont.)

Pin Number	Pin Name	Guidelines
3	Q4BOOT	Connect the bootstrap supply capacitor as close as possible to the Q4Boot and Q4Source pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
4	Q4GATE	The trace connecting this pin to the gate terminal of the Q4 MOSFET must be routed in parallel to the trace connecting the Q4SRC pin to the source terminal of the Q4 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
5	Q4SRC	The trace connecting the Q4SRC pin to the source terminal of the Q4 MOSFET must be routed in parallel to the trace connecting the Q4Gate pin to the gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. This trace must also be routed in parallel to the trace connecting the CSIN pin and the current sense resistor as they form the inputs to the high-side phase comparator. It must also be ensured that this pin is directly connected to the Source pin of the MOSFET and not through a copper plane.
6	Q3BOOT	Connect the bootstrap supply capacitor as close as possible to the Q3BOOT and Q3SOURCE pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
7	Q3GATE	The trace connecting this pin to the gate terminal of the Q3 MOSFET must be routed in parallel to the trace connecting the Q3SRC pin to the source terminal of the Q3 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
8	Q3SOURCE	The trace connecting the Q3SRC pin to the source terminal of the Q3 MOSFET must be routed in parallel to the trace connecting the Q3Gate pin to its gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. It must also be ensured that this pin is directly connected to the Source pin of the MOSFET and not through a copper plane.
9	PROG	This pin must be connected to a resistor based on the desired programming option. The resistor can be placed in general proximity to the IC.
10	Q2BOOT	Connect the bootstrap supply capacitor as close as possible to the Q2BOOT and Q2SOURCE pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
11	Q2GATE	The trace connecting this pin to the gate terminal of the Q2 MOSFET must be routed in parallel to the trace connecting the Q2SRC pin to the source terminal of the Q2 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
12	Q2SOURCE	The trace connecting the Q2SRC pin to the source terminal of the Q2 MOSFET must be routed in parallel to the trace connecting the Q2GATE pin to its gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. It must also be ensured that this pin is directly connected to the source pin of the MOSFET and not through a copper plane.
13	VDDP	This pin must be connected to a decoupling capacitor placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
14	Q1GATE	The trace connecting this pin to the gate terminal of the Q1 MOSFET. The trace must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. Ensure a continuous connection to GND parallel to this trace that connects to the source terminal of Q1 MOSFET.
15	GND	This pin must be connected to the ground copper plane with low impedance. Renesas recommends using four to five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
16	EN/CMIN	This pin is an input signal and is recommended to be connected to a pull-down resistor placed close to the IC.
17	QPCN	The pins interface an external capacitor to the internal charge pump (QP). QPCN and QPCP are to be connected to an external capacitor which is placed close to the IC. The traces must be routed parallel to each other as the currents flowing through them are differential in nature.
18	QPCP	
19	EXT5V	Connect a decoupling capacitor to this pin. The decoupling capacitor must be placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
20	VDD	
21	VIN	Connect an RC filter to this pin from the applied input voltage source terminal. The VIN pin must be connected to the DRAIN terminal of the Isolation MOSFET when used on the input side. The decoupling capacitor must be placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
22	VCOMP	Connect the compensation components in general proximity to the IC. Ensure no digital or switching signals are routed close to these components or traces connecting them.

Table 3. Pin-wise Layout Recommendations (Cont.)

Pin Number	Pin Name	Guidelines
23	IMON	Connect an RC filter to this pin. The filter components must be placed in close proximity to the IC. This pin can be left floating when not used.
24	INT#/CMOUT#	Connect a pull-up resistor placed in general proximity to the IC. This pin can be left floating when not used.
25	SCL	Connect a pull-up resistor placed in general proximity to the IC.
26	SDA	
27	PGOOD	
28	GND	This pin must be connected to the ground copper plane with low impedance. Renesas recommends to use four to five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
29	CSOP	The trace connecting the CSOP pin to the current sense resistor must be routed differentially to the trace connecting the CSON pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC.
30	CSON	The trace connecting the CSOP pin to the current sense resistor must be routed differentially to the trace connecting the CSON pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC. Additionally, connect a RC filter between this pin and the current sense resistor that in placed in close proximity to the IC.
31	CSIP	The trace connecting the CSIP pin to the current sense resistor must be routed differentially to the trace connecting the CSIN pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC. Additionally, connect a RC filter between this pin and the current sense resistor that in placed in close proximity to the IC.
32	CSIN	The trace connecting the CSIP pin to the current sense resistor must be routed differentially to the trace connecting the CSIN pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC.

4.2 Schematic Diagrams

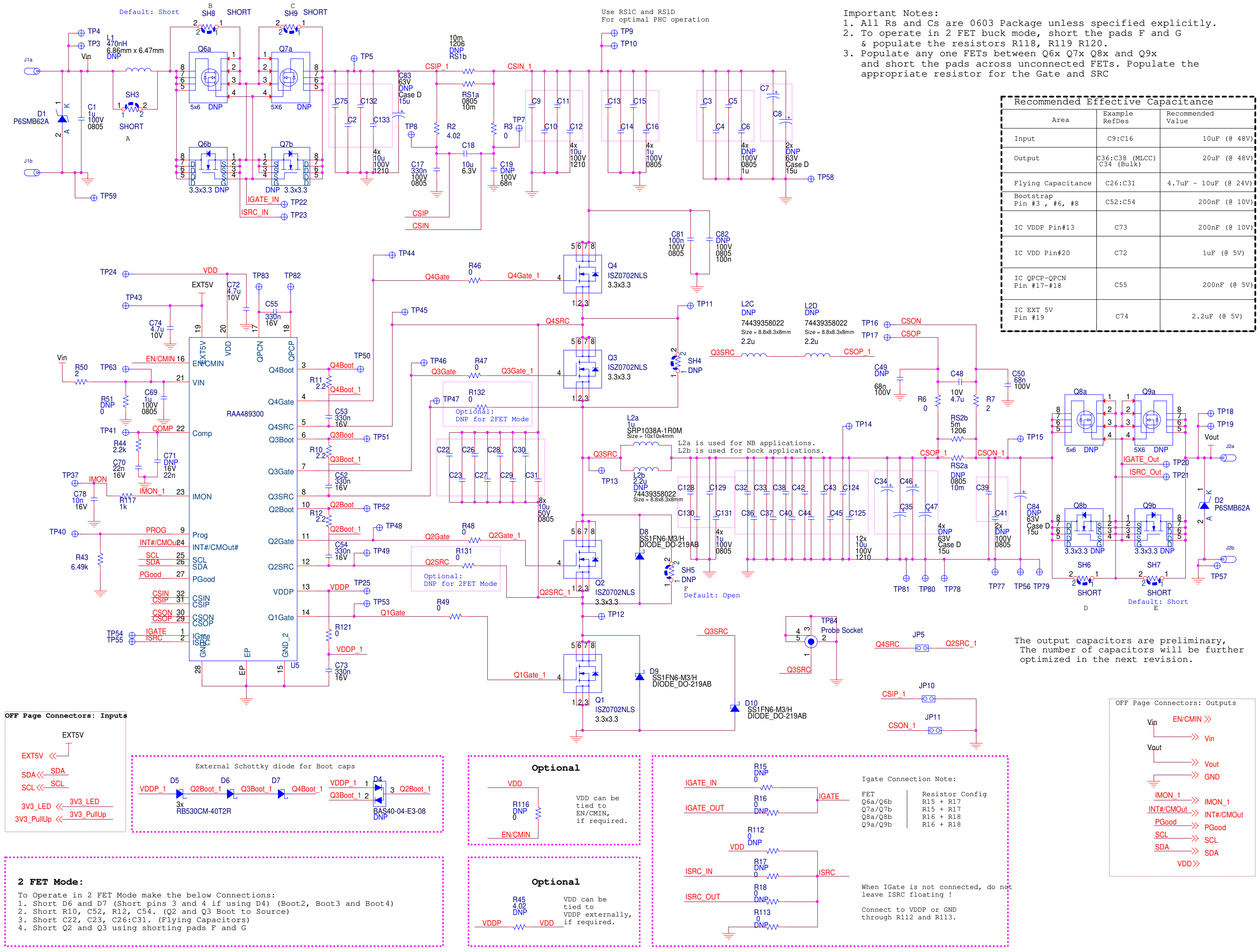


Figure 18. Schematics (1 of 3)

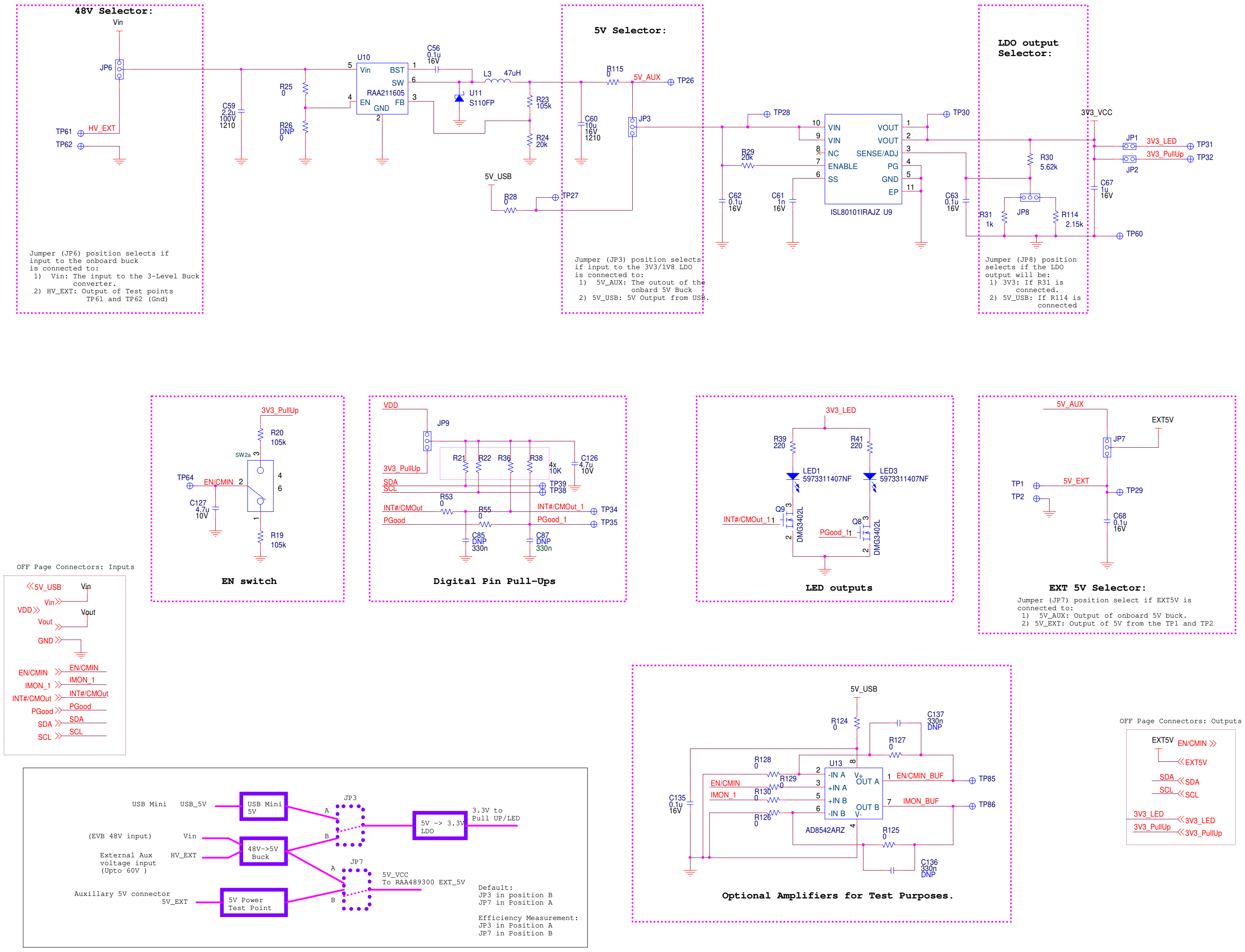


Figure 19. Schematics (2 of 3)

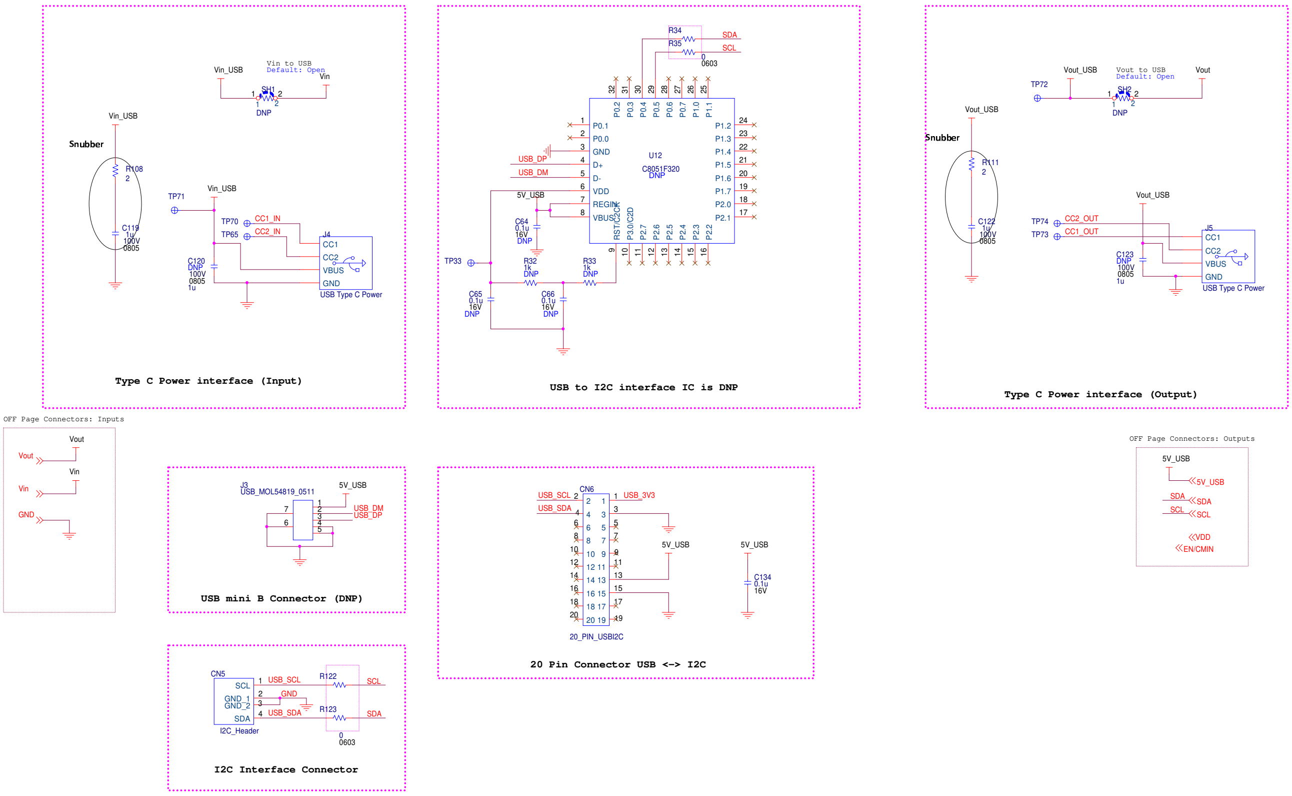


Figure 20. Schematics (3 of 3)

4.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	CN5	CONN RCPT 4POS 0.1 TIN EDGE MNT	Molex	38001334
1	CN6	CONN HEADER R/A 20POS 1.27mm	Harwin Inc.	M50-3901042
18	C1, C3, C4, C5, C6, C13, C14, C15, C16, C69, C119, C120, C122, C123, C128, C129, C130, C131	CAP CER 1µF 100V X7S 0805	Murata Electronics	GRM21BC72A105KE01L
20	C2, C9, C10, C11, C12, C32, C33, C36, C37, C38, C40, C42, C43, C44, C45, C75, C124, C125, C132, C133	CAP CER 10µF 100V X7S 1210	Murata Electronics	GRM32EC72A106KE05L
8	C7, C8, C34, C35, C46, C47, C83, C84	CAP TANT POLY 15µF 63V 2917	KEMET	T521X156M063ATE035
1	C17	CAP CER 0.33µF 100V X7S 0805	TDK Corporation	C2012X7S2A334K125AB
1	C18	CAP CER 10µF 6.3V X7S 0603	TDK Corporation	C1608X7S0J106M080AC
3	C19, C49, C50	CAP CER 0.068µF 100V X7R 0805	YAGEO	CC0805KKX7R0BB683

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
8	C22, C23, C26, C27, C28, C29, C30, C31	COmmERCIAL GRADE GENERAL PURPOSE	TDK Corporation	C2012X5R1H106K125AC
2	C39, C41	CAP CER 10µF 75V X7R 1210	TDK Corporation	CGA6P1X7R1N106M250AC
5	C48, C72, C74, C126, C127	CAP CER 4.7µF 10V X7T 0603	Murata Electronics	GRM188D71A475ME11D
9	C52, C53, C54, C55, C73, C85, C87, C136, C137	CAP CER 0.33µF 16V X7R 0603	YAGEO	CC0603KRX7R7BB334
9	C56, C62, C63, C64, C65, C66, C68, C134, C135	CAP CER 0.1µF 16V X7R 0603	Taiyo Yuden	EMK107B7104KA-T
1	C59	CAP CER 2.2µF 100V X7R 1210	TDK Corporation	C3225X7R2A225M230AB
1	C60	CAP CER 10µF 16V X8R 1210	TDK Corporation	C3225X8R1C106K250AB
1	C61	CAP CER 1000PF 16V X7R 0603	KEMET	C0603C102K4RAC7867
1	C67	CAP CER 1µF 16V X5R 0603	Taiyo Yuden	EMK107BJ105KA-T
2	C70, C71	CAP CER 0.022µF 16V X7R 0603	YAGEO	CC0603JRX7R7BB223
1	C78	CAP CER 10000PF 16V X7R 0603	KEMET	C0603C103K4RAC7867
2	C81, C82	CAP CER 0.1µF 100V X7R 0603	KYOCERA AVX	06031C104KAT2A
2	D1, D2	TVS DIODE 53VWM 85VC DO214AA	Bourns Inc.	P6SMB62A
1	D4	DIODE ARRAY SCHOTTKY 40V SOT23	Vishay General Semiconductor - Diodes Division	BAS40-04-E3-08
3	D5, D6, D7	40V, 100MA, SOD-923, SCHOTTKY BA	Rohm Semiconductor	RB530CM-40T2R
3	D8, D9, D10	DIODE SCHOTTKY 60V 1A DO219AB	Vishay General Semiconductor - Diodes Division	SS1FN6-M3/H
5	JP1, JP2, JP5, JP10, JP11	CONN HEADER VERT 2POS 2.54mm	Amphenol ICC (FCI)	69190-202HLF
5	JP3, JP6, JP7, JP8, JP9	CONN HEADER VERT 3POS 2.54mm	Amphenol ICC (FCI)	68000-103HLF
2	J1a, J2a	CONN BIND POST KNURLED RED	Cinch Connectivity Solutions Johnson	111-0702-001
2	J1b, J2b	CONN BIND POST KNURLED BLACK	Cinch Connectivity Solutions Johnson	111-0703-001
1	J3	CONN RCPT USB2.0 MINI B 5P R/A	Molex	548190519
2	J4, J5	CONN RCPT TYPE C 24POS SMD RA	CUI Devices	UJC-HP-3-SMT-TR
2	LED1, LED3	LED GREEN CLEAR 1206 SMD	Dialight	5973311407NF
1	L1	FIXED IND 470NH 17.5A 4.2MΩ SM	Vishay Dale	IHLP2525CZERR47M01
3	L2b, L2D, L2C	FIXED IND 2.2µH 13A 3.7MΩ SMD	Würth Elektronik	74439358022
1	L2a	FIXED IND 1µH 18A 3.3MΩ SMD	Bourns Inc.	SRP1038A-1R0M
1	L3	FIXED IND 47µH 800MA 351MΩ SMD	Würth Elektronik	74408943470
4	Q1, Q2, Q3, Q4	MOSFET N-CH 60V 17A/86A TSDSON	Infineon Technologies	ISZ0702NLSATMA1

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
4	Q6a, Q7a, Q8a, Q9a	MOSFET N-CH 80V 25A/130A POWER56	onsemi	FDMS86350
4	Q6b, Q7b, Q8b, Q9b	MOSFET N-CH 80V 14A/68A POWER33	onsemi	FDMC86340ET80
2	Q8, Q9	MOSFET N-CH 30V 4A SOT23	Diodes Incorporated	DMG3402L-7
2	RS1a, RS2a	RES 10MΩ 1% 3/4W 0805	Ohmite	MCS1320R010FER
1	RS1b	1W 0.010Ω 0.5% 1206	Ohmite	PCS1206DR0100ET
1	RS2b	RES 5MΩ 1% 1.5W 1206	KOA Speer Electronics, Inc.	TLR2BPDTD5L00F75
2	R2, R45	RES 4.02Ω 1% 1/10W 0603	YAGEO	RC0603FR-074R02L
37	R3, R6, R10, R11, R12, R15, R16, R17, R18, R25, R26, R28, R34, R35, R46, R47, R48, R49, R51, R53, R55, R112, R113, R115, R116, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132	RES 0Ω JUMPER 1/10W 0603	YAGEO	RC0603FR-070RL
4	R7, R50, R108, R111	RES SMD 2Ω 1% 1/3W 0603	Vishay Dale	CRCW06032R00FKEAHP
3	R19, R20, R23	RES SMD 105kΩ 0.1% 1/10W 0603	YAGEO	RT0603BRE07105KL
4	R21, R22, R36, R38	RES 10kΩ 1% 1/8W 0603	Stackpole Electronics Inc	RNCP0603FTD10K0
2	R24, R29	CHIP RESISTOR THIN FLIM HIGH PRE	YAGEO	RT0603FRE1320KL
1	R30	RES 5.62kΩ 1% 1/10W 0603	YAGEO	RC0603FR-075K62L
4	R31, R32, R33, R117	RES 1kΩ 5% 1/5W 0603	YAGEO	RC0603JR-7W1KL
2	R39, R41	RES 220Ω 5% 1/10W 0603	YAGEO	RC0603JR-07220RL
1	R43	RES 6.49kΩ 1% 1/10W 0603	YAGEO	RC0603FR-076K49L
1	R44	CHIP RESISTOR THIN FLIM HIGH PRE	YAGEO	RT0603FRE132K2L
1	R114	RES 2.15kΩ 1% 1/10W 0603	YAGEO	RC0603FR-072K15L
9	SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9	RES 0Ω JUMPER 1206	KOA Speer Electronics, Inc.	TLRZ2BTTD
1	SW2a	SWITCH TOGGLE SPDT 0.4VA 20V	C&K	GT11MSCBE
2	TP1, TP61	PC TEST POINT MULTIPURPOSE RED	Keystone Electronics	5010
2	TP2, TP62	PC TEST POINT MULTIPURPOSE BLACK	Keystone Electronics	5011

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
65	TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP37, TP38, TP39, TP40, TP41, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP54, TP55, TP58, TP59, TP60, TP63, TP64, TP65, TP70, TP71, TP72, TP73, TP74, TP82, TP83, TP85, TP86	PC TEST POINT MINIATURE WHITE	Keystone Electronics	5002
7	TP56, TP57, TP77, TP78, TP79, TP80, TP81	TERM TURRET SINGLE L = 7.65mm TIN	Keystone Electronics	1598-2
1	TP84	Test Connectors	Tektronix	131-5031-00
1	U5	IC 3-Level Buck VR w. PTM	Renesas Electronics America Inc	RAA489300
1	U9	IC REG LINEAR POS ADJ 1A 10DFN	Renesas Electronics America Inc	ISL80101IRAJZ
1	U10	IC REG BUCK ADJ 500MA TSOT23-6	Renesas Electronics America Inc	RAA2116054GP3#JA0
1	U11	DIODE SCHOTTKY 100V 1A SOD123HE	onsemi	S110FP
1	U12	IC MCU 8BIT 16KB FLASH 32LQFP	Silicon Labs	C8051F320-GQR
1	U13	IC OPAMP GP 2 CIRCUIT 8SOIC	Analog Devices Inc.	AD8542ARZ

4.4 Board Layout

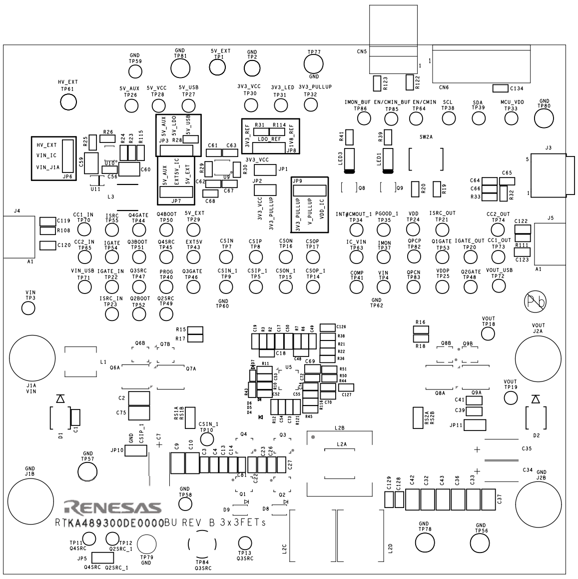


Figure 21. Silk Top Layer

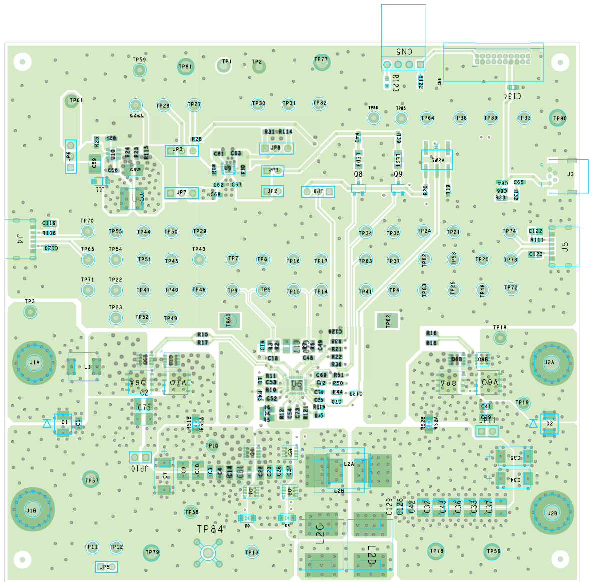


Figure 22. Layer 1

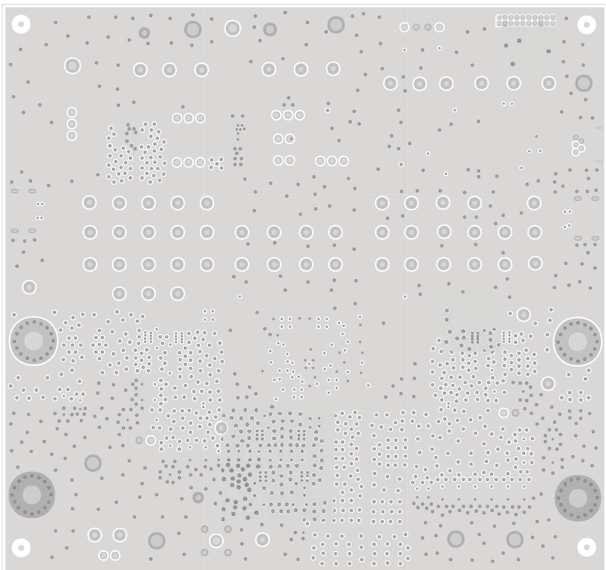


Figure 23. Layer 2

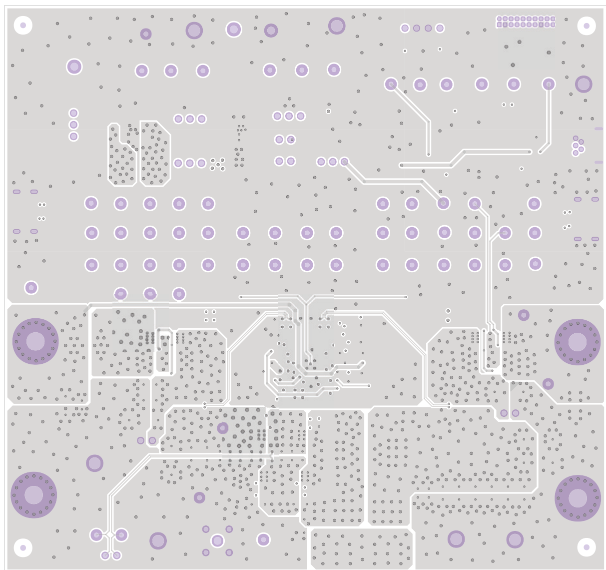


Figure 24. Layer 3

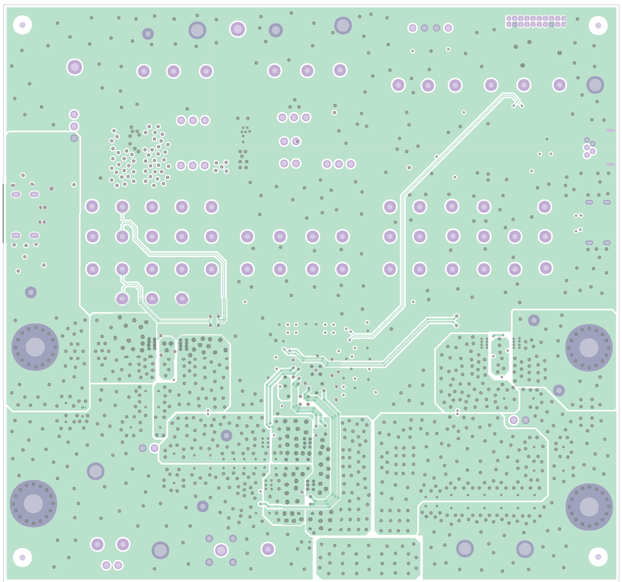


Figure 25. Layer 4

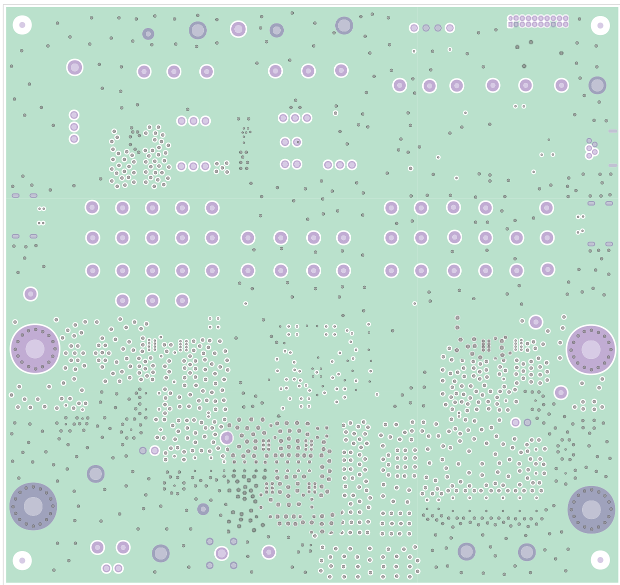


Figure 26. Layer 5

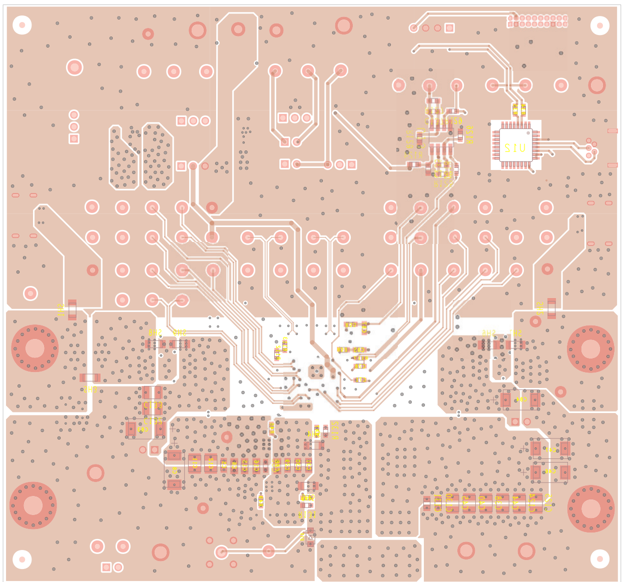


Figure 27. Layer 6

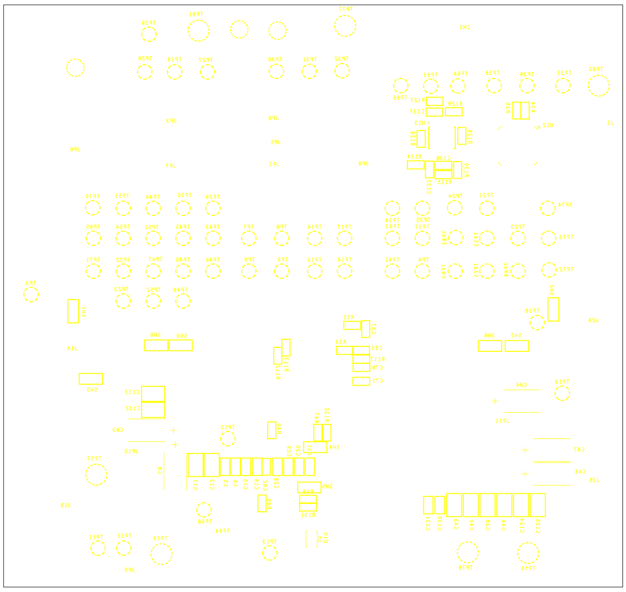


Figure 28. Silk Bottom Layer

5. Ordering Information

Part Number	Description
RTKA489300DE0000BU	RAA489300 Evaluation Board

6. Revision History

Revision	Date	Description
1.00	Nov 4, 2024	Initial release.

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