

### RTKP63175DE00000BC, RTKP63175DE00010BC

RPP63175 Low-Side Driver Evaluation Board with GaN/MOSFET In Boost System

#### **Description**

The RRP63175 evaluation boards (RTKP63175DE00000BC, RTKP63175DE00010BC) facilitate a rapid and thorough evaluation of RRP63175, a single low-side driver capable of 7.2A source and 5.3A sink current driving. These boards effectively drive the gates of GaN (RTKP63175DE00000BC) or silicon FETs (RTKP63175DE00010BC) in a boost system configuration. They include an inductor-capacitor (LC) filter and a power FET, enabling comprehensive system evaluation, with a 100V overvoltage protection feature at the output.

#### **Features**

- 7.2A source and 5.3A sink driver for GaN/MOSFET
- Accept 3.3V/5V logic level PWM inputs
- Fast propagation delay and matching: 5ns typical delay
- 4ns typical rise and fall time
- 5V power supply
- Support positive, negative PWM or EN input logic

#### **Specifications**

The following input and output parameters are based on evaluation tests. See the following specifications and check the recommended test conditions in Table 1 for more details.

Parameter	Rating
VDD Voltage	5V
Input Voltage	Up to 54V <sup>[1]</sup>
Input Current	Up to 5A <sup>[1]</sup>
PWM Switching Frequency	500kHz <sup>[1]</sup>
PWM Input Voltage	3.3V/5V
Output Voltage	Up to 100V <sup>[1]</sup>
Over Voltage Protection	100V
Output current	Up to 3.6A <sup>[1]</sup>

 Voltages and currents outside the indicated range can still be applied if needed but it is important to note that improper input/output configurations might lead to damage to the board.

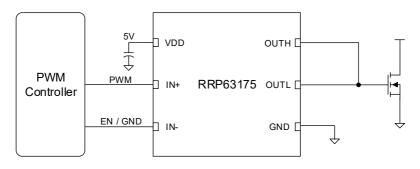


Figure 1. RRP63175 Typical Application Block Diagram

# **Contents**

1.	Fund	tional D	escription	3
	1.1	-	ng Range and Recommended Test Condition	
	1.2 1.3		mended Equipment	
		•	nd Configuration	
2.	Boar	d Desigr	1	5
	2.1	PCB La	yout Guidelines	5
	2.2	RTKP63	3175DE00000BC	6
		2.2.1	Schematic	7
		2.2.2	Bill of Materials	8
		2.2.3	Board Layout	9
	2.3	RTKP63	3175DE00010BC	12
		2.3.1	Schematic	14
		2.3.2	Bill of Materials	14
		2.3.3	Board Layout	16
3.	Desi	gn Refer	ence	20
	3.1	Input, C	Output and Duty Cycle	20
	3.2	Switchir	ng Frequency and Switching Current	20
	3.3		r Selection	
	3.4	Input Ca	apacitor and Output Capacitor	20
	3.5	Other C	Components	20
4.	Typic	cal Perfo	rmance Curves	21
5.	Orde	ring Info	ormation	22
6	Revie	sion Hist	tory	22

# 1. Functional Description

The RRP63175 evaluation boards (RTKP63175DE00000BC, RTKP63175DE00010BC) evaluate a boost system with either a enhance mode GaN or a logic level gate MOSFET application. The RRP63175 single low-side driver is provided in a 6-lead SCTDFN package. This series of evaluation boards operate with a supply voltage of 5V DC and is capable of driving a low-side power FET within the boost system, featuring a overvoltage protection (OVP) function.

### 1.1 Operating Range and Recommended Test Condition

The RRP63175 evaluation boards incorporate a 100V overvoltage protection feature, with  $V_{OUT}$  recommended to be set between 20V and 100V. The input current supports up to 5A on these evaluation boards. The VIN (also referred as VBUS) and LOAD settings should be adjusted based on  $V_{OUT}$ ,  $I_{IN}$ , and PWM duty conditions, as the board functions within a boost system. *IMPORTANT*:  $V_{OUT}$  might exceed the anticipated value when no load is applied, potentially causing the system to enter overvoltage protection (OVP) mode unexpectedly.

The inductance and capacitance values of the LC filter are determined based on a switching frequency of 500kHz for evaluation purposes. The components can be replaced with different values if a different switching frequency is required. Table 1 provides the recommended test conditions to evaluate the boost system application.

PWM Duty	V <sub>IN</sub> /V <sub>BUS</sub> (V)	I <sub>IN</sub> (A)	V <sub>OUT</sub> (V)	Max I <sub>OUT</sub> (A) <sup>[1]</sup>
10%	54	4	60	3.6
50%	30	5	60	2.0
90%	5	5	50	0.4

**Table 1. Recommended Test Condition** 

### 1.2 Recommended Equipment

- A power supply that can deliver 5V or higher with at least 1A source current capability to supply VDD
- A power supply that can deliver 60V or higher with at least 6A source current capability to supply VIN(VBUS)
- A square wave or pulse generator with 0V to 3.3V/5V logic levels output and 500kHz capability (one coaxial cable with a BNC male connector on one end and an SMA male connector on the other end)
- A DC electronic load to draw current on output with up to 120V/4A capability
- Minimum 4-channel oscilloscope to monitor VIN(VBUS), VOUT, SW and VDD signals

# 1.3 Setup and Configuration

- 1. Place a jumper between Pin 1 and Pin 2 on J14 and another jumper between Pin 2 and Pin 3 on J13 for non-inverting input logic mode. *Note:* For inverting input logic mode, place the jumper between Pin 2 and Pin 3 on J14 and the other jumper between Pin 1 and Pin 2 on J13.
- 2. Connect a 5V power supply with a current limit of 1A to the VDD (TP1) and GND (TP22/TP25).
- 3. Connect a power supply that can provide 60V or higher, with a current limit of 6A, to the VIN/VBUS (TP39) and GND (TP40).
- 4. Connect a function generator configured to output a square wave signal with a voltage range of 0V to 3.3V or 5V, a frequency of 500 kHz, and a 50% duty cycle to the PWM SMA connector J5 (IN+) for non-inverting input logic mode. Set the function generator channels to 50Ω impedance. *Note*: For inverting input logic mode, the square wave signal should be applied to the IN- terminal using connector J7, while maintaining the IN+ terminal at a high state.
- 5. Connect an electronic load to the VOUT pin and set the E-load to 0A.



<sup>1.</sup> I<sub>OUT</sub> is limited due to evaluation board safety concern.

- 6. Connect an oscilloscope to monitor VOUT, VIN, SW and VDD.
- 7. Turn on the electronic load, setting it to 0.5A for safety purpose.
- 8. Turn on the power supply connected to VDD, setting it to 5V.
- 9. Turn on the functional generator connected to J5 with the 0V to 3.3V/5V, 500kHz, 50% duty square wave signal set.
- 10. Turn on the supply connected to VIN(VBUS), setting it to 30V.
- 11. Verify if the SW signal is switching in 50% duty and the output voltage is equal to or above 60V.
- 12. Increase the electronic load up to 2A if needed.

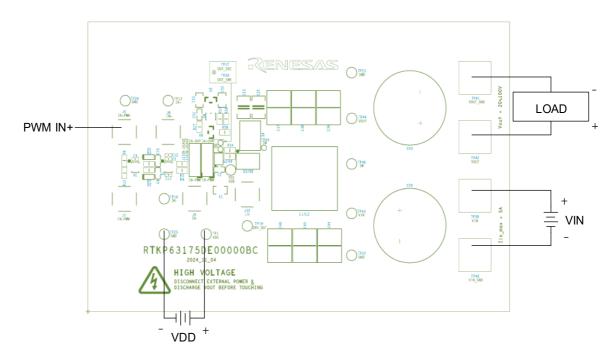


Figure 2. RTKP63175DE00000BC Setup Connection

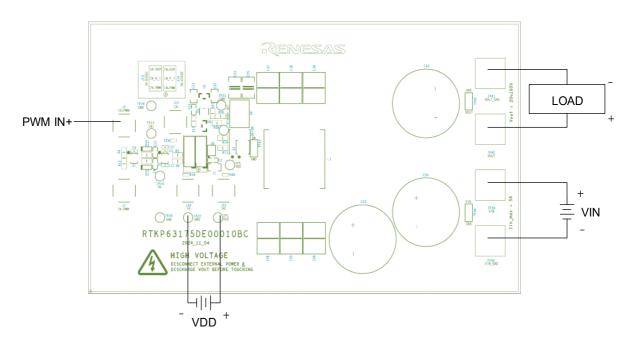


Figure 3. RTKP63175DE00010BC Setup Connection

# 2. Board Design

### 2.1 PCB Layout Guidelines

For best thermal performance, connect the driver thermal pad to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to the ground planes on other PCB layers. For best electrical performance, connect the PGND and AGND pins through the thermal pad to maintain a low impedance connection between the two pins.

Place the VDD decoupling capacitors close to the VDD-GND respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance.

#### In addition:

- Keep power loops as short as possible by paralleling the source and return traces.
- Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the outputs, add series gate resistors to dampen the oscillations.
- Large power components (such as power FETs, electrolytic capacitors, and power resistors) have internal
  parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit
  design.
- If you simulate your circuits, consider including parasitic components.



### 2.2 RTKP63175DE00000BC



Figure 4. RTKP63175DE00000BC Evaluation Board (Top)



Figure 5. RTKP63175DE00000BC Evaluation Board (Bottom)

### 2.2.1 Schematic

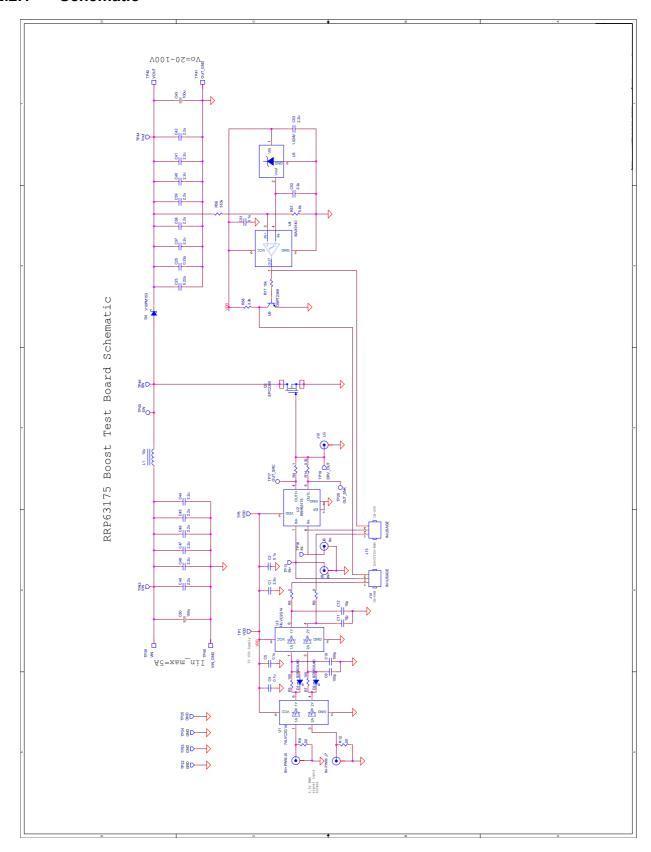


Figure 6. RTKP63175DE00000BC Schematic

#### 2.2.2 Bill of Materials

Table 2. RTKP63175DE00000BC BOM

Qty	Designator	Description	Part Number
1	PCB	-	RTKP63175DE00000BCREVAP CB
1	PLACE ASSY IN BAG	BAG, STATIC, 5X8, ZIPLOC, ROHS	5X8-STATIC-BAG
2	C4, C5	CAP, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	GRM155R71C104KA88D-T
2	C11, C12	CAP, SMD, 0402, 10pF, 16V, 1%, RF, TNF, ROHS	0402YJ100FBSTR-T
2	C2, C51	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	CC0603KRX7R7BB104-T
2	C9, C10	CAP, SMD, 0603, 100pF, 16V, 5%, PPS, ROHS	ECH-U1C101JX5-T
3	C1, C52, C53	CAP, SMD, 0805, 2.2µF, 10V, 10%, X7R, ROHS	GRM21BR71A225KA01K-T
2	C23, C25	CAP, SMD, 1210, 0.22µF, 200V, 10%, X7R, ROHS	12102C224KAT2A-T
12	C37, C38, C39, C40, C41, C42, C44, C45, C46, C47, C48, C49	CAP, SMD, 2220, 1µF, 250V, 10%, X7R, ROHS	GRJ55DR72E105KWJ1
2	C43, C50	CAP-RADIAL, TH, 18mm DIA, 100μF, 160V, 20%, ROHS	EEU-EB2C101S
1	L1	COIL-FIXED, SMD, 10µH, 22A, 20%, AEC-Q200, ROHS	XAL1510-103MED-T
5	J5, J7, J8, J9, J10	CONN-COAXIAL, 1 INNER HOLE, POSITIVE PIN, $50\Omega$ , ROHS	BWSMA-KE-Z001
2	J13, J14	CONN-HEADER, TH, 2.54mm, 3P, ROHS	HTS-103-T-A
8	TP1, TP5, TP13, TP16, TP19, TP43, TP44, TP46	CONN-MINI TEST POINT, VERTICAL, YEL, ROHS	5004
4	TP22, TP23, TP24, TP25	CONN-MINI TEST PT, VERTICAL, BLK, ROHS	5001
2	D1, D2	DIODE-RECTIFIER, SMD, 2P, SOD-523, 40V, 30mA, ROHS	SDM03U40-7-T
1	D4	DIODE-SHOTTKY, SMD, 150V, 3.6A, TO-227A, ROHS	V10PM153HM3/H-T
1	U5	IC-1.024V LDO VOLTAGE REFERENCE, 3P, SOT23, ROHS	ISL21010DFH310Z
1	U4	IC-COMPARATOR, SMD, 5-TSSOP, SC-70-5, ROHS	MAX9140EXK+T-T
1	U2	IC-FET DRIVER, 5V, 7A, WSON6-2x2, SCTDFN, ROHS	RRP63175-NH0
2	U1, U3	IC-INVERTER, SMD, 2 INPUT, 1.65-5.5V, 6-TSSOP, ROHS	74LVC2G14GW, 125-T
1	AFFIX TO BACK OF PCB	LABEL-DATE CODE=LINE 1:YRWK-REV#, LINE 2;BOM NAME	LABEL-DATE CODE
4	TP39, TP40, TP41, TP42	PLUGIN, WELDING TERMINAL, ROHS	T44008
2	R3, R7	RES, SMD, 0603, 100Ω, 1/10W, 1%, TKF, ROHS	RC0603FR-07100RL-T
1	R17	RES, SMD, 0603, 10K, 1/10W, 1%, TKF, ROHS	RC0603FR-0710KL-T
1	R4	RES, SMD, 0603, 1Ω, 1/10W, 1%, TKF, ROHS	RC0603FR-071RL-T
1	R58	RES, SMD, 0603, 3.3K, 1/10W, 1%, TKF, ROHS	RC0603FR-073K3L-T
1	R14	RES, SMD, 0603, 330mΩ, 1/10W, 1%, TKF, ROHS	RL0603FR-070R33L-T
2	R6, R12	RES, SMD, 0603, 49.9Ω, 1/8W, 1%, TNF, ROHS	RNCP0603FTD49R9-T

Qty	Designator	Description	Part Number
1	R57	RES, SMD, 0603, 5.6K, 1/10W, 1%, TKF, ROHS	RC0603FR-135K6L-T
1	R56	RES, SMD, 0603, 510K, 1/10W, 1%, TKF, ROHS	RC0603FR-13510KL-T
2	R5, R9	RES-AEC-Q200, SMD, 0603, 0Ω, 1/2W, ME, ROHS	PA0603-R-070RL-T
4	4 CORNERS OF PCB	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, SS, ROHS	4-40X1/4-SCREW-SS
4	4 CORNERS OF PCB	STANDOFF, 4-40×3/4in, F/F, HEX, ALUMINUM, ROHS	4-40X3/4-STANDOFF-METAL
1	U6	TRANS-BJT, SMD, NPN, 15V, 500mA, 500MHz, SOT-23, ROHS	CMPT2369 TR PBFREE
1	Q3	TRANS-GAN, SMD, 7-QFN, N-CHAN, 150V, 80A, ROHS	EPC2305-T

### 2.2.3 Board Layout

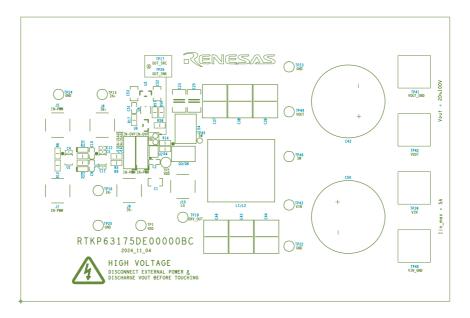


Figure 7. Silkscreen Top Layer

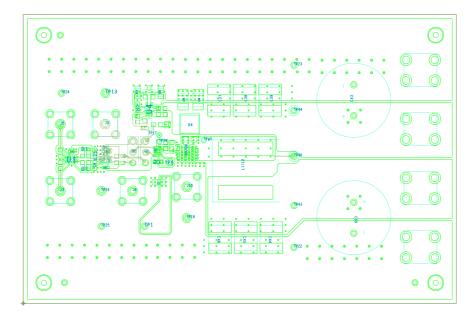


Figure 8. Layer 1

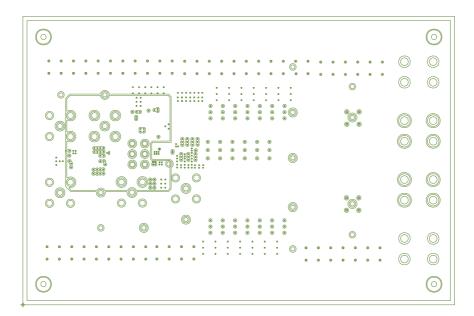


Figure 9. Layer 2

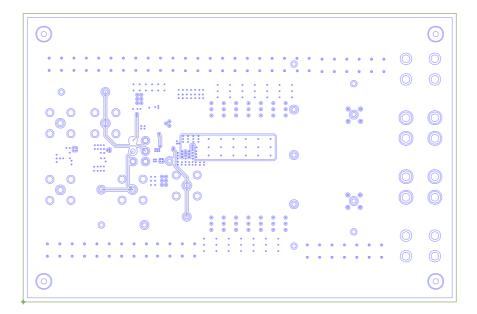


Figure 10. Layer 3

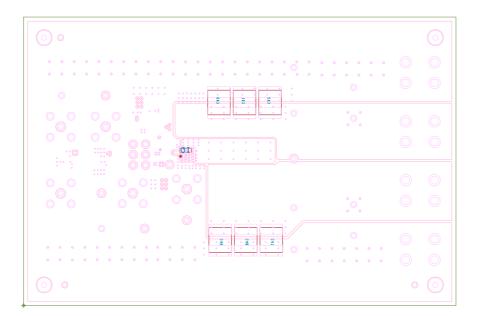


Figure 11. Layer 4

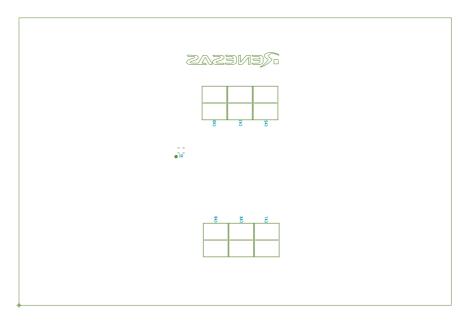


Figure 12. Silkscreen Bottom Layer

# 2.3 RTKP63175DE00010BC



Figure 13. RTKP63175DE00010BC Evaluation Board (Top)



Figure 14. RTKP63175DE00010BC Evaluation Board (Bottom)

#### 2.3.1 Schematic

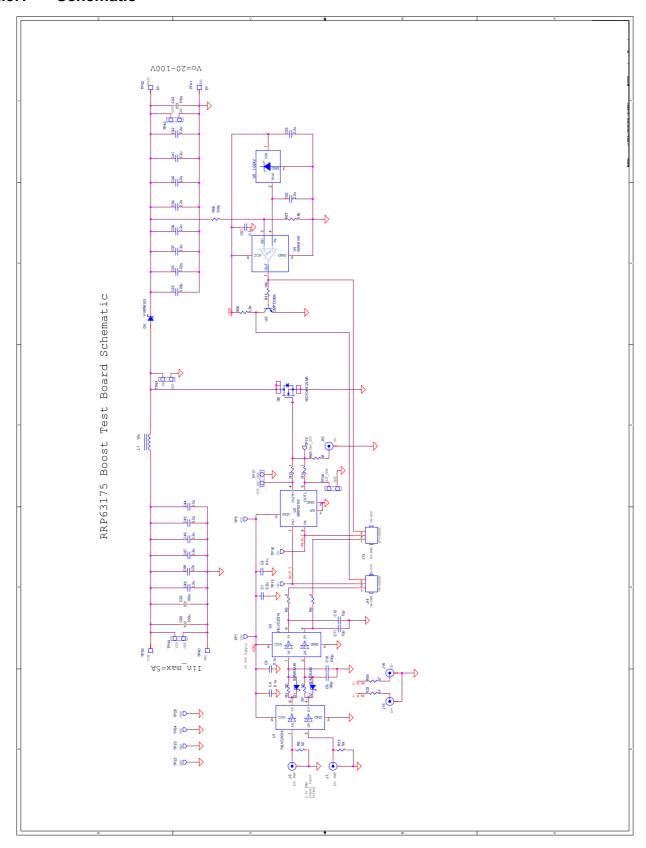


Figure 15. RTKP63175DE00010BC Schematic

## 2.3.2 Bill of Materials

#### Table 3. RTKP63175DE00010BC BOM

Qty	Designator	Description	Part Number
1	PCB	-	RTKP63175DE00010BCREVAPCB
1	PLACE ASSY IN BAG	BAG, STATIC, 5X8, ZIPLOC, ROHS	5X8-STATIC-BAG
2	C4, C5	CAP, SMD, 0402, 0.1uF, 16V, 10%, X7R, ROHS	GRM155R71C104KA88D-T
2	C11, C12	CAP, SMD, 0402, 10pF, 16V, 1%, RF, TNF, ROHS	0402YJ100FBSTR-T
2	C2, C51	CAP, SMD, 0603, 0.1uF, 16V, 10%, X7R, ROHS	CC0603KRX7R7BB104-T
2	C9, C10	CAP, SMD, 0603, 100pF, 16V, 5%, PPS, ROHS	ECH-U1C101JX5-T
3	C1, C52, C53	CAP, SMD, 0805, 2.2uF, 10V, 10%, X7R, ROHS	GRM21BR71A225KA01K-T
2	C23, C25	CAP, SMD, 1210, 0.22uF, 200V, 10%, X7R, ROHS	12102C224KAT2A-T
12	C37, C38, C39, C40, C41, C42, C44, C45, C46, C47, C48, C49	CAP, SMD, 2220, 1uF, 250V, 10%, X7R, ROHS	GRJ55DR72E105KWJ1
3	C33, C43, C50	CAP-ALUM, RADIAL, 100uF, 160v, 20%, ROHS	EEU-EB2C101SB
1	L1	COIL-FIXED, SMD, 10uH, 22A, 20%, AEC- Q200, ROHS	XAL1510-103MED-T
5	J5, J7, J10, J15, J16	CONN-COAXIAL, 1 INNER HOLE, POSITIVE PIN, $50\Omega$ , ROHS	BWSMA-KE-Z001
2	J13, J14	CONN-HEADER, TH, 2.54mm, 3P, ROHS	HTS-103-T-A
5	TP1, TP5, TP13, TP16, TP19	CONN-MINI TEST POINT, VERTICAL, YEL, ROHS	5004
4	TP22, TP23, TP24, TP25	CONN-MINI TEST PT, VERTICAL, BLK, ROHS	5001
2	D1, D2	DIODE-RECTIFIER, SMD, 2P, SOD-523, 40V, 30mA, ROHS	SDM03U40-7-T
1	D4	DIODE-SHOTTKY, SMD, 150V, 3.6A, TO-227A, ROHS	V10PM153HM3/H-T
1	U5	IC-1.024V LDO VOLTAGE REFERENCE, 3P, SOT23, ROHS	ISL21010DFH310Z
1	U4	IC-COMPARATOR, SMD, 5-TSSOP, SC-70-5, ROHS	MAX9140EXK+T-T
1	U2	IC-FET DRIVER, 5V, 7A, WSON6-2x2, SCTDFN, ROHS	RRP63175-NH0
2	U1, U3	IC-INVERTER, SMD, 2 INPUT, 1.65-5.5V, 6-TSSOP, ROHS	74LVC2G14GW, 125-T
1	AFFIX TO BACK OF PCB	LABEL-DATE CODE=LINE 1:YRWK-REV#, LINE 2;BOM NAME	LABEL-DATE CODE
4	TP39, TP40, TP41, TP42	PLUGIN, WELDING TERMINAL, ROHS	T44008
3	R23, R59, R60	RES, SMD, 0402, 47Ω, 1/16W, 1%, TKF, ROHS	RC0402FR-0747RL-T
2	R3, R7	RES, SMD, 0603, 100Ω, 1/10W, 1%, TKF, ROHS	RC0603FR-07100RL-T
1	R17	RES, SMD, 0603, 10K, 1/10W, 1%, TKF, ROHS	RC0603FR-0710KL-T
2	R13, R14	RES, SMD, 0603, 1Ω, 1/10W, 1%, TKF, ROHS	RC0603FR-071RL-T
1	R58	RES, SMD, 0603, 3.3K, 1/10W, 1%, TKF, ROHS	RC0603FR-073K3L-T
2	R6, R12	RES, SMD, 0603, 49.9Ω, 1/8W, 1%, TNF, ROHS	RNCP0603FTD49R9-T
1	R57	RES, SMD, 0603, 5.6K, 1/10W, 1%, TKF, ROHS	RC0603FR-135K6L-T

Table 3. RTKP63175DE00010BC BOM (Cont.)	KP63175DE00010BC BOM (Co	nt.)
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Qty	Designator	Description	Part Number
1	R56	RES, SMD, 0603, 510K, 1/10W, 1%, TKF, ROHS	RC0603FR-13510KL-T
2	R5, R9	RES-AEC-Q200, SMD, 0603, 0Ω, 1/2W, ME, ROHS	PA0603-R-070RL-T
4	4 CORNERS OF PCB	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, SS, ROHS	4-40X1/4-SCREW-SS
4	4 CORNERS OF PCB	STANDOFF, 4-40×3/4in, F/F, HEX, ALUMINUM, ROHS	4-40X3/4-STANDOFF-METAL
1	U6	TRANS-BJT, SMD, NPN, 15V, 500mA, 500MHz, SOT-23, ROHS	CMPT2369 TR PBFREE
1	Q6	TRANS-MOSFET, N-CHAN, SMD, 120V, 11A, 63A, ROHS	ISC104N12LM6ATMA1-T

# 2.3.3 Board Layout

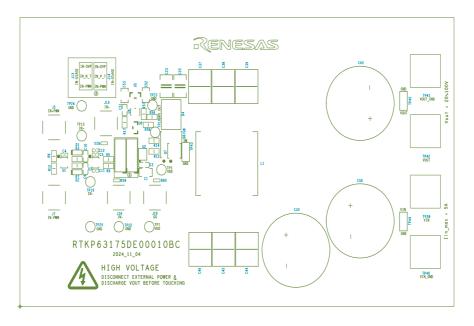


Figure 16. Silkscreen Top Layer

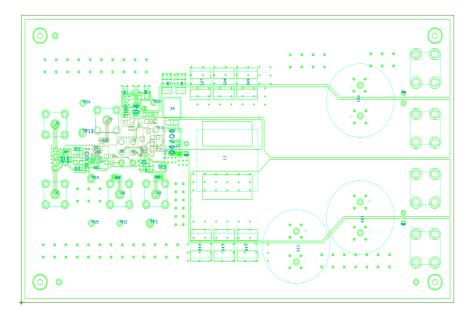


Figure 17. Layer 1

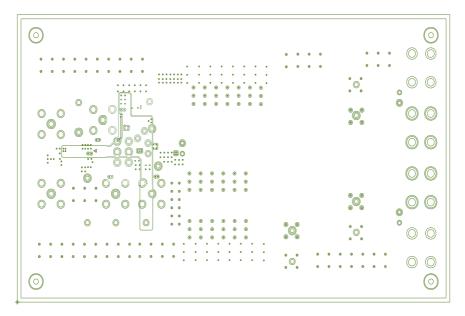


Figure 18. Layer 2

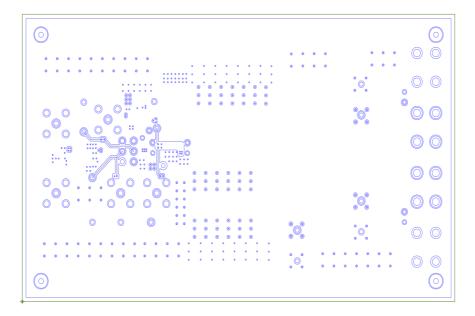


Figure 19. Layer 3

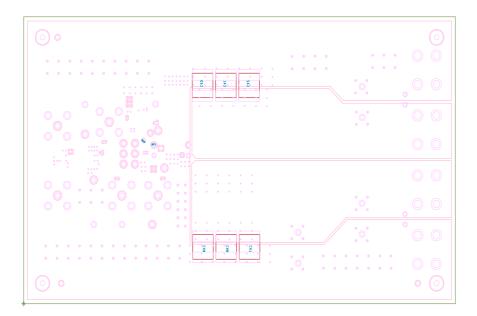


Figure 20. Layer 4

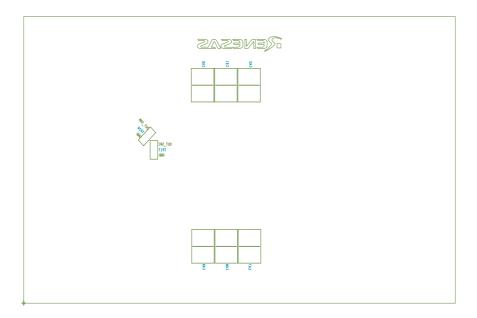


Figure 21. Silkscreen Bottom Layer

# 3. Design Reference

#### 3.1 Input, Output and Duty Cycle

Key parameters need to be determined before choosing components:

- VIN: input voltage (minimum, typical, maximum)
- VOUT: desired output voltage
- IIN: input current (maximum)
- IOUT: output current (maximum)

When the parameters above are decided, use Equation 1 to calculate the duty cycle (D).

(EQ. 1) 
$$D = 1 - V_{IN} / V_{OLIT}$$

#### 3.2 Switching Frequency and Switching Current

The switching frequency (f<sub>SW</sub>) is a crucial parameter, as it influences system efficiency and performance. An increased switching frequency can result in reduced efficiency.

It is also essential to consider the switching current when selecting power FETs and other components.

#### 3.3 Inductor Selection

Inductor selection is critical due to the unavoidable nature of inductor current ripple. A smaller inductor might lead to higher inductor ripple current, while opting for a larger inductor can result in slower load transients and reduced efficiency. Equation 2 can serve as a reference for inductor selection, with I<sub>ripple\_peak</sub> referring to the peak inductor ripple current.

(EQ. 2) 
$$L = \frac{D \times V_{IN}}{f_{SW} \times I_{ripple peak}}$$

# 3.4 Input Capacitor and Output Capacitor

Input and output capacitors play a vital role in stabilizing input and output voltages. Ceramic capacitors with low equivalent series resistance (ESR) are recommended. While larger output capacitors can effectively reduce output voltage ripple, they can also necessitate an increase in overall capacitor size. Equation 3 is provided as a reference for calculating the appropriate capacitor value, with V<sub>ripple\_peak</sub> referring to the peak output ripple voltage.

(EQ. 3) 
$$C_{OUT} = \frac{D \times I_{OUT}}{f_{SW} \times V_{ripple\_peak}}$$

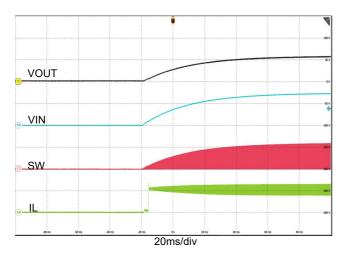
### 3.5 Other Components

It is essential to consider the voltage and current ratings of other key components, such as power FETs (MOSFETs or GaN FETs) and diodes. Ensure that these ratings encompass the peak voltage and current during operation.



# 4. Typical Performance Curves

VDD = 5V, VIN = 30V, PWM 0V to 3.3V 500kHz square wave 50% duty, load = 2.5A under room temperature *Note*: Tested with large load condition



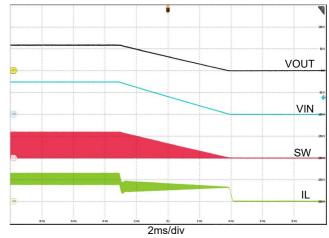
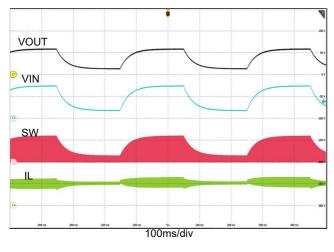


Figure 22. VIN Power Up

Figure 23. VIN Power Off



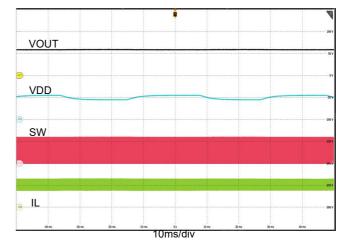
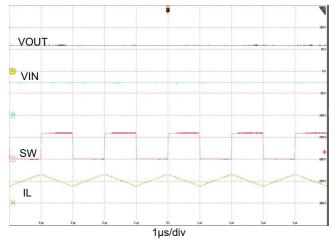


Figure 24. VIN Line Transient

Figure 25. VDD Line Transient



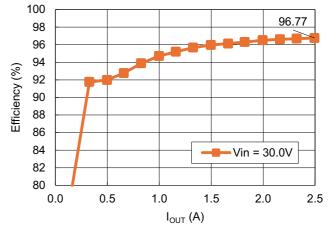


Figure 26. Steady State

Figure 27. Efficiency

# 5. Ordering Information

Part Number	Description
RTKP63175DE00000BC	RRP63175-NH0 6 Ld SCTDFN Evaluation Board, GaN FET Version
RTKP63175DE00010BC	RRP63175-NH0 6 Ld SCTDFN Evaluation Board, MOSFET Version

# 6. Revision History

Revision	Date	Description
1.00	Dec 2, 2024	Initial release

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