User's Manual

# RZ/G2L, RZ/V2L SMARC Module Board

## User's Manual: Hardware

## Renesas Microprocessor
## RZ Family / RZ/G, RZ/V Series

RTK9744L23C01000BE
RTK9754L23C01000BE



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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# Table of Contents

# 1. Overview

## 1.1 Overview

To begin with, only RZ/G2L SMARC Module Board will be explained here.

The difference between RZ/G2L SMARC Module Board (RTK9744L23C01000BE) and RZ/V2L SMARC Module Board (RTK9754L23C01000BE) is that RTK9754L23C01000BE uses Renesas Electronics microprocessor RZ/V2L "R9A07G054L23GBG", which is pin-compatible with RZ/G2L. In other words, they are functionally the same.

This document describes the specification of RTK9744L23C01000BE to evaluate the functions and performance of the Renesas Electronics microprocessor RZ/G2L "R9A07G044L23GBG" and evaluate application software programs.

The RTK9744L23C01000BE complies with the SMARC v2.1 and has following features.

- It is mounted with the following external memories.

  DDR4 SDRAM: 2GB × 1pc

  QSPI flash memory: 512Mb × 1pc

  eMMC memory: 64GB × 1pc
- The microSD card slot is implemented and used as an eSD for boot.
- It is implemented a 5-output clock generator "5P35023".
- It is implemented a PMIC "RAA215300" as power supply circuit.
- The Ethernet PHY is implemented as standard and can send/receive data at 10/100/1000Mbps.
- Terminals not used on this board are connected to the 314-pin 0.5-mm pitch connector, which can be used in conjunction with a Carrier Board. It also allows for the development of the Carrier Board that meet the needs of development.
- The 10-pin pin header for ARM Cortex Debug is implemented for connection to debug interface.
- The 10-pin pin header is implemented for connection to ADC interface.

## 1.2 Configuration

**Figure 1.1** shows an example of system configuration using RTK9744L23C01000BE.

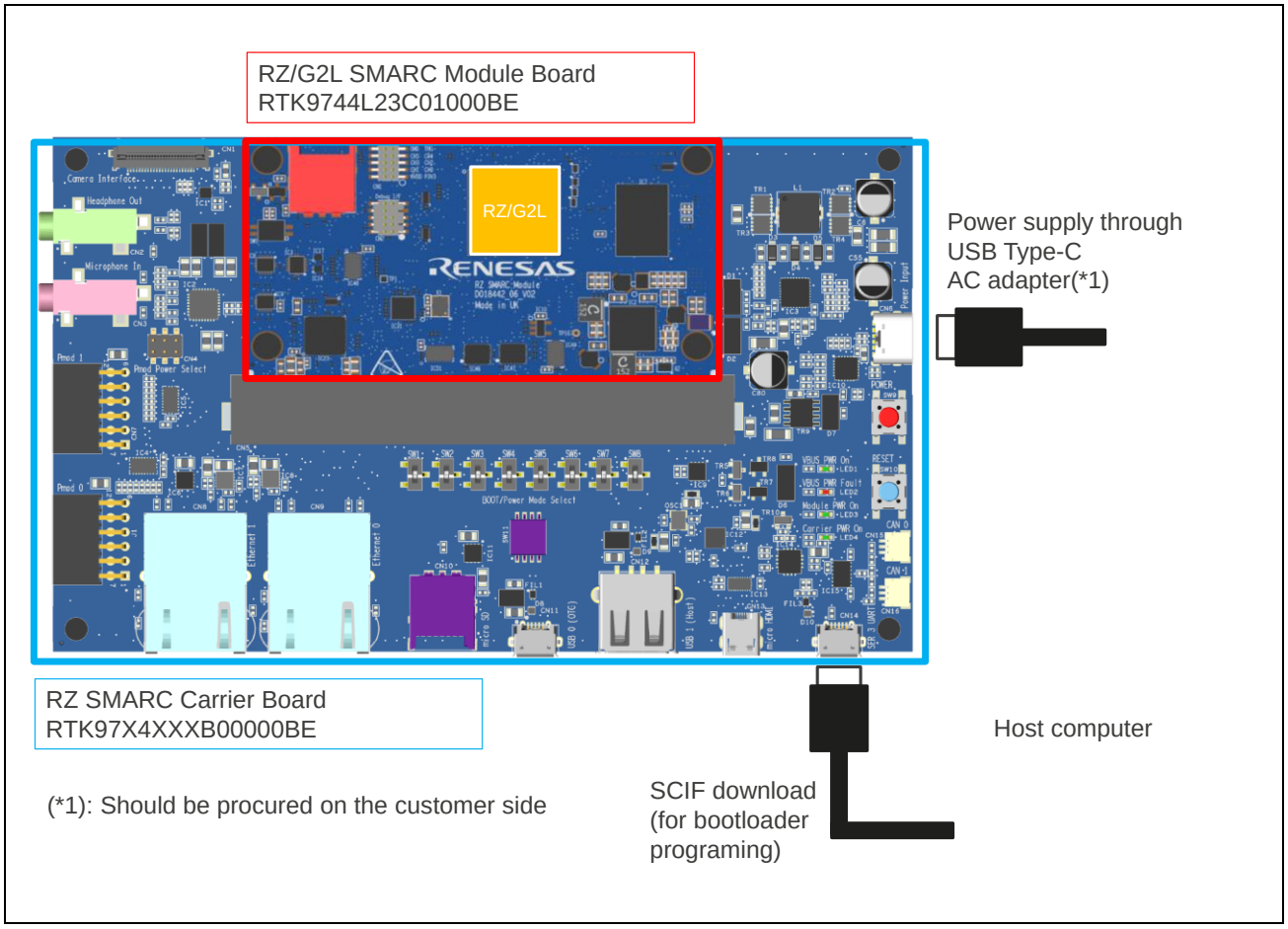



Figure 1.1 Example of System Configuration Using RTK9744L23C01000BE

## 1.3 Features

**Table 1.1** shows the features of the RTK9744L23C01000BE.

Table 1.1 Features of the RTK9744L23C01000BE

| Item | Details |
|---|---|
| CPU | RZ/G2L<br>Input (Xin) clock: 24MHz<br>Arm Cortex-A55 clock: 1.2GHz<br>Arm Cortex-M33 clock: 200MHz<br>AXI-bus clock: 200MHz<br>APB-bus clock: 100MHz<br>Internal memory<br>Instruction cache: 32KB<br>Data cache: 32KB<br>Power voltage: 1.1V, I/O: 3.3V<br>456-Pin PBGA 0.5-mm pitch |
| Memory | QSPI flash memory: 512Mbit * 1pc<br>DDR4 SDRAM: 2GB * 1pc<br>eMMC memory: 64GB * 1pc |
| Clock IC | Clock generator: 1pc |
| Ethernet IC | Ethernet PHY: 2pcs |
| Connector | microSD card slot (4 bits): 1pc<br>10-pin pin header for JTAG: 1pc<br>10-pin pin header for ADC: 1pc<br>SMARC edge connector (314 pins): 1pc |
| Switch | System setting DIP switch: 2 bits |
| Circuit board specifications | Dimensions: 82 mm * 50 mm<br>Mount: Double-sided mounting (6 layers) |

## 1.4 Physical View

**Figure 1.2** and **Figure 1.3** show the top and bottom views of the RTK9744L23C01000BE.


Figure 1.2 Top View of the RTK9744L23C01000BE


Figure 1.3 Bottom View of the RTK9744L23C01000BE

## 1.5 Block Diagram

**Figure 1.4** shows the block diagram of the RTK9744L23C01000BE.

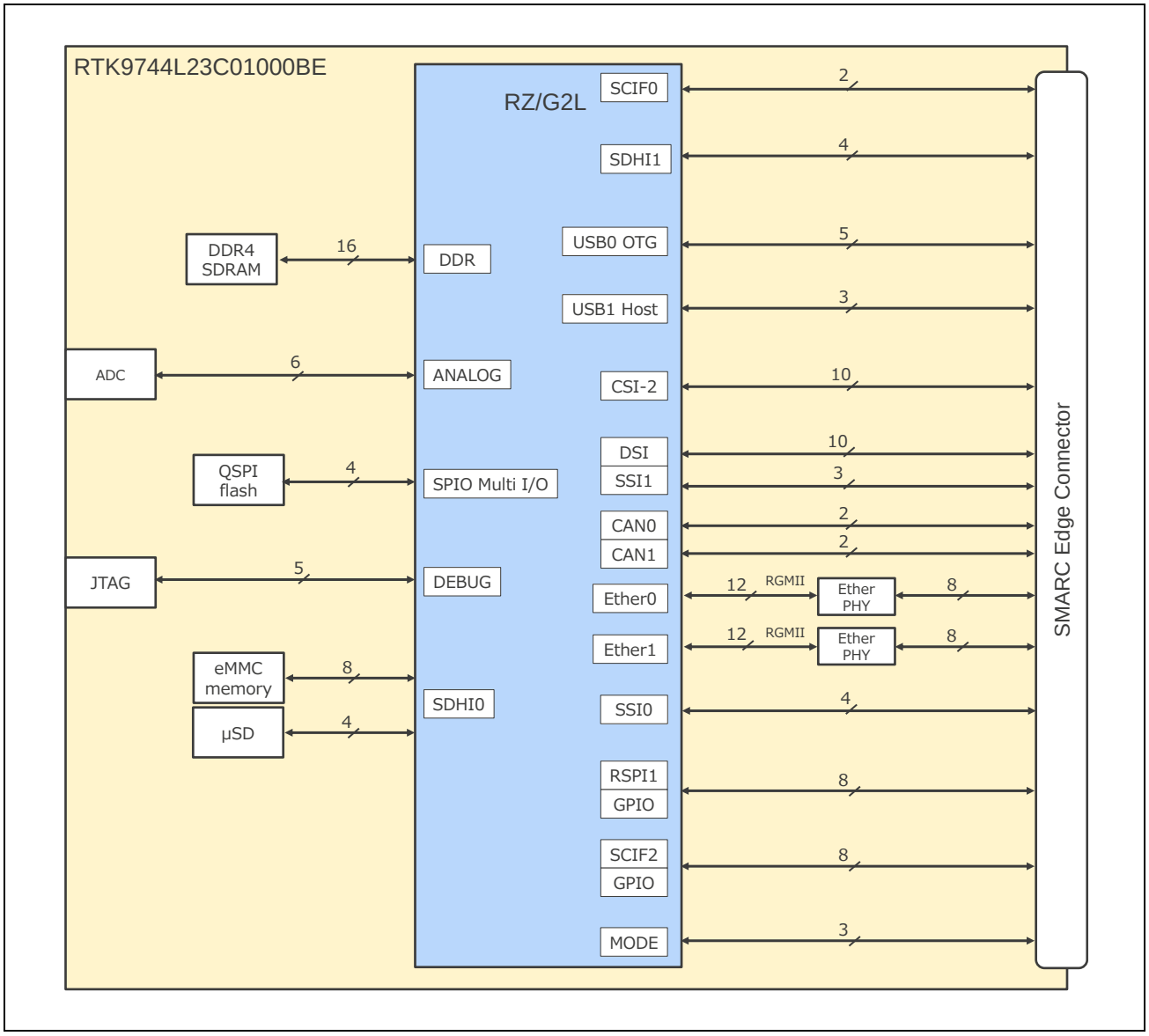



Figure 1.4 Block Diagram of the RTK9744L23C01000BE

## 1.6 Component Layout

**Figure 1.5** and **Figure 1.6** show the layout of main components of the RTK9744L23C01000BE.

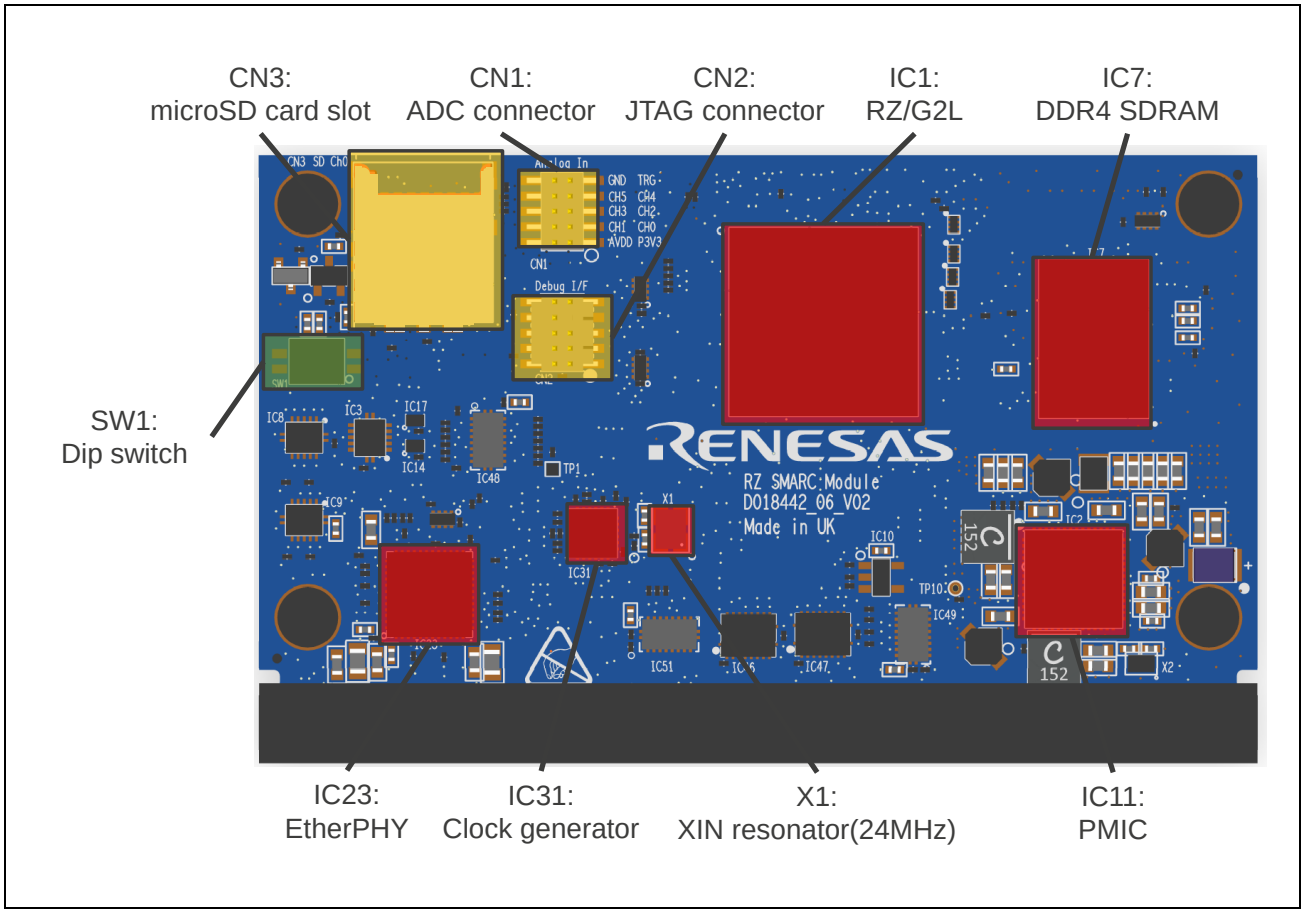



Figure 1.5 Layout of Components of the RTK9744L23C01000BE (Top View)

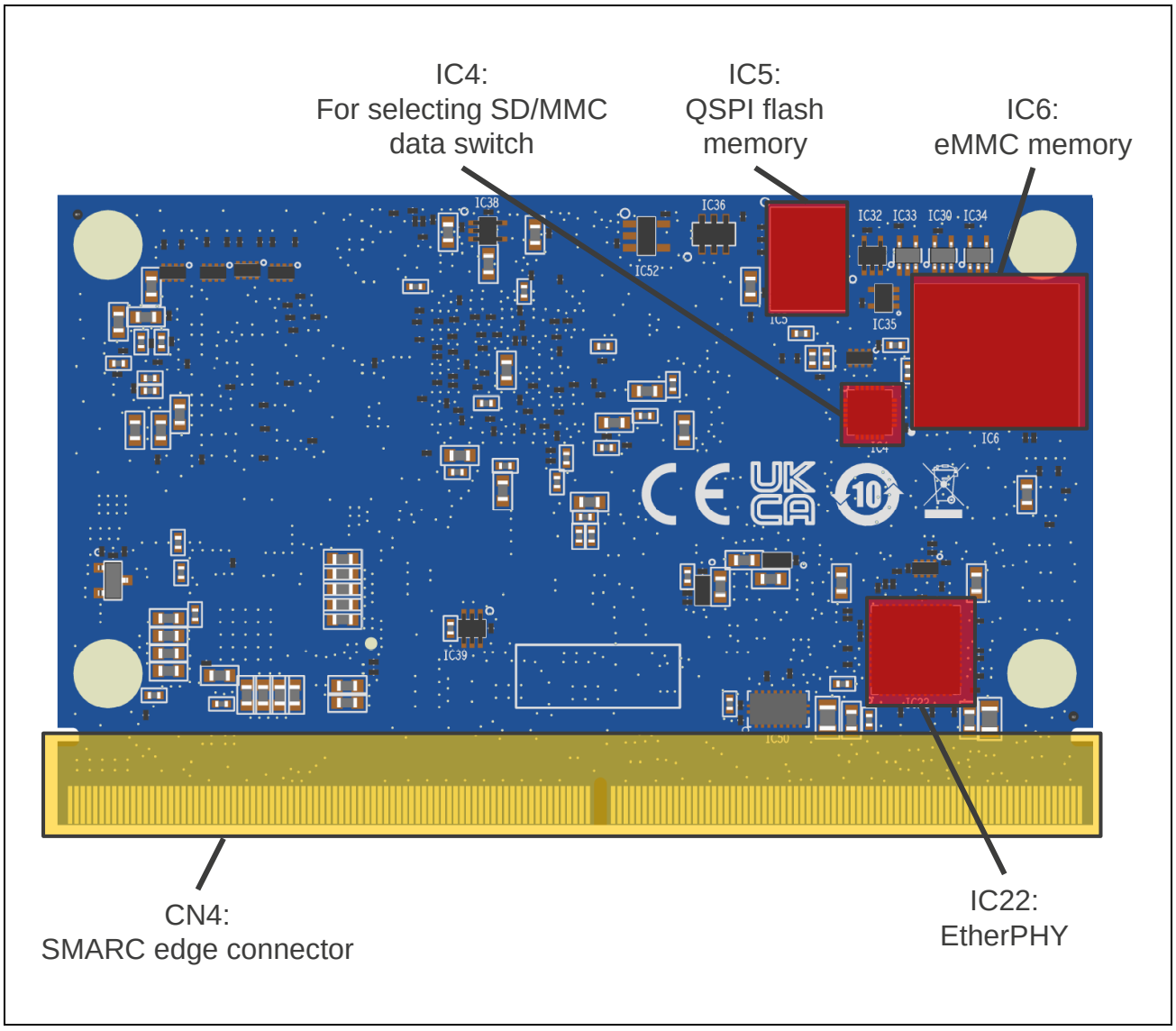



Figure 1.6 Layout of Components of the RTK9744L23C01000BE (Bottom View)

**Table 1.2** and **Table 1.3** list main components mounted on the RTK9744L23C01000BE.

Table 1.2 Main Components on the RTK9744L23C01000BE (1) IC

| Component Number | Component Name | Type (Manufacturer) |
|---|---|---|
| IC1 | MPU | R9A07G044L23GBG<br>(Renesas Electronics) |
| IC2 | PMIC | RAA215300A2GNP#HA0<br>(Renesas Electronics) |
| IC4 | Data switch IC | MAX4996LETG+<br>(MAXIM) |
| IC5 | QSPI flash memory | MT25QU512ABB8E12-0SIT<br>(Micron) |
| IC6 | eMMC memory | MTFC64GASAQHD-IT<br>(Micron) |
| IC7 | DDR4 SDRAM | MT40A1G16KD-062E:E<br>(Micron) |
| IC22 | Ethernet PHY | KSZ9131RNXC<br>(Microchip) |
| IC23 | Ethernet PHY | KSZ9131RNXC<br>(Microchip) |
| IC31 | Clock generator | 5P35023B-629NLGI<br>(Renesas Electronics) |
| X1 | Crystal resonator for XIN | FL2400022<br>(Diodes Inc) |

Table 1.3 Main Components on the RTK9744L23C01000BE (2) Connector

| Components Number | Component Name | Type (Manufacturer) |
|---|---|---|
| CN1 | ADC connector<br>(10pin) | FTSH-105-01-L-DV<br>(Samtec) |
| CN2 | JTAG connector<br>(10pin) | FTSH-105-01-F-DV-007-K<br>(Samtec) |
| CN3 | microSD card slot | 504077-1891<br>(Molex) |
| CN4 | SMARC edge connector<br>(314pin) | |

## 1.7 Absolute Maximum Ratings

**Table 1.4** lists absolute maximum ratings of the RTK9744L23C01000BE.

Table 1.4 Absolute Maximum Ratings of the RTK9744L23C01000BE

| Symbol | Item | Rated Value | Note |
|---|---|---|---|
| VDD_IN | power voltage | 5.25V | Reference: Vss |
| — | Maximum power consumption | 3A | Includes continuous RZ SMARC Series Carrier Board current consumption |
| Topr | Operating ambient temperature*1 | 0°C to 50°C | Do not expose to condensation or corrosive gases |
| Tstg | Storage temperature*1 | -10°C to 60°C | Do not expose to condensation or corrosive gases |

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

## 1.8 Operating Condition

**Table 1.5** lists operating conditions of the RTK9744L23C01000BE.

Table 1.5 Operating Conditions of the RTK9744L23C01000BE

| Symbol | Item | Rated Value | Note |
|---|---|---|---|
| VDD_IN | Power volotage | 3.0V to 5.25V | Reference: Smarc v2.1 specification |
| Topr | Operating ambient temperature*1 | 0°C to 40°C | Do not expose to condensation or corrosive gases |

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

# 2. Functional Specifications

## 2.1 Overview of Functions

**Table 2.1** lists function modules of the RTK9744L23C01000BE.

Table 2.1 Function Modules of the RTK9744L23C01000BE

| Section | Function | Description |
|---|---|---|
| **2.2** | **MPU** | RZ/G2L<br>Input (Xin) clock: 24MHz<br>Arm Cortex-A55 clock: 1.2GHz<br>Arm Cortex-M33 clock: 200MHz<br>AXI-bus clock: 200MHz<br>APB-bus clock: 100MHz |
| **2.3** | **Memory** | QSPI flash memory: 512Mbit * 1pc<br>DDR4 SDRAM: 2GB * 1pc<br>eMMC memory: 64GB * 1pc |
| **2.4** | **Gigabit Ethernet Interface** | Connection between the Ethernet controller (E-MAC) and LAN connector via Ethernet PHY |
| **2.5** | **ADC Interface** | Connection between ADC module and connector |
| **2.6** | **Clock Configuration** | System clock configuration |
| **2.7** | **Reset Control** | Reset control for RZ/G2L mounted on the RTK9744L23C01000BE. |
| **2.8** | **Power Supply Configuration** | System power supply configuration of the RTK9744L23C01000BE and RTK97X4XXXB00000BE |
| **2.9** | **PMIC** | Connection between RZ/G2L and PMIC |
| **2.10** | **Debug Interface** | Connection between Debug Interface and connector |
| **2.11** | **SD/MMC Host Interface** | Connection between SD/MMC Host Interface (SDHI) channel 0 and microSD card slot |
| — | Operating specification | Connectors and switches<br>Details are described in Chapter 3 |

# 2.2 MPU

## 2.2.1 Overview of RZ/G2L

RTK9744L23C01000BE contains a 64-bit microprocessor RZ/G2L that runs in synchronization with the CPU clock (max.1.2 GHz).

## 2.2.2 List of Pin Functions

**Table 2.2** lists pin functions used in RTK9744L23C01000BE.

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (1/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| G12 | VDD18 | VDD18 | 1.8V | — | — |
| B11 | ABG_NCP_OUT | ABG_NCP_OUT | Connected to GND via the 1uF bypass capacitor (*1) | — | — |
| E22 | ADC_AVDD18 | ADC_AVDD18 | 1.8V | — | — |
| A28 | ADC_CH0 | ADC_CH0 | Pin header CN1 for ADC input | — | — |
| B27 | ADC_CH1 | ADC_CH1 | Pin header CN1 for ADC input | — | — |
| B28 | ADC_CH2 | ADC_CH2 | Pin header CN1 for ADC input | — | — |
| A27 | ADC_CH3 | ADC_CH3 | Pin header CN1 for ADC input | — | — |
| C26 | ADC_CH4 | ADC_CH4 | Pin header CN1 for ADC input | — | — |
| B26 | ADC_CH5 | ADC_CH5 | Pin header CN1 for ADC input | — | — |
| A26 | ADC_CH6 | ADC_CH6 | Connected to GND (*1) | — | — |
| B25 | ADC_CH7 | ADC_CH7 | Connected to GND (*1) | — | — |
| E12 | AUDIO_CLK1 | AUDIO_CLK1 | Input 11.2896MHz from 5P35023 for generating the CD sampling rate (44.1kHz) | — | — |
| B8 | AUDIO_CLK2 | AUDIO_CLK2 | Input 12.2880MHz from 5P35023 for generating the DVD sampling rate (48.0kHz) | — | — |
| AB23 | BSCANP | BSCANP | Initial setting: 0 (Pull down), should be controllable by resistor. | — | — |
| AB24 | VSS | VSS | GND | — | — |
| AG12 | CSI_CLKN | CSI_CLKN | 24-pin FFC connector on the carrier board | P4 | CSI1_CLK- |
| AG13 | CSI_CLKP | CSI_CLKP | 24-pin FFC connector on the carrier board | P3 | CSI1_CLK+ |
| AH13 | CSI_DATA0_N | CSI_DATA0_N | 24-pin FFC connector on the carrier board | P8 | CSI1_RX0- |
| AJ13 | CSI_DATA0_P | CSI_DATA0_P | 24-pin FFC connector on the carrier board | P7 | CSI1_RX0+ |
| AH12 | CSI_DATA1_N | CSI_DATA1_N | 24-pin FFC connector on the carrier board | P11 | CSI1_RX1- |
| AJ12 | CSI_DATA1_P | CSI_DATA1_P | 24-pin FFC connector on the carrier board | P10 | CSI1_RX1+ |
| AH14 | CSI_DATA2_N | CSI_DATA2_N | 24-pin FFC connector on the carrier board | P14 | CSI1_RX2- |
| AJ14 | CSI_DATA2_P | CSI_DATA2_P | 24-pin FFC connector on the carrier board | P13 | CSI1_RX2+ |
| AH11 | CSI_DATA3_N | CSI_DATA3_N | 24-pin FFC connector on the carrier board | P17 | CSI1_RX3- |
| AJ11 | CSI_DATA3_P | CSI_DATA3_P | 24-pin FFC connector on the carrier board | P16 | CSI1_RX3+ |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (2/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AD12 | CSI_VDD18 | CSI_VDD18 | 1.8V | — | — |
| AD13 | CSI_VDD18 | CSI_VDD18 | 1.8V | — | — |
| G29 | DDR_ADDR0 | DDR_ADDR0 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| M27 | DDR_ADDR1 | DDR_ADDR1 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| R29 | DDR_ADDR10 | DDR_ADDR10 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| K28 | DDR_ADDR11 | DDR_ADDR11 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| P29 | DDR_ADDR12 | DDR_ADDR12 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| E29 | DDR_ADDR13 | DDR_ADDR13 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| H29 | DDR_ADDR14 | DDR_ADDR14 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| G27 | DDR_ADDR15 | DDR_ADDR15 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| F28 | DDR_ADDR2 | DDR_ADDR2 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| F29 | DDR_ADDR3 | DDR_ADDR3 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| L29 | DDR_ADDR4 | DDR_ADDR4 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| D29 | DDR_ADDR5 | DDR_ADDR5 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| L28 | DDR_ADDR6 | DDR_ADDR6 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| C28 | DDR_ADDR7 | DDR_ADDR7 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| H28 | DDR_ADDR8 | DDR_ADDR8 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| E28 | DDR_ADDR9 | DDR_ADDR9 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| H27 | DDR_BA0 | DDR_BA0 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| M28 | DDR_BA1 | DDR_BA1 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| G28 | DDR_BA2 | DDR_BA2 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| C29 | DDR_CALIBRATION | DDR_CALIBRATION | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| K29 | DDR_CAS# | DDR_CAS# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| N28 | DDR_CKE | DDR_CKE | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| T28 | DDR_CLK_N | DDR_CLK_N | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| T29 | DDR_CLK_P | DDR_CLK_P | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| P28 | DDR_CS0# | DDR_CS0# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| M29 | DDR_CS1# | DDR_CS1# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| W29 | DDR_DM0 | DDR_DM0 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AC29 | DDR_DM1 | DDR_DM1 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| V28 | DDR_DQ0 | DDR_DQ0 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AB29 | DDR_DQ1 | DDR_DQ1 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AC28 | DDR_DQ10 | DDR_DQ10 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AE29 | DDR_DQ11 | DDR_DQ11 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AH29 | DDR_DQ12 | DDR_DQ12 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AE28 | DDR_DQ13 | DDR_DQ13 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AF29 | DDR_DQ14 | DDR_DQ14 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AG29 | DDR_DQ15 | DDR_DQ15 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| U28 | DDR_DQ2 | DDR_DQ2 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AB28 | DDR_DQ3 | DDR_DQ3 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| V27 | DDR_DQ4 | DDR_DQ4 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| W28 | DDR_DQ5 | DDR_DQ5 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| U27 | DDR_DQ6 | DDR_DQ6 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (3/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| V29 | DDR_DQ7 | DDR_DQ7 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AF28 | DDR_DQ8 | DDR_DQ8 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AD29 | DDR_DQ9 | DDR_DQ9 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| Y28 | DDR_DQS0_N | DDR_DQS0_N | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AA29 | DDR_DQS0_P | DDR_DQS0_P | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AC27 | DDR_DQS1_N | DDR_DQS1_N | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AC26 | DDR_DQS1_P | DDR_DQS1_P | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| N29 | DDR_ODT0 | DDR_ODT0 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| N27 | DDR_ODT1 | DDR_ODT1 | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| J29 | DDR_RAS# | DDR_RAS# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| B29 | DDR_RESET# | DDR_RESET# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| H25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| M25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| N25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| U25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| V25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| AA25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| AB25 | DDR_VDDQ | DDR_VDDQ | 1.2V | — | — |
| J28 | DDR_WE# | DDR_WE# | DDR4 SDRAM (MT40A1G16KD-062E:E) | — | — |
| AE18 | DEBUGEN | DEBUGEN | DIP_SW (SW1) | — | — |
| AG18 | DSI_CLKN | DSI_CLKN | MIPI DSI to HDMI conversion IC on the carrier board | S135 | DSI0_CLK- |
| AG17 | DSI_CLKP | DSI_CLKP | MIPI DSI to HDMI conversion IC on the carrier board | S134 | DSI0_CLK+ |
| AJ16 | DSI_DATA0_N | DSI_DATA0_N | MIPI DSI to HDMI conversion IC on the carrier board | S126 | DSI0_D0- |
| AH16 | DSI_DATA0_P | DSI_DATA0_P | MIPI DSI to HDMI conversion IC on the carrier board | S125 | DSI0_D0+ |
| AJ17 | DSI_DATA1_N | DSI_DATA1_N | MIPI DSI to HDMI conversion IC on the carrier board | S129 | DSI0_D1- |
| AH17 | DSI_DATA1_P | DSI_DATA1_P | MIPI DSI to HDMI conversion IC on the carrier board | S128 | DSI0_D1+ |
| AJ15 | DSI_DATA2_N | DSI_DATA2_N | MIPI DSI to HDMI conversion IC on the carrier board | S132 | DSI0_D2- |
| AH15 | DSI_DATA2_P | DSI_DATA2_P | MIPI DSI to HDMI conversion IC on the carrier board | S131 | DSI0_D2+ |
| AJ18 | DSI_DATA3_N | DSI_DATA3_N | MIPI DSI to HDMI conversion IC on the carrier board | S138 | DSI0_D3- |
| AH18 | DSI_DATA3_P | DSI_DATA3_P | MIPI DSI to HDMI conversion IC on the carrier board | S137 | DSI0_D3+ |
| AC17 | DSI_VDD18 | DSI_VDD18 | 1.8V | — | — |
| AC18 | DSI_VDD18 | DSI_VDD18 | 1.8V | — | — |
| N6 | PVDD182533_0 | PVDD182533_0 | 1.8V | — | — |
| U7 | PVDD182533_1 | PVDD182533_1 | 1.8V | — | — |
| AG2 | EXCLK | EXCLK | Input 24MHz from 5P35023 for generating system clock | — | — |
| V7 | VDD18 | VDD18 | 1.8V | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (4/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| E8 | MD_BOOT0 | MD_BOOT0 | Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states | P123, P124, P125 | BOOT_SEL 0#,1#,2# |
| E7 | MD_BOOT1 | MD_BOOT1 | Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states | P123, P124, P125 | BOOT_SEL 0#,1#,2# |
| G7 | MD_BOOT2 | MD_BOOT2 | Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states | P123, P124, P125 | BOOT_SEL 0#,1#,2# |
| D23 | MD_CLKS | MD_CLKS | Initial setting: 1 (Pull Up), should be controllable by resistor. | — | — |
| E23 | MD_OSCDRV0 | MD_OSCDRV0 | Initial setting: 0 (Pull Down), should be controllable by resistor. | — | — |
| D27 | MD_OSCDRV1 | MD_OSCDRV1 | Initial setting: 0 (Pull Down), should be controllable by resistor. | — | — |
| AJ2 | NMI | NMI | Connected to the test pin (TP1) | — | — |
| G17 | OTP_VDD18 | OTP_VDD18 | 1.8V | — | — |
| A11 | P0_0/IRQ0/SCI0_RXD/GTIOC0A/MTIOC0A/SCIF3_TXD | P0_0 | For selecting the device connected to the SD/MMC ch0 interface<br>Input SD0_DEV_SEL signal to identify the device connected to the SD ch0 interface by software | — | — |
| B12 | P0_1/IRQ1/SCI0_TXD/GTIOC0B/MTIOC0B/SCIF3_RXD | IRQ1 | Unused | — | — |
| C13 | P1_0/IRQ2/SCI0_SCK/GTIOC1A/MTIOC0C/SCIF3_SCK | IRQ2 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| A12 | P1_1/IRQ3/SCI0_CTS_N_RTS_N/GTIOC1B/MTIOC0D | IRQ3 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AJ22 | P10_0/DISP_DATA6/CAN_CLK/MTIOC6A/GTETRGA | P10_0 | Unused | — | — |
| AH22 | P10_1/DISP_DATA7/CAN0_TX/MTIOC6B/GTETRGB | CAN0_TX | CAN transceiver ch0 (*2) on the carrier board (*2) | P143 | CAN0_TX |
| AG22 | P11_0/DISP_DATA8/CAN0_RX/MTIOC6C/GTETRGC | CAN0_RX | CAN transceiver ch0 (*2) on the carrier board (*2) | P144 | CAN0_RX |
| AF22 | P11_1/DISP_DATA9/CAN0_TX_DATARATE_EN/MTIOC6D/GTETRGD | P11_1 | Unused | — | — |
| AE22 | P12_0/DISP_DATA10/CAN0_RX_DATARATE_EN/POE0_N/GTIOC7A | P12_0 | Unused | — | — |
| AE23 | P12_1/DISP_DATA11/CAN1_TX/POE4_N/GTIOC7B | CAN1_TX | CAN transceiver ch1 (*2) on the carrier board (*2) | P145 | CAN1_TX |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (5/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AF23 | P13_0/DISP_DATA12/CAN1_RX/POE8_N/IRQ0 | CAN1_RX | CAN transceiver ch1 (*2) on the carrier board (*2) | P146 | CAN1_RX |
| AG23 | P13_1/DISP_DATA13/CAN1_TX_DATARATE_EN/POE10_N/IRQ1 | P13_1 | Unused | — | — |
| AG26 | P13_2/DISP_DATA14/CAN1_RX_DATARATE_EN/IRQ7/IRQ2 | P13_2 | Unused | — | — |
| AF27 | P14_0/DISP_DATA15/SSI1_BCK/SD1_CD/MTCLKA | P14_0 | Unused | — | — |
| AJ23 | P14_1/DISP_DATA16/SSI1_RCK/SD1_WP/MTCLKB | P14_1 | Unused | — | — |
| AH23 | P15_0/DISP_DATA17/SSI1_TXD/GTIOC4A/MTCLKC | P15_0 | Unused | — | — |
| AJ24 | P15_1/DISP_DATA18/SSI1_RXD/GTIOC4B/MTCLKD | P15_1 | Unused | — | — |
| AH24 | P16_0/DISP_DATA19/SCIF2_TXD/GTIOC5A/IRQ3 | P16_0 | RAA215300 | — | — |
| AJ25 | P16_1/DISP_DATA20/SCIF2_RXD/GTIOC5B/IRQ4 | P16_1 | RAA215300 | — | — |
| AH25 | P17_0/DISP_DATA21/SCIF2_SCK/GTIOC6A/IRQ5 | P17_0 | Unused | — | — |
| AJ26 | P17_1/DISP_DATA22/SCIF2_CTS/GTIOC6B/IRQ6 | P17_1 | Unused | — | — |
| AH26 | P17_2/DISP_DATA23/SCIF2_RTS/IRQ7 | P17_2 | Unused | — | — |
| C2 | P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A | RIIC3_SDA | RAA215300 and 5P35023<br>PMOD1 Type-6A and audio codec on the carrier board | S49 | I2C_GP_DAT |
| D3 | P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B | RIIC3_SCL | RAA215300 and 5P35023<br>PMOD1 Type-6A and audio codec on the carrier board | S48 | I2C_GP_CK |
| B1 | P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA | SD1_CD | uSD ch1 card slot on the carrier board | P35 | SDIO_CD# |
| B2 | P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL | P19_1 | Unused | P33 | SDIO_WP |
| B13 | P2_0/IRQ4/ADC_TRG/GTIOC2A/MTIOC1A/SCIF4_TXD | P2_0 | 24-pin FFC connector on the carrier board | P109 | GPIO1/CAM1_PWR# |
| A13 | P2_1/IRQ5/GTIOC2B/MTIOC1B/SCIF4_RXD | IRQ5 | MIPI-DSI to HDMI conversion IC on the carrier board | P110 | GPIO2/CAM0_RST# |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (6/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| N1 | P20_0/ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK | ET0_TXC_TX_CLK | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| N2 | P20_1/ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX | ET0_TX_CTL_TX_EN | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| M1 | P20_2/ET0_TXD0/RSPI0_MISO/CAN0_RX | ET0_TXD0 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| M2 | P21_0/ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN | ET0_TXD1 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| L1 | P21_1/ET0_TXD2/CAN0_RX_DATARATE_EN | ET0_TXD2 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| L2 | P22_0/ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA | ET0_TXD3 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| M3 | P22_1/ET0_TX_ERR/SSI0_RCK/CAN1_RX/MTCLKB | ET0_TX_ERR | Unused | — | — |
| N4 | P23_0/ET0_TX_COL/SSI0_TXD/CAN1_TX_DATARATE_EN/MTCLKC | ET0_TX_COL | Unused | — | — |
| M4 | P23_1/ET0_TX_CRS/SSI0_RXD/CAN1_RX_DATARATE_EN/MTCLKD | ET0_TX_CRS | Unused | — | — |
| P2 | P24_0/ET0_RXC_RX_CLK/SSI1_BCK/POE0_N | ET0_RXC_RX_CLK | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| P1 | P24_1/ET0_RX_CTL_RX_DV/SSI1_RCK/POE4_N | ET0_RX_CTL_RX_DV | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| R2 | P25_0/ET0_RXD0/SSI1_TXD/POE8_N | ET0_RXD0 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| R1 | P25_1/ET0_RXD1/SSI1_RXD/POE10_N | ET0_RXD1 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| T2 | P26_0/ET0_RXD2/RSPI1_CK/MTIOC8A | ET0_RXD2 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| T1 | P26_1/ET0_RXD3/RSPI1_MOSI/MTIOC8B | ET0_RXD3 | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| N3 | P27_0/ET0_RX_ERR/RSPI1_MISO/MTIOC8C | ET0_RX_ERR | Unused | — | — |
| U2 | P27_1/ET0_MDC/RSPI1_SSL/MTIOC8D | ET0_MDC | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| U1 | P28_0/ET0_MDIO | ET0_MDIO | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| R3 | P28_1/ET0_LINKSTA | ET0_LINKSTA | Ethernet0 PHY (KSZ9131RNXC) | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (7/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AB2 | P29_0/ET1_TXC_TX_CLK/CAM_PCLK/USB1_VBUSEN/SSI2_BCK | ET1_TXC_TX_CLK | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| Y1 | P29_1/ET1_TX_CTL_TX_EN/CAM_HREF/USB1_OVRCUR/SSI2_RCK | ET1_TX_CTL_TX_EN | Ethernet0 PHY (KSZ9131RNXC) | — | — |
| A14 | P3_0/IRQ6/RIIC2_SDA/GTIOC3A/MTIOC2A/SCIF4_SCK | P3_0/IRQ6 | Unused | P108 | GPIO0/CAM0_PWR# |
| B14 | P3_1/IRQ7/RIIC2_SCL/GTIOC3B/MTIOC2B/CAM_FIELD | P3_1/IRQ7 | PMOD1 Type-3A on the carrier board | P118 | GPIO10 |
| AB1 | P30_0/ET1_TXD0/CAM_VSYNC/SSI2_DATA | ET1_TXD0 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AA2 | P30_1/ET1_TXD1/CAM_DATA15 | ET1_TXD1 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AA1 | P31_0/ET1_TXD2/CAM_DATA0/SCI1_RXD/SSI3_BCK | ET1_TXD2 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| Y2 | P31_1/ET1_TXD3/CAM_DATA1/SCI1_TXD/SSI3_RCK | ET1_TXD3 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| U3 | P32_0/ET1_TX_ERR/CAM_DATA2/SCI1_SCK/MTIOC3A/SSI3_TXD | ET1_TX_ERR | Unused | — | — |
| V4 | P32_1/ET1_TX_COL/CAM_DATA3/SCI1_CTS_N_RTS_N/MTIOC3B/SSI3_RXD | ET1_TX_COL | Unused | — | — |
| U4 | P33_0/ET1_TX_CRS/CAM_DATA4/GTIOC2A/SCIF2_TXD/GTIOC0A | ET1_TX_CRS | Unused | — | — |
| AC1 | P33_1/ET1_RXC_RX_CLK/CAM_DATA5/GTIOC2B/SCIF2_RXD/GTIOC0B | ET1_RXC_RX_CLK | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AC2 | P34_0/ET1_RX_CTL_RX_DV/CAM_DATA6/GTIOC3A/MTIOC0A/GTIOC1A | ET1_RX_CTL_RX_DV | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AC3 | P34_1/ET1_RXD0/CAM_DATA7/GTIOC3B/MTIOC0B/GTIOC1B | ET1_RXD0 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AC4 | P35_0/ET1_RXD1/CAM_DATA8/SSI0_BCK/MTIOC0C/GTIOC2A | ET1_RXD1 | Ethernet1 PHY (KSZ9131RNXC) | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (8/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AB4 | P35_1/ET1_RXD2/CAM_DATA9/SSI0_RCK/MTIOC0D/GTIOC2B | ET1_RXD2 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| AB3 | P36_0/ET1_RXD3/CAM_DATA10/SSI0_TXD/MTIOC3C/GTETRGA | ET1_RXD3 | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| V3 | P36_1/ET1_RX_ERR/CAM_DATA11/SSI0_RXD/MTIOC3D/GTETRGB | ET1_RX_ERR | Unused | — | — |
| W2 | P37_0/ET1_MDC/CAM_DATA12/SCIF2_SCK/GTETRGC | ET1_MDC | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| W1 | P37_1/ET1_MDIO/CAM_DATA13/SCIF2_CTS/GTETRGD | ET1_MDIO | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| V2 | P37_2/ET1_LINKSTA/CAM_DATA14/SCIF2_RTS | ET1_LINKSTA | Ethernet1 PHY (KSZ9131RNXC) | — | — |
| A15 | P38_0/SCIF0_TXD/GTETRGA/CAN_CLK/MTIOC4A/USB1_VBUSEN | SCIF0_TXD | Debug UART on the carrier board | P140 | SER3_TX |
| B15 | P38_1/SCIF0_RXD/GTETRGB/CAN0_TX/MTIOC4B/USB1_OVRCUR | SCIF0_RXD | Debug UART on the carrier board | P141 | SER3_RX |
| A16 | P39_0/SCIF0_SCK/GTETRGC/CAN0_RX/MTIOC4C | P39_0 | For selecting voltage of the uSD ch0 card | — | — |
| C15 | P39_1/SCIF0_CTS/GTETRGD/CAN0_TX_DATARATE_EN/MTIOC4D | P39_1 | RAA215300<br>For selecting voltage of the uSD ch1 card on the carrier board | — | — |
| B16 | P39_2/SCIF0_RTS/CAN0_RX_DATARATE_EN | P39_2 | uSD ch1 card slot on the carrier board<br>For controlling power on/off of the card slot | P37 | SDIO_PWR_EN |
| AJ5 | P4_0/USB0_VBUSEN/SCIF2_TXD/MTIOC7A/ADC_TRG | USB0_VBUSEN | USB2.0 OTG on the carrier board<br>Include gate USB0_VBUSEN state | P62 | USB0_EN_OC# |
| AH6 | P4_1/SCIF2_RXD/MTIOC7B | P4_1 | uSD ch0 card slot<br>For controlling power on/off of the card slot | P108 | — |
| C17 | P40_0/SCIF1_TXD/GTIOC6A/CAN1_TX/MTIC5U/SCI0_RXD | SCIF1_TXD | Unused | P134 | SER1_TX |
| B17 | P40_1/SCIF1_RXD/GTIOC6B/CAN1_RX/MTIC5V/SCI0_TXD | SCIF1_RXD | Unused | P135 | SER1_RX |
| A17 | P40_2/SCIF1_SCK/CAN1_TX_DATARATE_EN/MTIC5W/SCI0_SCK | P40_2 | 24-pin FFC connector on the carrier board | P111 | GPIO3/CAM1_RST# |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (9/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| E17 | P41_0/SCIF1_CTS/GTIOC7A/CAN1_RX_DATARATE_EN/GTIOC3A/SCI0_CTS_N_RTS_N | P41_0 | PMOD0 Type-2A on the carrier board | P114 | GPIO6/TACHIN |
| A18 | P41_1/SCIF1_RTS/GTIOC7B/GTIOC3B | P41_1 | For selecting the device connected to the SD/MMC ch0 interface | P113 | — |
| AG4 | P42_0/USB1_VBUSEN/RSPI2_CK/CAN_CLK/SCIF2_TXD/MTIOC7A | USB1_VBUSEN | USB2.0 Host on the carrier board<br>Include gate USB1_VBUSEN state | P67 | USB1_EN_OC# |
| AE7 | P42_1/USB1_OVRCUR/RSPI2_MOSI/CAN0_TX/SCIF2_RXD/MTIOC7B | USB1_OVRCUR | USB2.0 Host on the carrier board<br>Include gate USB1_OVRCUR state | P67 | USB1_EN_OC# |
| AJ3 | P42_2/ADC_TRG/RSPI2_MISO/CAN0_RX/SCIF2_SCK/MTIOC7C | P42_2 | CAN transceiver ch0 (*2) or PMOD1 Type-6A on the carrier board | P116 | GPIO8 |
| AH3 | P42_3/RIIC2_SDA/RSPI2_SSL/CAN0_TX_DATARATE_EN/SCIF2_CTS/MTIOC7D | P42_3 | CAN transceiver ch1 (*2) or PMOD1 Type-6A on the carrier board | P117 | GPIO9 |
| AC5 | P42_4/RIIC2_SCL/CAM_FIELD/CAN0_RX_DATARATE_EN/SCIF2_RTS | P42_4 | PMOD1 Type-6A on the carrier board | S142 | GPIO12 |
| B18 | P43_0/RSPI0_CK/GTIOC4A/GTIOC6A/IRQ4/MTIOC8A | P43_0/IRQ4 | PMOD0 Type-2A on the carrier board | P112 | GPIO4/HDA_RST# |
| D17 | P43_1/RSPI0_MOSI/GTIOC4B/GTIOC6B/IRQ5/MTIOC8B | P43_1 | PMOD0 Type-2A on the carrier board | P115 | GPIO7 |
| E18 | P43_2/RSPI0_MISO/GTIOC5A/IRQ6/MTIOC8C | P43_2 | PMOD0 Type-2A on the carrier board | P113 | GPIO5/PWM_OUT# |
| C18 | P43_3/RSPI0_SSL/GTIOC5B/IRQ7/MTIOC8D | P43_3 | Unused | — | — |
| A19 | P44_0/RSPI1_CK/SSI1_BCK/CAN1_TX/MTIOC3A/GTIOC6A | RSPI1_CK | PMOD0 Type-2A on the carrier board | P56 | SPI1_Clock |
| F17 | P44_1/RSPI1_MOSI/SSI1_RCK/CAN1_RX/MTIOC3B/GTIOC6B | RSPI1_MOSI | PMOD0 Type-2A on the carrier board | P57 | SPI1_DIN |
| D18 | P44_2/RSPI1_MISO/SSI1_TXD/CAN1_TX_DATARATE_EN/MTIOC3C/GTIOC7A | RSPI1_MISO | PMOD0 Type-2A on the carrier board | P58 | SPI1_DO |
| B19 | P44_3/RSPI1_SSL/SSI1_RXD/CAN1_RX_DATARATE_EN/MTIOC3D/GTIOC7B | RSPI1_SSL | PMOD0 Type-2A on the carrier board | P54 | SPI1_CS0# |
| A8 | P45_0/SSI0_BCK/POE0_N/SCI1_RXD | SSI0_BCK | Audio codec on the carrier board | S42 | I2S0_CK |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (10/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| D12 | P45_1/SSI0_RCK/POE4_N/SCI1_TXD | SSI0_RCK | Audio codec on the carrier board | S39 | I2S0_LRCK |
| A9 | P45_2/SSI0_TXD/POE8_N/SCI1_SCK | SSI0_TXD | Audio codec on the carrier board | S40 | I2S0_SDOUT |
| B9 | P45_3/SSI0_RXD/POE10_N/SCI1_CTS_N_RTS_N | SSI0_RXD | Audio codec on the carrier board | S41 | I2S0_SDIN |
| B10 | P46_0/SSI1_BCK/GTETRGA/CAN1_TX/RIIC2_SDA | SSI1_BCK | MIPI DSI to HDMI conversion IC on the carrier board | S53 | I2S2_CK |
| A10 | P46_1/SSI1_RCK/GTETRGB/CAN1_RX/RIIC2_SCL | SSI1_RCK | MIPI DSI to HDMI conversion IC on the carrier board | S50 | I2S2_LRCK |
| C12 | P46_2/SSI1_TXD/GTETRGC/CAN1_TX_DATARATE_EN/RIIC3_SDA | SSI1_TXD | MIPI DSI to HDMI conversion IC on the carrier board | S51 | I2S2_SDOUT |
| D13 | P46_3/SSI1_RXD/GTETRGD/CAN1_RX_DATARATE_EN/RIIC3_SCL | SSI1_RXD | Unused | S52 | I2S2_SDIN |
| B20 | P47_0/SCI0_RXD/SD0_CD/IRQ0/SSI1_BCK/RSPI0_CK | SD0_CD | uSD ch0 card slot | — | — |
| A20 | P47_1/SCI0_TXD/SD0_WP/IRQ1/SSI1_RCK/RSPI0_MOSI | P47_1 | Unused | — | — |
| A21 | P47_2/SCI0_SCK/SD1_CD/IRQ2/SSI1_TXD/RSPI0_MISO | P47_2 | PMOD1 Type-6A on the carrier board | S123 | GPIO13 |
| B21 | P47_3/SCI0_CTS_N_RTS_N/SD1_WP/IRQ3/SSI1_RXD/RSPI0_SSL | P47_3 | Unused | P118 | — |
| B22 | P48_0/SCIF2_TXD/RSPI1_CK/RIIC2_SDA/MTCLKA | SCIF2_TXD | PMOD1 Type-3A on the carrier board | P129 | SER0_TX |
| A23 | P48_1/SCIF2_RXD/RSPI1_MOSI/RIIC2_SCL/MTCLKB | SCIF2_RXD | PMOD1 Type-3A on the carrier board | P130 | SER0_RX |
| A22 | P48_2/SCIF2_SCK/RSPI1_MISO/RIIC3_SDA/MTCLKC | P48_2 | Unused | — | — |
| C22 | P48_3/SCIF2_CTS/RSPI1_SSL/RIIC3_SCL/MTCLKD | SCIF2_CTS | PMOD1 Type-3A on the carrier board | P132 | SER0_CTS# |
| B23 | P48_4/SCIF2_RTS/ADC_TRG | SCIF2_RTS | PMOD1 Type-3A on the carrier board | P131 | SER0_RTS# |
| AJ4 | P5_0/USB0_OVRCUR/SCIF2_SCK/MTIOC7C/SSI2_BCK | USB0_OVRCUR | USB2.0 OTG on the carrier board include gate USB0_OVRCUR state | P62 | USB0_EN_OC# |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (11/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AH4 | P5_1/USB0_OTG_ID/SCIF2_CTS/MTIOC7D/SSI2_RCK | USB0_OTG_ID | USB2.0 OTG on the carrier board<br>USB_OTG_ID state | P64 | USB0_OTG_ID |
| AH5 | P5_2/USB0_OTG_EXICEN/SCIF2_RTS/SSI2_DATA | P5_2 | PMOD1 Type-3A on the carrier board | P119 | GPIO11 |
| AJ27 | P6_0/DISP_CLK/SSI0_BCK/USB0_VBUSEN/MTIOC1A | P6_0 | Unused | — | — |
| AH27 | P6_1/DISP_HSYNC/SSI0_RCK/MTIOC1B | P6_1 | Unused | — | — |
| AJ28 | P7_0/DISP_VSYNC/SSI0_TXD/USB0_OVRCUR/MTIC5U | P7_0 | Unused | — | — |
| AH28 | P7_1/DISP_DE/SSI0_RXD/USB0_OTG_ID/MTIC5V | P7_1 | Unused | — | — |
| AJ19 | P7_2/DISP_DATA0/USB0_OTG_EXICEN/MTIC5W | P7_2 | Unused | — | — |
| AH19 | P8_0/DISP_DATA1/USB1_VBUSEN/RSPI2_CK/RIIC3_SCL | P8_0 | Unused | — | — |
| AJ20 | P8_1/DISP_DATA2/USB1_OVRCUR/RSPI2_MOSI/RIIC3_SDA | P8_1 | Unused | — | — |
| AH20 | P8_2/DISP_DATA3/RSPI2_MISO | P8_2 | Unused | — | — |
| AJ21 | P9_0/DISP_DATA4/ADC_TRG/RSPI2_SSL/MTIOC2A | ADC_TRG | Pin header CN1 for ADC input | — | — |
| AH21 | P9_1/DISP_DATA5/MTIOC2B | P9_1 | Unused | — | — |
| N7 | PLL1_AVDD18 | PLL1_AVDD18 | 1.8V | — | — |
| W9 | PLL23_AVDD18 | PLL23_AVDD18 | 1.8V | — | — |
| V5 | PLL23_DVDD11 | PLL23_DVDD11 | 1.1V | — | — |
| U23 | PLL4_AVDD18 | PLL4_AVDD18 | 1.8V | — | — |
| AA15 | PLL5_DVDD11 | PLL5_DVDD11 | 1.1V | — | — |
| G13 | PLL6_AVDD18 | PLL6_AVDD18 | 1.8V | — | — |
| AF3 | PRST# | PRST# | Input system reset signal from RAA215300 | — | — |
| AC7 | PVDD | PVDD | 3.3V | — | — |
| AC12 | PVDD | PVDD | 3.3V | — | — |
| AC22 | PVDD | PVDD | 3.3V | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (12/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AC23 | PVDD | PVDD | 3.3V | — | — |
| H7 | PVDD | PVDD | 3.3V | — | — |
| E13 | PVDD | PVDD | 3.3V | — | — |
| G18 | PVDD | PVDD | 3.3V | — | — |
| G23 | PVDD | PVDD | 3.3V | — | — |
| B6 | QSPI_INT# | QSPI_INT# | Connected to pull-up by SPI_PVDD power supply (*1) | — | — |
| A5 | QSPI_RESET# | QSPI_RESET# | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| B5 | QSPI_WP# | QSPI_WP# | Unused | — | — |
| A3 | QSPI0_IO0 | QSPI0_IO0 | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| B3 | QSPI0_IO1 | QSPI0_IO1 | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| A4 | QSPI0_IO2 | QSPI0_IO2 | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| B4 | QSPI0_IO3 | QSPI0_IO3 | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| C4 | QSPI0_SPCLK | QSPI0_SPCLK | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| A2 | QSPI0_SSL | QSPI0_SSL | QSPI Flash Memory (MT25QU512ABB8E12-0SIT) | — | — |
| C7 | QSPI1_IO0 | QSPI1_IO0 | Unused | — | — |
| D7 | QSPI1_IO1 | QSPI1_IO1 | Unused | — | — |
| A6 | QSPI1_IO2 | QSPI1_IO2 | Unused | — | — |
| D8 | QSPI1_IO3 | QSPI1_IO3 | Unused | — | — |
| B7 | QSPI1_SPCLK | QSPI1_SPCLK | Unused | — | — |
| C8 | QSPI1_SSL | QSPI1_SSL | Unused | — | — |
| B24 | RIIC0_SCL | RIIC0_SCL | 24-pin FFC connector on the carrier board | S1 | I2C_CAM1_CK |
| A25 | RIIC0_SDA | RIIC0_SDA | 24-pin FFC connector on the carrier board | S2 | I2C_CAM1_DAT |
| C23 | RIIC1_SCL | RIIC1_SCL | MIPI DSI to HDMI conversion IC on the carrier board | S139 | I2C_LCD_CK |
| A24 | RIIC1_SDA | RIIC1_SDA | MIPI DSI to HDMI conversion IC on the carrier board | S140 | I2C_LCD_DAT |
| F1 | SD0_CLK | SD0_CLK | eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot | — | — |
| F2 | SD0_CMD | SD0_CMD | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| G2 | SD0_DATA0 | SD0_DATA0 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (13/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| H4 | SD0_DATA1 | SD0_DATA1 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| G3 | SD0_DATA2 | SD0_DATA2 | eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot | — | — |
| G4 | SD0_DATA3 | SD0_DATA3 | eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot | — | — |
| E1 | SD0_DATA4 | SD0_DATA4 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| D1 | SD0_DATA5 | SD0_DATA5 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| E2 | SD0_DATA6 | SD0_DATA6 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| D2 | SD0_DATA7 | SD0_DATA7 | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| H5 | SD0_PVDD | SD0_PVDD | 1.8V/3.3V | — | — |
| C1 | SD0_RST# | SD0_RST# | eMMC Memory (MTFC64GASAQHD-IT) | — | — |
| H3 | SD1_CLK | SD1_CLK | uSD ch1 card slot on the carrier board | P36 | SDIO_CK |
| J2 | SD1_CMD | SD1_CMD | uSD ch1 card slot on the carrier board | P34 | SDIO_CMD |
| H1 | SD1_DATA0 | SD1_DATA0 | uSD ch1 card slot on the carrier board | P39 | SDIO_D0 |
| H2 | SD1_DATA1 | SD1_DATA1 | uSD ch1 card slot on the carrier board | P40 | SDIO_D1 |
| K2 | SD1_DATA2 | SD1_DATA2 | uSD ch1 card slot on the carrier board | P41 | SDIO_D2 |
| J1 | SD1_DATA3 | SD1_DATA3 | uSD ch1 card slot on the carrier board | P42 | SDIO_D3 |
| M6 | SD1_PVDD | SD1_PVDD | 1.8V/3.3V | — | — |
| F8 | SPI_PVDD | SPI_PVDD | 1.8V | — | — |
| AE1 | TCK/SWDCLK | TCK/SWDCLK | Connected to JTAG connector (CN2) | — | — |
| AF1 | TDI | TDI | Connected to JTAG connector (CN2) | — | — |
| AE2 | TDO | TDO | Connected to JTAG connector (CN2) | — | — |
| AD18 | VSS | VSS | GND | — | — |
| AD2 | TMS/SWDIO | TMS/SWDIO | Connected to JTAG connector (CN2) | — | — |
| AF2 | TRST# | TRST# | Connected to JTAG connector (CN2) | — | — |
| AB7 | VDD18 | VDD18 | 1.8V | — | — |
| AG8 | USB_AVDD18 | USB_AVDD18 | 1.8V | — | — |
| AG7 | USB_RREF | USB_RREF | Connected to GND via the 1.8Ω resistor | — | — |
| AF7 | USB_VDD18 | USB_VDD18 | 1.8V | — | — |
| AF8 | USB_VDD18 | USB_VDD18 | 1.8V | — | — |
| AD8 | USB_VDD33 | USB_VDD33 | 3.3V | — | — |
| AE8 | USB_VDD33 | USB_VDD33 | 3.3V | — | — |
| AJ6 | VSS | VSS | GND | — | — |
| AH7 | VSS | VSS | GND | — | — |
| AC8 | VSS | VSS | GND | — | — |
| AJ9 | VSS | VSS | GND | — | — |
| AJ8 | USB0_DM | USB0_DM | USB2.0 OTG on the carrier board | P61 | USB0- |
| AH9 | USB0_DP | USB0_DP | USB2.0 OTG on the carrier board | P60 | USB0+ |
| AH10 | USB0_VBUSIN | USB0_VBUSIN | USB2.0 OTG on the carrier board | P63 | USB0_VBUS_DET |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (14/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| AJ7 | USB1_DM | USB1_DM | USB2.0 Host on the carrier board | P66 | USB1- |
| AH8 | USB1_DP | USB1_DP | USB2.0 Host on the carrier board | P65 | USB1+ |
| J9 | VDD | VDD | 1.1V | — | — |
| L9 | VDD | VDD | 1.1V | — | — |
| N9 | VDD | VDD | 1.1V | — | — |
| R9 | VDD | VDD | 1.1V | — | — |
| U9 | VDD | VDD | 1.1V | — | — |
| AA9 | VDD | VDD | 1.1V | — | — |
| K10 | VDD | VDD | 1.1V | — | — |
| M10 | VDD | VDD | 1.1V | — | — |
| P10 | VDD | VDD | 1.1V | — | — |
| T10 | VDD | VDD | 1.1V | — | — |
| V10 | VDD | VDD | 1.1V | — | — |
| Y10 | VDD | VDD | 1.1V | — | — |
| J11 | VDD | VDD | 1.1V | — | — |
| AA11 | VDD | VDD | 1.1V | — | — |
| K12 | VDD | VDD | 1.1V | — | — |
| Y12 | VDD | VDD | 1.1V | — | — |
| J13 | VDD | VDD | 1.1V | — | — |
| AA13 | VDD | VDD | 1.1V | — | — |
| K14 | VDD | VDD | 1.1V | — | — |
| Y14 | VDD | VDD | 1.1V | — | — |
| J15 | VDD | VDD | 1.1V | — | — |
| K16 | VDD | VDD | 1.1V | — | — |
| Y16 | VDD | VDD | 1.1V | — | — |
| J17 | VDD | VDD | 1.1V | — | — |
| AA17 | VDD | VDD | 1.1V | — | — |
| K18 | VDD | VDD | 1.1V | — | — |
| Y18 | VDD | VDD | 1.1V | — | — |
| J19 | VDD | VDD | 1.1V | — | — |
| AA19 | VDD | VDD | 1.1V | — | — |
| K20 | VDD | VDD | 1.1V | — | — |
| M20 | VDD | VDD | 1.1V | — | — |
| P20 | VDD | VDD | 1.1V | — | — |
| T20 | VDD | VDD | 1.1V | — | — |
| V20 | VDD | VDD | 1.1V | — | — |
| Y20 | VDD | VDD | 1.1V | — | — |
| J21 | VDD | VDD | 1.1V | — | — |
| L21 | VDD | VDD | 1.1V | — | — |
| N21 | VDD | VDD | 1.1V | — | — |
| R21 | VDD | VDD | 1.1V | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (15/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| U21 | VDD | VDD | 1.1V | — | — |
| W21 | VDD | VDD | 1.1V | — | — |
| AA21 | VDD | VDD | 1.1V | — | — |
| A1 | VSS | VSS | GND | — | — |
| G1 | VSS | VSS | GND | — | — |
| K1 | VSS | VSS | GND | — | — |
| V1 | VSS | VSS | GND | — | — |
| AD1 | VSS | VSS | GND | — | — |
| AJ1 | VSS | VSS | GND | — | — |
| AH2 | VSS | VSS | GND | — | — |
| G5 | VSS | VSS | GND | — | — |
| M5 | VSS | VSS | GND | — | — |
| N5 | VSS | VSS | GND | — | — |
| U5 | VSS | VSS | GND | — | — |
| AB5 | VSS | VSS | GND | — | — |
| H6 | VSS | VSS | GND | — | — |
| U6 | VSS | VSS | GND | — | — |
| V6 | VSS | VSS | GND | — | — |
| AB6 | VSS | VSS | GND | — | — |
| A7 | VSS | VSS | GND | — | — |
| M7 | VSS | VSS | GND | — | — |
| G8 | VSS | VSS | GND | — | — |
| AJ10 | VSS | VSS | GND | — | — |
| L11 | VSS | VSS | GND | — | — |
| N11 | VSS | VSS | GND | — | — |
| R11 | VSS | VSS | GND | — | — |
| U11 | VSS | VSS | GND | — | — |
| W11 | VSS | VSS | GND | — | — |
| F12 | VSS | VSS | GND | — | — |
| M12 | VSS | VSS | GND | — | — |
| P12 | VSS | VSS | GND | — | — |
| T12 | VSS | VSS | GND | — | — |
| V12 | VSS | VSS | GND | — | — |
| AE12 | VSS | VSS | GND | — | — |
| AF12 | VSS | VSS | GND | — | — |
| F13 | VSS | VSS | GND | — | — |
| L13 | VSS | VSS | GND | — | — |
| N13 | VSS | VSS | GND | — | — |
| R13 | VSS | VSS | GND | — | — |
| U13 | VSS | VSS | GND | — | — |
| W13 | VSS | VSS | GND | — | — |
| AE13 | VSS | VSS | GND | — | — |
| AF13 | VSS | VSS | GND | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (16/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| M14 | VSS | VSS | GND | — | — |
| P14 | VSS | VSS | GND | — | — |
| T14 | VSS | VSS | GND | — | — |
| V14 | VSS | VSS | GND | — | — |
| L15 | VSS | VSS | GND | — | — |
| N15 | VSS | VSS | GND | — | — |
| R15 | VSS | VSS | GND | — | — |
| U15 | VSS | VSS | GND | — | — |
| W15 | VSS | VSS | GND | — | — |
| AG15 | VSS | VSS | GND | — | — |
| M16 | VSS | VSS | GND | — | — |
| P16 | VSS | VSS | GND | — | — |
| T16 | VSS | VSS | GND | — | — |
| V16 | VSS | VSS | GND | — | — |
| L17 | VSS | VSS | GND | — | — |
| N17 | VSS | VSS | GND | — | — |
| R17 | VSS | VSS | GND | — | — |
| U17 | VSS | VSS | GND | — | — |
| W17 | VSS | VSS | GND | — | — |
| AD17 | VSS | VSS | GND | — | — |
| AE17 | VSS | VSS | GND | — | — |
| AF17 | VSS | VSS | GND | — | — |
| F18 | VSS | VSS | GND | — | — |
| M18 | VSS | VSS | GND | — | — |
| P18 | VSS | VSS | GND | — | — |
| T18 | VSS | VSS | GND | — | — |
| V18 | VSS | VSS | GND | — | — |
| AF18 | VSS | VSS | GND | — | — |
| L19 | VSS | VSS | GND | — | — |
| N19 | VSS | VSS | GND | — | — |
| R19 | VSS | VSS | GND | — | — |
| U19 | VSS | VSS | GND | — | — |
| W19 | VSS | VSS | GND | — | — |
| F22 | VSS | VSS | GND | — | — |
| G22 | VSS | VSS | GND | — | — |
| AD22 | VSS | VSS | GND | — | — |
| V23 | VSS | VSS | GND | — | — |
| H24 | VSS | VSS | GND | — | — |
| U24 | VSS | VSS | GND | — | — |
| V24 | VSS | VSS | GND | — | — |

Table 2.2 List of Pin Function Selection Used on the RTK9744L23C01000BE (17/17)

| Pin Location | Pin Name | Pin Function | Description | SMARC Pin No. | SMARC Pin Name |
|---|---|---|---|---|---|
| G25 | VSS | VSS | GND | — | — |
| AC25 | VSS | VSS | GND | — | — |
| G26 | VSS | VSS | GND | — | — |
| H26 | VSS | VSS | GND | — | — |
| M26 | VSS | VSS | GND | — | — |
| N26 | VSS | VSS | GND | — | — |
| U26 | VSS | VSS | GND | — | — |
| V26 | VSS | VSS | GND | — | — |
| AB27 | VSS | VSS | GND | — | — |
| D28 | VSS | VSS | GND | — | — |
| R28 | VSS | VSS | GND | — | — |
| AA28 | VSS | VSS | GND | — | — |
| AD28 | VSS | VSS | GND | — | — |
| AG28 | VSS | VSS | GND | — | — |
| A29 | VSS | VSS | GND | — | — |
| U29 | VSS | VSS | GND | — | — |
| Y29 | VSS | VSS | GND | — | — |
| AJ29 | VSS | VSS | GND | — | — |
| D22 | WDTOVF_ PERROUT# | WDTOVF_ PERROUT# | Input hardware reset signal from RAA215300 | — | — |
| AH1 | XIN | XIN | GND | — | — |
| AG1 | XOUT | XOUT | Open | — | — |

NOTES

1. This pin is treated as open in the schematic, but this is incorrect.
2. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted.
   The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already.
   S.LOT# in the outer box label: 000251812 or later
   S.LOT# label on the carrier board: 251812 or later

## 2.3 Memory

QSPI flash memory and DDR4 SDRAM are mounted in RTK9744L23C01000BE as external memories.

Please refer to the following for details

### 2.3.1 QSPI Flash Memory

**Figure 2.1** shows a block diagram of the Serial Flash Memory interface.

The QSPI flash memory is controlled by the SPI multi-I/O bus controller (SPIBSC) that is with built-in to the RZ/G2L. This memory supports both single data rate (SDR) and double data rate (DDR) transfers at 66MHz and 50MHz clock frequency.

NOTE

The pull-up resistor on the clock line "RZ_QSPI0_SPCLK" is optional.

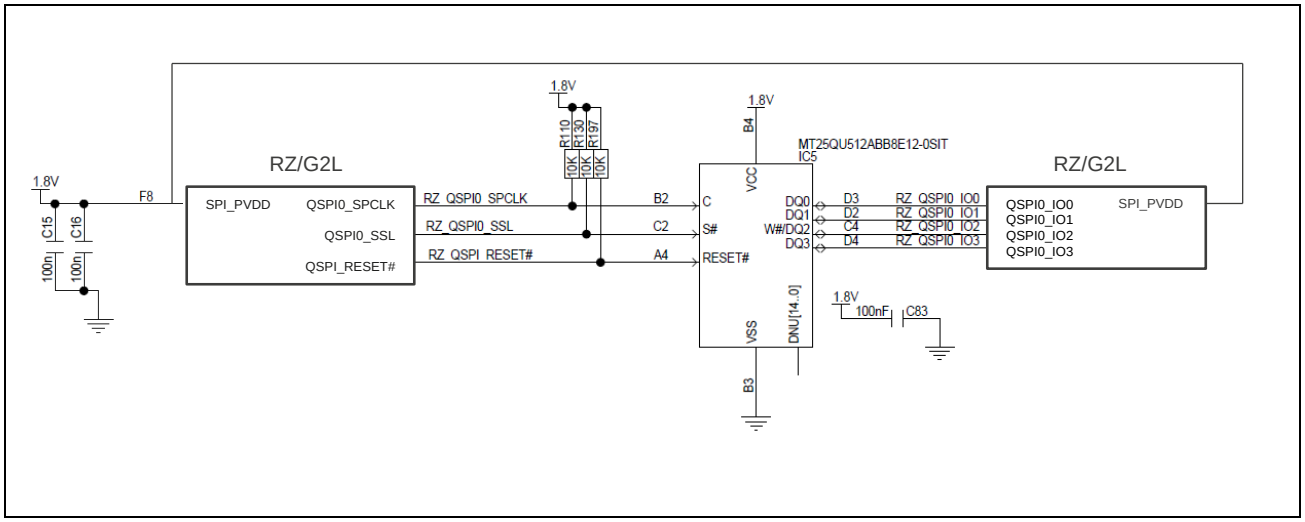



Figure 2.1 Block Diagram of Serial Flash Memory I/F

## 2.3.2 DDR4 SDRAM

**Figure 2.2** shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the DDD3L/DDR4 SDRAM Memory Controller (MEMC) that is with built-in to the RZ/G2L. This interface supports up to DDR4-1600 SDRAM, a data bus width of 16-bit and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

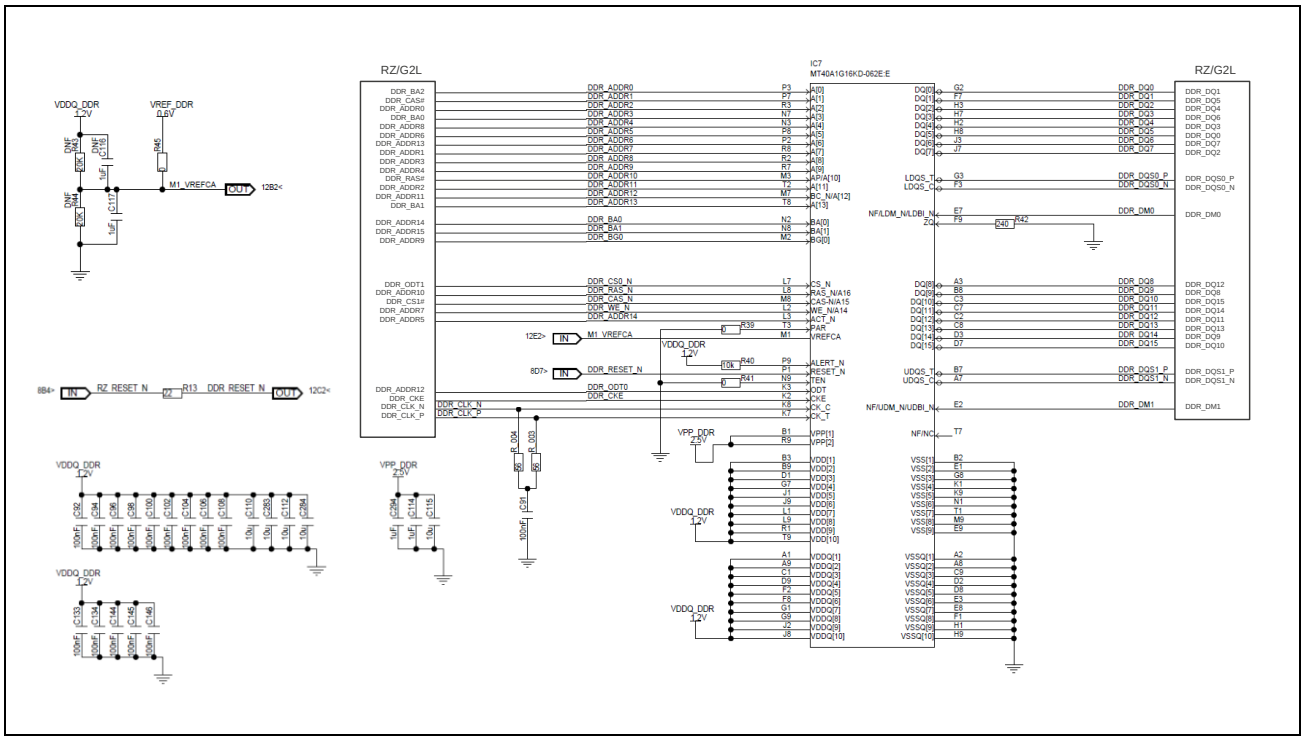



Figure 2.2 Block Diagram of DDR4 SDRAM

## 2.4 Gigabit Ethernet Interface

**Figure 2.3** and **Figure 2.4** show a block diagram of Gigabit Ethernet0 and Ethernet1 interface.

The Gigabit Ethernet Interface is controlled by the Ethernet controller (E-MAC) hat conforms to the definition of the MAC (Media Access Control) layer that is with built-in to the RZ/G2L. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

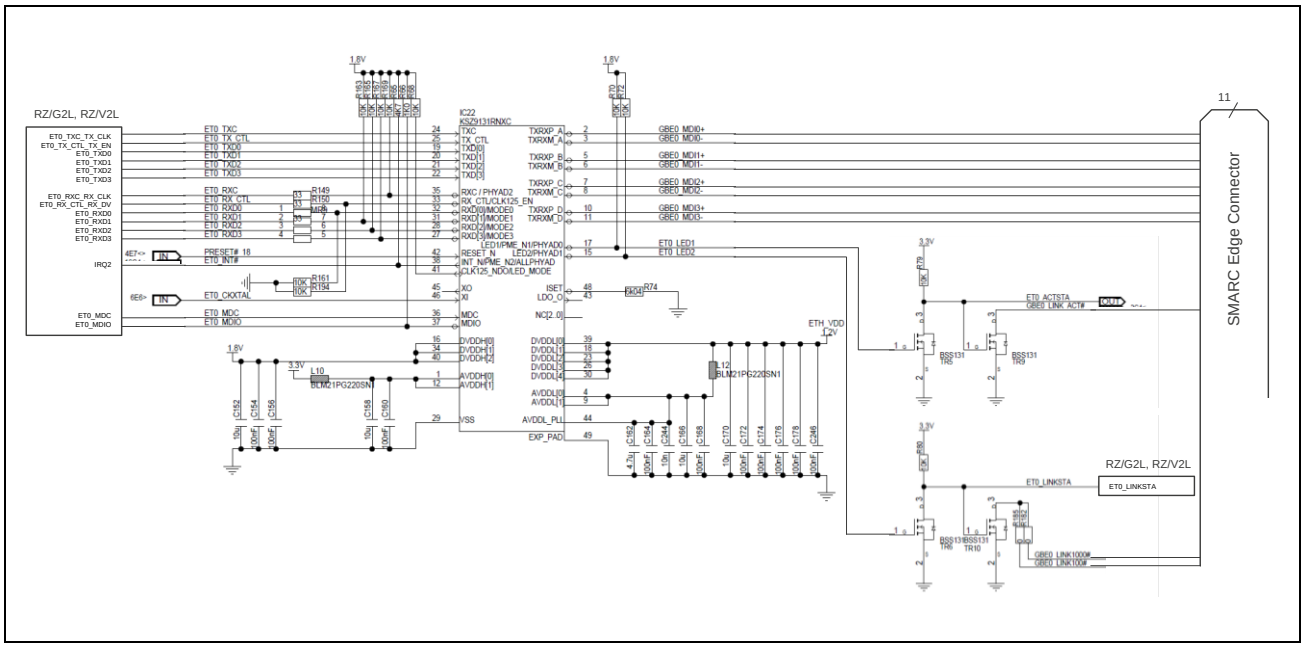



Figure 2.3 Block Diagram of Gigabit Ethernet0 I/F

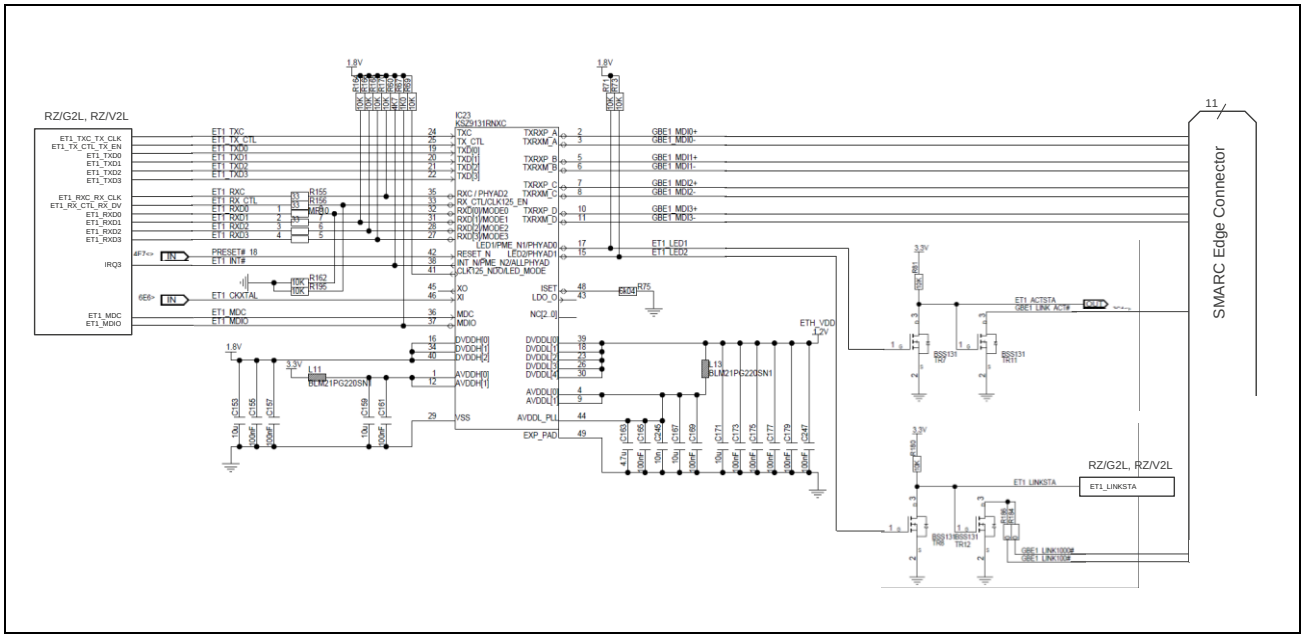



Figure 2.4 Block Diagram of Gigabit Ethernet1 I/F

## 2.5 ADC Interface

**Figure 2.5** shows a block diagram of the ADC interface.

RTK9744L23C01000BE is implemented the 10-pin pin header for connection to the ADC interface. Six input channels can be used.

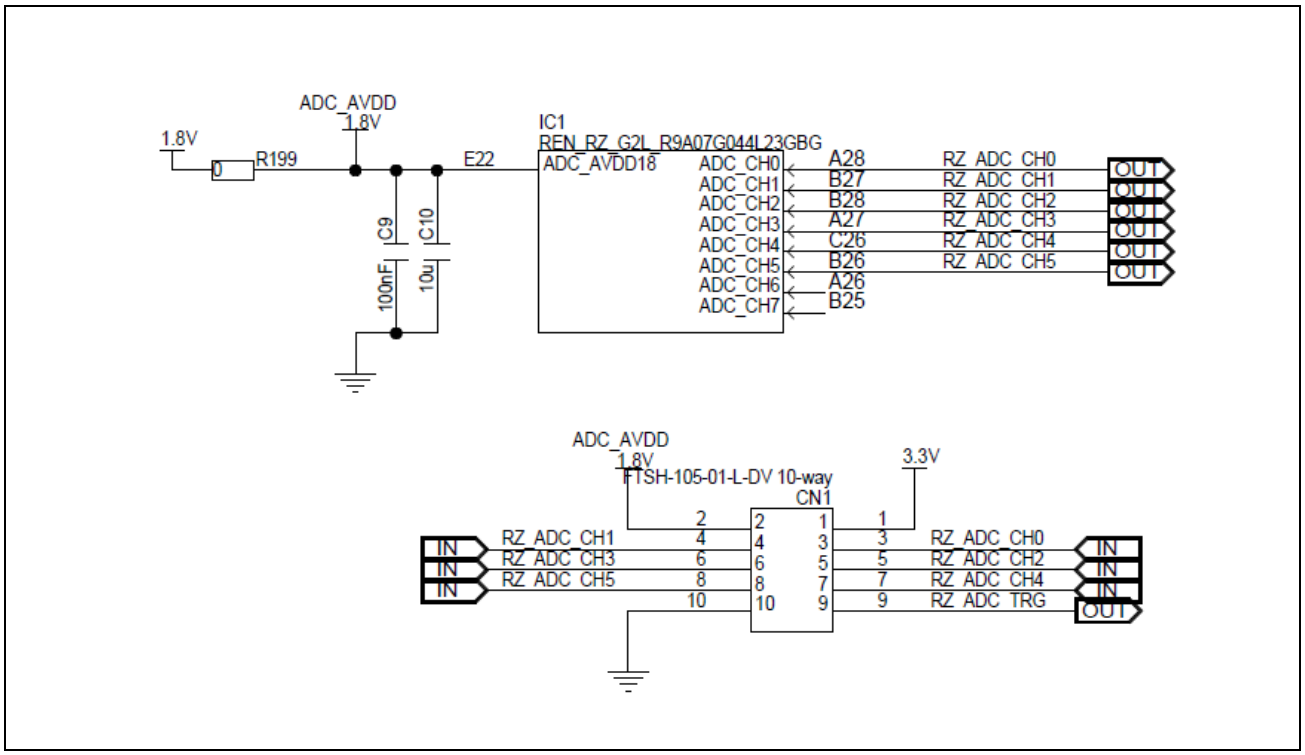



Figure 2.5 Block Diagram of ADC I/F

## 2.6 Clock Configuration

**Figure 2.6** shows a block diagram of the Clock configuration.

NOTE

MIPI-DSI Interface supports operation up to Full HD, 60fps mode.

SD Interface supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

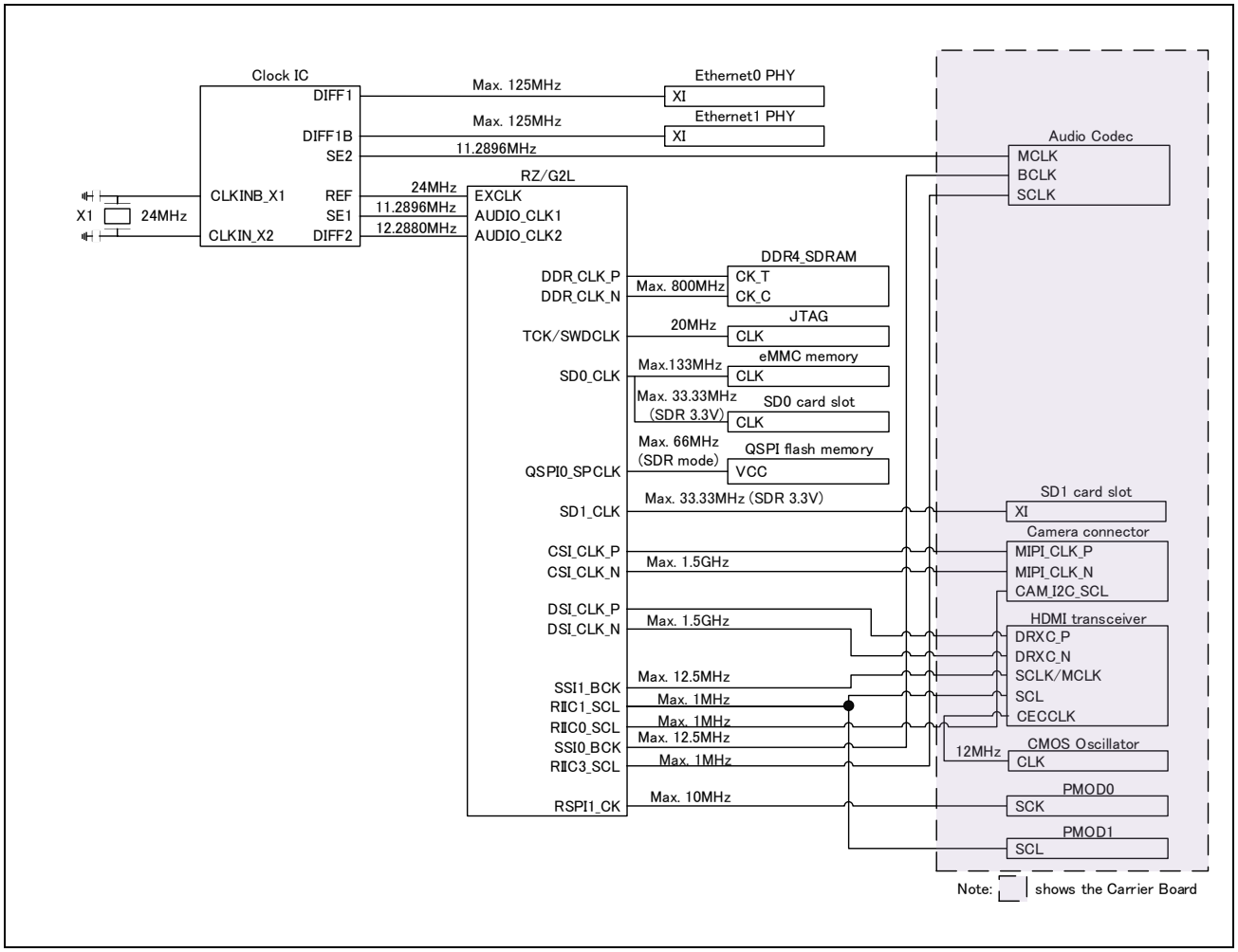



Figure 2.6 Block Diagram of Clock Configuration

## 2.7 Reset Control

**Figure 2.7** shows block diagrams of a reset control for RTK9744L23S01000BE (Evaluation board Kit for RZ/G2L MPU).

For the RTK9744L23C01000BE, the interfaces of DDR4 SDRAM, QSPI flash memory, eMMC memory, Ethernet and Debug are controlled by reset signal from the PMIC.

There are two types of system resets: power-on reset and reset by the button switch.

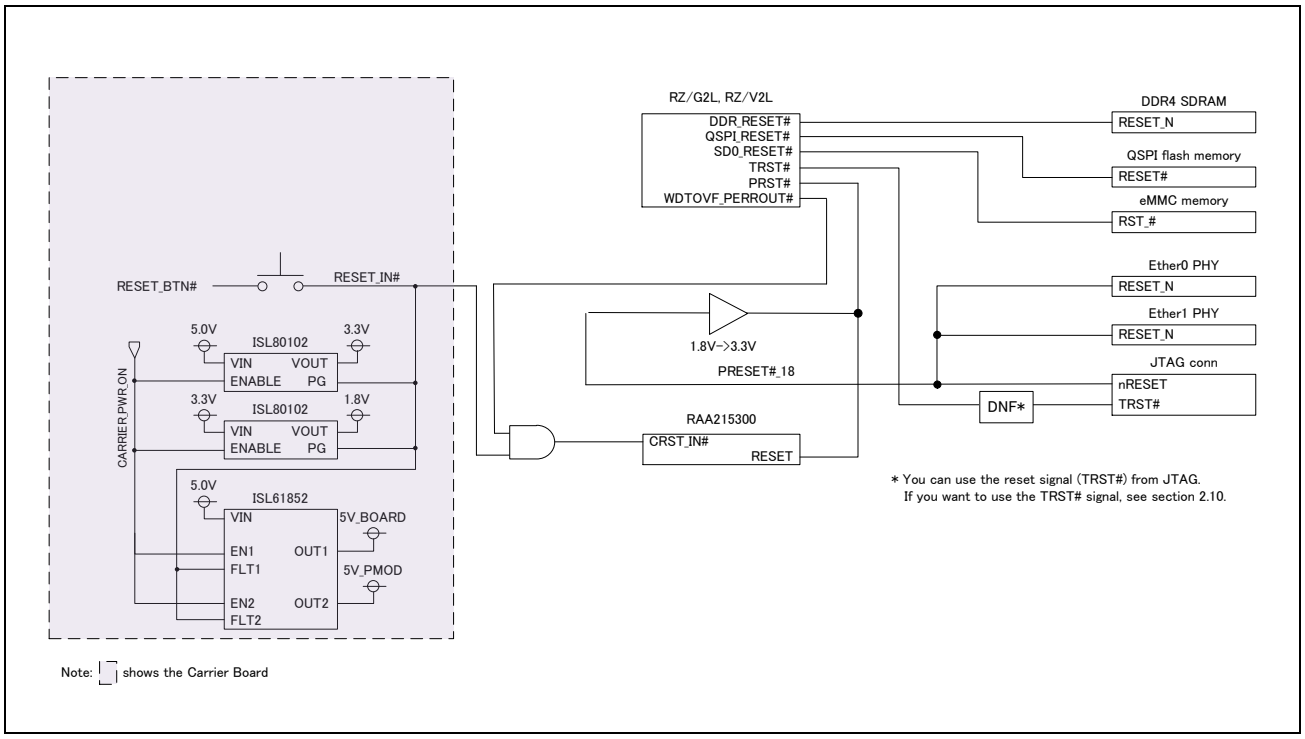



Figure 2.7 Block Diagram of Reset Control

## 2.8 Power Supply Configuration

**Figure 2.8** shows a block diagram of power configuration for RTK9744L23S01000BE (Evaluation board Kit for RZ/G2L MPU).

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5V and 9V.

The default setting for controlling the input voltage level is 5V (max 3A input) with SW11-4 is turned on. When the switch is turned off, the input voltage is 9V (max 3A input). Only when RTK9744L23S01000BE is connected to external devices that requires a lot of power and is expected to run out of power, the SW 11-4 is turned off.

The 5V power supply is supplied to the PMIC installed in RTK9744L23C01000BE, and the PMIC generates the power supply voltage for each interface.

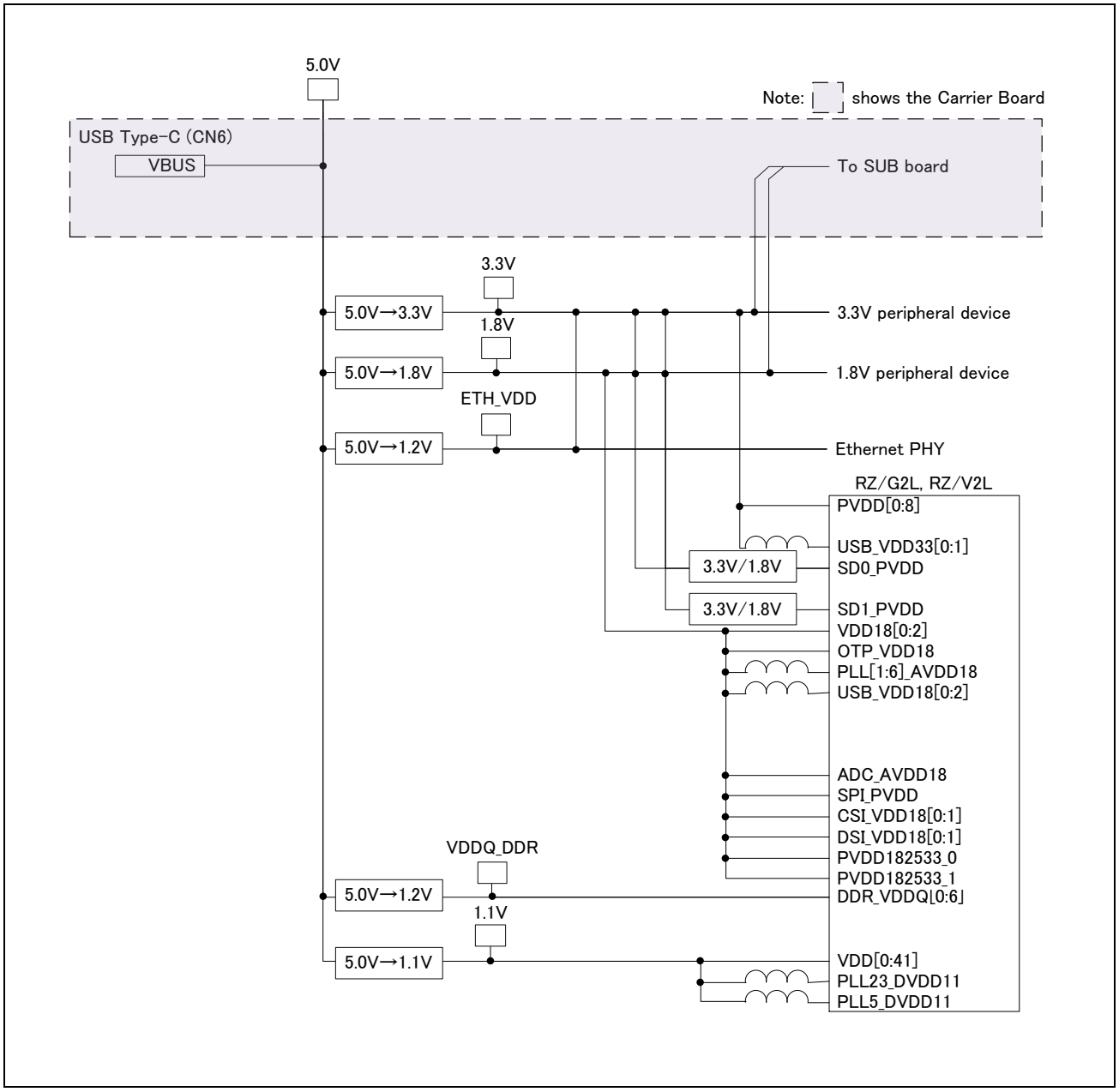



Figure 2.8 Block Diagram of Power Configuration

**Figure 2.9** shows block diagrams of power regulation for the RTK9744L23C01000BE.

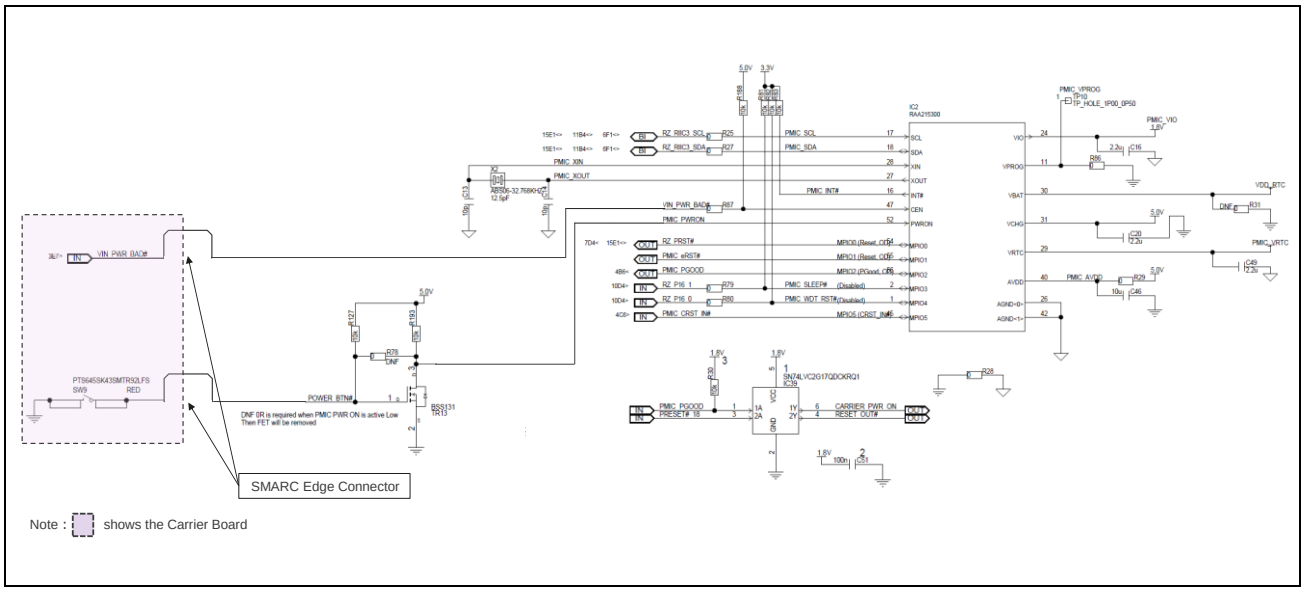



Figure 2.9 Block Diagrams of Power Regulation

## 2.9 PMIC

**Figure 2.10** shows the RZ/G2L pin assignment for PMIC.

LDO1 and LDO2 output voltage value are fixed by P39_0 and P39_1.

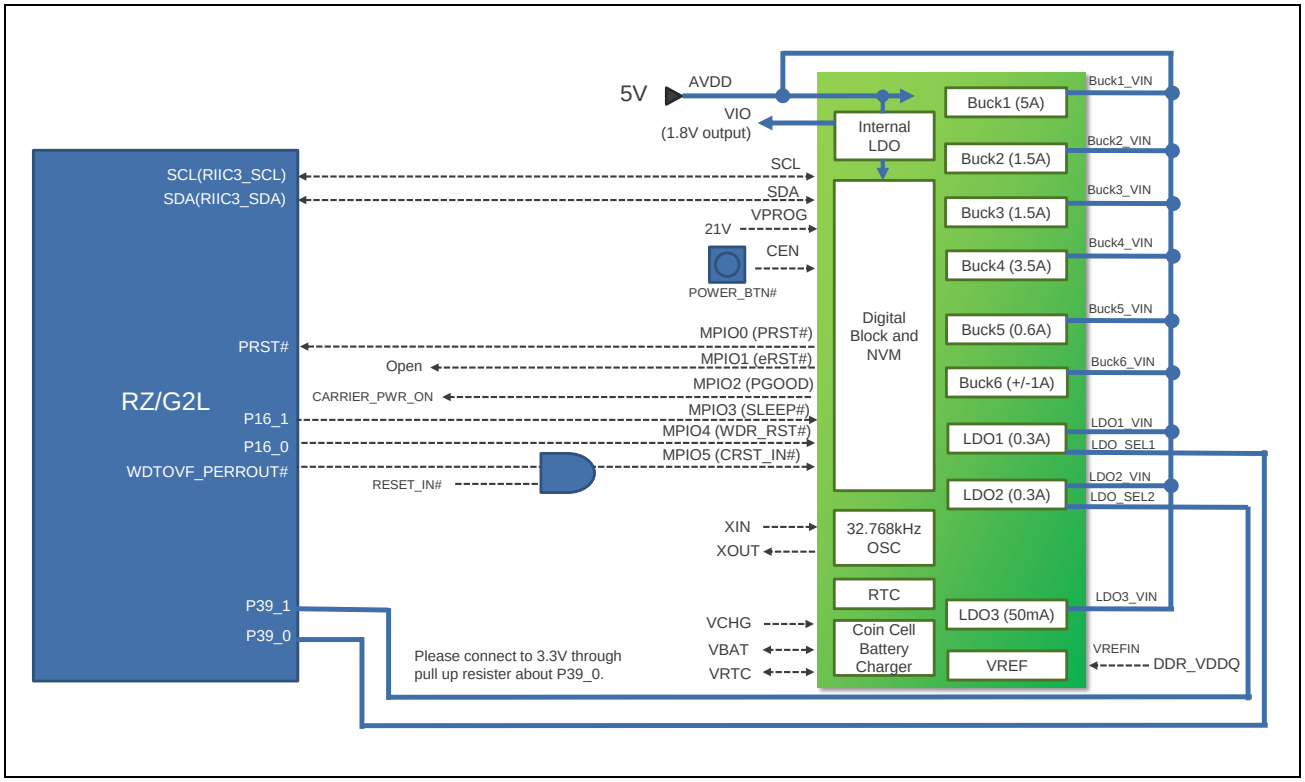



Figure 2.10 Block Diagram around PMIC

## 2.10 Debug Interface

**Figure 2.11** shows a block diagram of debug interface.

This interface supports JTAG and SWD and has debug support for Cortex-A55 and Cortex-M33.

The default operation for the debug interface uses pin 9 as a ground detect, although with resitor (R20) fitting options, it is possible to use this to independently drive the JTAG_TRST#.

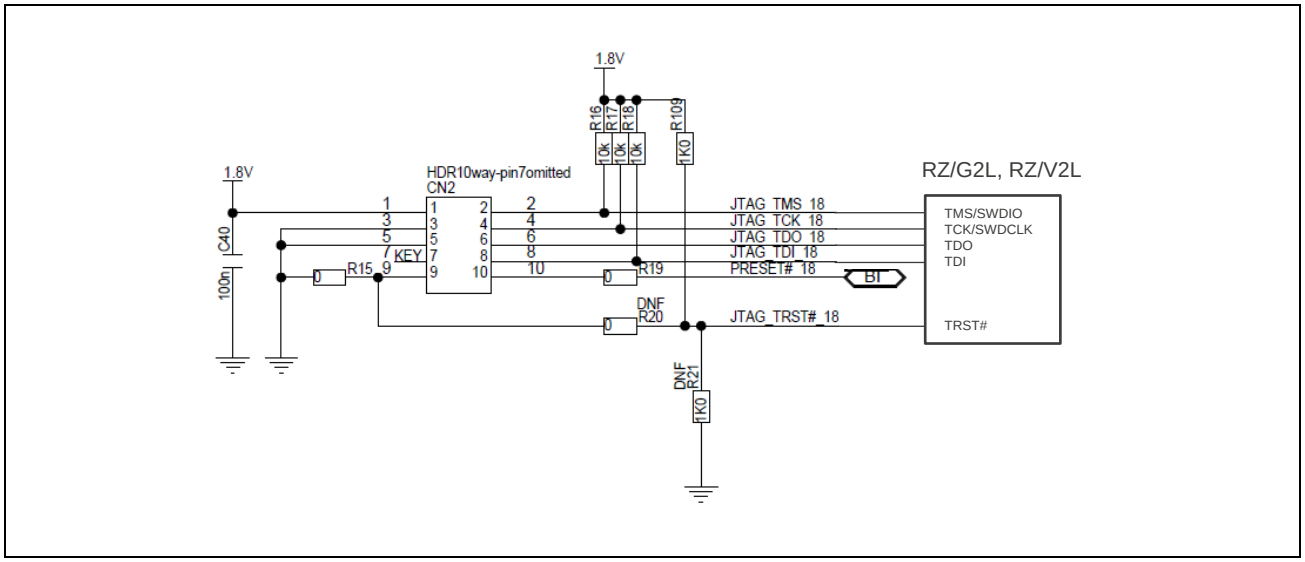



Figure 2.11 Block Diagram of Debug I/F

# 2.11 SD/MMC Host Interface

## 2.11.1 eMMC Memory

**Figure 2.12** shows a block diagram of the MMC interface.

The eMMC memory is connected to channel0 of SD/MMC interface that is with built-in to the RZ/G2L. This memory is used in conjunction with SD card.

The eMMC memory may be used when

- the SW_SD0_DEV_SEL is enabled (SW1-2: Selection SD/MMC is OFF).

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

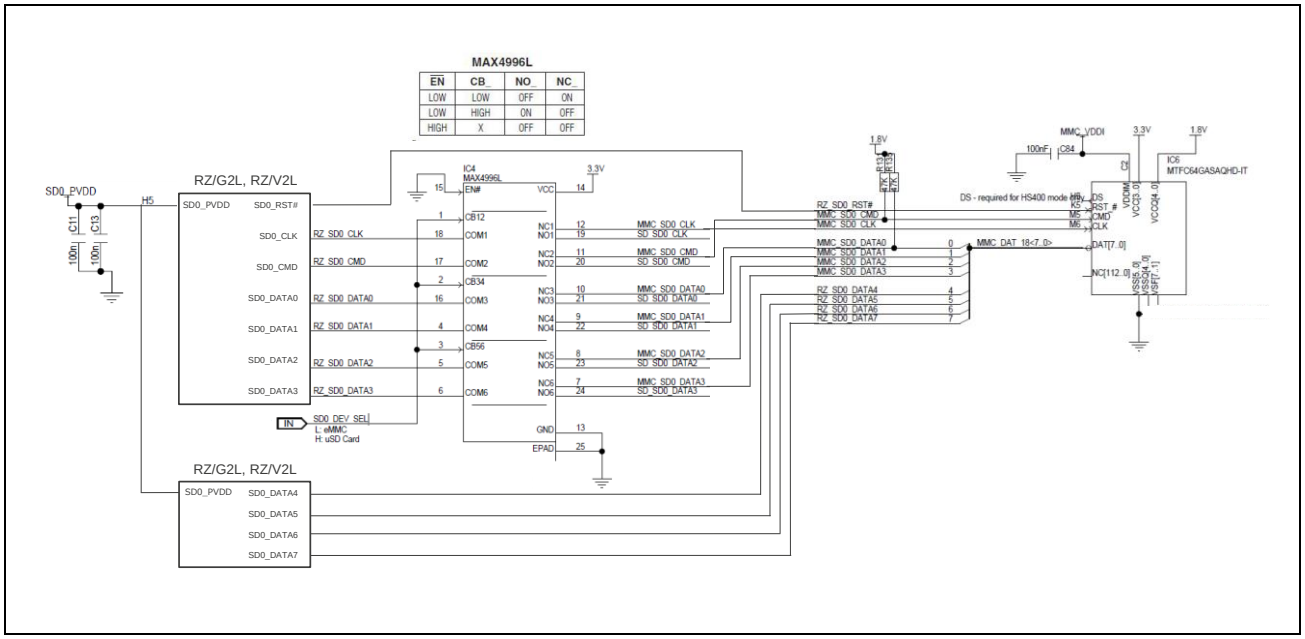



Figure 2.12 Block Diagram of eMMC I/F

## 2.11.2 SD Card

**Figure 2.13** shows a block diagram of the SDHI interface.

The microSD card is connected to channel0 of SD/MMC interface that is with built-in to the RZ/G2L. This memory is used in conjunction with eMMC memory.

The microSD card may be used when

- the microSD is the selected boot mode (SW11-1: ON, SW11-2: ON, SW11-3: OFF)
- the SW_SD0_DEV_SEL is disabled (SW1-2: Selection SD/MMC is ON) and eMMC memory is not the selected boot mode (SW11-1: ON, SW11-2: OFF, SW11-3: OFF).

This interface complies with the memory card standard version 3.0 and supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

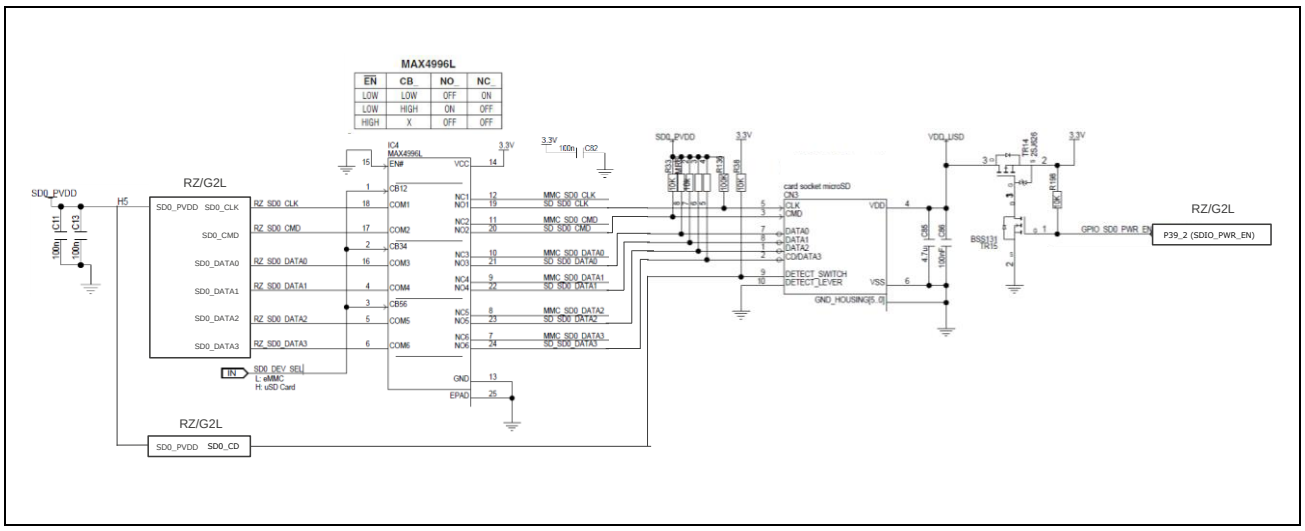



Figure 2.13 Block Diagram of SDHI I/F

# 3. Operation Specifications

## 3.1 Overview of Connectors

**Figure 3.1** Illustrates the layout of connectors of the RTK9744L23C01000BE.

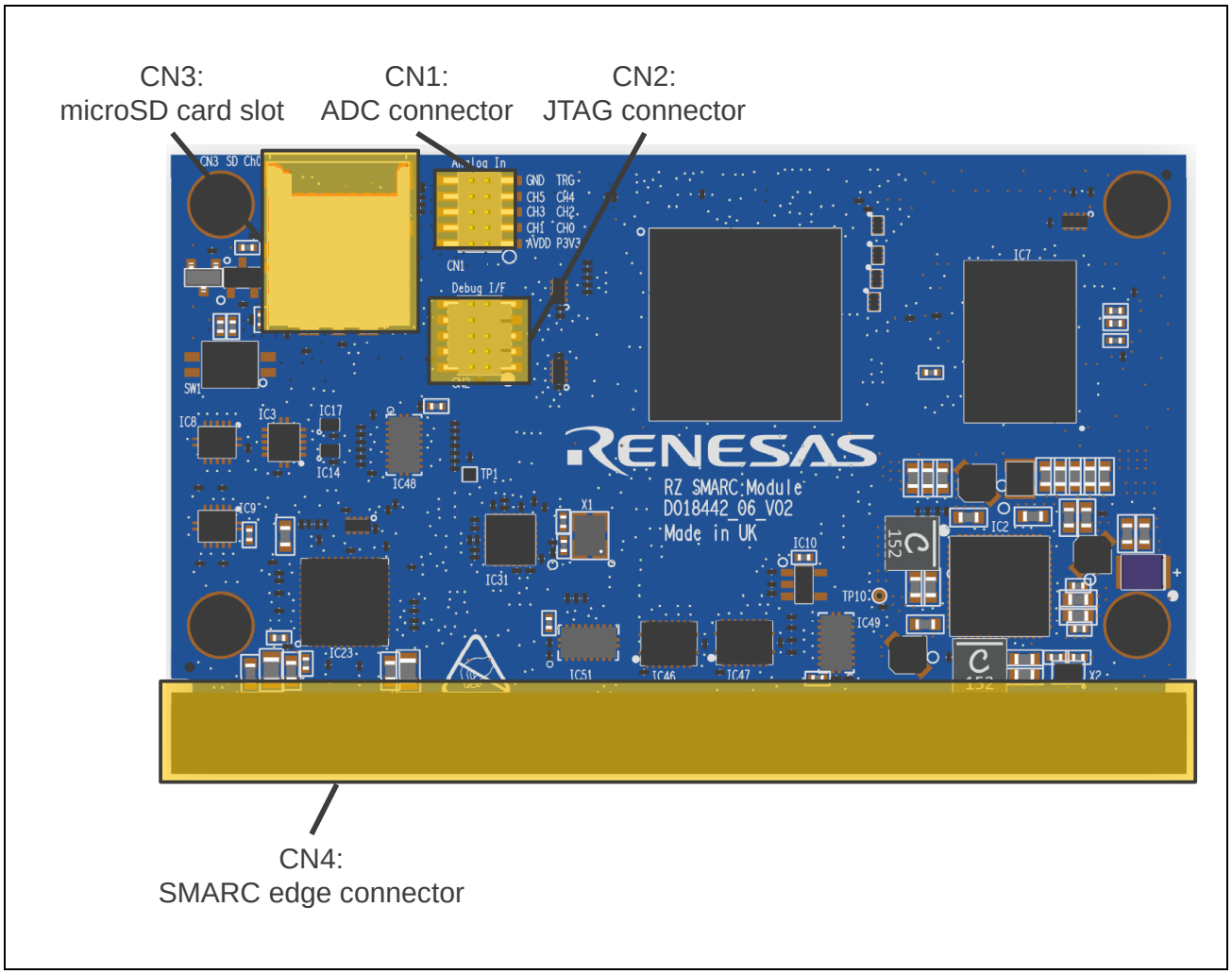



Figure 3.1 Layout of connectors of the RTK9744L23C01000BE (Top side)

### 3.1.1 ADC Connector (CN1)

RTK9744L23C01000BE contains a connector of ADC interface (CN1).

**Figure 3.2** illustrates the layout of connector pins. **Table 3.1** shows the assignment of connector pins.

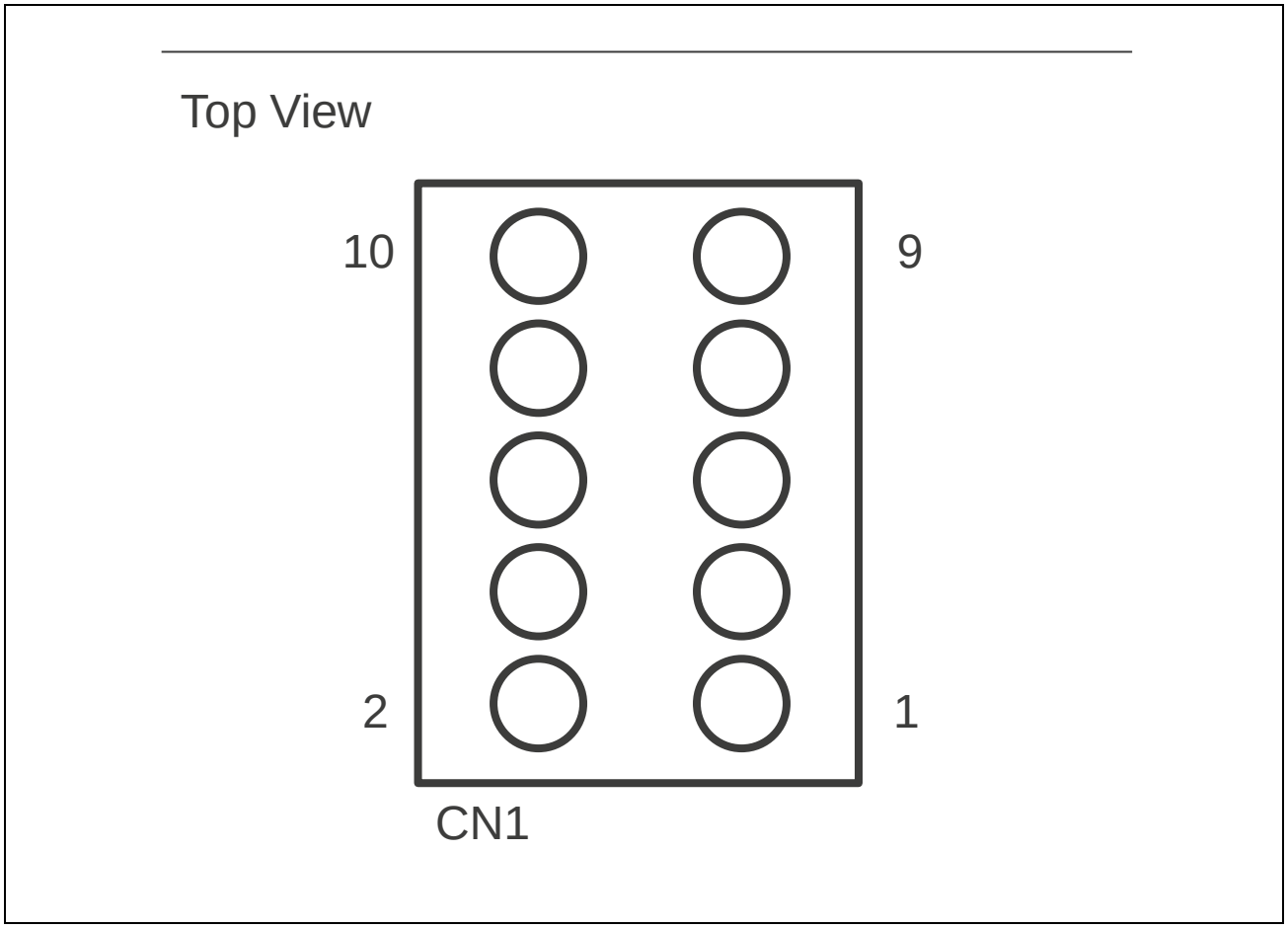



Figure 3.2 ADC Connector (CN1) Pin Layout Diagram

Table 3.1 ADC Connector (CN1) Pin Layout Table

| Pin | Signal Name |
|---|---|
| 1 | PVDD |
| 2 | ADC_AVDD18 |
| 3 | ADC_CH0 |
| 4 | ADC_CH1 |
| 5 | ADC_CH2 |
| 6 | ADC_CH3 |
| 7 | ADC_CH4 |
| 8 | ADC_CH5 |
| 9 | ADC_TRG |
| 10 | VSS |

### 3.1.2 JTAG Connector (CN2)

RTK9744L23C01000BE contains a connector of debug interface (CN2).

**Figure 3.3** illustrates the layout of connector pins. **Table 3.2** shows the assignment of connector pins.

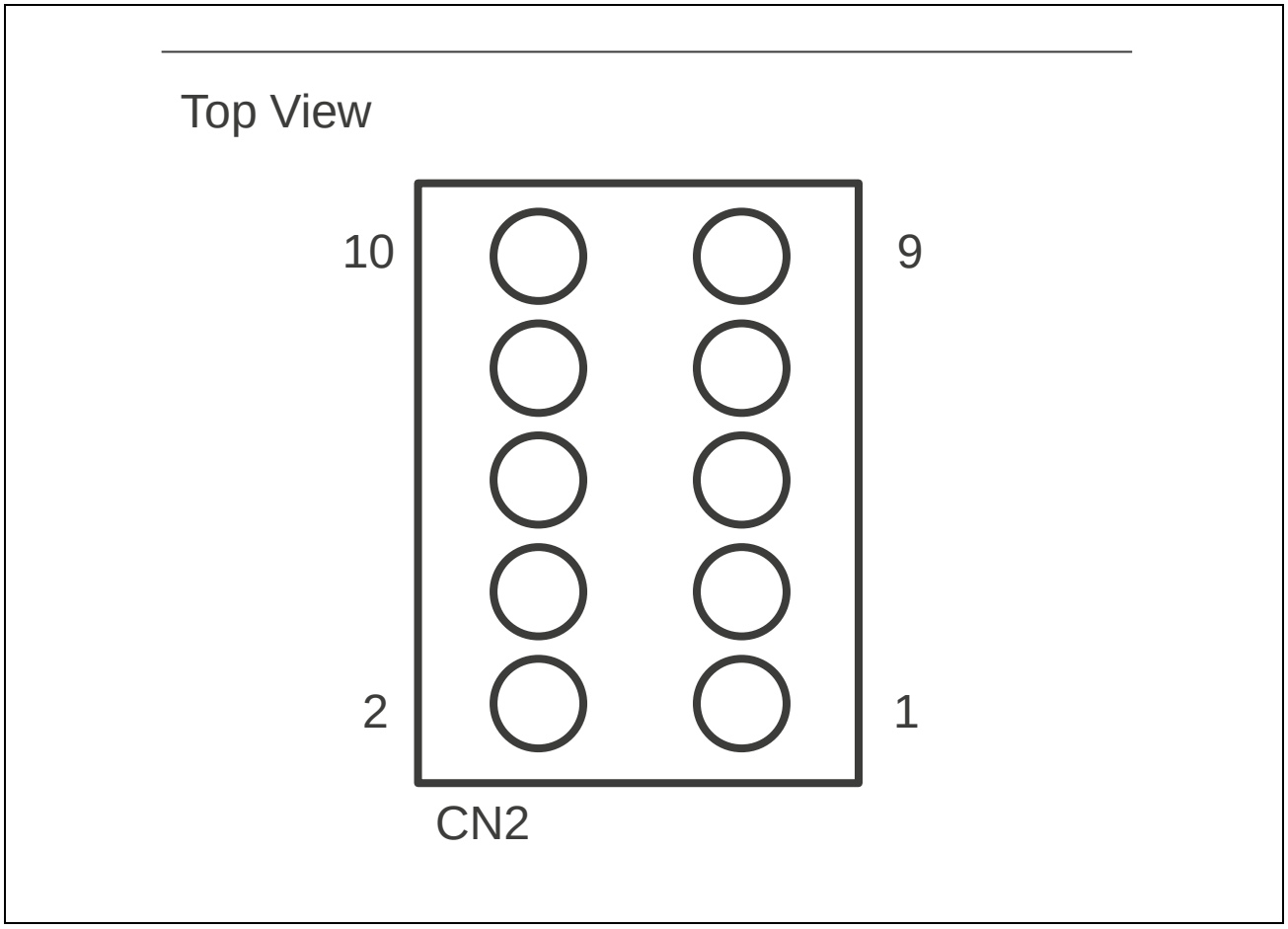



Figure 3.3 JTAG Connector (CN2) Pin Layout Diagram

Table 3.2 JTAG Connector (CN2) Pin Layout Table

| Pin | Signal Name |
|---|---|
| 1 | PVDD18 |
| 2 | TMS/SWDIO |
| 3 | VSS |
| 4 | TCK/SWDCLK |
| 5 | VSS |
| 6 | TDO |
| 7 | — |
| 8 | TDI |
| 9 | VSS |
| 10 | TRST# |

### 3.1.3 MicroSD Card Slot (CN3)

RTK9744L23C01000BE contains a microSD card slot (CN3).

**Figure 3.4** illustrates the layout of microSD card slot pins. **Table 3.3** shows the assignment of microSD card slot pins.

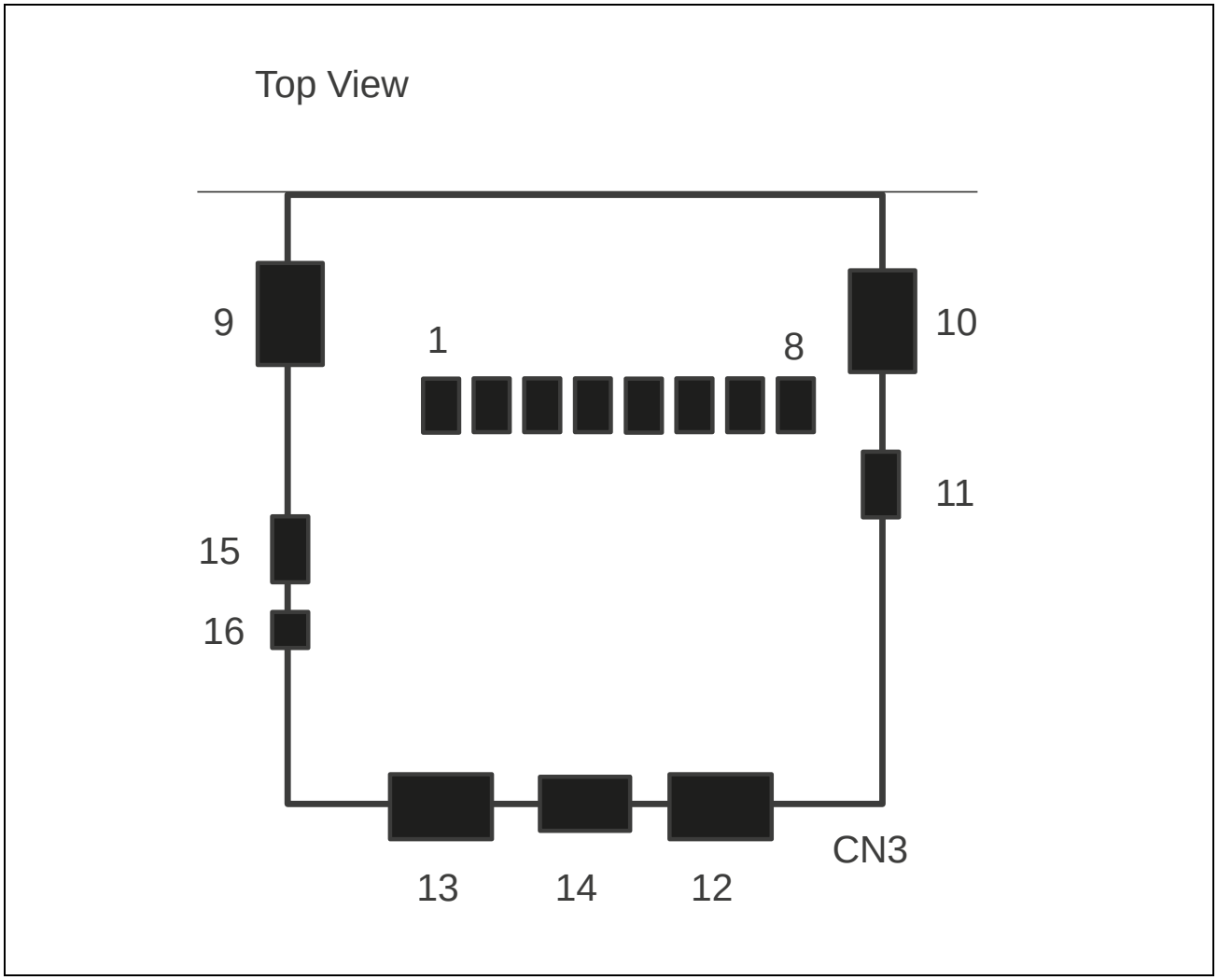



Figure 3.4 microSD Card Slot (CN3) Pin Layout Diagram

Table 3.3 microSD Card Slot (CN3) Pin Layout Table

| Pin | Signal Name |
|---|---|
| 1 | SD0_DATA2 |
| 2 | CD/SD0_DATA3 |
| 3 | SD0_CMD |
| 4 | SD0_PVDD |
| 5 | SD0_CLK |
| 6 | VSS |
| 7 | SD0_DATA0 |
| 8 | SD0_DATA1 |
| 9 | DETECT_SWITCH |
| 10 | DETECT_LEVER |

### 3.1.4 SMARC edge Connector (CN4)

RTK9744L23C01000BE can be connected to an external expansion board through the Carrier board connecting connector (CN4).

**Figure 3.5** illustrates the layout of Carrier board connecting connector pins. For the assignment of Carrier board connecting connector pins, please refer to the section4 “MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification (sget.org)”.

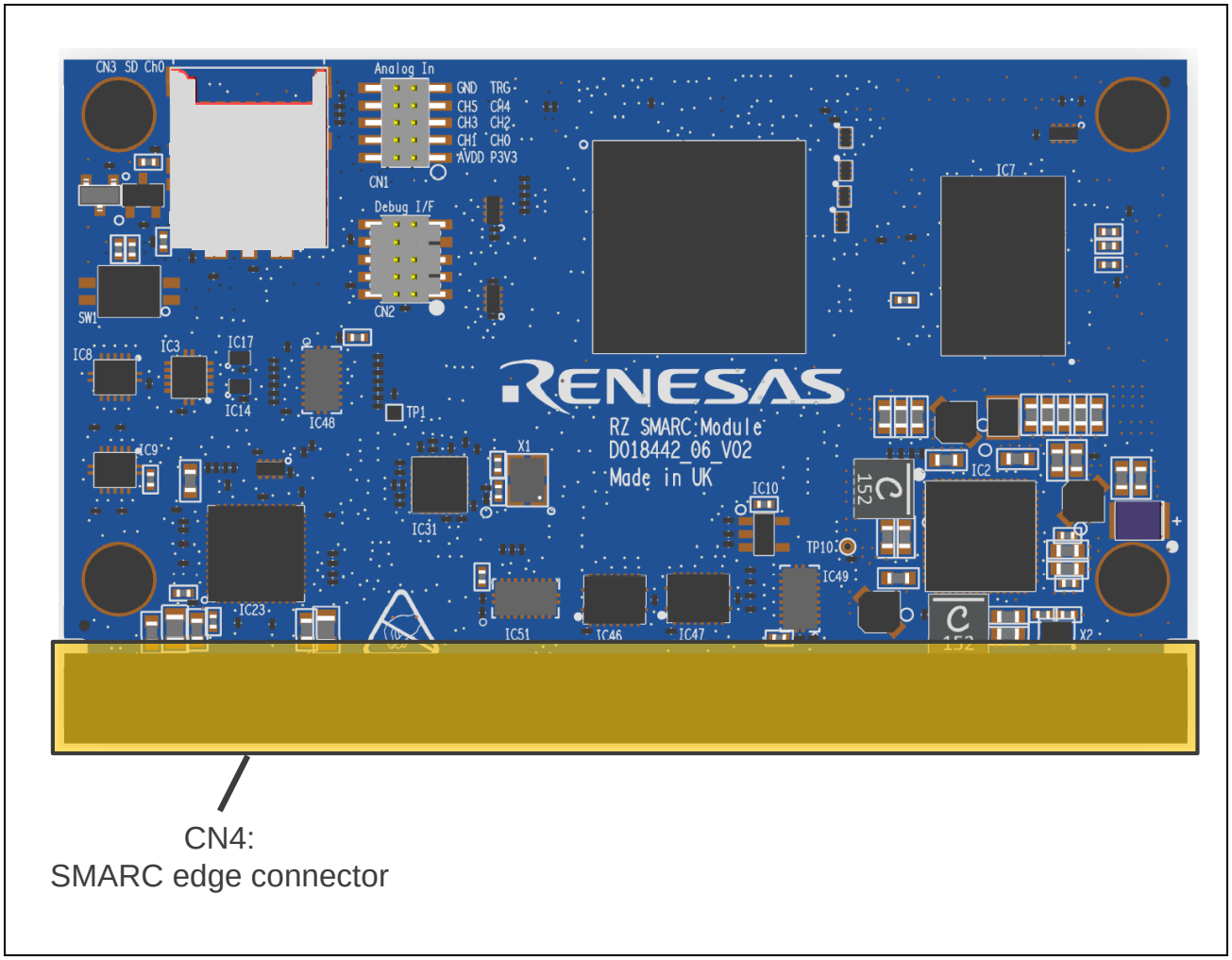



Figure 3.5 Layout of Carrier Board Connecting Pins

## 3.2 Layout of Operation Components

**Figure 3.6** illustrates the layout of operation components of the RTK9744L23C01000BE.

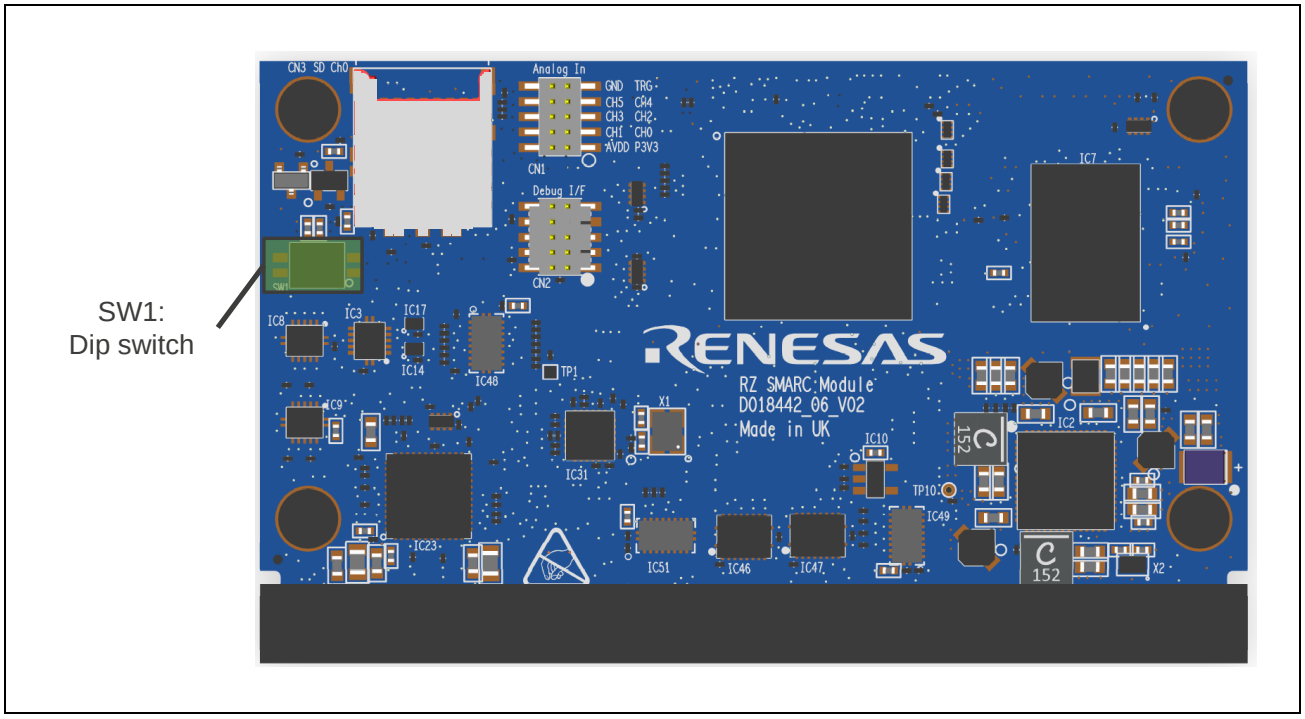



Figure 3.6 Layout of Operation Components of the RTK9744L23C01000BE

### 3.2.1 Functions of Switches and Mode Terminals

RTK9744L23C01000BE contains one switch.

**Table 3.4** lists mounted switches. **Figure 3.7** shows a block diagram of the System Setting interface.

Table 3.4 Switches Mounted on RTK9744L23C01000BE

| No. | Function | Note |
|---|---|---|
| SW1 | System setting DIP switch | For details, see **Table 3.5** |

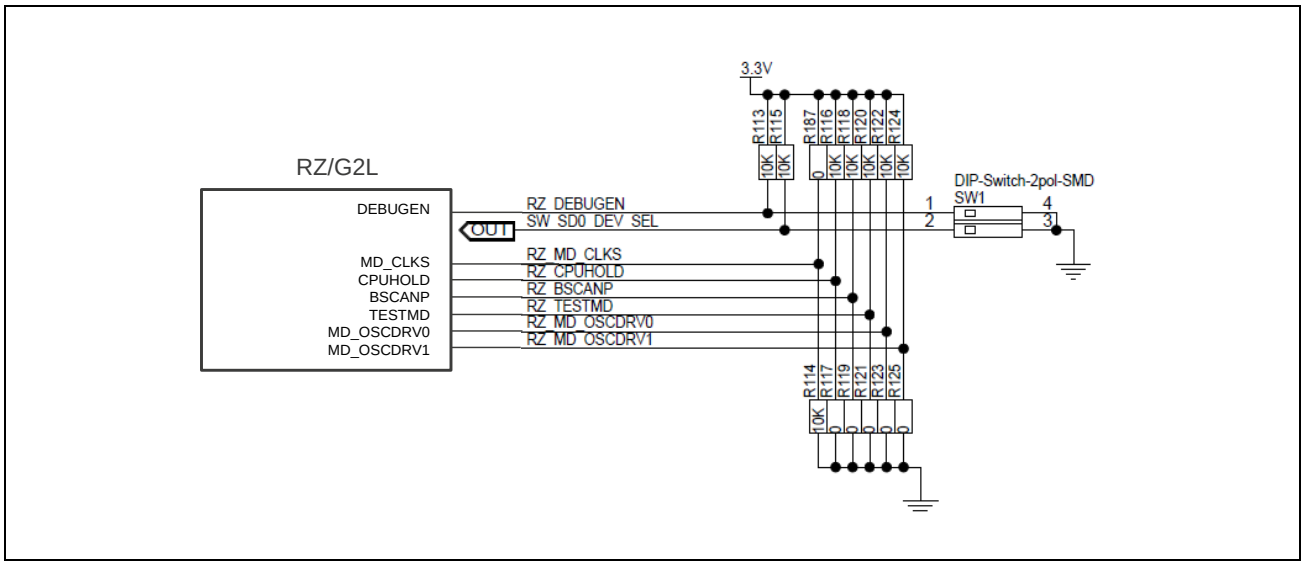



Figure 3.7 Block Diagram of System Setting I/F

**Table 3.5** provides functions of the DIP switch and **Figure 3.8** indicates a default terminal state.

Table 3.5 Functions of System Setting DIP Switch (SW1)

| No. | Setting | | Function |
|---|---|---|---|
| SW1-1 DEBUGEN | OFF | DEBUGEN="H" | Debugging with debuggers for ARM |
| | ON | DEBUGEN="L" | Normal operation |
| SW1-2 Selection SD/MMC | OFF | Selection="H" | Select the eMMC memory |
| | ON | Selection="L" | Select the SD card |

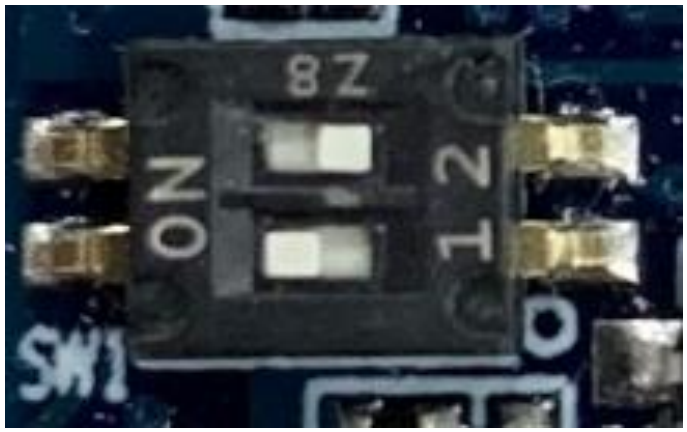



Figure 3.8 Default Setting of System Setting DIP Switch (SW1)

**Table 3.6** provides functions of mode terminals.

Table 3.6 Functions of System Setting

| No. | Setting | | Function |
|---|---|---|---|
| MD_CLKS | 0 | MD_CLKS="H" | SSCG ON |
| | 1 | MD_CLKS="L" | SSCG OFF |
| BSCANP | 0 | BSCANP="H" | Select the eMMC memory |
| | 1 | BSCANP="L" | Select the SD card |
| MD_OSCDRV0 | 0 | MD_OSCDRV0="H" | Not supported |
| | 1 | MD_OSCDRV0="L" | |
| MD_OSCDRV1 | 0 | MD_OSCDRV1="H" | Not supported |
| | 1 | MD_OSCDRV1="L" | |

# 4. Appendix

## 4.1 Type Name and Features of Each Board

This section describes the the type name and feature of each board here.

The SMARC Module Board is as follows. This picture is of the RTK9744L23C01000BE.


Figure 4.1 Top View of the SMARC Module Board

Please refer to the chapter 2 “Functional Specifications” onwards for the actual functions of the board.

| Board Name | Type Name | MPU |
|---|---|---|
| RZ/G2L SMARC Module Board | RTK9744L23C01000BE | RZ/G2L (R9A07G044L23GBG) |

The RZ SMARC Series Carrier Board is as follows. This picture is of the RTK97X4XXXB00000BE.


Figure 4.2 Top View of the RZ SMARC Series Carrier Board

| Board Name | Type Name |
|---|---|
| RZ SMARC Series Carrier Board | RTK97X4XXXB00000BE |

The Evaluation board Kit is as follows. This board consists of the SMARC Module Board and the RZ SMARC Series Carrier Board via a 314-pin 0.5-mm pitch connector. This picture is of the RTK9744L23S01000BE.

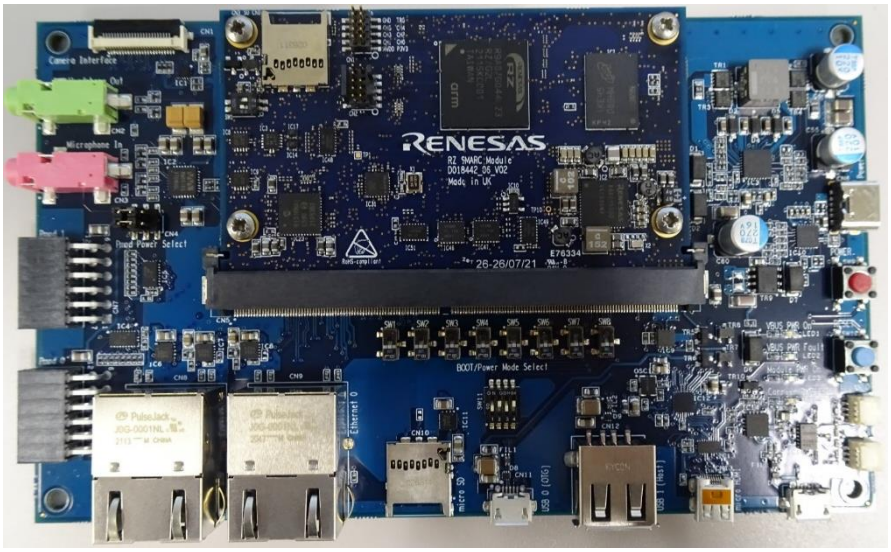



Figure 4.3 Top View of the Evaluation board Kit

The Evaluation board Kits are similarly designed to use a common board layout and to be pin-compatible.

| Board Name | Type Name | MPU |
|---|---|---|
| Evaluation board Kit for RZ/G2L MPU | RTK9744L23S01000BE | RZ/G2L (R9A07G044L23GBG) |

## 4.2 How to Identify Each SMARC Module Board

The differences between each SMARC Module Board are as follows. This picture is of the RTK9744L23C01000BE.

Table 4.1 Comparison of the RTK9744L23C01000BE and the RTK9754L23C01000BE

| Type Name | RTK9744L23C01000BE | RTK9754L23C01000BE |
|---|---|---|
| IC1 | RZ/G2L (R9A07G044L23GBG) | RZ/V2L (R9A07G054L23GBG) |

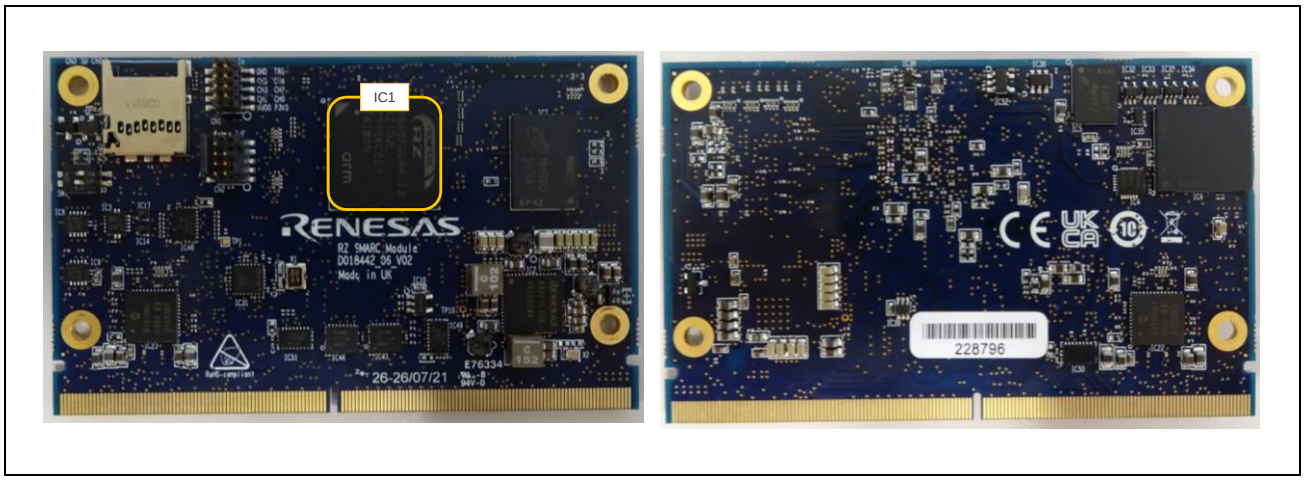



Figure 4.4 Comparison of Each SMARC Module Board

## 4.3 How to replace the SMARC Module Board

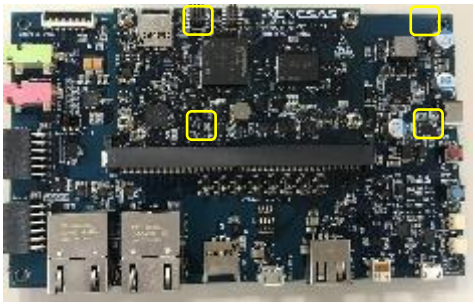
Please be careful when replacing the board as follows.

1. Remove the four screws.

NOTE

The screw thread is a special shape, so be careful not to crush the screw thread.

Please recommend to prepare a torx screwdriver which is a “T6” head size.




Specially shaped screw threads

Figure 4.5 How to remove the screws

2. Remove the screw and the SMARC Module Board will stand up at an angle. Slide it out.

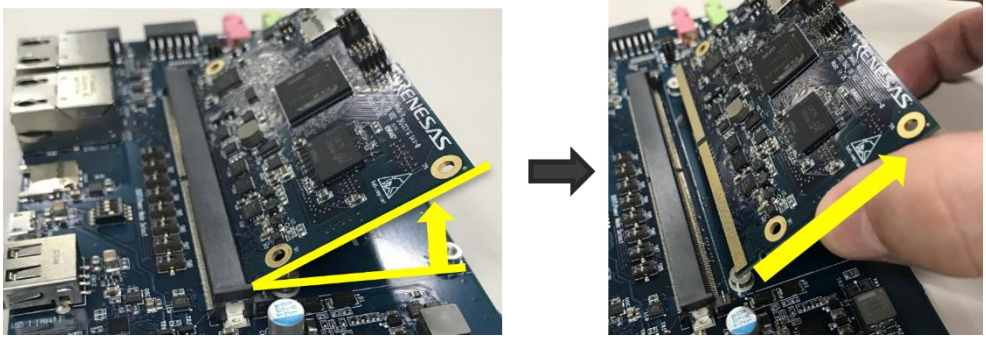


Figure 4.6 How to remove the SMARC Module Board

3. Insert the replacement the SMARC Module Board diagonally, then roll the board parallel to the RZ SMARC Series Carrier Board and fix it with screws.

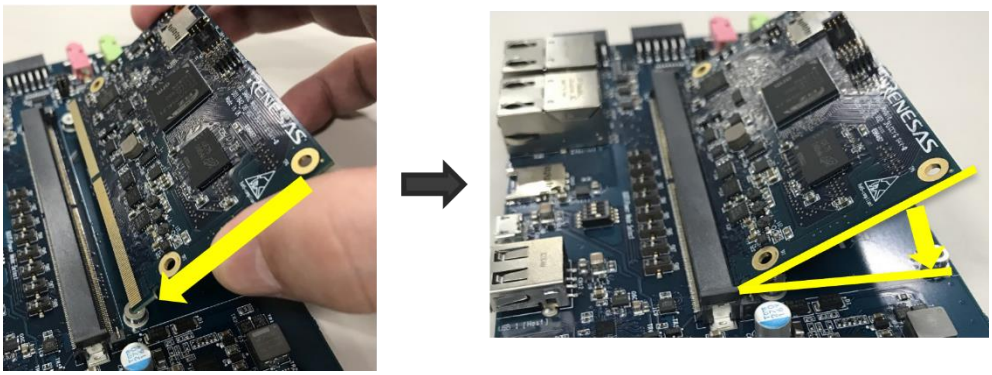


Figure 4.7 How to install the SMARC Module Board

| REVISION HISTORY | RZ Family / RZ/G, RZ/V Series<br>RZ/G2L, RZ/V2L SMARC Module Board |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Sep 27, 2021 | — | First edition issued |
| 1.01 | Oct 07, 2021 | 1 | For front cover, it is changed the description from "RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ/G2L, RZ/V2L SMARC Module Board".<br>It is changed the description from "RZ Family / RZ/G Series" to "RZ Family / RZ/G, RZ/V Series"<br>It is added the description "RTK9754L23C01000BE". |
| | | 7 | For Tytle, it is changed the description from "RZ Family / RZ/G Series RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ Family / RZ/G, RZ/V Series RZ/G2L, RZ/V2L SMARC Module Board".<br>For section "Overview", it is added the description "To begin with, only RTK9744L23C01000BE will be explained here. The difference between RTK9744L23C01000BE and RTK9754L23C01000BE is that RTK9754L23C01000BE uses Renesas Electronics microprocessor RZ/V2L "R9A07G054L23GBG", which is pin-compatible with RZ/G2L. In other words, they are functionally the same". |
| | | 60 | For Revision History, it is changed the description from "RZ Family / RZ/G Series RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ Family / RZ/G, RZ/V Series RZ/G2L, RZ/V2L SMARC Module Board". |
| | | 62 | For back cover, it is changed the description from "RZ Family / RZ/G Series" to "RZ Family / RZ/G, RZ/V Series". |
| 1.02 | Apr 26, 2022 | 8, 11 to 14, 52 to 57 | For each figure, the figure style has been improved. |
| | | 10 | For section title, it is changed the description from "Outside View" to "Physical View".<br>Figure 1.2 is modified. |
| | | 15 | For Table 1.2 and Table 1.3, the Recommend Optional Parts is removed. |
| | | 40, 42, 49 to 51 | For each interface, the description is added. |
| | | 41 | For DDR4 SDRAM, the description is added.<br>For Figure 2.2, the pin swap is modified. |
| | | 60 to 64 | Section 4 Appendix is added. |
| 1.10 | Dec 09, 2022 | 23, 39 | Restrictions on use are added.<br>When used in combination with the RZ SMARC Series Carrier Board (P/N: RTR97X4XXXB00000BE), CAN0 and CAN1 interface cannot be used because a CAN transceiver is not fitted on the RTK97X4XXXB00000BE. |
| 1.20 | Apr 03, 2024 | 18 to 34 | For section 2.2.2 "List of Pin Functions", the pin names, pin functions, and descriptions in the table are modified. |
| | | 34 | Restrictions on use are modified.<br>The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted.<br>The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already.<br>S.LOT# in the outer box label: 000251812 or later<br>S.LOT# label on the carrier board: 251812 or later |
| | | 37 | For section 2.4 "Gigabit Ethernet Interface", the figures are modified. |
| | | 40 | For section 2.7 "Reset Control", the figure is modified. |
| | | 41 | For section 2.8 "Power Supply Configuration", the figure is modified. |
| | | 43 | For section 2.9 "PMIC", the figure is modified |
| | | 44 | For section 2.10 "Debug Interface", the figure is modified. |
| | | 45 | For section 2.11.1 "eMMC Memory", the figure is modified. |

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