User's Manual

RZ/G2LC SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

RTK9744C22C01000BE

Renesas Electronics
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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

1.1 Overview

This document describes the specification of RTK9744C22C01000BE which is a Module board to evaluate the functions and performance of the Renesas Electronics microprocessor RZ/G2LC “R9A07G044C22GBG” and evaluate application software programs

The RTK9744C22C01000BE complies with the SMARC v2.1 and has following features.

- It is mounted with the following external memories.

  DDR4 SDRAM: 1GB × 1pc

  QSPI flash memory: 512Mb × 1pc

  eMMC memory: 64GB × 1pc
- The microSD card slot is implemented and used as an eSD for boot.
- It is implemented a 5-output clock generator “5P35023”.
- It is implemented a PMIC “RAA215300” as power supply circuit.
- The Ethernet PHY is implemented as standard and can send/receive data at 10/100/1000Mbps.
- Terminals not used on this board are connected to the 314-pin 0.5-mm pitch connector, which can be used in conjunction with a Carrier Board. It also allows for the development of the Carrier Board that meet the needs of development.
- The 10-pin connector for ARM Cortex Debug is implemented for connection to debug interface.

1.2 Configuration

Figure 1.1 shows an example of system configuration using RTK9744C22C01000BE.

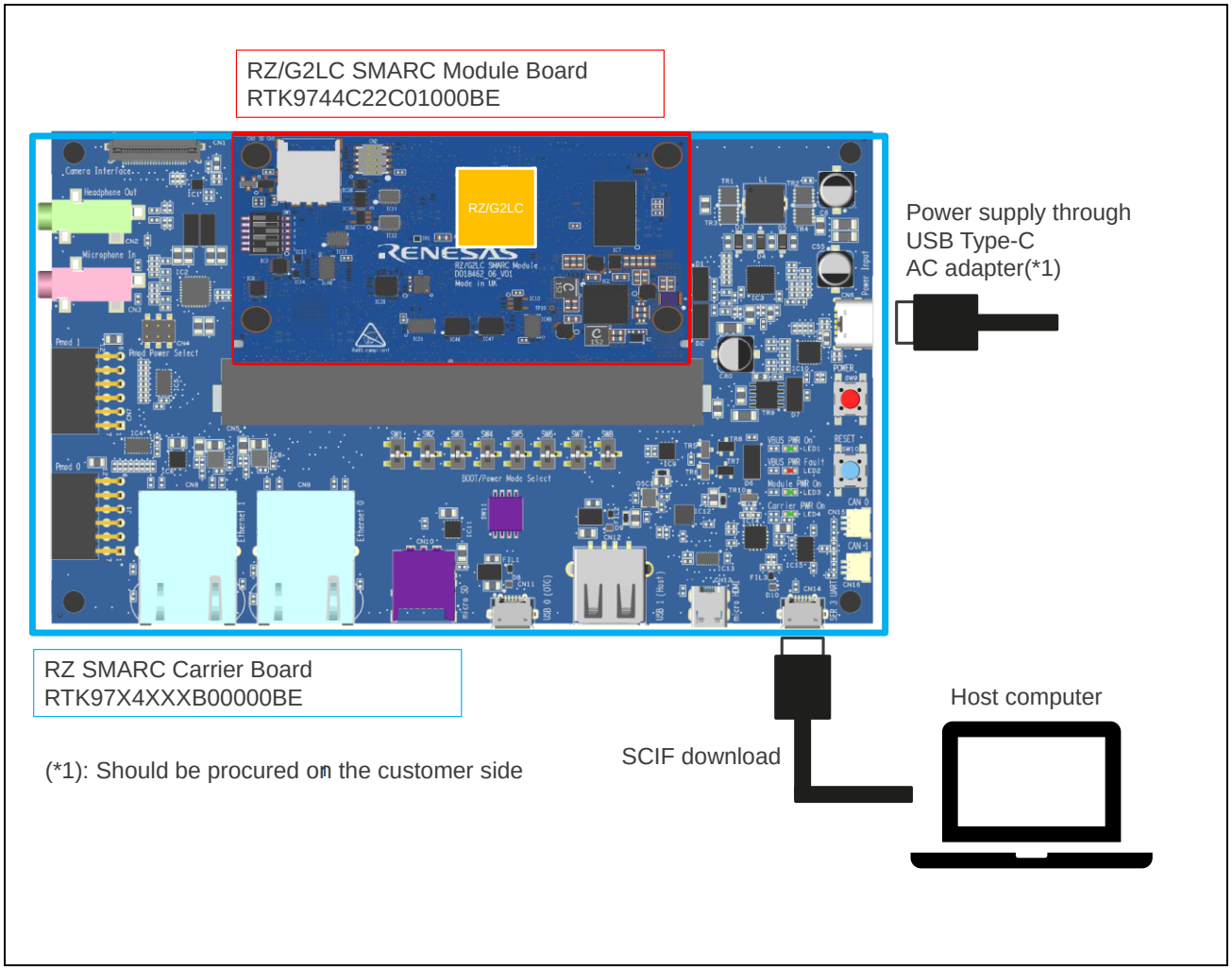

Figure 1.1 Example of System Configuration Using RTK9744C22C01000BE

1.3 Features

Table 1.1 shows the features of RTK9744C22C01000BE.

Table 1.1 Features of RTK9744C22C01000BE

Item	Details
CPU	RZ/G2LC Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.2GHz Arm Cortex-M33 clock: 200MHz AXI-bus clock: 200MHz APB-bus clock: 100MHz Internal memory Instruction cache: 32KB Data cache: 32KB Power voltage: 1.1V, I/O: 3.3V 361-Pin PBGA 0.5-mm pitch
Memory	QSPI flash memory: 512Mbit * 1pc DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc
Clock IC	Clock generator: 1pc
Ethernet IC	Ethernet PHY: 1pc
Connector	microSD card slot (4 bits): 1pc 10-pin connector for JTAG: 1pc SMARC edge connector (314 pins): 1pc
Switch	System setting DIP switch: 5 bits
Circuit board specifications	Dimensions: 82 mm * 50 mm Mount: Double-sided mounting (6 layers)

1.4 Outside View

Figure 1.2 and **Figure 1.3** show the outside view of RTK9744C22C01000BE.

Figure 1.2 Outside View of RTK9744C22C01000BE (Top View)

Figure 1.3 Outside View of RTK9744C22C01000BE (Bottom View)

1.5 Block Diagram

Figure 1.4 shows the block diagram of RTK9744C22C01000BE.

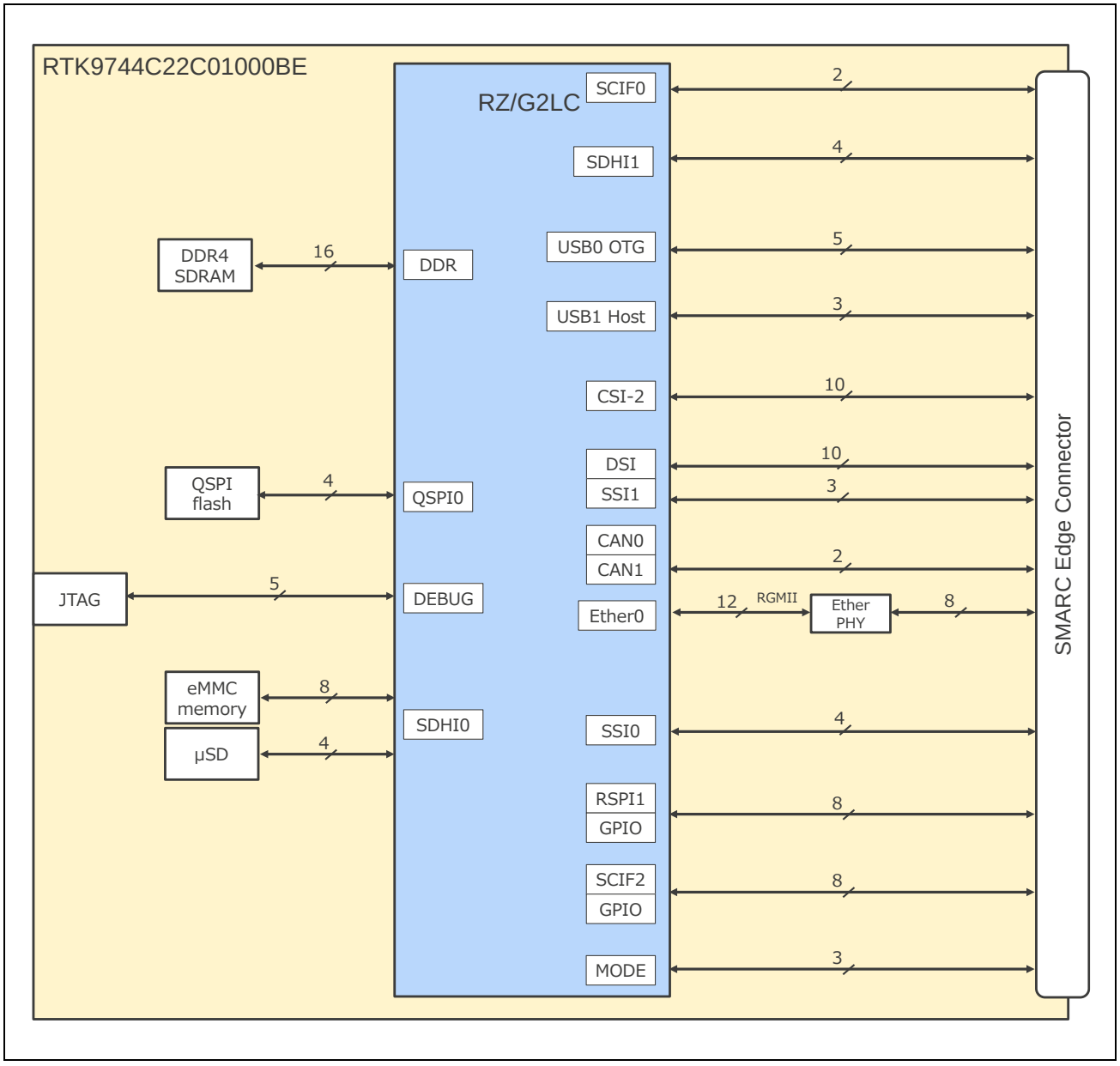

Figure 1.4 Block Diagram of RTK9744C22C01000BE

1.6 Layout Components

Figure 1.5 and **Figure 1.6** show the layout of main components of RTK9744C22C01000BE.

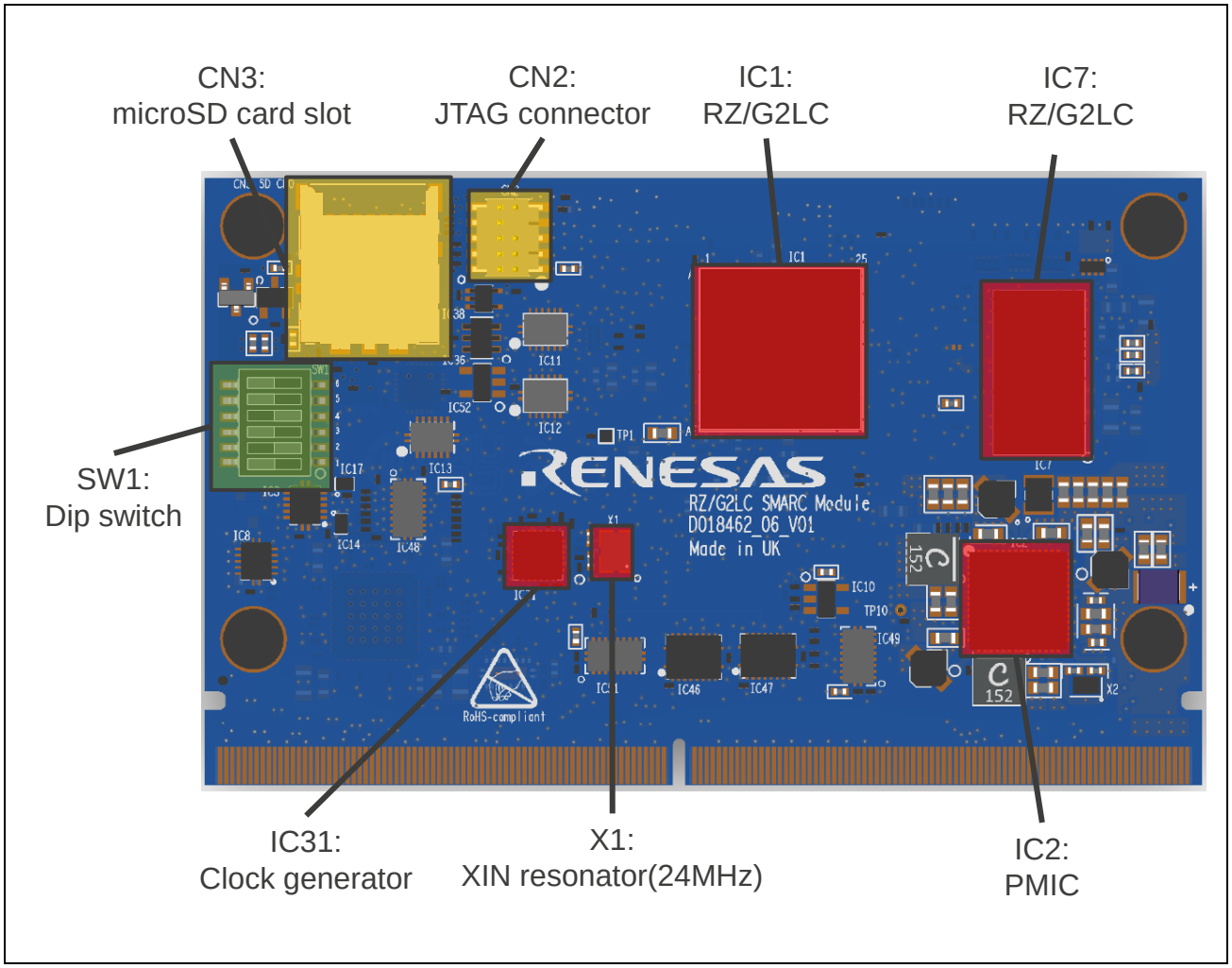

Figure 1.5 Layout of Components of RTK9744C22C01000BE (Top View)

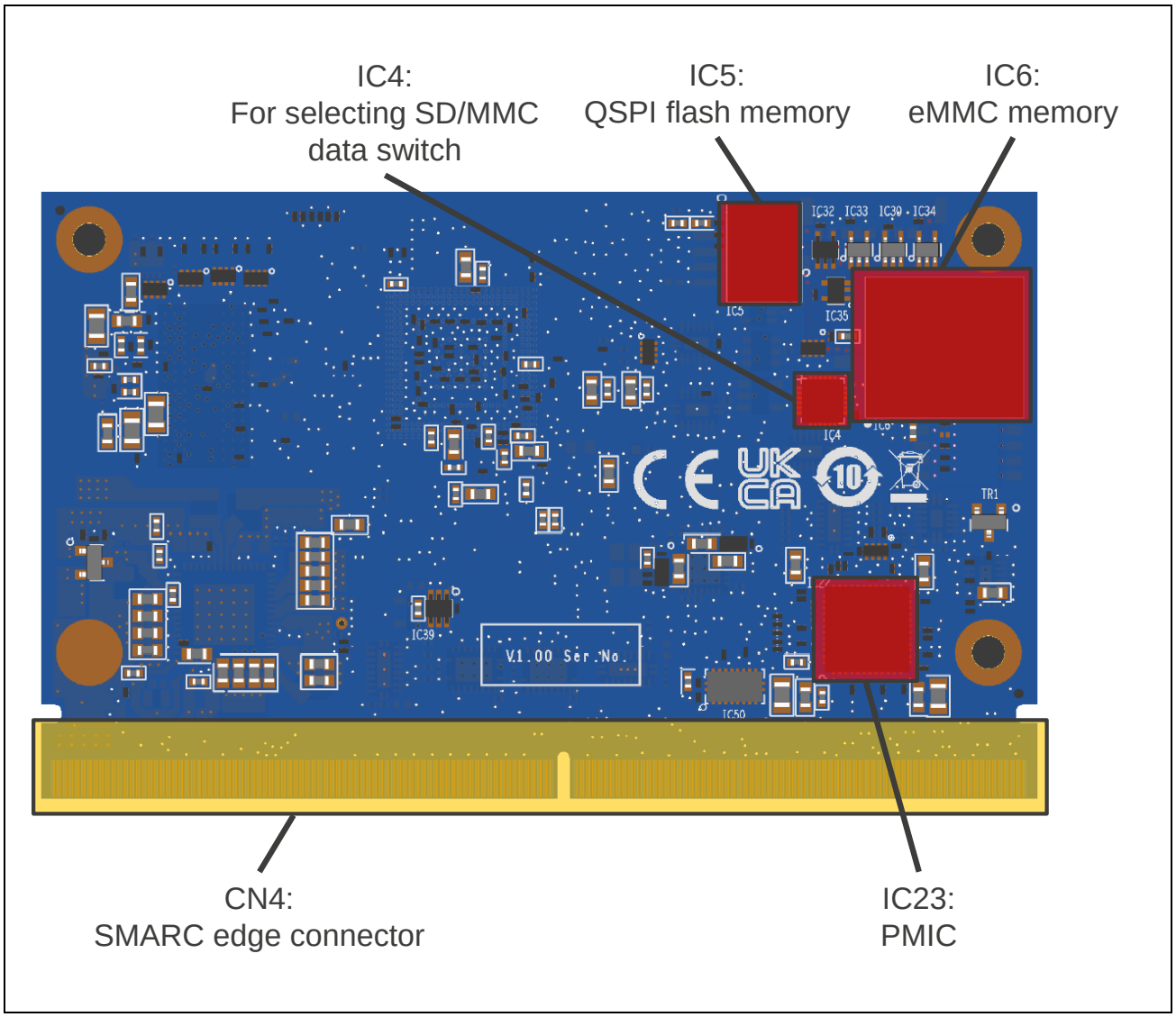

Figure 1.6 Layout of Components of RTK9744C22C01000BE (Bottom View)

Table 1.2 and **Table 1.3** list main components mounted on RTK9744C22C01000BE.

Table 1.2 Main Components on RTK9744C22C01000BE (1) IC

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Components
IC1	MPU	R9A07G044C22GBG (Renesas Electronics)	
IC2	PMIC	RAA215300A2GNP#HA0 (Renesas Electronics)	
IC4	Data switch IC	MAX4996LETG+ (MAXIM)	
IC5	QSPI flash memory	MT25QU512ABB8E12-0SIT (Micron)	
IC6	eMMC memory	MTFC64GASAQHD-IT (Micron)	
IC7	DDR4 SDRAM	MT40A512M16LY-062EIT:E (Micron)	
IC22	Ethernet PHY	KSZ9131RNXC (Microchip)	
IC31	Clock generator	5P35023B-629NLGI (Renesas Electronics)	
X1	Crystal resonator for XIN	FL2400022 (Diodes Inc)	24MHz

Table 1.3 Main Components on RTK9744C22C01000BE (2) Connector

Components Number	Component Name	Type (Manufacturer)	Recommend Optional Parts
CN2	JTAG connector (10pin)	FTSH-105-01-F-DV-007-K (Samtec)	
CN3	microSD card slot	504077-1891 (Molex)	
CN4	SMARC edge connector (314pin)		

1.7 Absolute Maximum Ratings

Table 1.4 lists absolute maximum ratings of RTK9744C22C01000BE.

Table 1.4 Absolute Maximum Ratings of RTK9744C22C01000BE

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	5.25V	Reference: Vss
—	Maximum power consumption	3A	Includes continuous RZ SMARC Series Carrier Board current consumption
Topr	Operating ambient temperature*1	0°C to 50°C	Do not expose to condensation or corrosive gases
Tstg	Storage temperature*1	-10°C to 60°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

1.8 Operating Condition

Table 1.5 lists operating conditions of RTK9744C22C01000BE.

Table 1.5 Operating Conditions of RTK9744C22C01000BE

Symbol	Item	Rated Value	Note
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

2. Functional Specifications

2.1 Overview of Functions

Table 2.1 lists function modules of RTK9744C22C01000BE.

Table 2.1 Function Modules of RTK9744C22C01000BE

Section	Function	Description
2.2	**MPU**	RZ/G2LC Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.2GHz Arm Cortex-M33 clock: 200MHz AXI-bus clock: 200MHz APB-bus clock: 100MHz
2.3	**Memory**	QSPI flash memory: 512Mbit * 1pc DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc
2.4	**Gigabit Ethernet Interface**	Connection between the Ethernet controller (E-MAC) and LAN connector via Ethernet PHY
2.5	**Clock Configuration**	System clock configuration
2.6	**Reset Control**	Reset control for RZ/G2LC mounted on RTK9744C22C01000BE.
2.7	**Power Supply Configuration**	System power supply configuration of RTK9744C22C01000BE and RTK97X4XXXB00000BE
2.8	**PMIC**	Connection between RZ/G2LC and PMIC
2.9	**Debug Interface**	Connection between Debug Interface and connector
2.10	**SD/MMC Host Interface**	Connection between SD/MMC Host Interface (SDHI) channel 0 and microSD card slot
—	Operating specification	Connectors and switches Details are described in section 3

2.2 MPU

2.2.1 Overview of RZ/G2LC

RTK9744C22C01000BE contains a 64-bit microprocessor RZ/G2LC that runs in synchronization with the CPU clock (max.1.2 GHz).

2.2.2 List of RZ/G2LC Functions

Table 2.2 lists RZ/G2LC pin functions used in RTK9744C22C01000BE.

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (1/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
F11	VDD18	VDD18	1.8V	—	—
C11	ABG_NCP_OUT	ABG_NCP_OUT	Connected to VSS via 1uF bypass capacitor (*1)	—	—
B10	AUDIO_CLK1	AUDIO_CLK1	Input 11.2896MHz from 5P35023 for generating the CD sampling rate (44.1kHz)	S38	AUDIO_MCK
B9	AUDIO_CLK2	AUDIO_CLK2	Input 12.2880MHz from 5P35023 for generating the DVD sampling rate (48.0kHz)	—	—
AC21	BSCANP	BSCANP	Initial setting: 0 (Pull down), should be controllable by resistor.	—	—
AC20	VSS	VSS	GND	—	—
AE13	CSI_CLKN	CSI_CLKN	24-pin FFC connector on the carrier board	P4	CSI1_CLK-
AD13	CSI_CLKP	CSI_CLKP	24-pin FFC connector on the carrier board	P3	CSI1_CLK+
AE14	CSI_DATA0_N	CSI_DATA0_N	24-pin FFC connector on the carrier board	P8	CSI1_RX0-
AD14	CSI_DATA0_P	CSI_DATA0_P	24-pin FFC connector on the carrier board	P7	CSI1_RX0+
AE12	CSI_DATA1_N	CSI_DATA1_N	24-pin FFC connector on the carrier board	P11	CSI1_RX1-
AD12	CSI_DATA1_P	CSI_DATA1_P	24-pin FFC connector on the carrier board	P10	CSI1_RX1+
AE15	CSI_DATA2_N	CSI_DATA2_N	24-pin FFC connector on the carrier board	P14	CSI1_RX2-
AD15	CSI_DATA2_P	CSI_DATA2_P	24-pin FFC connector on the carrier board	P13	CSI1_RX2+
AE11	CSI_DATA3_N	CSI_DATA3_N	24-pin FFC connector on the carrier board	P17	CSI1_RX3-
AD11	CSI_DATA3_P	CSI_DATA3_P	24-pin FFC connector on the carrier board	P16	CSI1_RX3+
Y10	CSI_VDD18	CSI_VDD18	1.8V	—	—
Y9	CSI_VDD18	CSI_VDD18	1.8V	—	—
E25	DDR_ADDR0	DDR_ADDR0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K25	DDR_ADDR1	DDR_ADDR1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P23	DDR_ADDR10	DDR_ADDR10	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H25	DDR_ADDR11	DDR_ADDR11	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
N23	DDR_ADDR12	DDR_ADDR12	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
D23	DDR_ADDR13	DDR_ADDR13	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H23	DDR_ADDR14	DDR_ADDR14	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
D25	DDR_ADDR15	DDR_ADDR15	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
C25	DDR_ADDR2	DDR_ADDR2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (2/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C24	DDR_ADDR3	DDR_ADDR3	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K23	DDR_ADDR4	DDR_ADDR4	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B24	DDR_ADDR5	DDR_ADDR5	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
J25	DDR_ADDR6	DDR_ADDR6	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
A24	DDR_ADDR7	DDR_ADDR7	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
F25	DDR_ADDR8	DDR_ADDR8	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B25	DDR_ADDR9	DDR_ADDR9	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
E24	DDR_BA0	DDR_BA0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
L24	DDR_BA1	DDR_BA1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
F23	DDR_BA2	DDR_BA2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
A23	DDR_CALIBRATION	DDR_CALIBRATION	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
J24	DDR_CAS#	DDR_CAS#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
M25	DDR_CKE	DDR_CKE	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P24	DDR_CLK_N	DDR_CLK_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P25	DDR_CLK_P	DDR_CLK_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
N24	DDR_CS0#	DDR_CS0#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
L23	DDR_CS1#	DDR_CS1#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
U23	DDR_DM0	DDR_DM0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y24	DDR_DM1	DDR_DM1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T24	DDR_DQ0	DDR_DQ0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y25	DDR_DQ1	DDR_DQ1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W23	DDR_DQ10	DDR_DQ10	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AD25	DDR_DQ11	DDR_DQ11	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AE23	DDR_DQ12	DDR_DQ12	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AA23	DDR_DQ13	DDR_DQ13	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AC24	DDR_DQ14	DDR_DQ14	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AE24	DDR_DQ15	DDR_DQ15	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
R24	DDR_DQ2	DDR_DQ2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W24	DDR_DQ3	DDR_DQ3	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T25	DDR_DQ4	DDR_DQ4	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
U25	DDR_DQ5	DDR_DQ5	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
R25	DDR_DQ6	DDR_DQ6	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T23	DDR_DQ7	DDR_DQ7	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AD24	DDR_DQ8	DDR_DQ8	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AA24	DDR_DQ9	DDR_DQ9	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V24	DDR_DQS0_N	DDR_DQS0_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V25	DDR_DQS0_P	DDR_DQS0_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB25	DDR_DQS1_N	DDR_DQS1_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB24	DDR_DQS1_P	DDR_DQS1_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
M24	DDR_ODT0	DDR_ODT0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (3/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
L25	DDR_ODT1	DDR_ODT1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H24	DDR_RAS#	DDR_RAS#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B23	DDR_RESET#	DDR_RESET#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB23	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
G25	DDR_WE#	DDR_WE#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y18	DEBUGEN	DEBUGEN	DIP_SW (SW1)	—	—
AD19	DSI_CLKN	DSI_CLKN	MIPI-DSI to HDMI conversion IC on the carrier board	S135	DSI0_CLK-
AE19	DSI_CLKP	DSI_CLKP	MIPI-DSI to HDMI conversion IC on the carrier board	S134	DSI0_CLK+
AD18	DSI_DATA0_N	DSI_DATA0_N	MIPI-DSI to HDMI conversion IC on the carrier board	S126	DSI0_D0-
AE18	DSI_DATA0_P	DSI_DATA0_P	MIPI-DSI to HDMI conversion IC on the carrier board	S125	DSI0_D0+
AD20	DSI_DATA1_N	DSI_DATA1_N	MIPI-DSI to HDMI conversion IC on the carrier board	S129	DSI0_D1-
AE20	DSI_DATA1_P	DSI_DATA1_P	MIPI-DSI to HDMI conversion IC on the carrier board	S128	DSI0_D1+
AD17	DSI_DATA2_N	DSI_DATA2_N	MIPI-DSI to HDMI conversion IC on the carrier board	S132	DSI0_D2-
AE17	DSI_DATA2_P	DSI_DATA2_P	MIPI-DSI to HDMI conversion IC on the carrier board	S131	DSI0_D2+
AD21	DSI_DATA3_N	DSI_DATA3_N	MIPI-DSI to HDMI conversion IC on the carrier board	S138	DSI0_D3-
AE21	DSI_DATA3_P	DSI_DATA3_P	MIPI-DSI to HDMI conversion IC on the carrier board	S137	DSI0_D3+
Y14	DSI_VDD18	DSI_VDD18	1.8V	—	—
Y15	DSI_VDD18	DSI_VDD18	1.8V	—	—
N1	P28_1/ET0_LINKSTA	ET0_LINKSTA	Ethernet0 PHY (KSZ9131RNXC)	—	—
T1	P27_1/ET0_MDC/RSPI1_SSL/MTIOC8D	ET0_MDC	Ethernet0 PHY (KSZ9131RNXC)	—	—
R2	P28_0/ET0_MDIO	ET0_MDIO	Ethernet0 PHY (KSZ9131RNXC)	—	—
N2	P24_1/ET0_RX_CTL_RX_DV/SSI1_RCK/POE4_N	ET0_RX_CTL_RX_DV	Ethernet0 PHY (KSZ9131RNXC)	—	—
P2	P24_0/ET0_RXC_RX_CLK/SSI1_BCK/POE0_N	ET0_RXC_RX_CLK	Ethernet0 PHY (KSZ9131RNXC)	—	—
N3	P25_0/ET0_RXD0/SSI1_TXD/POE8_N	ET0_RXD0	Ethernet0 PHY (KSZ9131RNXC)	—	—
P3	P25_1/ET0_RXD1/SSI1_RXD/POE10_N	ET0_RXD1	Ethernet0 PHY (KSZ9131RNXC)	—	—
R1	P26_0/ET0_RXD2/RSPI1_CK/MTIOC8A	ET0_RXD2	Ethernet0 PHY (KSZ9131RNXC)	—	—
P1	P26_1/ET0_RXD3/RSPI1_MOSI/MTIOC8B	ET0_RXD3	Ethernet0 PHY (KSZ9131RNXC)	—	—
L1	P20_1/ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX	ET0_TX_CTL_TX_EN	Ethernet0 PHY (KSZ9131RNXC)	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (4/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
M2	P20_0/ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK	ET0_TXC_TX_CLK	Ethernet0 PHY (KSZ9131RNXC)	—	—
L2	P20_2/ET0_TXD0/RSPI0_MISO/CAN0_RX	ET0_TXD0	Ethernet0 PHY (KSZ9131RNXC)	—	—
K1	P21_0/ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN	ET0_TXD1	Ethernet0 PHY (KSZ9131RNXC)	—	—
J1	P21_1/ET0_TXD2/CAN0_RX_DATARATE_EN	ET0_TXD2	Ethernet0 PHY (KSZ9131RNXC)	—	—
J2	P22_0/ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA	ET0_TXD3	Ethernet0 PHY (KSZ9131RNXC)	—	—
M3	PVDD182533_0	PVDD182533_0	1.8V	—	—
N6	PVDD182533_0	PVDD182533_0	1.8V	—	—
AA3	EXCLK	EXCLK	Input 24MHz from 5P35023 for generating system clock	—	—
T3	VDD18	VDD18	1.8V	—	—
A4	MD_BOOT0	MD_BOOT0	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
C5	MD_BOOT1	MD_BOOT1	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
B5	MD_BOOT2	MD_BOOT2	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
A21	MD_CLKS	MD_CLKS	Initial setting: 1 (Pull Up), should be controllable by resistor.	—	—
C21	MD_OSCDRV0	MD_OSCDRV0	Initial setting: 0 (Pull Down), should be controllable by resistor.	—	—
B21	MD_OSCDRV1	MD_OSCDRV1	Initial setting: 0 (Pull Down), should be controllable by resistor.		
AD2	NMI	NMI	Connected to the test pin (TP1)	—	—
F14	OTP_VDD18	OTP_VDD18	1.8V	—	—
M6	PLL1_AVDD18	PLL1_AVDD18	1.8V	—	—
V3	PLL23_AVDD18	PLL23_AVDD18	1.8V	—	—
W3	PLL23_AVDD18	PLL23_AVDD18	1.8V	—	—
T6	PLL23_DVDD11	PLL23_DVDD11	1.1V	—	—
U6	PLL23_DVDD11	PLL23_DVDD11	1.1V	—	—
P20	PLL4_AVDD18	PLL4_AVDD18	1.8V	—	—
Y11	PLL5_AVDD18	PLL5_AVDD18	1.8V	—	—
Y13	PLL5_DVDD11	PLL5_DVDD11	1.1V	—	—
F12	PLL6_AVDD18	PLL6_AVDD18	1.8V	—	—
Y2	PRST#	PRST#	Input system reset signal from RAA215300	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (5/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AC4	PVDD	PVDD	3.3V	—	—
Y6	PVDD	PVDD	3.3V	—	—
AC14	PVDD	PVDD	3.3V	—	—
AD10	PVDD	PVDD	3.3V	—	—
Y16	PVDD	PVDD	3.3V	—	—
Y19	PVDD	PVDD	3.3V	—	—
C3	PVDD	PVDD	3.3V	—	—
F15	PVDD	PVDD	3.3V	—	—
F17	PVDD	PVDD	3.3V	—	—
F20	PVDD	PVDD	3.3V	—	—
B8	QSPI_INT#	QSPI_INT#	Connected to pull-up by SPI_PVDD power supply (*1)	—	—
A8	QSPI_RESET#	QSPI_RESET#	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
A7	QSPI_WP#	QSPI_WP#	Unused	—	—
B7	QSPI0_IO0	QSPI0_IO0	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
A6	QSPI0_IO1	QSPI0_IO1	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
C8	QSPI0_IO1	QSPI0_IO1	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
C7	QSPI0_IO2	QSPI0_IO2	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
C6	QSPI0_IO3	QSPI0_IO3	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
A5	QSPI0_SPCLK	QSPI0_SPCLK	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
E1	QSPI0_SSL	QSPI0_SSL	QSPI Flash Memory (MT25QU512ABB8E12-0SIT)	—	—
C1	SD0_CLK	SD0_CLK	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
F3	SD0_CMD	SD0_CMD	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
E2	SD0_DATA0	SD0_DATA0	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
D1	SD0_DATA1	SD0_DATA1	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
B1	SD0_DATA2	SD0_DATA2	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
D2	SD0_DATA3	SD0_DATA3	eMMC Memory (MTFC64GASAQHD-IT) or uSD ch0 card slot	—	—
C2	SD0_DATA4	SD0_DATA4	eMMC Memory (MTFC64GASAQHD-IT)	—	—
D3	SD0_DATA5	SD0_DATA5	eMMC Memory (MTFC64GASAQHD-IT)	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (6/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
E3	SD0_DATA6	SD0_DATA6	eMMC Memory (MTFC64GASAQHD-IT)	—	—
F6	SD0_DATA7	SD0_DATA7	eMMC Memory (MTFC64GASAQHD-IT)	—	—
H6	SD0_PVDD	SD0_PVDD	1.8V/3.3V	—	—
B2	SD0_RST#	SD0_RST#	eMMC Memory (MTFC64GASAQHD-IT)	—	—
H3	SD1_CLK	SD1_CLK	uSD ch1 card slot on the carrier board	P36	SDIO_CK
F2	SD1_CMD	SD1_CMD	uSD ch1 card slot on the carrier board	P34	SDIO_CMD
G2	SD1_DATA0	SD1_DATA0	uSD ch1 card slot on the carrier board	P39	SDIO_D0
G3	SD1_DATA1	SD1_DATA1	uSD ch1 card slot on the carrier board	P40	SDIO_D1
G1	SD1_DATA2	SD1_DATA2	uSD ch1 card slot on the carrier board	P41	SDIO_D2
H2	SD1_DATA3	SD1_DATA3	uSD ch1 card slot on the carrier board	P42	SDIO_D3
J3	SD1_PVDD	SD1_PVDD	1.8V/3.3V	—	—
K6	SD1_PVDD	SD1_PVDD	1.8V/3.3V	—	—
B13	P38_1/SCIF0_RXD/ GTETRGB/CAN0_TX/ MTIOC4B/USB1_OV RCUR	SCIF0_RXD	Debug UART on the carrier board	P141	SER3_RX
C13	P38_0/SCIF0_TXD/ GTETRGA/CAN_CLK /MTIOC4A/USB1_VB USEN	SCIF0_TXD	Debug UART on the carrier board	P140	SER3_TX
AC22	VSS	VSS	GND	—	—
C22	VSS	VSS	GND	—	—
F10	SPI_PVDD	SPI_PVDD	1.8V	—	—
F8	SPI_PVDD	SPI_PVDD	1.8V	—	—
J13	VDD	VDD	1.1V	—	—
M14	VSS	VSS	GND	—	—
P14	VSS	VSS	GND	—	—
P6	VSS	VSS	GND	—	—
R6	VSS	VSS	GND	—	—
U11	VDD	VDD	1.1V	—	—
AD22	VSS	VSS	GND	—	—
T14	VSS	VSS	GND	—	—
U13	VDD	VDD	1.1V	—	—
U2	TCK/SWDCLK	TCK/SWDCLK	Connected to JTAG connector (CN2)	—	—
V6	VSS	VSS	GND	—	—
AE22	VSS	VSS	GND	—	—
F7	VSS	VSS	GND	—	—
J15	VDD	VDD	1.1V	—	—
L15	VSS	VSS	GND	—	—
W2	TDI	TDI	Connected to JTAG connector (CN2)	—	—
A9	VSS	VSS	GND	—	—
C23	VSS	VSS	GND	—	—
N15	VSS	VSS	GND	—	—
U15	VDD	VDD	1.1V	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (7/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
V2	TDO	TDO	Connected to JTAG connector (CN2)	—	—
C9	VSS	VSS	GND	—	—
E23	VSS	VSS	GND	—	—
J17	VDD	VDD	1.1V	—	—
R15	VSS	VSS	GND	—	—
Y17	VSS	VSS	GND	—	—
AC15	VSS	VSS	GND	—	—
F9	VSS	VSS	GND	—	—
G23	VSS	VSS	GND	—	—
L17	VDD	VDD	1.1V	—	—
V1	TMS/SWDIO	TMS/SWDIO	Connected to JTAG connector (CN2)	—	—
F16	VSS	VSS	GND	—	—
J23	VSS	VSS	GND	—	—
K10	VSS	VSS	GND	—	—
N17	VDD	VDD	1.1V	—	—
W1	TRST#	TRST#	Connected to JTAG connector (CN2)	—	—
W6	VDD18	VDD18	1.8V	—	—
R17	VDD	VDD	1.1V	—	—
M10	VSS	VSS	GND	—	—
K16	VSS	VSS	GND	—	—
M23	VSS	VSS	GND	—	—
AC9	USB_AVDD18	USB_AVDD18	1.8V	—	—
AC8	USB_RREF	USB_RREF	Connect to GND via the 1.8Ω resistor	—	—
AC5	USB_VDD18	USB_VDD18	1.8V	—	—
AC6	USB_VDD18	USB_VDD18	1.8V	—	—
Y7	USB_VDD33	USB_VDD33	3.3V	—	—
Y8	USB_VDD33	USB_VDD33	3.3V	—	—
AD6	VSS	VSS	GND	—	—
AE6	VSS	VSS	GND	—	—
AC7	VSS	VSS	GND	—	—
AE9	VSS	VSS	GND	—	—
AE8	USB0_DM	USB0_DM	USB2.0 OTG on the carrier board	P61	USB0-
AD8	USB0_DP	USB0_DP	USB2.0 OTG on the carrier board	P60	USB0+
AD9	USB0_VBUSIN	USB0_VBUSIN	USB2.0 OTG on the carrier board	P63	USB0_VBUS_DET
AE7	USB1_DM	USB1_DM	USB2.0 Host on the carrier board	P66	USB1-
AD7	USB1_DP	USB1_DP	USB2.0 Host on the carrier board	P65	USB1+
U17	VDD	VDD	1.1V	—	—
M20	VDD	VDD	1.1V	—	—
J9	VDD	VDD	1.1V	—	—
L9	VDD	VDD	1.1V	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (8/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
N9	VDD	VDD	1.1V	—	—
R9	VDD	VDD	1.1V	—	—
J11	VDD	VDD	1.1V	—	—
U9	VDD	VDD	1.1V	—	—
M16	VSS	VSS	GND	—	—
P10	VSS	VSS	GND	—	—
R23	VSS	VSS	GND	—	—
P16	VSS	VSS	GND	—	—
T10	VSS	VSS	GND	—	—
V23	VSS	VSS	GND	—	—
A1	VDD	VDD	1.1V	—	—
F1	VSS	VSS	GND	—	—
H1	VSS	VSS	GND	—	—
U1	VSS	VSS	GND	—	—
AA1	VSS	VSS	GND	—	—
AC1	VSS	VSS	GND	—	—
AE1	VSS	VSS	GND	—	—
T2	VSS	VSS	GND	—	—
AC10	VSS	VSS	GND	—	—
AE10	VSS	VSS	GND	—	—
L11	VSS	VSS	GND	—	—
N11	VSS	VSS	GND	—	—
R11	VSS	VSS	GND	—	—
AC11	VSS	VSS	GND	—	—
A12	VSS	VSS	GND	—	—
K12	VSS	VSS	GND	—	—
T16	VSS	VSS	GND	—	—
AC16	VSS	VSS	GND	—	—
AD16	VSS	VSS	GND	—	—
AE16	VSS	VSS	GND	—	—
AC17	VSS	VSS	GND	—	—
F18	VSS	VSS	GND	—	—
AC18	VSS	VSS	GND	—	—
F19	VSS	VSS	GND	—	—
Y23	VSS	VSS	GND	—	—
AC23	VSS	VSS	GND	—	—
AD23	VSS	VSS	GND	—	—
D24	VSS	VSS	GND	—	—
F24	VSS	VSS	GND	—	—
G24	VSS	VSS	GND	—	—
K24	VSS	VSS	GND	—	—
U24	VSS	VSS	GND	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (9/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A25	VSS	VSS	GND	—	—
AA2	VSS	VSS	GND	—	—
AC19	VSS	VSS	GND	—	—
AC2	VSS	VSS	GND	—	—
C20	VSS	VSS	GND	—	—
M12	VSS	VSS	GND	—	—
N25	VSS	VSS	GND	—	—
P12	VSS	VSS	GND	—	—
G20	VSS	VSS	GND	—	—
R3	VSS	VSS	GND	—	—
T12	VSS	VSS	GND	—	—
W25	VSS	VSS	GND	—	—
AA25	VSS	VSS	GND	—	—
J20	VSS	VSS	GND	—	—
U3	VSS	VSS	GND	—	—
Y12	VSS	VSS	GND	—	—
AC12	VSS	VSS	GND	—	—
AC25	VSS	VSS	GND	—	—
L20	VSS	VSS	GND	—	—
Y3	VSS	VSS	GND	—	—
B6	VSS	VSS	GND	—	—
G6	VSS	VSS	GND	—	—
F13	VSS	VSS	GND	—	—
L13	VSS	VSS	GND	—	—
N13	VSS	VSS	GND	—	—
R13	VSS	VSS	GND	—	—
N20	VSS	VSS	GND	—	—
R20	VSS	VSS	GND	—	—
U20	VSS	VSS	GND	—	—
Y20	VSS	VSS	GND	—	—
AE25	VSS	VSS	GND	—	—
AB3	VSS	VSS	GND	—	—
C4	VSS	VSS	GND	—	—
A22	VSS	VSS	GND	—	—
AC13	VSS	VSS	GND	—	—
B22	VSS	VSS	GND	—	—
J6	VSS	VSS	GND	—	—
K14	VSS	VSS	GND	—	—
L6	VSS	VSS	GND	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (10/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C19	WDTOVF_PERROUT#	WDTOVF_PERROUT#	Input hardware reset signal from RAA215300	—	—
AB2	XIN	XIN	GND	—	—
AB1	XOUT	XOUT	Open	—	—
A19	RIIC1_SCL	RIIC1_SCL	MIPI-DSI to HDMI conversion IC on the carrier board	S139	I2C_LCD_CK
A20	RIIC1_SDA	RIIC1_SDA	MPI-DSI to HDMI conversion IC on the carrier board	S140	I2C_LCD_DAT
B19	RIIC0_SDA	RIIC0_SDA	24-pin FFC connector on the carrier board	S1	I2C_CAM1_CK
B20	RIIC0_SCL	RIIC0_SCL	24-pin FFC connector on the carrier board	S2	I2C_CAM1_DAT
C12	P0_0/IRQ0/SCI0_RXD/GTIOC0A/MTIOC0A/SCIF3_TXD	IRQ0	Ethernet0 PHY (KSZ9131RNXC)	—	—
B12	P0_1/IRQ1/SCI0_TXD/GTIOC0B/MTIOC0B/SCIF3_RXD	P0_1	24-pin FFC connector on the carrier board	P109	GPIO1/CAM1_PWR#
B3	P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A	SD0_CD	uSD ch0 card slot	—	—
A3	P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B	P18_1	uSD ch0 card slot For controlling power on/off of the card slot	—	—
A2	P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA	SD1_CD	uSD ch1 card slot on the carrier board	P35	SDIO_CD#
B4	P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL	P19_1	For selecting the device connected to the SD/MMC ch0 interface Input SD0_DEV_SEL signal to identify the device connected to the SD ch0 interface by software	—	—
K2	P22_1/ET0_TX_ER/SSI0_RCK/CAN1_RX/MTCLKB	P22_1	PMOD0 Type-2A on the carrier board	P114	GPIO6/TACHIN
L3	P23_0/ET0_TX_COL/SSI0_TXD/CAN1_TX_DATARATE_EN/MTCLKC	P23_0	PMOD0 Type-2A on the carrier board	P115	GPIO7
K3	P23_1/ET0_TX_CRS/SSI0_RXD/CAN1_RX_DATARATE_EN/MTCLKD	P23_1	PMOD1 Type-6A on the carrier board	S142	GPIO12
M1	P27_0/ET0_RX_ER/RSPI1_MISO/MTIOC8C	P27_0	PMOD1 Type-6A on the carrier board	S123	GPIO13
A13	P39_0/SCIF0_SCK/GTETRGC/CAN0_RX/MTIOC4C	P39_0	RAA215300 For selecting voltage of the uSD ch0 card	—	—
B14	P39_1/SCIF0_CTS/GTETRGD/CAN0_TX_DATARATE_EN/MTIOC4D	P39_1	RAA215300 For selecting voltage of the uSD ch1 card	—	—

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (11/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A14	P39_2/SCIF0_RTS/CAN0_RX_DATARATE_EN	P39_2	uSD ch1 card slot on the carrier board For controlling power on/off of the card slot	P37	SDIO_PWR_EN
AE5	P4_0/USB0_VBUSEN/SCIF2_TXD/MTIOC7A/ADC_TRG	USB0_VBUSEN	USB2.0 OTG on the carrier board Include gate USB0_VBUSEN state	P62	USB0_EN_OC#
AD5	P4_1/SCIF2_RXD/MTIOC7B	P4_1	PMOD0 Type-2A on the carrier board	P113	GPIO5/PWM_OUT#
C14	P40_0/SCIF1_TXD/GTIOC6A/CAN1_TX/MTIC5U/SCI0_RXD	SCIF1_TXD CAN1_TX	PMOD1 Type-3A or CAN transceiver ch1 (*2) on the carrier board (*2)	P134 P145	SER1_TX CAN1_TX
B15	P40_1/SCIF1_RXD/GTIOC6B/CAN1_RX/MTIC5V/SCI0_TXD	SCIF1_TXD CAN1_RX	PMOD1 Type-3A or CAN transceiver ch1 (*2) on the carrier board (*2)	P135 P146	SER1_RX CAN1_RX
C15	P40_2/SCIF1_SCK/CAN1_TX_DATARATE_EN/MTIC5W/SCI0_SCK	P40_2	For selecting the device connected to the SD/MMC ch0 interface	—	—
A16	P41_0/SCIF1_CTS/GTIOC7A/CAN1_RX_DATARATE_EN/GTIOC3A/SCI0_CTS_N_RTS_N	SCIF1_CTS	PMOD1 Type-3A on the carrier board	P132	SER0_CTS#-
B16	P41_1/SCIF1_RTS/GTIOC7B/GTIOC3B	SCIF1_RTS	PMOD1 Type-3A on the carrier board	P131	SER0_RTS#-
AD3	P42_0/USB1_VBUSEN/RSPI2_CK/CAN_CLK/SCIF2_TXD/MTIOC7A	USB1_VBUSEN	USB2.0 Host on the carrier board Include gate USB1_OVRCUR state	P67	USB1_EN_OC#
AC3	P42_1/USB1_OVRCUR/RSPI2_MOSI/CAN0_TX/SCIF2_RXD/MTIOC7B	USB1_OVRCUR	USB2.0 Host on the carrier board Include gate USB1_VBUSEN state	P67	USB1_EN_OC#
AE2	P42_2/ADC_TRG/RSPI2_MISO/CAN0_RX/SCIF2_SCK/MTIOC7C	P42_2	PMOD1 Type-3A on the carrier board	P119	GPIO11
Y1	P42_3/RIIC2_SDA/RSPI2_SSL/CAN0_TX_DATARATE_EN/SCIF2_CTS/MTIOC7D	RIIC2_SDA	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the carrier board	S49	I2C_GP_DAT
AD1	P42_4/RIIC2_SCL/CAM_FIELD/CAN0_RX_DATARATE_EN/SCIF2_RTS	RIIC2_SCL	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the carrier board	S48	I2C_GP_CK
C16	P43_0/RSPI0_CK/GTIOC4A/GTIOC6A/IRQ4/MTIOC8A	IRQ4	PMOD0 Type-2A on the carrier board	P112	GPIO4/HAD_RST#
A15	P43_1/RSPI0_MOSI/GTIOC4B/GTIOC6B/IRQ5/MTIOC8B	P43_1	MIPI DSI to HDMI conversion IC on the carrier board	P110	GPIO2

Table 2.2 List of RZ/G2LC Pin Function Selection Used on the RTK9744C22C01000BE (12/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A17	P43_2/RSPI0_MISO/GTIOC5A/IRQ6/MTIOC8C	P43_2	Unused	P108	GPIO0/CAM0_PWR#
B17	P43_3/RSPI0_SSL/GTIOC5B/IRQ7/MTIOC8D	IRQ7	PMOD1 Type-3A on the carrier board	P118	GPIO10
B18	P44_0/RSPI1_CK/SSI1_BCK/CAN1_TX/MTIOC3A/GTIOC6A	RSPI1_CK CAN_TX	PMOD0 Type-2A or CAN transceiver ch1 (*2) on the carrier board	P56 P146	SPI1_CK CAN1_TX
C17	P44_1/RSPI1_MOSI/SSI1_RCK/CAN1_RX/MTIOC3B/GTIOC6B	RSPI1_MOSI CAN1_RX	PMOD0 Type-2A or CAN transceiver ch1 (*2) on the carrier board	P58 P145	SPI1_DO CAN1_RX
A18	P44_2/RSPI1_MISO/SSI1_TXD/CAN1_TX_DATARATE_EN/MTIOC3C/GTIOC7A	RSPI1_MISO P44_2	PMOD0 Type-2A or PMOD Type-6A on the carrier board	P57 P116	SPI1_DIN GPIO8
C18	P44_3/RSPI1_SSL/SSI1_RXD/CAN1_RX_DATARATE_EN/MTIOC3D/GTIOC7B	RSPI1_SSL P44_3	PMOD0 Type-2A or CAN transceiver ch1 (*2) used as standby input or PMOD Type-6A on the carrier board	P54 P117	SPI1_CS0# GPIO9
A10	P45_0/SSI0_BCK/POE0_N/SCI1_RXD	SSI0_BCK	Audio codec or MPI DSI to HDMI conversion IC on the carrier board	S42 S53	I2S0_CK I2S2_CK
C10	P45_1/SSI0_RCK/POE4_N/SCI1_TXD	SSI0_RCK	Audio codec or MPI DSI to HDMI conversion IC on the carrier board	S39 S50	I2S0_LRCK I2S2_LRCK
B11	P45_2/SSI0_TXD/POE8_N/SCI1_SCK	SSI0_TXD	Audio codec or MPI DSI to HDMI conversion IC on the carrier board	S40 S51	I2S0_SDOUT I2S2_SDOUT
A11	P45_3/SSI0_RXD/POE10_N/SCI1_CTS_N_RTS_N	SSI0_RXD	Audio codec on the carrier board	S41 S52	I2S0_SDIN I2S2_SDIN
AD4	P5_0/USB0_OVRCUR/SCIF2_SCK/MTIOC7C/SSI2_BCK	USB0_OVRCUR	USB 2.0 OTG on the carrier board Include gate USB0_OVRCUR state	P62	USB0_EN_OC#
AE3	P5_1/USB0_OTG_ID/SCIF2_CTS/MTIOC7D/SSI2_RCK	USB0_OTG_ID	USB 2.0 OTG on the carrier board USB0_OTG_ID state	P64	USB0_OTG_ID
AE4	P5_2/USB0_OTG_EXICEN/SCIF2_RTS/SSI2_DATA	P5_2	24-pin FFC connector on the carrier board	P111	GPIO3/CAM1_RST#

NOTES

1. This pin is treated as open in the schematic, but this is incorrect.
2. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted.
   The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already.
   S.LOT# in the outer box label: 000251812 or later
   S.LOT# label on the carrier board: 251812 or later

2.3 Memory

In addition to QSPI flash memory and DDR4 SDRAM are mounted in RTK9744C22C01000BE as external memory.

Refer to the following for details

2.3.1 QSPI Flash Memory

Figure 2.1 shows a block diagram of the QSPI interface.

The QSPI flash memory is controlled by the SPI multi-I/O bus controller (SPIBSC) with built-in RZ/G2LC. This flash memory defaults to standard SPI mode initially and supports operation at 66 MHz clock frequency.

NOTE

As for the pull-up resistor of the clock line “RZ_QSPI0_SPCLK”, please put the resistor as you wish.

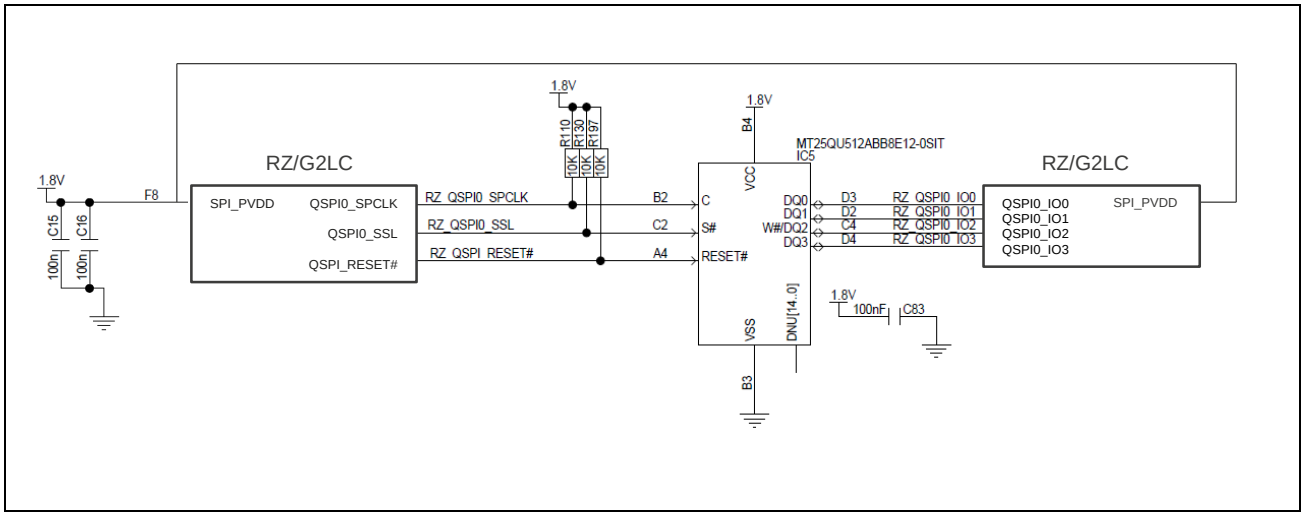

Figure 2.1 Block Diagram of QSPI I/F

2.3.2 DDR4 SDRAM

Figure 2.2 shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the memory controller (MEMC) with built-in RZ/G2LC. This interface supports a data bus width of 16-bit and a data transfer rate of 1600Mbps.

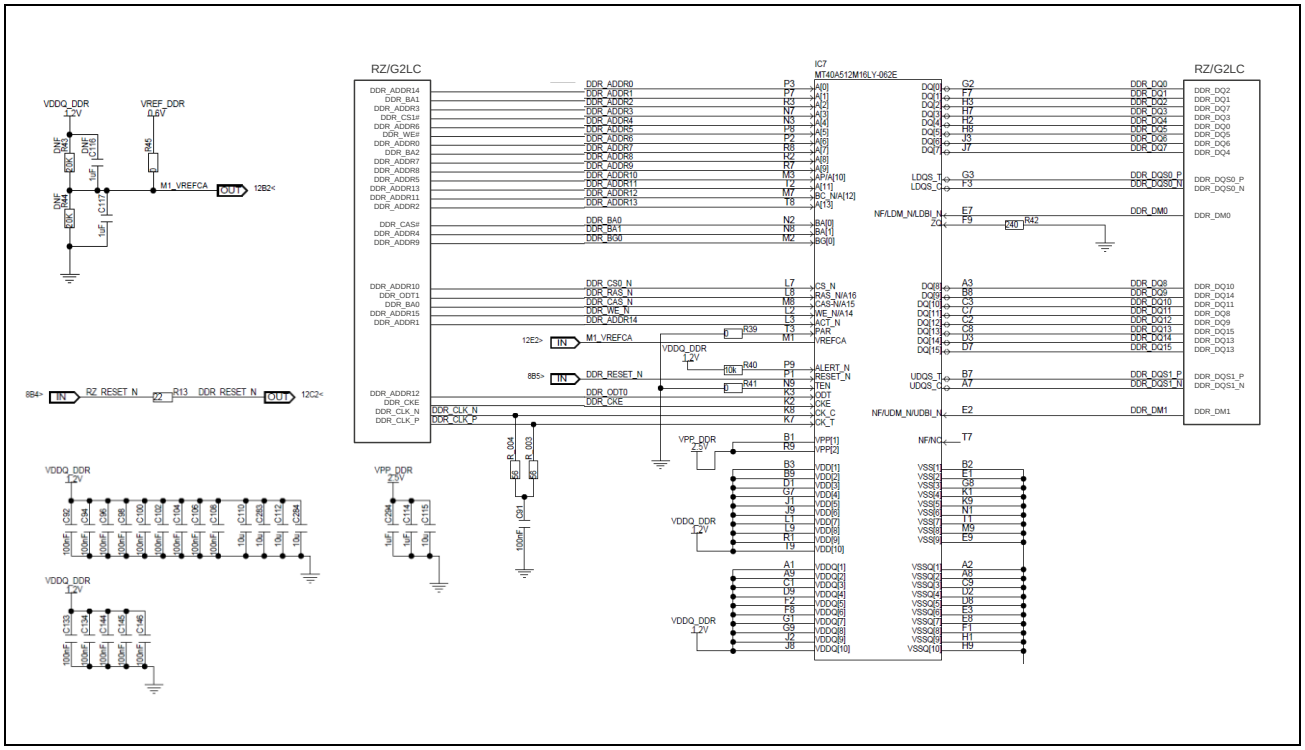

Figure 2.2 Block Diagram of DDR4 SDRAM

2.4 Gigabit Ethernet Interface

Figure 2.3 shows a block diagram of Ethernet0 interface.

The Ethernet interface uses an RGMII Ethernet Physical Layer Transceiver (PHY). The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY. This interface complies with IEEE802.3 PHY RGMII.

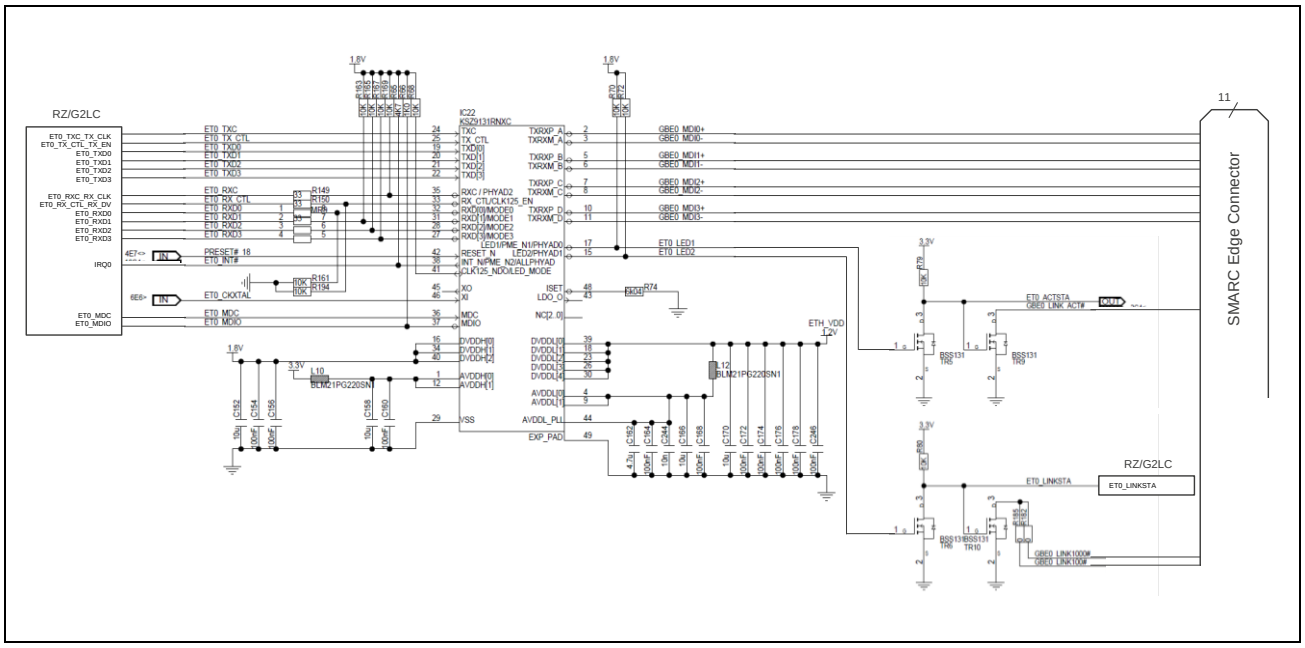

Figure 2.3 Block Diagram of Ethernet0 I/F

2.5 Clock Configuration

Figure 2.4 shows a block diagram of the Clock configuration.

NOTE

MIPI-DSI Interface supports operation up to Full HD, 60fps mode.

SD Interface supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

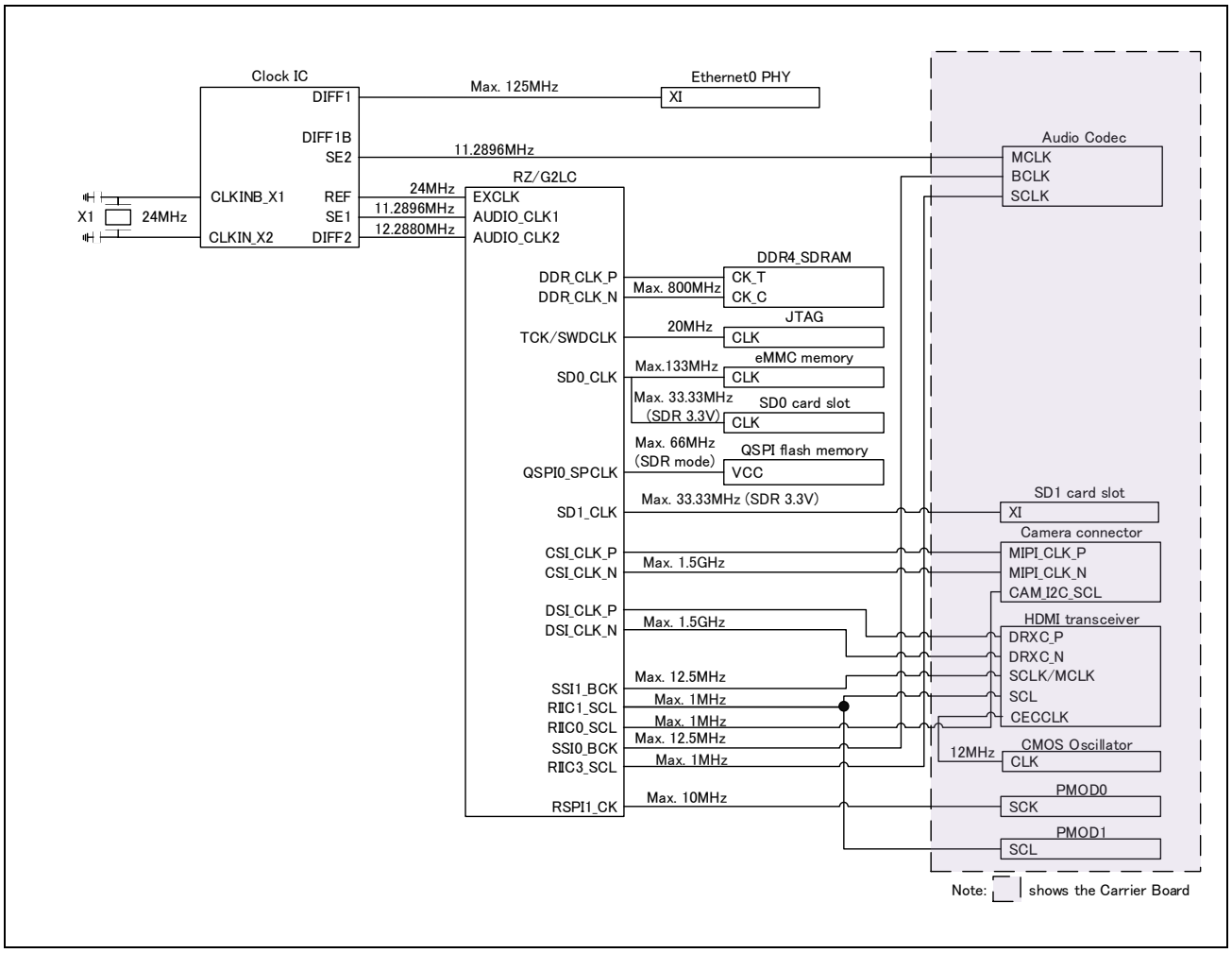

Figure 2.4 Block Diagram of Clock Configuration

2.6 Reset Control

Figure 2.5 shows a block diagram of a reset control for RTK9744C22S01000BE (RZ/G2LC Evaluation Board Kit).

For RTK9744C22C01000BE, the interfaces of DDR4 SDRAM, QSPI flash memory, eMMC memory, Ethernet and Debug are controlled by reset signal from the PMIC.

There are two types of system resets: power-on reset and reset by the button switch.

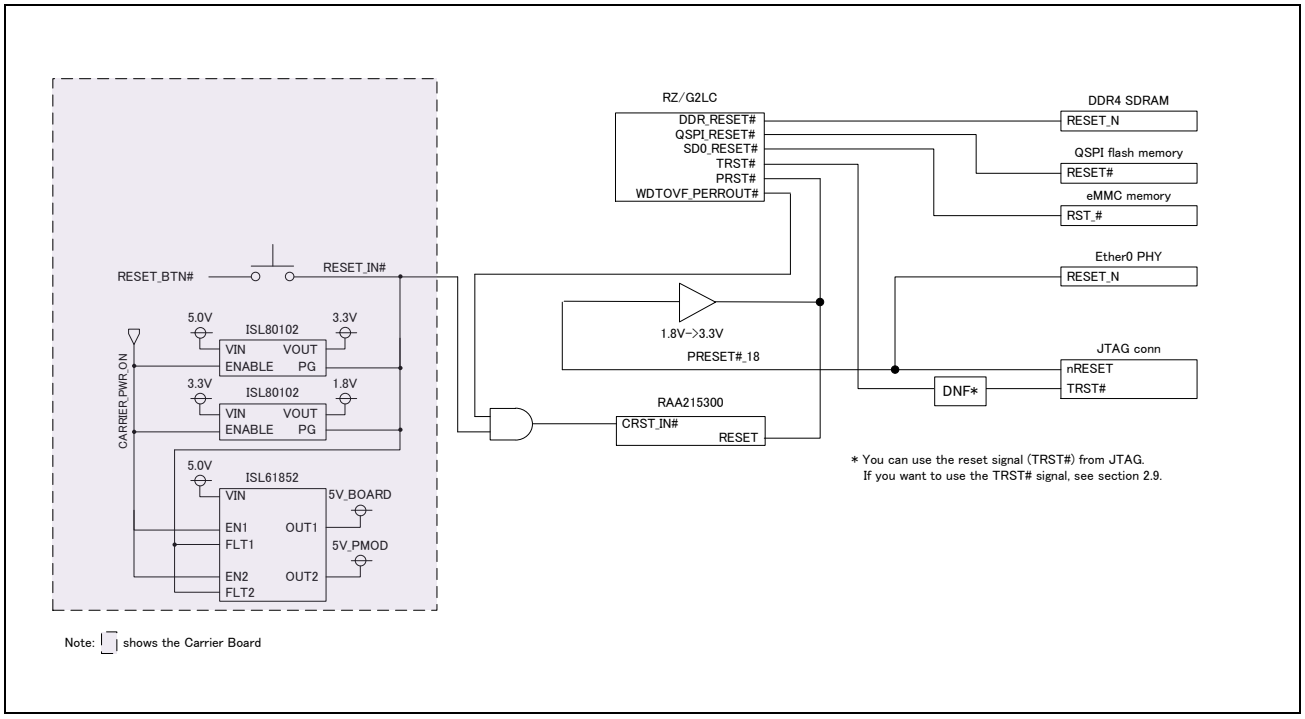

Figure 2.5 Block Diagram of Reset Control

2.7 Power Supply Configuration

Figure 2.6 shows a block diagram of power configuration for RTK9744C22S01000BE (RZ/G2LC Evaluation Board Kit).

This board has a USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5V and 9V.

The default setting for controlling the input voltage level is 5V (max 3A input) with SW11-4 is turned on. When the switch is turned off, the input voltage is 9V (max 3A input). Only when RTK9744C22S01000BE is connected to external devices that requires a lot of power and is expected to run out of power, the SW 11-4 is turned off.

The 5V power supply is supplied to the PMIC installed in RTK9744C22C01000BE, and the PMIC generates the power supply voltage for each interface.

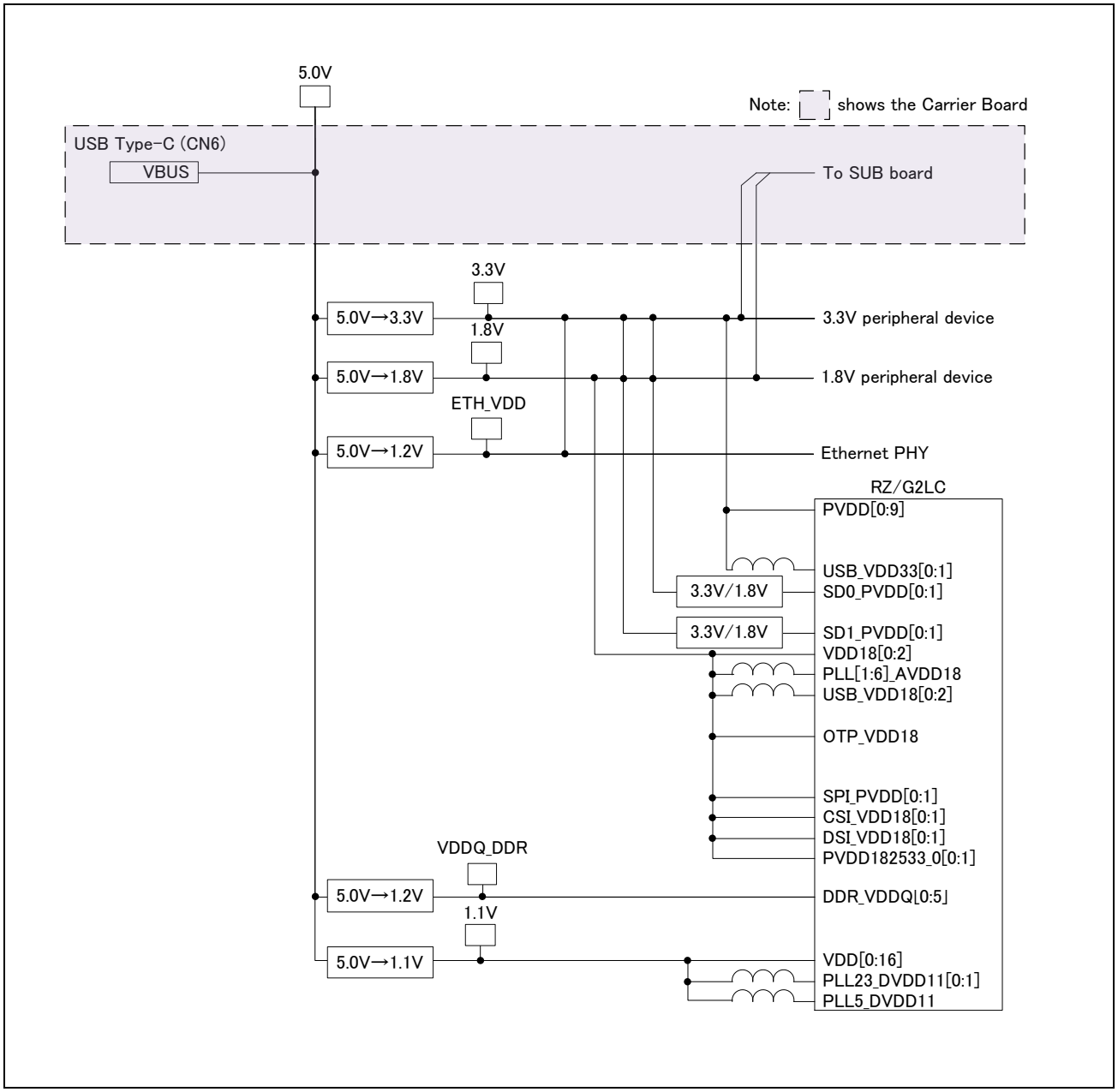

Figure 2.6 Power Configuration Diagram

Figure 2.7 shows a block diagram of power regulation for RTK9744C22C01000BE.

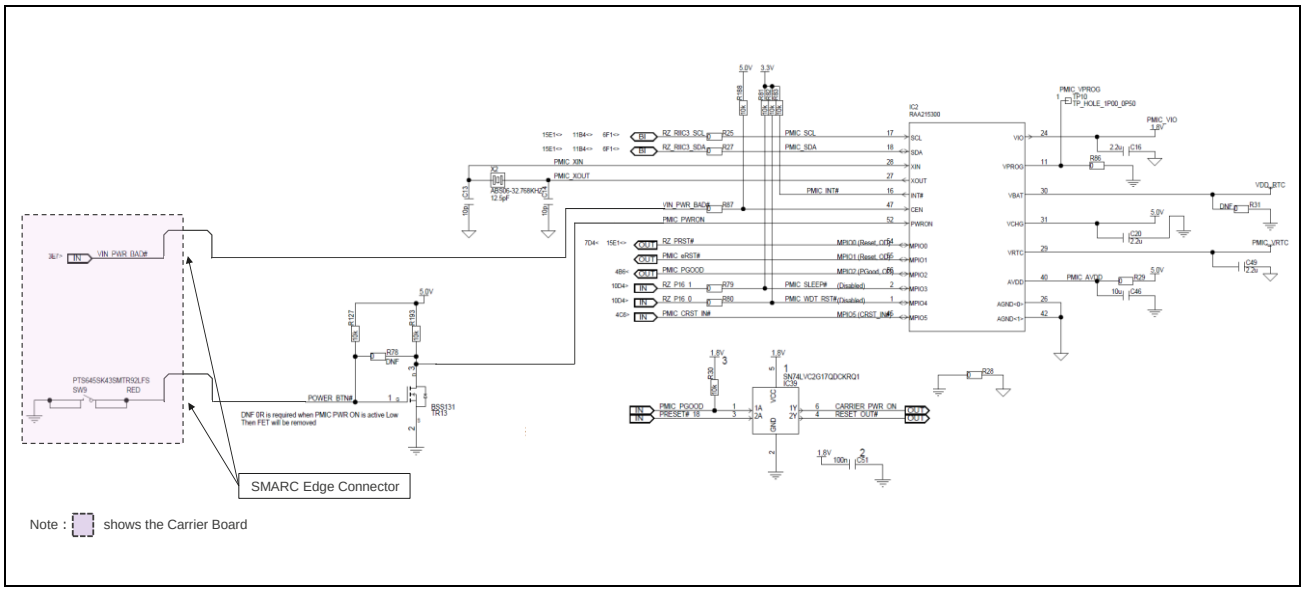

Figure 2.7 Block Diagram of Power Regulation

2.8 PMIC

Figure 2.8 shows the RZ/G2LC pin assignment for PMIC.

LDO1 and LDO2 output voltage value are fixed by P39_0 and P39_1.

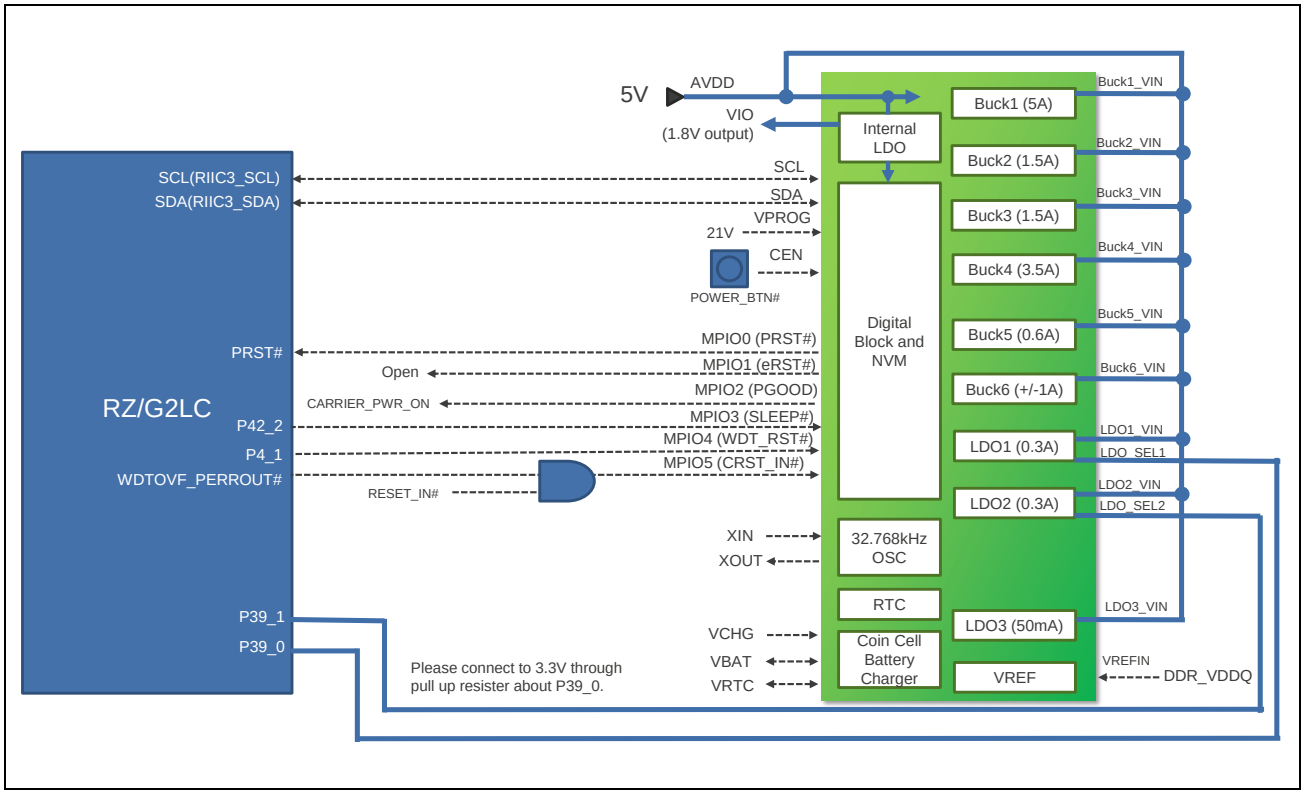

Figure 2.8 Block Diagram around PMIC

2.9 Debug Interface

Figure 2.9 shows a block diagram of debug interface.

The 10-pin Cortex® Debug Connector supports JTAG and SWD. This pin header may be used for external debug of RZ/G2LC.

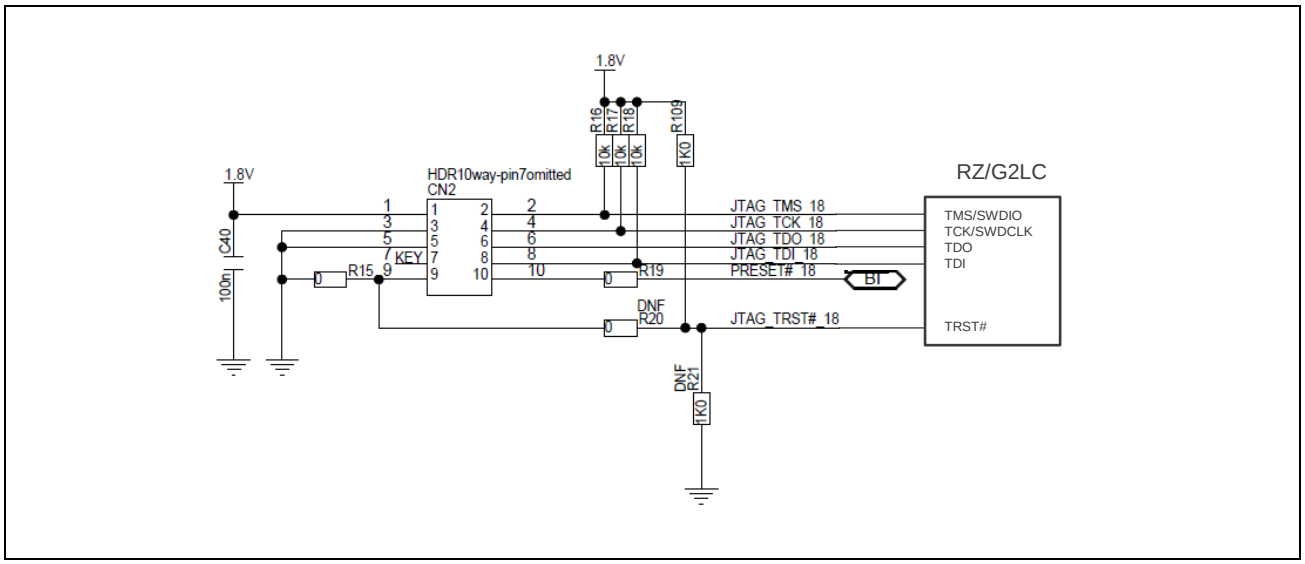

Figure 2.9 Block Diagram of Debug I/F

2.10 SD/MMC Host Interface

2.10.1 eMMC Memory

Figure 2.10 shows a block diagram of the MMC interface.

The eMMC memory is connected to channel0 of SD/MMC interface with built-in RZ/G2LC. This memory is used in conjunction with SD card.

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

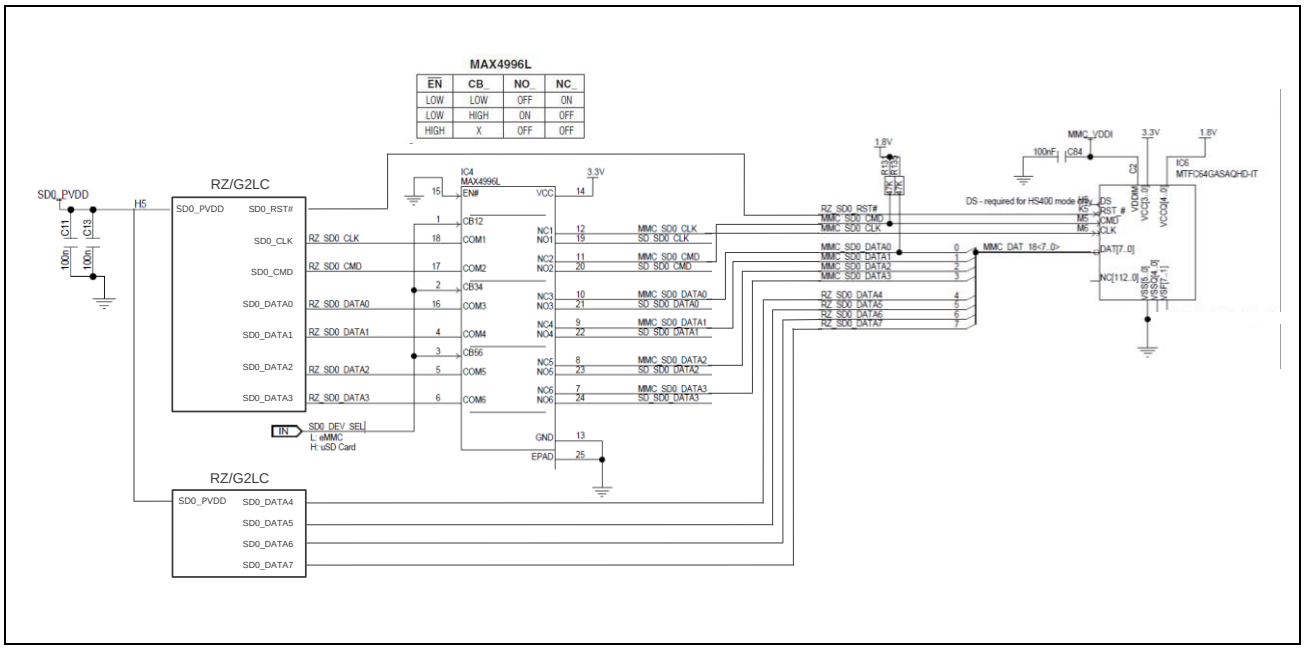

Figure 2.10 Block Diagram of eMMC I/F

2.10.2 SD Card

Figure 2.11 shows a block diagram of the SD0 interface.

The microSD card is connected to channel0 of SD/MMC interface with built-in RZ/G2LC. This memory is used in conjunction with eMMC memory.

This interface complies with the memory card standard version 3.0 and supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

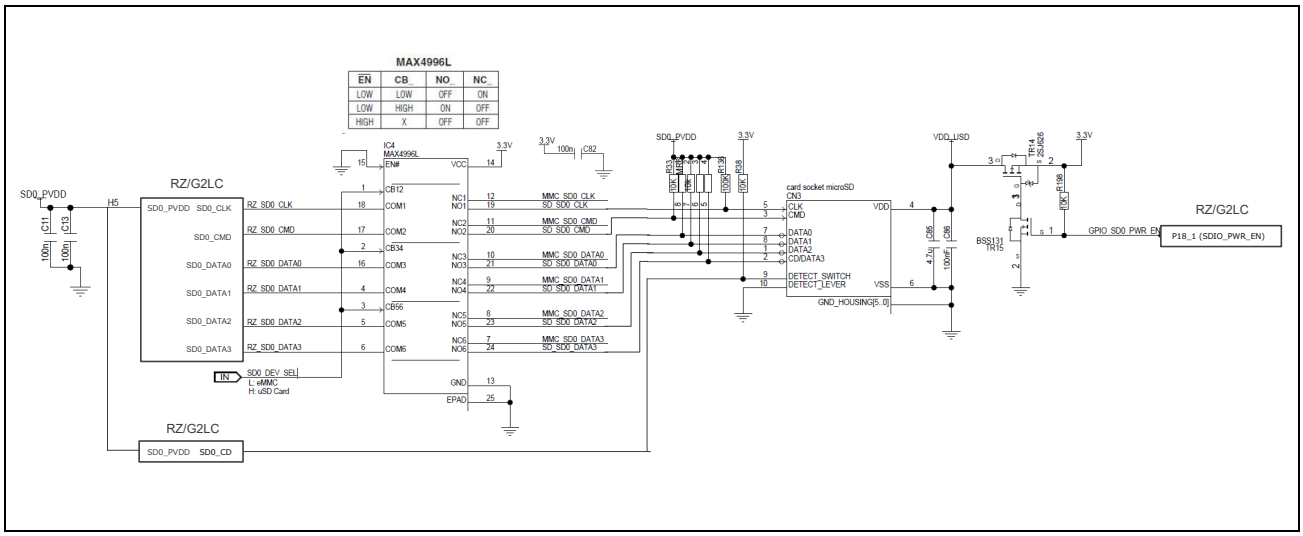

Figure 2.11 Block Diagram of SD0 I/F

3. Operation Specifications

3.1 Overview of Connectors

Figure 3.1 Illustrates the layout of connectors of RTK9744C22C01000BE.

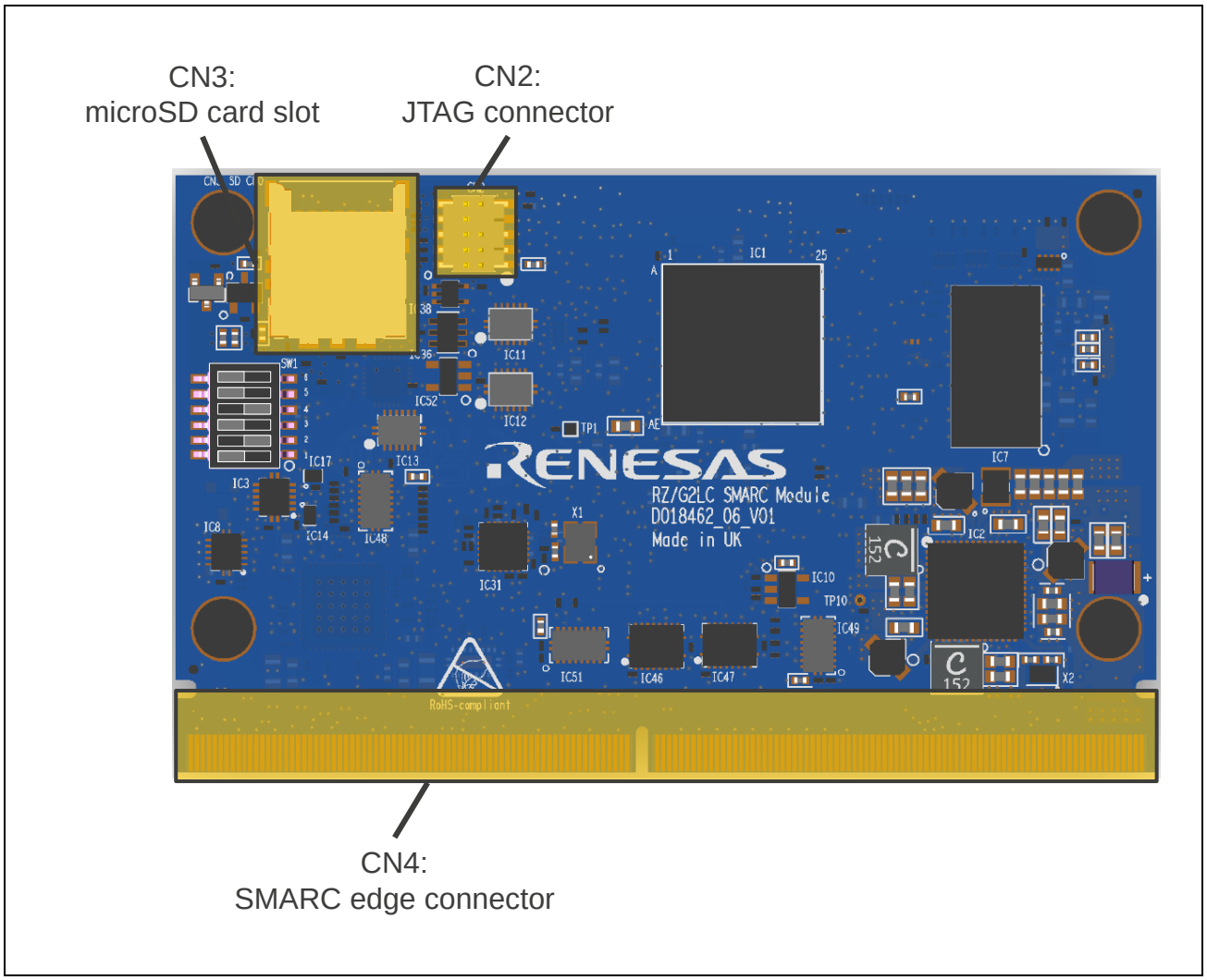

Figure 3.1 Layout of connectors of RTK9744C22C01000BE (Top side)

3.1.1 JTAG Connector (CN2)

RTK9744C22C01000BE contains a connector of JTAG interface (CN2).

Figure 3.2 illustrates the layout of the connector pins. **Table 3.1** shows the assignment of the connector pins.

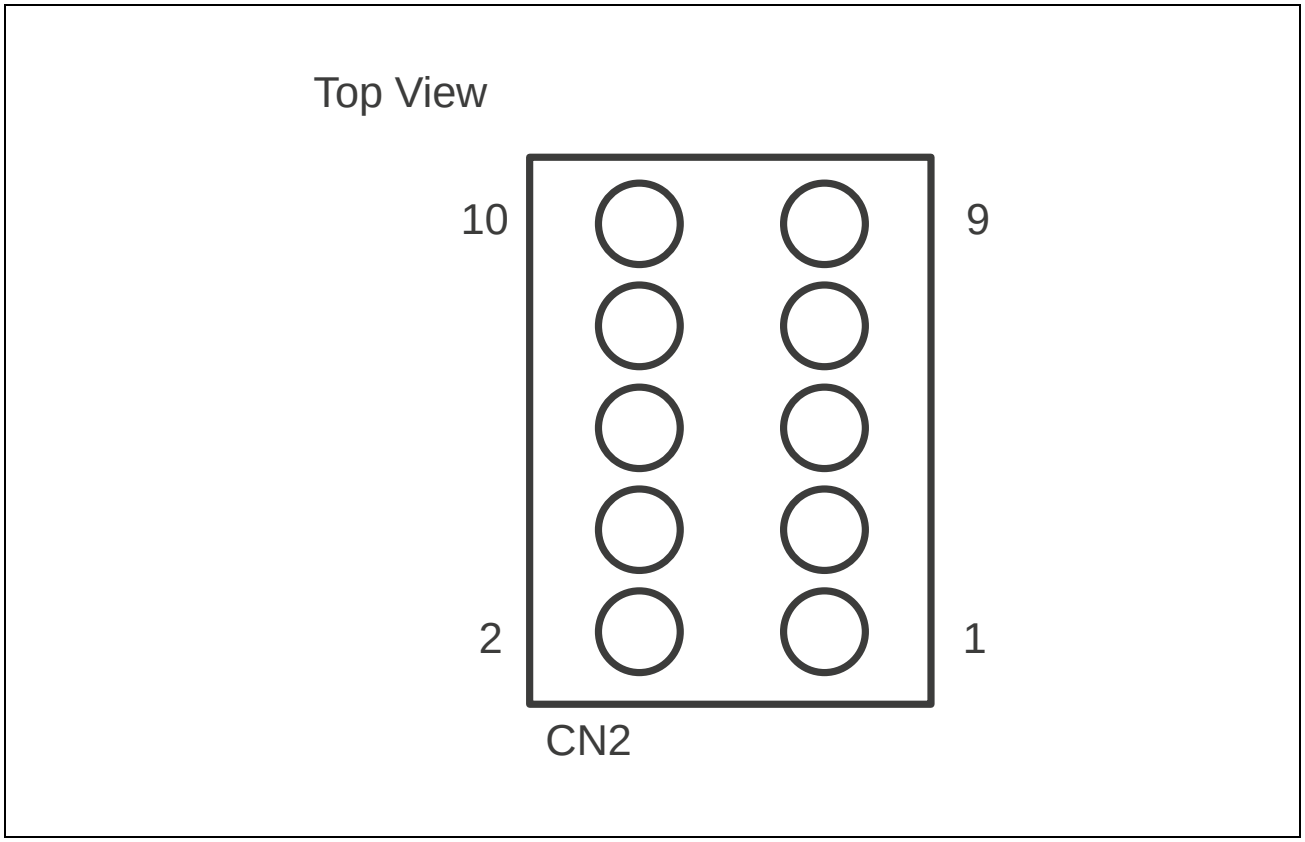

Figure 3.2 JTAG Connector (CN2) Pin Layout Diagram

Table 3.1 JTAG Connector (CN2) Pin Layout Table

Pin	Signal Name
1	PVDD18
2	TMS/SWDIO
3	VSS
4	TCK/SWDCLK
5	VSS
6	TDO
7	—
8	TDI
9	VSS
10	TRST#

3.1.2 MicroSD Card Slot (CN3)

RTK9744C22C01000BE contains a microSD card slot (CN3).

Figure 3.3 illustrates the layout of microSD card slot pins. **Table 3.2** shows the assignment of microSD card slot pins.

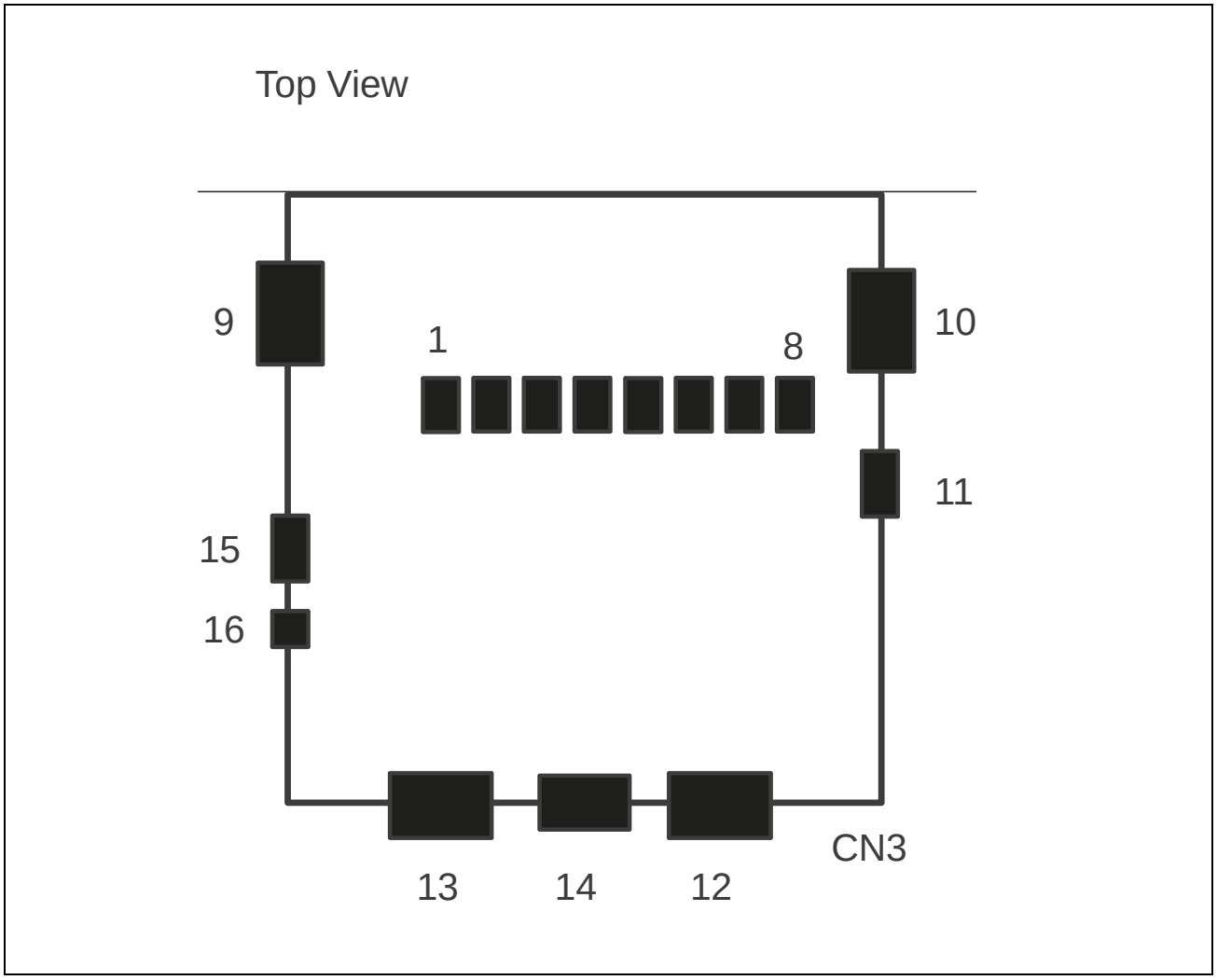

Figure 3.3 microSD Card Slot (CN3) Pin Layout Diagram

Table 3.2 microSD Card Slot (CN3) Pin Layout Table

Pin	Signal Name
1	SD0_DATA2
2	CD/SD0_DATA3
3	SD0_CMD
4	SD0_PVDD
5	SD0_CLK
6	VSS
7	SD0_DATA0
8	SD0_DATA1
9	DETECT_SWITCH
10	DETECT_LEVER

3.1.3 SMARC edge Connector (CN4)

RTK9744C22C01000BE can be connected to an external expansion board through the Carrier board connecting connector (CN4).

Figure 3.4 illustrates the layout of Carrier board connecting connector pins. For the assignment of Carrier board connecting connector pins, please refer to the section 4 “MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification (sget.org)”.

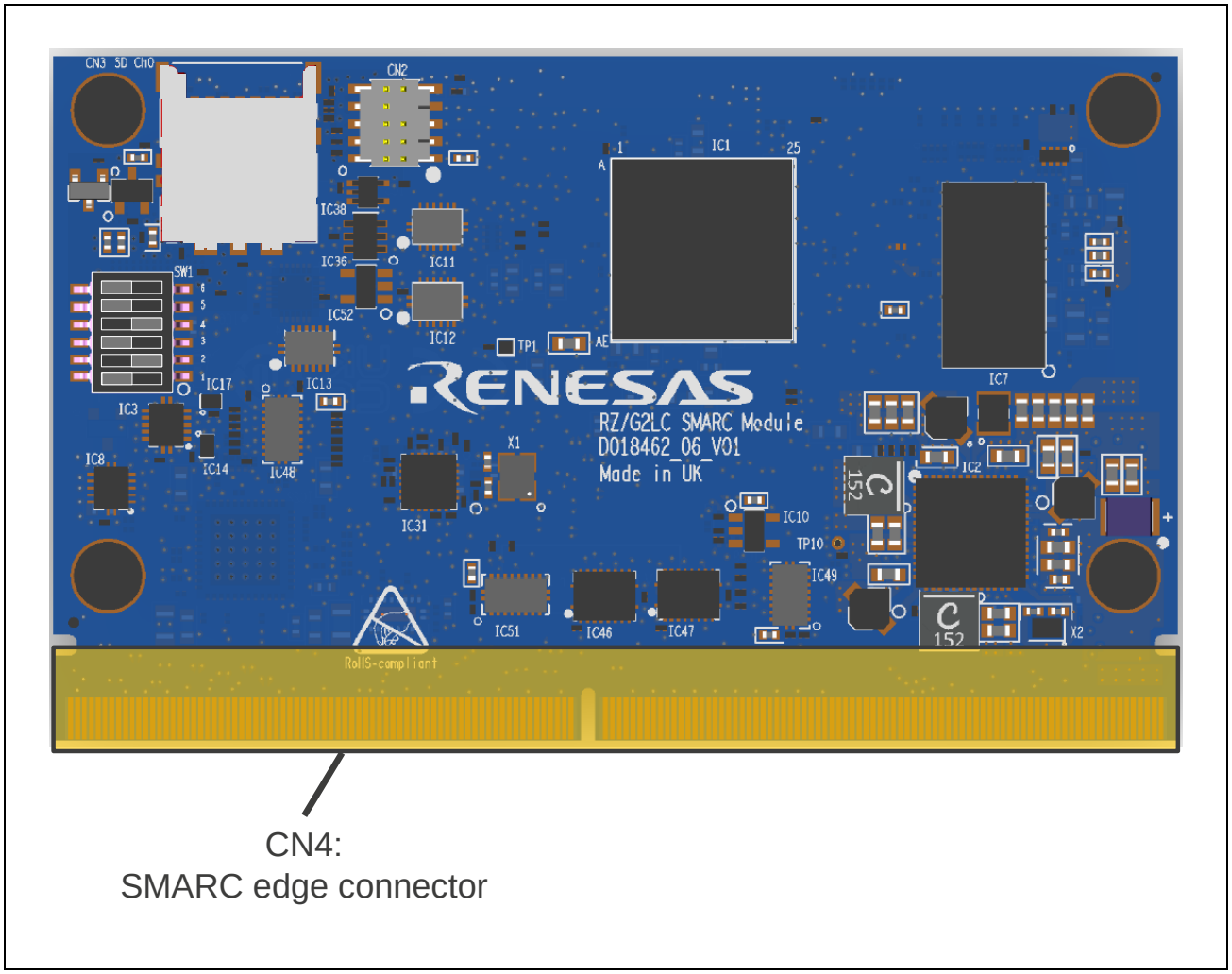

Figure 3.4 Layout of Carrier Board Connecting Pins

3.2 Layout of Operation Components

Figure 3.5 illustrates the layout of operation components of RTK9744C22C01000BE.

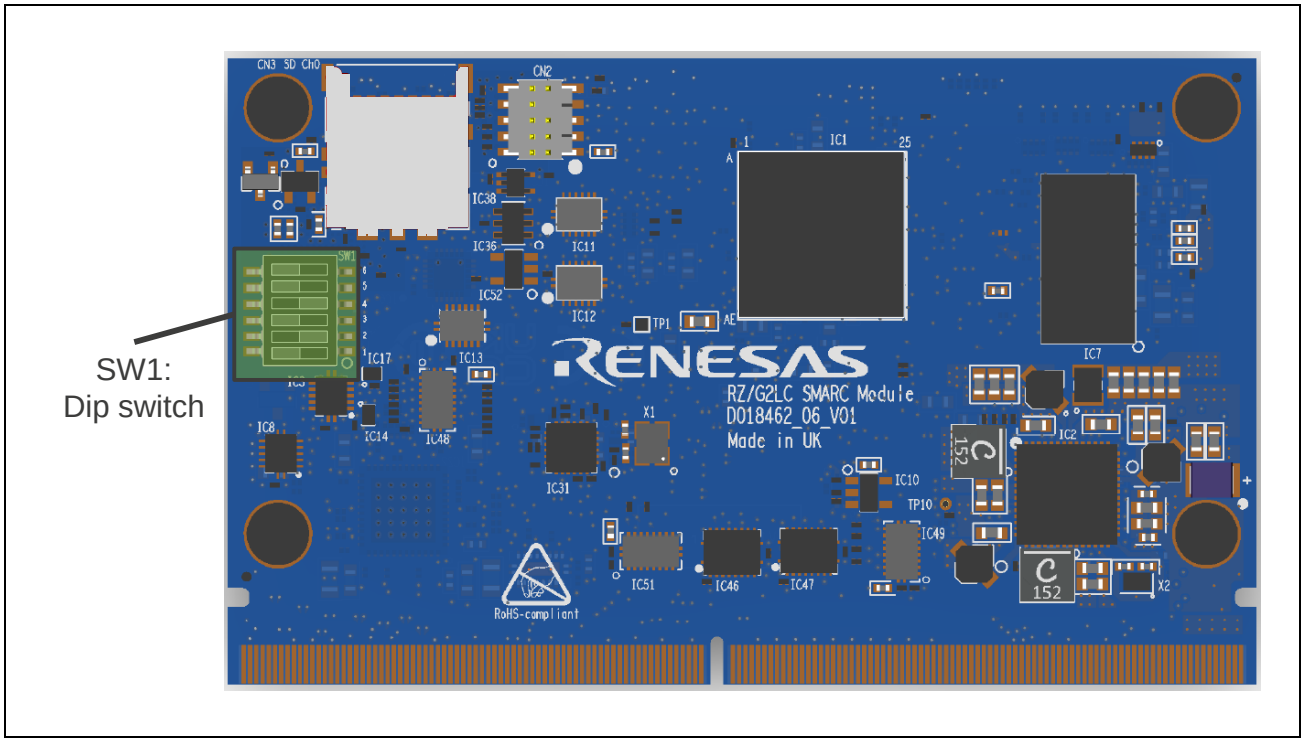

Figure 3.5 Layout of Operation Components of RTK9744C22C01000BE

3.2.1 Functions of Switches and Mode Terminals

RTK9744C22C01000BE contains one switch.

Table 3.3 lists mounted switches. **Table 3.4** provides a function of each DIP switch.

Table 3.3 Switches Mounted on RTK9744C22C01000BE

No.	Function	Note
SW1	System setting DIP switch	For details, see **Table 3.4**

Table 3.4 Functions of System Setting DIP Switch (SW1)

No.	Setting		Function
SW1-1 DEBUGEN	OFF	DEBUGEN="H"	Debugging with ARM debuggers
	ON	DEBUGEN="L"	Normal operation
SW1-2 Selection SD or MMC	OFF	Selection="H"	Select the eMMC memory
	ON	Selection="L"	Select the SD card
SW1-3 Selection SCIF or CAN	OFF	Selection="H"	Select the SCIF
	ON	Selection="L"	Select the CAN(*1)
SW1-4 Selection RSPI or CAN	OFF	Selection="H"	Select the RSPI
	ON	Selection="L"	Select the CAN(*1)
SW1-5 Selection Audio or Display	OFF	Selection="H"	Select the Audio
	ON	Selection="L"	Select the Display

Note 1. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

By setting SW1-3 and SW1-4 to the following settings, RTK9744C22C01000BE can be used various interfaces. **Table 3.5** and **Table 3.6** provide functions combined with the DIP switches.

Table 3.5 GPIO Signals combined with SW1-3 and SW1-4

		Setting			
		SW1-3 ="L"	SW1-3 ="L"	SW1-3 ="H"	SW1-3 ="H"
		SW1-4 ="L"	SW1-4 ="H"	SW1-4 ="L"	SW1-4 ="H"
Signal Name	P40_0	SCIF1_TXD	SCIF1_TXD	CAN1_TX (*2)	CAN1_TX (*2)
	P40_1	SCIF1_RXD	SCIF1_RXD	CAN1_RX (*2)	CAN1_RX (*2)
	P44_0	RSPI1_CK	CAN1_TX (*2)	RSPI1_CK	RSPI1_CK (*1)
	P44_1	RSPI1_MOSI	CAN1_RX (*2)	RSPI1_MOSI	RSPI1_MOSI (*1)
	P44_2	RSPI1_MISO	GPIO8 (*2)	RSPI1_MISO	RSPI1_MISO (*1)
	P44_3	RSPI1_SSL	GPIO9 (*2)	RSPI1_SSL	RSPI1_SSL (*1)

Note 1. IC13 is driven low regardless of the setting of SW1-4.
By removing R11, the setting of SW1-4 can be enabled.

Note 2. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

Table 3.6 GPIO Signals by SW1-5

		Setting	
		SW1-5 ="L"	SW1-5 ="H"
Signal Name	SSI0_BCK	I2S0_CK	I2S2_CK
	SSI0_RCK	I2S0_LRCK	I2S2_LRCK
	SSI0_TXD	I2S0_SDOUT	I2S2_SDOUT
	SSI0_RXD	I2S0_SDIN	I2S2_SDIN

Figure 3.6 shows a block diagram of the System Setting interface. **Table 3.7** provides functions of mode terminals.

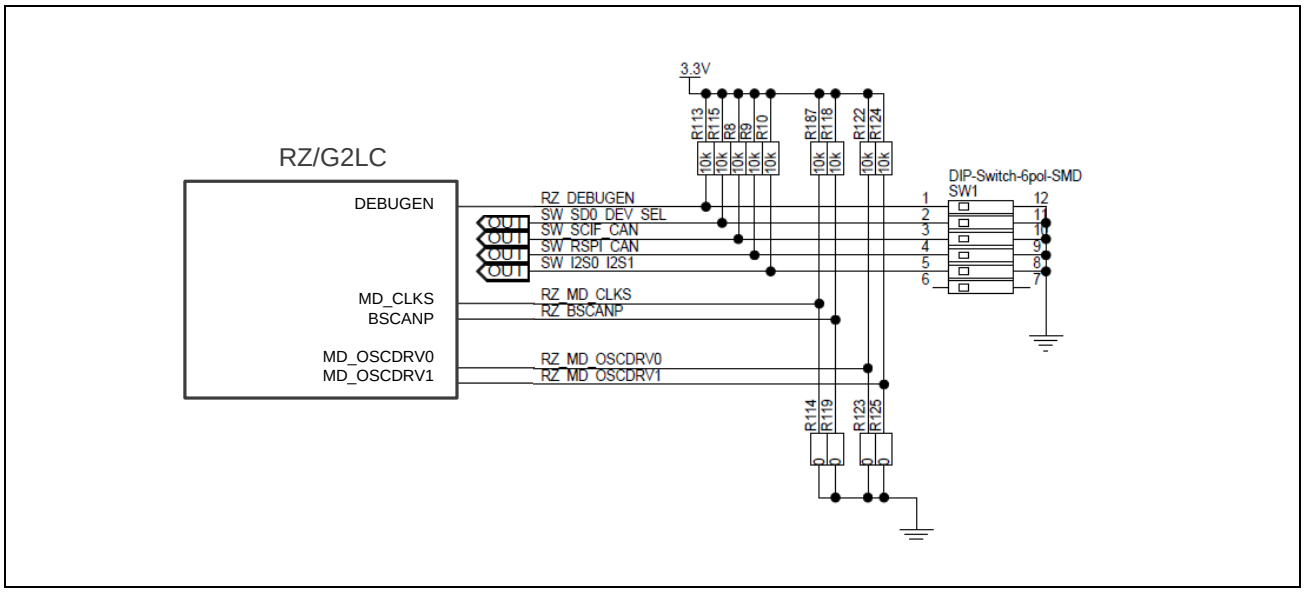

Figure 3.6 Block Diagram of System Setting I/F

Table 3.7 Functions of System Setting

No.	Setting		Function
MD_CLKS	0	MD_CLKS=“L”	SSCG OFF
	1	MD_CLKS=“H”	SSCG ON
BSCANP	0	BSCANP=“L”	Normal operation
	1	BSCANP=“H”	Connection test between LSI on the customer’s board
MD_OSCDRV0	0	MD_OSCDRV0=“L”	
	1	MD_OSCDRV0=“H”	Not supported
MD_OSCDRV1	0	MD_OSCDRV1=“L”	
	1	MD_OSCDRV1=“H”	Not supported

REVISION HISTORY	RZ Family / RZ/G Series RZ/G2LC SMARC Module Board RTK9744C22C01000BE

Rev.	Date	Description	
		Page	Summary
1.00	Sep 27, 2021	—	First edition issued
1.01	Jan 28, 2022	ALL	A Figure of RTK9744L23C01000BE is changed to RTK9744C22C01000BE.
		—	Section 3.1 is removed.
		51	A setting table of SW1-5 is added.
1.10	Dec 09, 2022	32 to 34, 51, 52	Restrictions on use are added. When used in combination with the RZ SMARC Series Carrier Board (P/N: RTR97X4XXXB00000BE), CAN1 interface cannot be used because a CAN transceiver is not fitted on the RTK97X4XXXB00000BE.
1.20	Apr 01, 2024	17 to 28	For section 2.2.2 "List of RZ/G2LC Functions", the pin names, pin functions, and descriptions in the table are modified.
		28, 45, 46	Restrictions on use are modified. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted. The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already. S.LOT# in the outer box label: 000251812 or later S.LOT# label on the carrier board: 251812 or later
		31	For section 2.4 "Gigabit Ethernet Interface", the figure is modified.
		33	For section 2.6 "Reset Control", the figure is modified.
		34	For section 2.7 "Power Supply Configuration", the figure is modified.
		36	For section 2.8 "PMIC", the figure is modified.
		37	For section 2.9 "Debug Interface", the figure is modified.
		38	For section 2.10.1 "eMMC Memory", the figure is modified.

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