User's Manual

RZ/G2UL, RZ/A3UL, RZ/Five
SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G, RZ/A Series

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

1.1 Purpose

The RZ/G2UL, RZ/A3UL, and RZ/Five SMARC Module Boards (hereafter referred to as “RZ/G2UL, RZ/A3UL, and RZ/Five SMARC Modules”) are platforms designed according to the SMARC 2.1 Specification to evaluate the Renesas microprocessors.

Basically, these SMARC Modules are connected to the Renesas RZ SMARC Series Carrier Board (hereafter referred to as “RZ SMARC Carrier”) and used as the RZ/G2UL, RZ/A3UL, and RZ/Five Evaluation Board Kits (hereafter referred to as “RZ/G2UL, RZ/A3UL, and RZ/Five EVKITs”).

This guide mainly includes system setup and configuration of the RZ/G2UL SMARC Module. The same PCB is used for the RZ/A3UL and RZ/Five SMARC Modules, which are designed to be pin-compatible. It also provides detailed information on the overall design and use of these boards from a hardware system perspective.

Please refer to the **section 6.1, Part Number and Features of Each Board** for the main features of each SMARC Module Board.

1.2 Configuration

Figure 1.1 and **Figure 1.2** show examples of system configuration using the RZ/G2UL, RZ/Five, and RZ/A3UL SMARC Modules.

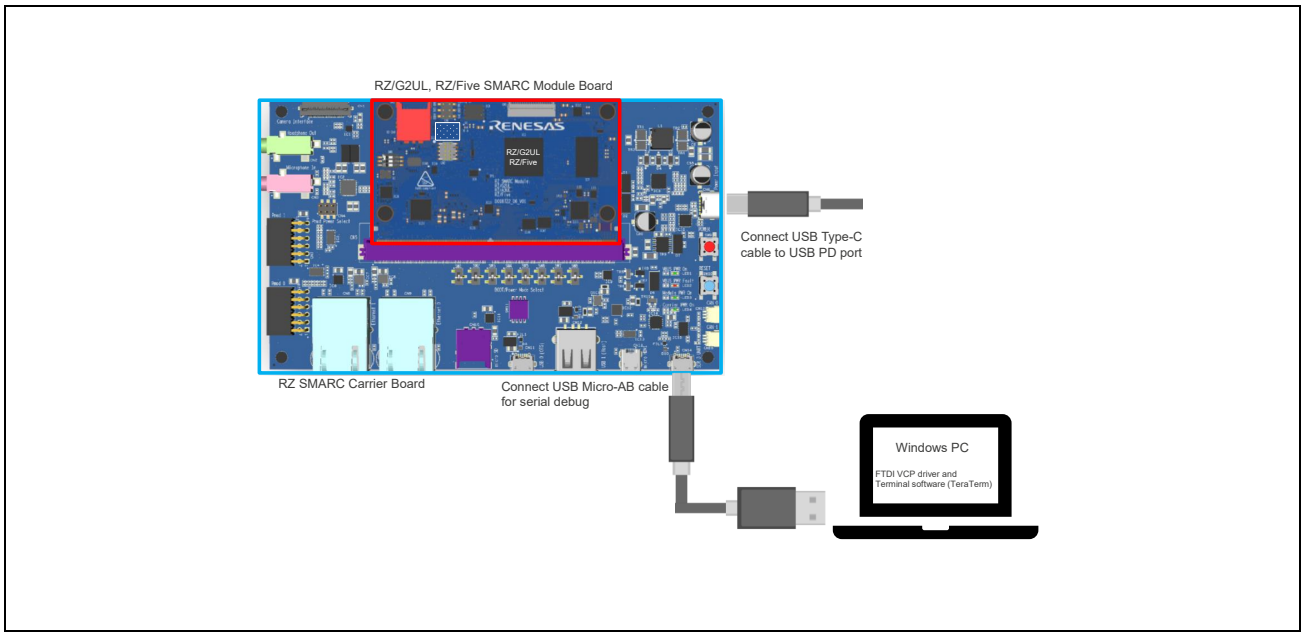


Figure 1.1 Example of System Configuration of the RZ/G2UL and RZ/Five SMARC Modules

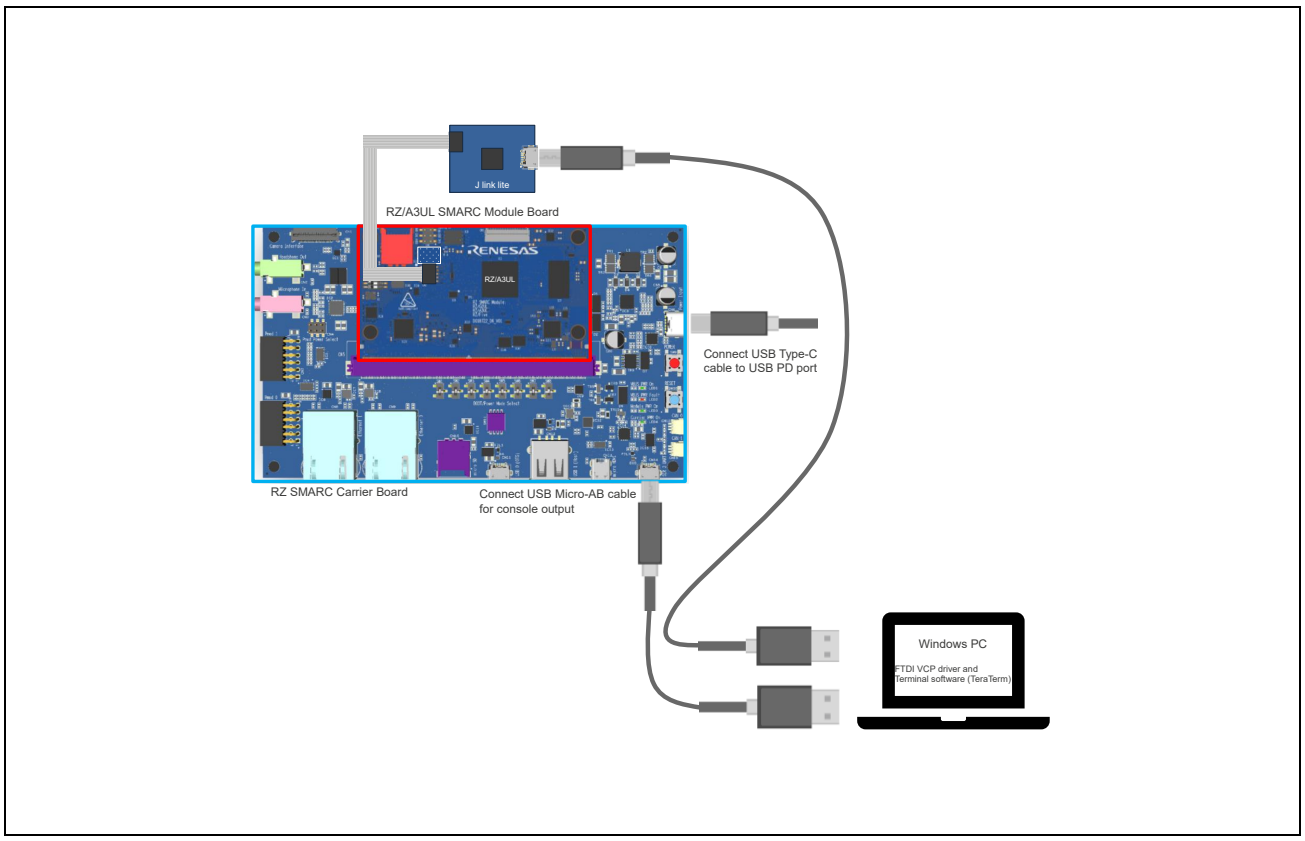


Figure 1.2 Example of System Configuration of the RZ/A3UL SMARC Module

1.3 Features

1.3.1 RZ/G2UL SMARC Module

Table 1.1 lists the features of the RZ/G2UL SMARC Module.

Table 1.1 Features of the RZ/G2UL SMARC Module

Item	Details
MPU	RZ/G2UL: R9A07G043U11GBG or R9A07G043U15GBG Package: 361-pin LFBGA, 13mm × 13 mm, 0.5-mm pitch
NOR Flash	AT25QL128A_MHE 128-Mbit
DDR4	Micron MT40A512M16LY-062E:E 1-GB 512Mx16, supporting the data rate up to 1600 MT/s
Ethernet Interface	Ethernet PHY: KSZ9131RNXC × 2
ADC Interface	Connector: 6-pin with 1.27-mm pitch
Clock	Clock generator: 5P35023B-629NLGI RZ/G2UL main: 24 MHz RZ/G2UL external clock 1 for audio: 11.2896 MHz RZ/G2UL external clock 2 for audio: 12.2880 MHz Ethernet PHY: 25 MHz Audio codec: 11.2896 MHz
Power Supply	PMIC: DA9062-52AM1
Debug Interface	Connector: 10-pin with 1.27-mm pitch
eMMC	MTFC64GASAQHD-IT 64-GB, supporting HS200 transfer mode
SD Interface	Connector: microSD card slot Support for default, high-speed, and UHS-I transfer modes, including SDR50 and SDR104
Parallel Output Interface	Connector: 45-pin FFC/FPC
Switch	For mode setting and peripheral selection: 3-bit DIP switch
Boot Mode	Support for eSD, 1.8-V eMMC, 1.8-V SPI, and SCIF download mode
Circuit board specifications	Dimensions: 82 mm (W) × 50 mm (L) × 1.2 mm (H) Mount: Double-sided mounting (6 layers)

1.3.2 RZ/A3UL SMARC Module

Table 1.2 lists the features of the RZ/A3UL SMARC Module.

This module has two types, each with a different external memory configuration. One is the QSPI version, which comprises QSPI flash memory and DDR4 SDRAM, while the other is the Octal-SPI version, which comprises OctaRAM, OctaFlash, and DDR4 SDRAM.

Table 1.2 Features of the RZ/A3UL SMARC Module

Item	Details
MPU	RZ/A3UL: R9A07G063U02GBG Package: 361-pin LFBGA, 13mm × 13 mm, 0.5-mm pitch
NOR Flash*1	Renesas AT25QL128A_MHE 128-Mbit
OctaFlash*2	Macronix MX66UW1G45GXDQ00 1-Gbit
OctaRAM*2	AP Memory APS51208N-OCHx-BD 512-Mbit
DDR4	Micron MT40A512M16LY-062E:E 1-GB 512Mx16, supporting the data rate up to 1600 MT/s
Ethernet Interface	Ethernet PHY: KSZ9131RNXC × 2
ADC Interface	Connector: 6-pin with 1.27-mm pitch
Clock	Clock generator: 5P35023B-629NLGI RZ/A3UL main: 24 MHz RZ/A3UL external clock 1 for audio: 11.2896 MHz RZ/A3UL external clock 2 for audio: 12.2880 MHz Ethernet PHY: 25 MHz Audio codec: 11.2896 MHz
Power Supply	PMIC: DA9062-52AM1
Debug Interface	Connector: 10-pin with 1.27-mm pitch On-chip debugging emulator: J link lite
eMMC	Micron MTFC64GASAQHD-IT 64 GB, supporting HS200 transfer mode
SD Interface	Connector: microSD card slot Support for default, high-speed, and UHS-I transfer modes, including SDR50 and SDR104
Parallel Output Interface	Connector: 45-pin FFC/FPC
Switch	For mode setting and peripheral selection: 6-bit DIP switch
Boot Mode	Support for 1.8-V SPI only
Circuit board specifications	Dimensions: 82 mm (W) × 50 mm (L) × 1.2 mm (H) Mount: Double-sided mounting (6 layers)

Note 1. The NOR flash is supported for the QSPI version.

Note 2. The OctaFlash and OctaRAM are supported for the Octal-SPI version.

1.3.3 RZ/Five SMARC Module

Table 1.3 lists the features of the RZ/Five SMARC Module.

Table 1.3 Features of the RZ/Five SMARC Module

Item	Details
MPU	RZ/Five: R9A07G043F01GBG or R9A07G043F05GBG Package: 361-pin LFBGA, 13 mm × 13 mm, 0.5-mm pith
NOR Flash	AT25QL128A_MHE 128-Mbit
DDR4	Micron MT40A512M16LY-062E:E 1-GB 512Mx16, supporting the data rate up to 1600 MT/s
Ethernet Interface	Ethernet PHY: KSZ9131RNXC × 2
ADC Interface	Connector: 6-pin with 1.27-mm pitch
Clock	Clock generator: 5P35023B-629NLGI RZ/Five main: 24 MHz RZ/Five external clock 1 for audio: 11.2896 MHz RZ/Five external clock 2 for audio: 12.2880 MHz Ethernet PHY: 25 MHz Audio codec: 11.2896 MHz
Power Supply	PMIC: DA9062-52AM1
Debug Interface	Connector: 10-pin with 1.27-mm pitch
eMMC	MTFC64GASAQHD-IT 64-GB, supporting HS200 transfer mode
SD Interface	Connector: microSD card slot Support for default, high-speed, and UHS-I transfer modes, including SDR50 and SDR104
Switch	For mode setting and peripheral selection: 6-bit DIP switch
Boot Mode	Support for eSD, 1.8-V eMMC, 1.8-V SPI, and SCIF download mode
Circuit board specifications	Dimensions: 82 mm (W) × 50 mm (L) × 1.2 mm (H) Mount: Double-sided mounting (6 layers)

1.4 Block Diagram

1.4.1 RZ/G2UL SMARC Module

Figure 1.3 shows a block diagram of the RZ/G2UL EVKIT.

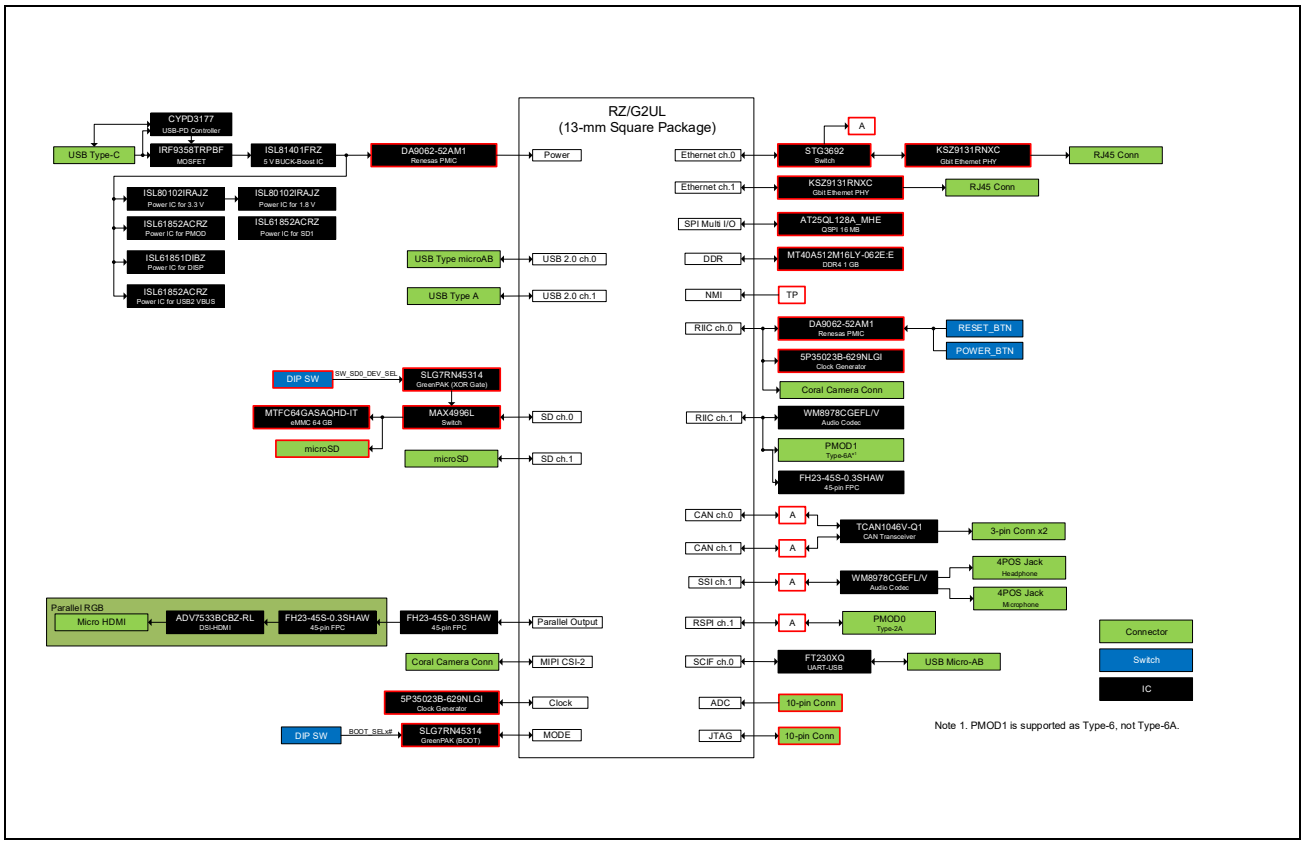


Figure 1.3 Block Diagram of the RZ/G2UL EVKIT

1.4.2 RZ/A3UL SMARC Module

Figure 1.4 and **Figure 1.5** show block diagrams of the RZ/A3UL EVKIT QSPI and Octal-SPI versions, respectively.

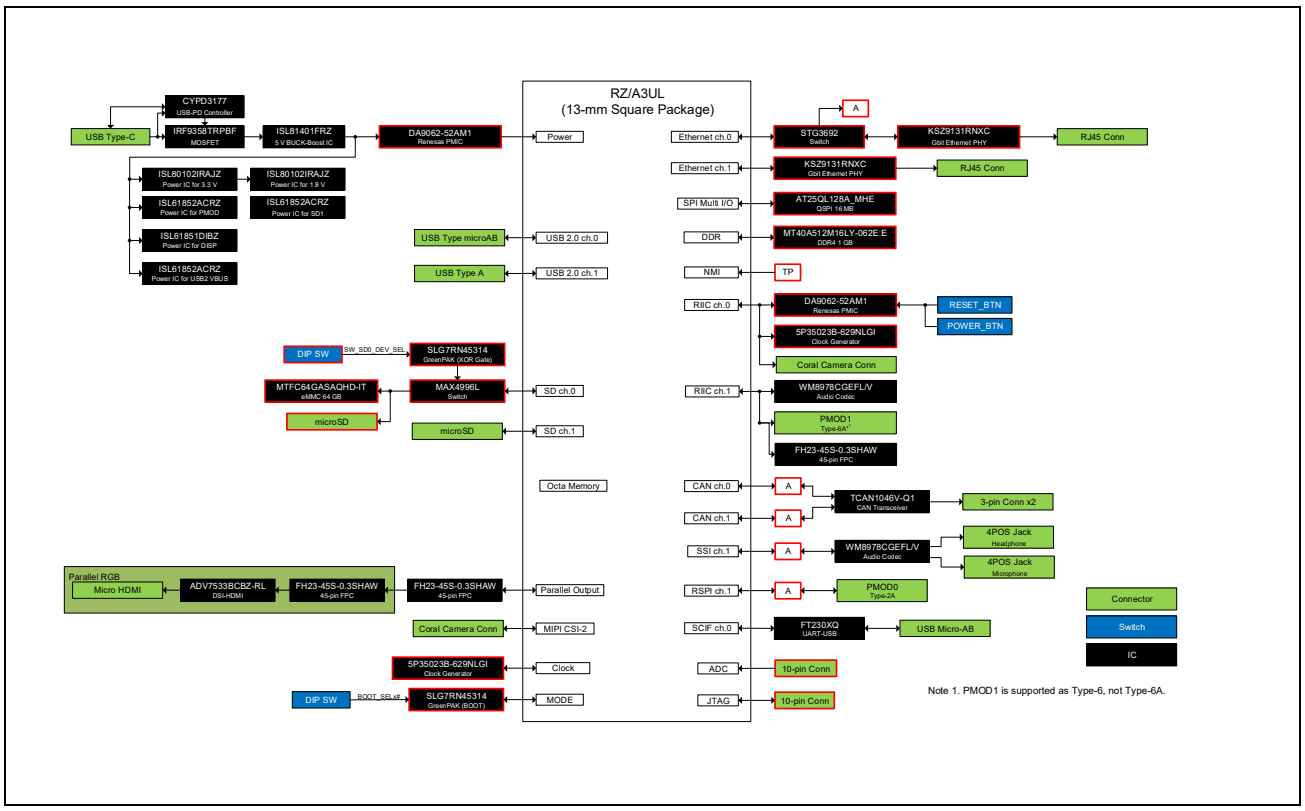


Figure 1.4 Block Diagram of the RZ/A3UL EVKIT QSPI Version

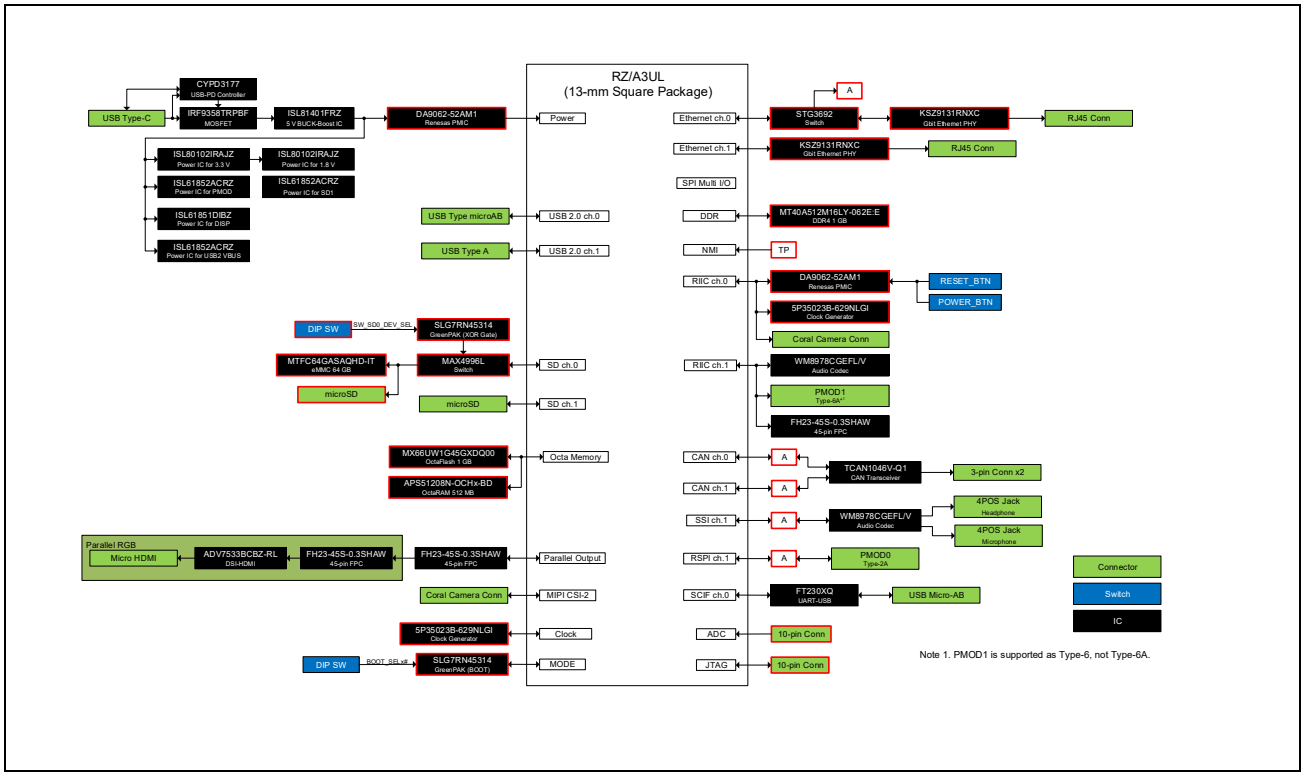


Figure 1.5 Block Diagram of the RZ/A3UL EVKIT Octal-SPI Version

1.4.3 RZ/Five SMARC Module

Figure 1.6 shows a block diagram of the RZ/Five EVKIT.

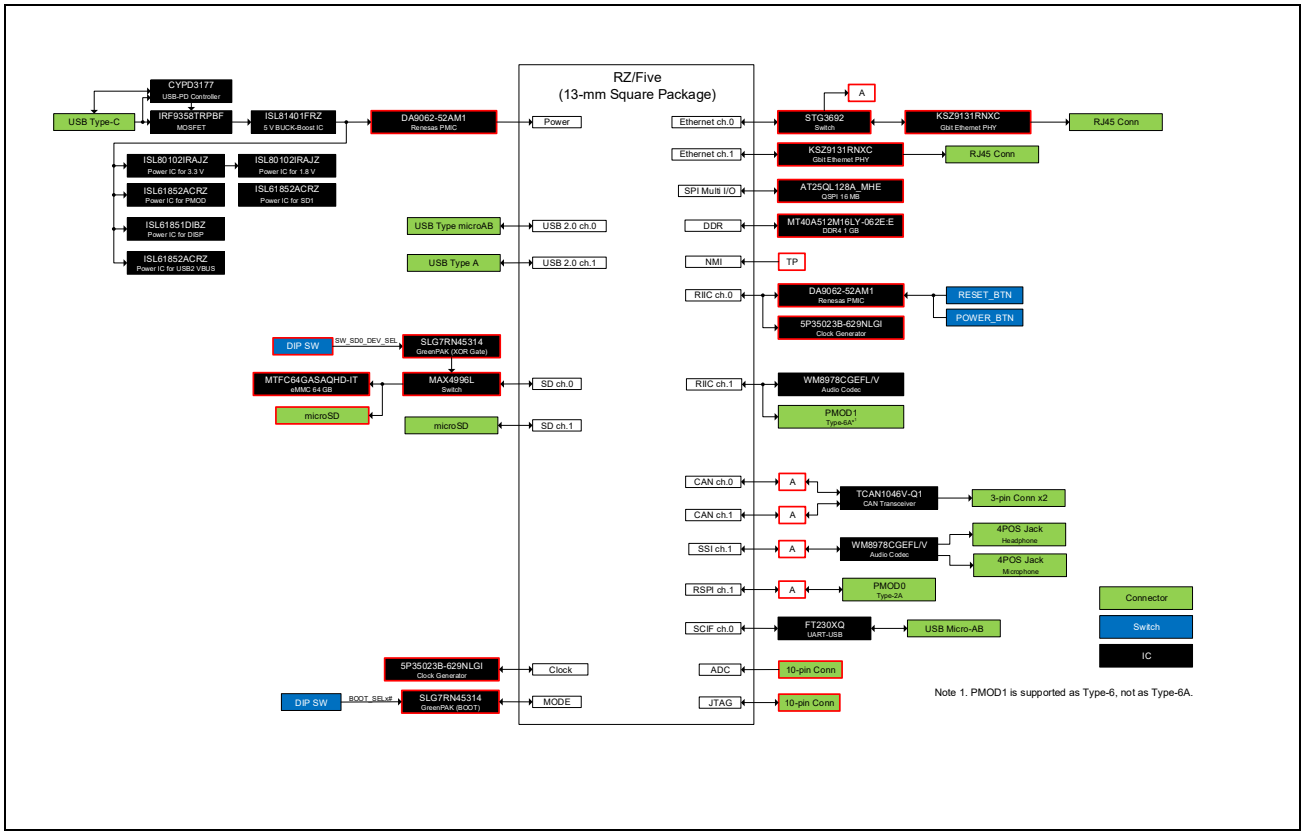


Figure 1.6 Block Diagram of the RZ/Five EVKIT

1.5 Component Layout

Figure 1.7 and **Figure 1.8** show the component layouts on the top and bottom sides of the RZ/G2UL SMARC Module.

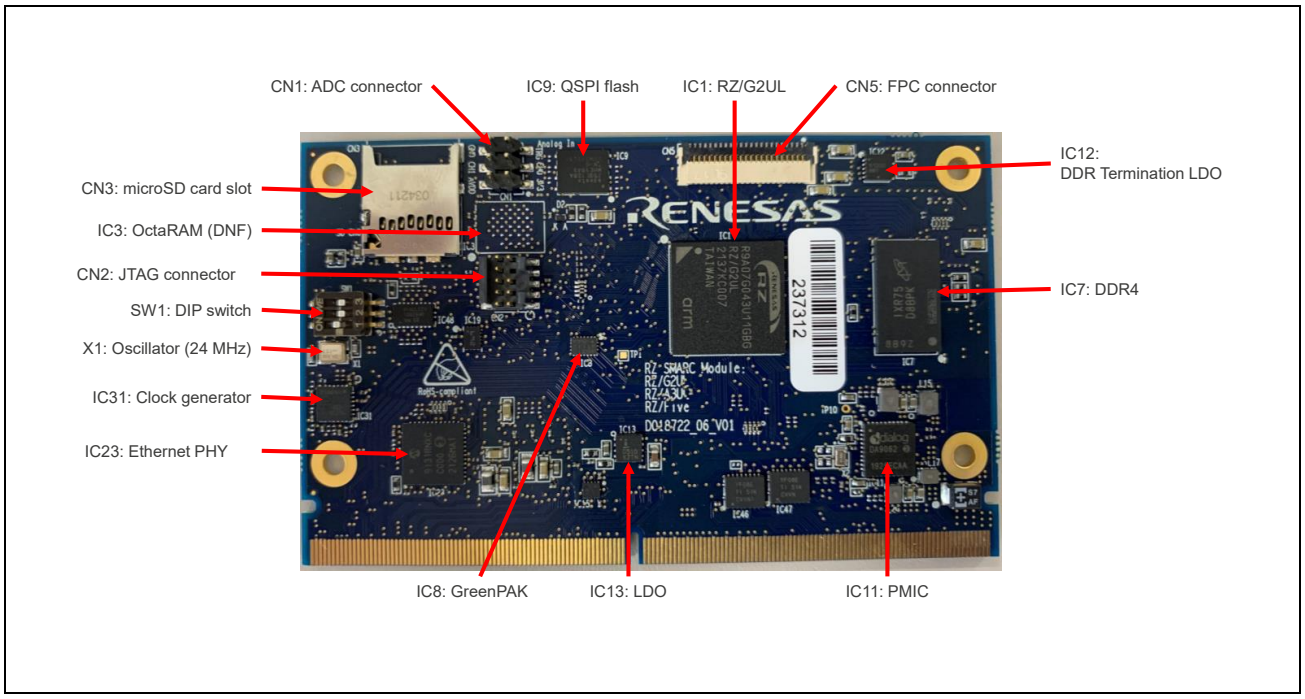


Figure 1.7 Component Layout of the RZ/G2UL SMARC Module (Top View)

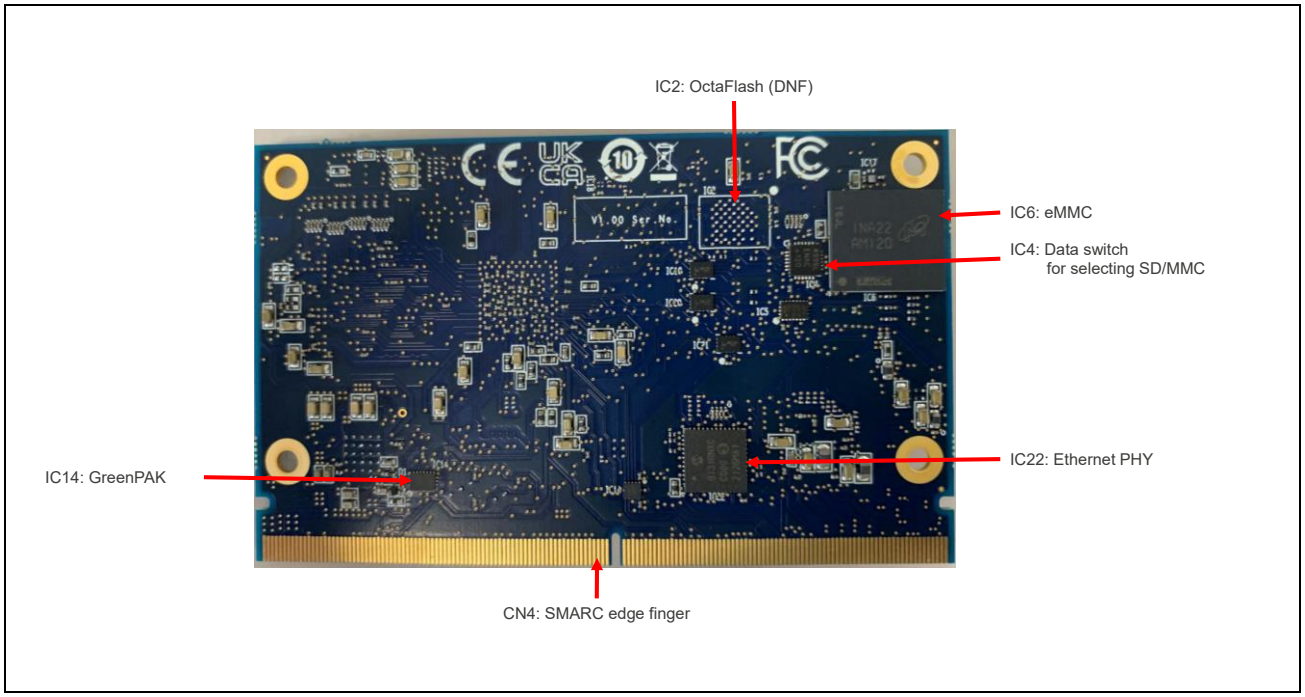


Figure 1.8 Component Layout of the RZ/G2UL SMARC Module (Bottom View)

1.6 Absolute Maximum Ratings

Table 1.4 lists the absolute maximum ratings of the RZ/G2UL EVKIT.

Table 1.4 Absolute Maximum Ratings

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	5.25 V	Reference: Vss
—	Maximum power consumption	3 A	Includes continuous RZ SMARC Carrier current consumption
Topr	Operating ambient temperature*1	0°C to 50°C	Do not expose to condensation or corrosive gases
Tstg	Storage temperature	-10°C to 60°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

1.7 Operating Condition

Table 1.5 lists the operating conditions of the RZ/G2UL EVKIT.

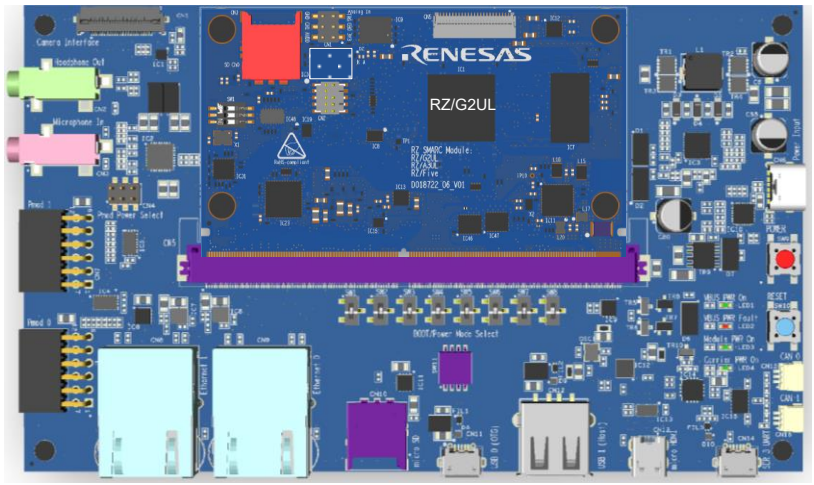
Table 1.5 Operating Conditions

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	3.0 V to 5.25 V	Reference: SMARC v2.1 specification
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

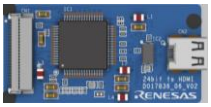
Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

2. Box Contents

Figure 2.1, **Figure 2.2**, and **Figure 2.3** show the components included in each box.



RZ/G2UL EVKIT



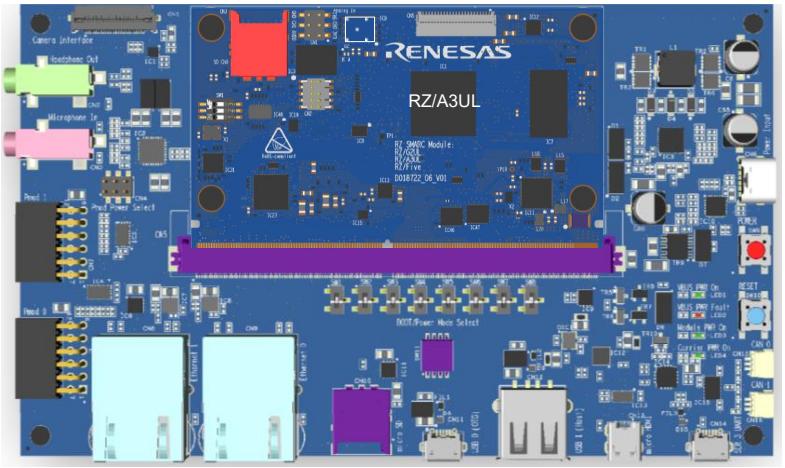
Parallel to HDMI conversion board

FPC cable

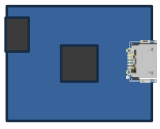
USB Type-A to micro B cable

Figure 2.1 RZ/G2UL EVKIT

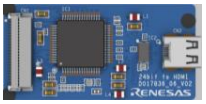
* This picture is of the Octal-SPI version.



RZ/A3UL EVKIT



J-Link Lite

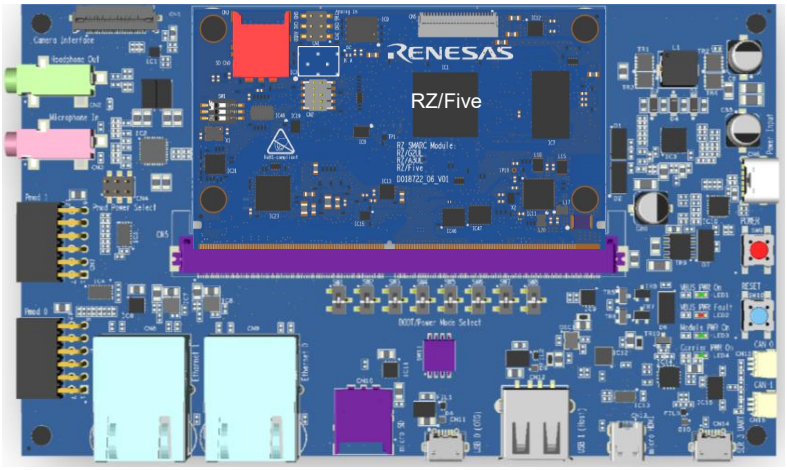


Parallel to HDMI conversion board

FPC cable

USB Type-A to micro B cable x2

Figure 2.2 RZ/A3UL EVKIT



RZ/Five EVKIT

USB Type-A to micro B cable

Figure 2.3 RZ/Five EVKIT

3. Ordering Information

- RZ/G2UL EVKIT orderable part numbers:

  RTK9743U11S01000BE

  RTK9743U15S01000BE

There are two types of RZ/G2UL EVKIT, as listed above.

RTK9743U11S01000BE is equipped with R9A07G043U11GBG (for which the security is not supported) as the microprocessor.

RTK9743U15S01000BE is equipped with R9A07G043U15GBG (for which the security is supported). RTK9743U15S01000BE can be evaluated the same as RTK9743U11S01000BE if you do not activate the security function.

- RZ/A3UL EVKIT orderable part numbers:

  RTK9763U02S01002BE

  RTK9763U02S01003BE

There are two types of RZ/A3UL EVKIT, as listed above and these kits are equipped with R9A07G063U02GBG (for which the security is not supported) as the microprocessor.

RTK9763U02S01002BE is equipped with QSPI flash memory and DDR4 SDRAM as external memory.

RTK9743U02S01003BE is equipped with OctaRAM, OctaFlash, and DDR4 SDRAM as external memory.

- RZ/Five EVKIT orderable part numbers:

  RTK9743F01S01000BE

  RTK9743F05S01000BE

There are two types of RZ/Five EVKIT, as listed above.

RTK9743F01S01000BE is equipped with R9A07G043F01GBG (for which the security is not supported) as the microprocessor.

RTK9743F05S01000BE is equipped with R9A07G043F05GBG (for which the security is supported). RTK9743F05S01000BE can be evaluated the same as RTK9743F01S01000BE if you do not activate the security function.

4. Functional Specifications

4.1 MPU

4.1.1 RZ/G2UL

The RZ/G2UL includes a single ARM Cortex-A55 core with speeds up to 1.0 GHz and a single Arm Cortex-M33 core with speeds up to 200 MHz. It also includes a 16-bit DDR3L/DDR4 interface and a simple LCD controller. In addition, it has many interfaces such as camera input, display output, USB 2.0, and Gigabit Ethernet.

The RZ/G2UL is useful for the following applications:

- Entry-level industrial gateway control, and embedded devices with simple GUI capabilities.

For details on the processor, refer to the “RZ/G2UL Group User’s Manual: Hardware”.

4.1.2 RZ/A3UL

The RZ/A3UL includes a single ARM Cortex-A55 core with speeds up to 1.0 GHz, a 16-bit DDR3L/DDR4 interface, and a simple LCD controller. In addition, it has many interfaces such as camera input, display output, USB 2.0, and Gigabit Ethernet, enabling the system to fully leverage the capabilities of a real-time operating system (RTOS).

The RZ/A3UL is useful for the following applications:

- Entry-level industrial gateway control, and embedded devices with simple GUI capabilities.

For details on the processor, refer to the “RZ/A3UL Group User’s Manual: Hardware”.

NOTE

If the TSU (Thermal Sensor Unit) correction code for the device mounted on the RZ/A3UL EVKIT is set to 0, you should use the following values instead:

- OTPTSUTRIM0 = 3148
- OTPTSUTRIM1 = 503

When using these substitute values, please note that the temperature measurement error can be as large as ±20°C.

4.1.3 RZ/Five

The RZ/Five includes a single RISC-V (AX45MP) core with speeds up to 1.0 GHz and a 16-bit DDR3L/DDR4 interface. In addition, it has many interfaces such as USB 2.0 and Gigabit Ethernet.

The RZ/Five is useful for the following applications:

- Entry-level industrial gateway control.

For details on the processor, refer to the “RZ/Five Group User’s Manual: Hardware”.

4.1.4 List of Pin Functions

As described in **section 1.1**, the RZ/G2UL is pin-compatible with the RZ/A3UL and RZ/Five.

Table 4.1 lists the pin functions of each product for use with the corresponding SMARC Module.

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (1/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
F17	ADC_AVDD18	ADC_AVDD18	ADC_AVDD18	NC	1.8 V *Note*: Unused on the board for the RZ/Five	—	—
B18	ADC_CH0	ADC_CH0	ADC_CH0	NC	Pin connector (CN1) for ADC input *Note*: Unused on the board for the RZ/Five	—	—
A18	ADC_CH1	ADC_CH1	ADC_CH1	NC	Pin connector (CN1) for ADC input *Note*: Unused on the board for the RZ/Five	—	—
A9	AUDIO_CLK1	AUDIO_CLK1	AUDIO_CLK1	AUDIO_CLK1	Input 11.2896 MHz from 5P35023 for generating the CD sampling rate (44.1 KHz)	—	—
B8	AUDIO_CLK2	AUDIO_CLK2	AUDIO_CLK2	AUDIO_CLK2	Input 12.2880 MHz from 5P35023 for generating the DVD sampling rate (48.0 KHz)	—	—
AE22	BSCANP	BSCANP	BSCANP	BSCANP	Initial setting: 0 (pull-down) It should be controllable by resistor.	—	—
AD21	VSS	VSS	VSS	VSS	GND	—	—
AE11	CSI_CLKN	CSI_CLKN	CSI_CLKN	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P4	CSI1_CK-
AD11	CSI_CLKP	CSI_CLKP	CSI_CLKP	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P3	CSI1_CK+
AE12	CSI_DATA0_N	CSI_DATA0_N	CSI_DATA0_N	NC	24-pin FFC connector on the RZ SMRC Carrier *Note*: Unused on the board for the RZ/Five	P8	CSI1_RX0-
AD12	CSI_DATA0_P	CSI_DATA0_P	CSI_DATA0_P	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P7	CSI1_RX0+
AE10	CSI_DATA1_N	CSI_DATA1_N	CSI_DATA1_N	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P11	CSI1_RX1-
AD10	CSI_DATA1_P	CSI_DATA1_P	CSI_DATA1_P	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P10	CSI1_RX1+

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (2/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AE13	CSI_DATA2_N	CSI_DATA2_N	CSI_DATA2_N	ADC_CH0	24-pin FFC connector on the RZ SMARC Carrier *Note*: On the board for the RZ/Five, this pin is used as ADC_CH0. A resistor (R8) is removed and a resistor (R10) is mounted for the CSI/ADC options.	P14	CSI1_RX2-
AD13	CSI_DATA2_P	CSI_DATA2_P	CSI_DATA2_P	ADC_CH1	24-pin FFC connector on the RZ SMARC Carrier *Note*: On the board for the RZ/Five, this pin is used as ADC_CH1. A resistor (R9) is removed and a resistor (R11) is mounted for the CSI/ADC options.	P13	CSI1_RX2+
AE9	CSI_DATA3_N	CSI_DATA3_N	CSI_DATA3_N	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P17	CSI1_RX3-
AD9	CSI_DATA3_P	CSI_DATA3_P	CSI_DATA3_P	NC	24-pin FFC connector on the RZ SMARC Carrier *Note*: Unused on the board for the RZ/Five	P16	CSI1_RX3+
F17	ADC_AVDD18	ADC_AVDD18	ADC_AVDD18	NC	1.8 V *Note*: Unused on the board for the RZ/Five	—	—
Y11	CSI_VDD18	CSI_VDD18	CSI_VDD18	NC	1.8 V *Note*: Unused on the board for the RZ/Five	—	—
Y12	CSI_VDD18	CSI_VDD18	CSI_VDD18	NC	1.8 V *Note*: Unused on the board for the RZ/Five	—	—
E25	DDR_ADDR0	DDR_ADDR0	DDR_ADDR0	SD1_CD	DDR4 SDRAM (IC7)	—	—
K25	DDR_ADDR1	DDR_ADDR1	DDR_ADDR1	DDR_ADDR1	DDR4 SDRAM (IC7)	—	—
P23	DDR_ADDR10	DDR_ADDR10	DDR_ADDR10	DDR_ADDR10	DDR4 SDRAM (IC7)	—	—
H25	DDR_ADDR11	DDR_ADDR11	DDR_ADDR11	DDR_ADDR11	DDR4 SDRAM (IC7)	—	—
N23	DDR_ADDR12	DDR_ADDR12	DDR_ADDR12	DDR_ADDR12	DDR4 SDRAM (IC7)	—	—
D23	DDR_ADDR13	DDR_ADDR13	DDR_ADDR13	DDR_ADDR13	DDR4 SDRAM (IC7)	—	—
H23	DDR_ADDR14	DDR_ADDR14	DDR_ADDR14	DDR_ADDR14	DDR4 SDRAM (IC7)	—	—
D25	DDR_ADDR15	DDR_ADDR15	DDR_ADDR15	DDR_ADDR15	DDR4 SDRAM (IC7)	—	—
C25	DDR_ADDR2	DDR_ADDR2	DDR_ADDR2	DDR_ADDR2	DDR4 SDRAM (IC7)	—	—
J25	DDR_ADDR6	DDR_ADDR6	DDR_ADDR6	DDR_ADDR6	DDR4 SDRAM (IC7)	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (3/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A24	DDR_ADDR7	DDR_ADDR7	DDR_ADDR7	DDR_ADDR7	DDR4 SDRAM (IC7)	—	—
F25	DDR_ADDR8	DDR_ADDR8	DDR_ADDR8	DDR_ADDR8	DDR4 SDRAM (IC7)	—	—
B24	DDR_ADDR9	DDR_ADDR9	DDR_ADDR9	DDR_ADDR9	DDR4 SDRAM (IC7)	—	—
E24	DDR_BA0	DDR_BA0	DDR_BA0	DDR_BA0	DDR4 SDRAM (IC7)	—	—
L24	DDR_BA1	DDR_BA1	DDR_BA1	DDR_BA1	DDR4 SDRAM (IC7)	—	—
F23	DDR_BA2	DDR_BA2	DDR_BA2	DDR_BA2	DDR4 SDRAM (IC7)	—	—
A23	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR4 SDRAM (IC7)	—	—
J24	DDR_CAS#	DDR_CAS#	DDR_CAS#	DDR_CAS#	DDR4 SDRAM (IC7)	—	—
M25	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR4 SDRAM (IC7)	—	—
P24	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR4 SDRAM (IC7)	—	—
P25	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR4 SDRAM (IC7)	—	—
N24	DDR_CS0#	DDR_CS0#	DDR_CS0#	DDR_CS0#	DDR4 SDRAM (IC7)	—	—
L23	DDR_CS1#	DDR_CS1#	DDR_CS1#	DDR_CS1#	DDR4 SDRAM (IC7)	—	—
U23	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR4 SDRAM (IC7)	—	—
Y24	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR4 SDRAM (IC7)	—	—
T25	DDR_DQ0	DDR_DQ0	DDR_DQ0	DDR_DQ0	DDR4 SDRAM (IC7)	—	—
W24	DDR_DQ1	DDR_DQ1	DDR_DQ1	DDR_DQ1	DDR4 SDRAM (IC7)	—	—
W23	DDR_DQ10	DDR_DQ10	DDR_DQ10	DDR_DQ10	DDR4 SDRAM (IC7)	—	—
AD25	DDR_DQ11	DDR_DQ11	DDR_DQ11	DDR_DQ11	DDR4 SDRAM (IC7)	—	—
AD23	DDR_DQ12	DDR_DQ12	DDR_DQ12	DDR_DQ12	DDR4 SDRAM (IC7)	—	—
AA23	DDR_DQ13	DDR_DQ13	DDR_DQ13	DDR_DQ13	DDR4 SDRAM (IC7)	—	—
AC24	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR4 SDRAM (IC7)	—	—
AE24	DDR_DQ15	DDR_DQ15	DDR_DQ15	DDR_DQ15	DDR4 SDRAM (IC7)	—	—
R24	DDR_DQ2	DDR_DQ2	DDR_DQ2	DDR_DQ2	DDR4 SDRAM (IC7)	—	—
Y25	DDR_DQ3	DDR_DQ3	DDR_DQ3	DDR_DQ3	DDR4 SDRAM (IC7)	—	—
T24	DDR_DQ4	DDR_DQ4	DDR_DQ4	DDR_DQ4	DDR4 SDRAM (IC7)	—	—
U25	DDR_DQ5	DDR_DQ5	DDR_DQ5	DDR_DQ5	DDR4 SDRAM (IC7)	—	—
R25	DDR_DQ6	DDR_DQ6	DDR_DQ6	DDR_DQ6	DDR4 SDRAM (IC7)	—	—
T23	DDR_DQ7	DDR_DQ7	DDR_DQ7	DDR_DQ7	DDR4 SDRAM (IC7)	—	—
AD24	DDR_DQ8	DDR_DQ8	DDR_DQ8	DDR_DQ8	DDR4 SDRAM (IC7)	—	—
AA24	DDR_DQ9	DDR_DQ9	DDR_DQ9	DDR_DQ9	DDR4 SDRAM (IC7)	—	—
V24	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR4 SDRAM (IC7)	—	—
V25	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR4 SDRAM (IC7)	—	—
AB25	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR4 SDRAM (IC7)	—	—
AB24	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR4 SDRAM (IC7)	—	—
M24	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR4 SDRAM (IC7)	—	—
L25	DDR_ODT1	DDR_ODT1	DDR_ODT1	DDR_ODT1	DDR4 SDRAM (IC7)	—	—
H24	DDR_RAS#	DDR_RAS#	DDR_RAS#	DDR_RAS#	DDR4 SDRAM (IC7)	—	—
B23	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR4 SDRAM (IC7)	—	—
H20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
K20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
M20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
R20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (4/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
U20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
W20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
G25	DDR_WE#	DDR_WE#	DDR_WE#	DDR_WE#	DDR4 SDRAM (IC7)	—	—
Y19	DEBUGEN	DEBUGEN	DEBUGEN	DEBUGEN	DIP_SW (SW1)	—	—
P3	PVDD182533_0	PVDD182533_0	PVDD182533_0	PVDD182533_0	Input for controlling the PVDD182533_0 power level with SW1-3 High level: 3.3 V; low level: 1.8 V	—	—
Y17	PVDD182533_1	PVDD182533_1	PVDD182533_1	PVDD182533_1	1.8 V	—	—
Y3	EXCLK	EXCLK	EXCLK	EXCLK	Input 24 MHz from 5P35023 for generating system clock	—	—
P6	VDD18	VDD18	VDD18	VDD18	1.8 V	—	—
G6	MD_BOOT0	MD_BOOT0	MD_BOOT0	MD_BOOT0	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
C5	MD_BOOT1	MD_BOOT1	MD_BOOT1	MD_BOOT1	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
C4	MD_BOOT2	MD_BOOT2	MD_BOOT2	MD_BOOT2	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
F20	MD_CLKS	MD_CLKS	MD_CLKS	MD_CLKS	Initial setting: 1 (pull-up) It should be controllable by resistor.	—	—
A22	MD_OSCDRV0	MD_OSCDRV0	MD_OSCDRV0	MD_OSCDRV0	Initial setting: 0 (pull-down) It should be controllable by resistor.	—	—
C21	MD_OSCDRV1	MD_OSCDRV1	MD_OSCDRV1	MD_OSCDRV1	Initial setting: 0 (pull-down) It should be controllable by resistor.	—	—
AA2	NMI	NMI	NMI	NMI	Unused	—	—
B2	OM_CS1#	NC	OM_CS1#	P24_0	OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
A4	OM_DQS	NC	OM_DQS	P24_1	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
B4	OM_SIO4	NC	OM_SIO4	P24_2	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
A3	OM_SIO5	NC	OM_SIO5	P24_3	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
B3	OM_SIO6	NC	OM_SIO6	P24_4	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
A2	OM_SIO7	NC	OM_SIO7	P24_5	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused on the board for the RZ/G2UL	—	—
F14	OTP_VDD18	OTP_VDD18	OTP_VDD18	NC	1.8 V *Note*: Unused on the board for the RZ/Five	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (5/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
B1	P0_0/SD0_CD/ RIIC3_SDA/ MTIOC2A/ SCI0_TXD	P0_0/SD0_CD	P0_0/SD0_CD	P0_0/SD0_CD	Card detection microSD ch. 0 card slot *Note*: Only available when SW_SD0_DEV_SEL(SW 1-2) is disabled; otherwise this is used for GPIO0.	P108	GPIO0
C2	P0_1/SD0_WP/ RIIC3_SCL/ MTIOC2B/ SCI0_RXD	P0_1	P0_1	P0_1	24-pin FFC connector on the RZ SMARC Carrier, used as CAM1_RST#	P111	GPIO3
D3	P0_2/SD1_CD/ MTIOC1A/ RIIC2_SDA/IRQ0	SD1_CD	SD1_CD	SD1_CD	Card detection High level: No card; low level: Card inserted microSD ch. 1 card slot on the RZ SMARC Carrier	P35	SDIO_ CD#
C3	P0_3/SD1_WP/ MTIOC1B/ RIIC2_SCL/IRQ1	P0_3	P0_3	P0_3	microSD ch. 1 card slot on the RZ SMARC Carrier For switching the power of the card slot on or off	P37	SDIO_ PWR_EN
P1	P4_5/ ET0_LINKSTA/ MTIOC3D	P4_5/ ET0_LINKSTA	P4_5/ ET0_LINKSTA	P4_5/ ET0_LINKSTA	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD1 connector (J2) on the RZ SMARC Carrier	P119	GPIO11
T3	P4_3/ET0_MDC/ RSPI1_SSL/ MTIOC8D/ MTIOC3B	RSPI1_SSL/ ET0_MDC	RSPI1_SSL/ ET0_MDC	RSPI1_SSL/ ET0_MDC	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	P54	SPI_CS0#
T2	P4_4/ET0_MDIO/ MTIOC3C	P4_4/ET0_MDIO	P4_4/ET0_MDIO	P4_4/ET0_MDIO	Exclusive operation between Ethernet PHY_0 (IC22) and the 24-pin FFC connector on the RZ SMARC Carrier, used as CAM1_PWR#	P109	GPIO1
N1	P3_1/ ET0_RX_CTL/ RX_DV/ SSI1_RCK/ POE4#/MTIOC0B	SSI1_RCK/ ET0_RX_CTL/ RX_DV	SSI1_RCK/ ET0_RX_CTL/ RX_DV	SSI1_RCK/ ET0_RX_CTL/ RX_DV	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	S39	I2S0_LRCK
N2	P4_2/ ET0_RX_ERR/ RSPI1_MISO/ MTIOC8C/ MTIOC3A	RSPI1_MISO	RSPI1_MISO	RSPI1_MISO	PMOD0 connector (J1) on the RZ SMARC Carrier	P57	SPI1_DIN
AD20	P10_0/ ET1_RXD3/ SSI0_BCK/IRQ4/ MTIOC6A/IRQ2	ET1_RXD3	ET1_RXD3	ET1_RXD3	Ethernet PHY_1 (IC23)	—	—
AD18	P10_1/ ET1_RX_ERR/ SSI0_RCK/ SSI3_BCK/ MTIOC6B	ET1_ERR	ET1_ERR	ET1_ERR	Unused	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (6/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AC20	P10_2/ ET1_MDC/ SSI0_TXD/ SSI3_RCK/ MTIOC6C	ET1_MDC	ET1_MDC	ET1_MDC	Ethernet PHY_1 (IC23)	—	—
AE21	P10_3/ ET1_MDIO/ SSI0_RXD/ SSI3_TXD/ USB1_VBUSEN/ MTIOC6D	ET1_MDIO	ET1_MDIO	ET1_MDIO	Ethernet PHY_1 (IC23)	—	—
AC19	P10_4/ ET1_LINKSTA/ ADC_TRG/ SSI3_RXD/ USB1_OVRCUR	ET1_LINKSTA	ET1_LINKSTA	ET1_LINKSTA	Ethernet PHY_1 (IC23)	—	—
A10	P11_3/SSI0_RXD /POE10#/ SCI1_CTS#/ RTS#/ RSPI2_SSL/ DISP_CLK	DISP_CLK	DISP_CLK	P11_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	A10
B10	P11_2/SSI0_TXD /POE8#/ SCI1_SCK/ RSPI2_MISO/ DISP_DATA0/ SCIF1_TXD	DISP_DATA0	DISP_DATA0	P11_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	B10
A11	P13_1/ SCIF0_RXD/ CAN0_TX/ MTIOC4B/ USB1_OVRCUR/ DISP_DATA1/ SCIF1_RXD	DISP_DATA1	DISP_DATA1	P13_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	A11
A14	P16_0/ SCIF1_CTS#/ CAN1_RX_DATA RATE_EN/ SCI0_CTS#/ RTS#/ DISP_DATA10	DISP_DATA10	DISP_DATA10	P16_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	A14
C14	P15_0/RSPI0_CK /IRQ4/MTIOC8A/ DISP_DATA11	DISP_DATA11	DISP_DATA11	P15_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	C14
B14	P16_1/ SCIF1_RTS#/ DISP_DATA12	DISP_DATA12	DISP_DATA12	P16_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C15	P15_1/ RSPI0_MOSI/ IRQ5/MTIOC8B/ DISP_DATA13	DISP_DATA13	DISP_DATA13	P15_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A15	P15_3/ RSPI0_SSL/ IRQ7/MTIOC8D/ DISP_DATA14	DISP_DATA14	DISP_DATA14	P15_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (7/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
F16	P18_0/IRQ2/ ADC_TRG/ SCI0_SCK/ DISP_DATA15/ SCIF3_SCK	DISP_DATA15	DISP_DATA15	P18_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B15	P15_2/ RSPI0_MISO/ IRQ6/MTIOC8C/ DISP_DATA16/ SCI1_TXD	DISP_DATA16	DISP_DATA16	P15_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C16	P17_0/ RRRSPI2_CK/ SSI1_BCK/ CAN1_TX/ MTIOC3A/ DISP_DATA17/ SCI1_RXD	DISP_DATA17	DISP_DATA17	P17_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A16	P17_2/ RSPI1_MISO/ SSI1_TXD/ CAN1_TX_ DATARATE_EN/ MTIOC3C/ DISP_DATA18	DISP_DATA18	DISP_DATA18	P17_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B16	P17_1/ RSPI1_MOSI/ SSI1_RCK/ CAN1_RX/ MTIOC3B/ DISP_DATA19	DISP_DATA19	DISP_DATA19	P17_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B11	P13_0/ SCIF0_TXD/ CAN_CLK/ MTIOC4A/ USB1_VBUSEN/ DISP_DATA2	DISP_DATA2	DISP_DATA2	P13_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A17	P18_1/IRQ3/ SCIF3_SCK/ SCI0_TXD/ DISP_DATA20/ SCIF3_RXD	DISP_DATA20	DISP_DATA20	P18_1	Connected to 45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B17	P18_2/IRQ4/ RSPI0_CK/ SCI0_SCK/ SCIF3_RXD/ SCI0_RXD/ DISP_DATA21/ SCIF3_TXD	DISP_DATA21	DISP_DATA21	P18_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C17	P17_3/ RSPI1_SSL/ SSI1_RXD/ CAN1_RX_ DATARATE_EN/ MTIOC3D/ DISP_DATA22	DISP_DATA22	DISP_DATA22	P17_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (8/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C20	P18_3/IRQ5/ RSPI0_MOSI/ SCI0_TXD/ SCIF3_TXD/ SCI0_CTS#/ RTS#/ DISP_DATA23/ SCIF4_SCK	DISP_DATA23	DISP_DATA23	P18_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A12	P13_4/ SCIF0_RTS#/ CAN0_RX_ DATARATE_EN/ DISP_DATA3	DISP_DATA3	DISP_DATA3	P13_4	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B12	P13_3/ SCIF0_CTS#/ CAN0_TX_ DATARATE_EN/ MTIOC4D/ DISP_DATA4	DISP_DATA4	DISP_DATA4	P13_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C17	P17_3/ RSPI1_SSL/ SSI1_RXD/ CAN1_RX_ DATARATE_EN/ MTIOC3D/ DISP_DATA22	DISP_DATA22	DISP_DATA22	P17_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C20	P18_3/IRQ5/ RSPI0_MOSI/ SCI0_TXD/ SCIF3_TXD/ SCI0_CTS#/ RTS#/ DISP_DATA23/ SCIF4_SCK	DISP_DATA23	DISP_DATA23	P18_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A12	P13_4/ SCIF0_RTS#/ CAN0_RX_ DATARATE_EN/ DISP_DATA3	DISP_DATA3	DISP_DATA3	P13_4	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B12	P13_3/ SCIF0_CTS#/ CAN0_TX_ DATARATE_EN/ MTIOC4D/ DISP_DATA4	DISP_DATA4	DISP_DATA4	P13_3	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C11	P12_1/IRQ1/ SCI0_TXD/ MTIOC0B/ SCIF3_RXD/ DISP_DATA5	DISP_DATA5	DISP_DATA5	P12_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C12	P13_2/ SCIF0_SCK/ CAN0_RX/ MTIOC4C/ DISP_DATA6	DISP_DATA6	DISP_DATA6	P13_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (9/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C13	P14_0/ SCIF1_TXD/ CAN1_TX/ MTIC5U/ SCI0_RXD/ DISP_DATA7	DISP_DATA7	DISP_DATA7	P14_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
A13	P14_2/ SCIF1_SCK/ ADC_TRG/ CAN1_TX_ DATARATE_EN/ MTIC5W/ SCI0_SCK/ DISP_DATA8/ IRQ3	DISP_DATA8	DISP_DATA8	P14_2	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B13	P14_1/ SCIF1_RXD/ CAN1_RX/ MTIC5V/ SCI0_TXD/ DISP_DATA9/ IRQ2	DISP_DATA9	DISP_DATA9	P14_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C9	P11_1/ SSI0_RCK/ POE4#/ SCI1_TXD/ RSPI2_MOSI/ DISP_DE	DISP_DE	DISP_DE	P11_1	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B9	P11_0/SSI0_BCK /POE0#/ SCI1_RXD/ RSPI2_CK/ DISP_HSYNC	DISP_HSYNC	DISP_HSYNC	P11_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
C10	P12_0/IRQ0/ SCI0_RXD/ MTIOC0A/ SCIF3_TXD/ DISP_VSYNC	DISP_VSYNC	DISP_VSYNC	P12_0	45-pin FFC/FPC connector (CN5) *Note*: Unused on the board for the RZ/Five	—	—
B22	P18_4/IRQ6/ RSPI0_MISO/ SCI0_RXD/ USB1_VBUSEN/ ADC_TRG/ SCI1_TXD/ SCIF4_RXD	IRQ6	IRQ6	IRQ6	PMOD0 connector (J1) on the RZ SMARC Carrier	P114	GPIO4
A21	P18_5/IRQ7/ RSPI0_SSL/ SCI0_CTS#/ RTS#/ USB1_OVRCUR/ SCI1_RXD/ SCIF4_TXD	IRQ7	IRQ7	IRQ7	Ethernet PHY_1 (IC23), used as an interrupt signal	—	—
N3	P3_0/ET0_RXC/ RX_CLK/ SSI1_BCK/ POE0#/MTIOC0A	ET0_RXC/ RX_CLK/ SSI1_BCK	ET0_RXC/ RX_CLK/ SSI1_BCK	ET0_RXC/ RX_CLK/ SSI1_BCK	Exclusive operation between Ethernet PHY_0 (IC22) and the Audio Codec (IC2) on the RZ SMARC Carrier	S42	I2S0_CK

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (10/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
P2	P3_2/ET0_RXD0/ SSI1_TXD/ POE8#/MTIOC0C	ET0_RXD0/ SSI1_TXD	ET0_RXD0/ SSI1_TXD	ET0_RXD0/ SSI1_TXD	Exclusive operation between Ethernet PHY_0 (IC22) and the Audio Codec (IC2) on the RZ SMARC Carrier	S40	I2S0_ SDOUT
R3	P3_3/ET0_RXD1/ SSI1_RXD/ POE10#/ MTIOC0D	ET0_RXD1/ SSI1_RXD	ET0_RXD1/ SSI1_RXD	ET0_RXD1/ SSI1_RXD	Exclusive operation between Ethernet PHY_0 (IC22) and the Audio Codec (IC2) on the RZ SMARC Carrier	S41	I2S0_SDIN
R2	P4_0/ET0_RXD2/ RRRSPI2_CK/ MTIOC8A/ MTIOC2A/ USB1_VBUSEN	ET0_RXD2/ RSPI1_CK	ET0_RXD2/ RSPI1_CK	ET0_RXD2/ RSPI1_CK	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	P56	SPI1_CK
R1	P4_1/ET0_RXD3/ RSPI1_MOSI/ MTIOC8B/ MTIOC2B/ USB1_OVRCUR	ET0_RXD3/ RSPI1_MOSI	ET0_RXD3/ RSPI1_MOSI	ET0_RXD3/ RSPI1_MOSI	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	P58	SPI1_DO
M3	P2_2/ET0_TX_ COL/SSI0_TXD/ CAN1_TX_ DATARATE_EN/ MTCLKC/ SCI0_TXD/ RSPI0_MOSI	ET0_TX_COL	ET0_TX_COL	ET0_TX_COL	Unused	—	—
M6	P2_3/ET0_TX_ CRS/SSI0_RXD/ CAN1_RX_ DATARATE_EN/ MTCLKD/ SCI0_RXD/ RSPI0_MISO	ET0_TX_CRS	ET0_TX_CRS	ET0_TX_CRS	Unused	—	—
M1	P1_1/ ET0_TX_CTL/ TX_EN/ RSPI0_MOSI/ CAN0_TX/ MTIOC1B	ET0_TX_CTL/ TX_EN/CAN0_ TX	ET0_TX_CTL/ TX_EN/CAN0_ TX	ET0_TX_CTL/ TX_EN/CAN0_ TX	Exclusive operation between Ethernet PHY_0 (IC22) and the CAN0 connector (CN15)*1 on the RZ SMARC Carrier	P143	CAN0_TX
K6	P2_1/ ET0_TX_ERR/ SSI0_RCK/ CAN1_RX/ MTCLKB/ SCI0_CLK/ RSPI0_CK	CAN1_RX	CAN1_RX	CAN1_RX	CAN1 connector (CN16)*1 on the RZ SMARC Carrier	P146	CAN1_RX
M2	P1_0/ET0_TXC/ TX_CLK/ RSPI0_CK/ CAN_CLK/ MTIOC1A	ET0_TXC_TX_ CLK/P1_0	ET0_TXC_TX_ CLK/P1_0	ET0_TXC_TX_ CLK/P1_0	Ethernet PHY_0 (IC22)	P113	GPIO5
L1	P1_2/ET0_TXD0/ RSPI0_MISO/ CAN0_RX/ MTIC5U	ET0_TXD0/ CAN0_RX	ET0_TXD0/ CAN0_RX	ET0_TXD0/ CAN0_RX	Exclusive operation between Ethernet PHY_0 (IC22) and the CAN0 connector (CN15)*1 on the RZ SMARC Carrier	P144	CAN0_RX

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (11/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
L2	P1_3/ET0_TXD1/ RSPI0_SSL/ CAN0_TX_ DATARATE_EN/ MTIC5V	ET0_TXD1/P1_3	ET0_TXD1/P1_3	ET0_TXD1/P1_3	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	P114	GPIO6
K1	P1_4/ET0_TXD2/ CAN0_RX_ DATARATE_EN/ MTIC5W	ET0_TXD2/P1_4	ET0_TXD2/P1_4	ET0_TXD2/P1_4	Exclusive operation between Ethernet PHY_0 (IC22) and the PMOD0 connector (J1) on the RZ SMARC Carrier	P115	GPIO7
K2	P2_0/ET0_TXD3/ SSI0_BCK/ CAN1_TX/ MTCLKA	ET0_TXD3/ CAN1_TX	ET0_TXD3/ CAN1_TX	ET0_TXD3/ CAN1_TX	Exclusive operation between Ethernet PHY_0 (IC22) and the CAN1 connector (CN16)*1 on the RZ SMARC Carrier	P145	CAN1_TX
AD3	P5_0/ USB0_VBUSEN/ SCIF2_TXD/ MTIOC7A	USB0_VBUSEN	USB0_VBUSEN	USB0_VBUSEN	Enables power to the USB2.0 OTG, USB Type-microAB (CN11) on the RZ SMARC Carrier, including the gate USB0_VBUSEN state	P62	USB0_EN_ OC#
AC3	P5_1/ SCIF2_RXD/ MTIOC7B/ ADC_TRG/ SCI0_CTS#/ RTS#/ RSPI0_SSL/IRQ2	IRQ2	IRQ2	IRQ2	Ethernet PHY_0 (IC22), used as an interrupt signal Carrier board connector connected to the PMOD1 connector (J2)	P118	GPIO10
AE3	P5_2/ USB0_OVRCUR/ SCIF2_SCK/ MTIOC7C/ SSI2_BCK	USB0_OVRCUR	USB0_OVRCUR	USB0_OVRCUR	Active low input when USB0 is over-current USB2.0 Host, USB Type-A (CN12) on the RZ SMARC Carrier, including the gate USB0_OVRCUR state	P62	USB0_EN_ OC#
AD2	P5_3/ USB0_OTG_ID/ SCIF2_CTS#/ MTIOC7D/ SSI2_RCK/ USB1_VBUSEN	USB0_OTG_ID	USB0_OTG_ID	USB0_OTG_ID	OTG identification input USB2.0 OTG, USB Type-microAB (CN11) on the RZ SMARC Carrier	P64	USB0_OTG_ ID
AB3	P5_4/ USB0_OTG_ EXICEN/ SCIF2_RTS#/ SSI2_DATA/ USB1_OVRCUR	USB1_OVRCUR	USB1_OVRCUR	USB1_OVRCUR	Active low input when USB1 is over-current USB2.0 Host, USB Type-A (CN12) on the RZ SMARC Carrier, including the gate USB1_OVRCUR state	P67	USB1_EN_ OC#
AD1	P6_0/ USB1_VBUSEN/ RSPI2_CK/ CAN_CLK/ SCIF2_TXD/ MTIOC7A	USB1_VBUSEN	USB1_VBUSEN	USB1_VBUSEN	Enables power to the USB2.0 Host, USB Type-A (CN12) on the RZ SMARC Carrier, including the gate USB1_VBUSEN state	P67	USB1_EN_ OC#
AE2	P6_1/ USB1_OVRCUR/ RSPI2_MOSI/ CAN0_TX/ SCIF2_RXD/ MTIOC7B	SD1_PWR_SEL	SD1_PWR_SEL	SD1_PWR_SEL	Input for controlling SD1_PVDD power level High level: 3.3 V; low level: 1.8 V	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (12/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AB2	P6_2/ADC_TRG/ RSPI2_MISO/ CAN0_RX/ SCIF2_SCK/ MTIOC7C/IRQ2	SD0_PWR_SEL/ ADC_TRG	SD0_PWR_SEL/ ADC_TRG	SD0_PWR_SEL/ ADC_TRG	Exclusive operation between the pin connector (CN1) for ADC input and the input for controlling the SD0_PVDD power level High level: 3.3 V; low level: 1.8 V *Note*: Only available when microSD is being used; otherwise this is for ADC_TRG input.	—	—
AC1	P6_3/RIIC2_SDA/ RSPI2_SSL/ CAN0_TX_ DATARATE_EN/ SCIF2_CTS#/ MTIOC7D/ SCIF0_RXD/ IRQ3	SCIF0_RXD	SCIF0_RXD	SCIF0_RXD	Debug UART (CN14) on the RZ SMARC Carrier	P141	SER3_RX
AC2	P6_4/RIIC2_SCL/ CAN0_RX_ DATARATE_EN/ SCIF2_RTS#/ ADC_TRG/ SCIF0_TXD/IRQ4	SCIF0_TXD	SCIF0_TXD	SCIF0_TXD	Debug UART (CN14) on the RZ SMARC Carrier	P140	SER3_TX
AE18	P7_0/ET1_TXC/ TX_CLK/ ADC_TRG/ RSPI2_CK/ CAN_CLK/ MTIOC0A/ SCIF2_TXD/IRQ5	ET1_TXC/ TX_CLK	ET1_TXC/ TX_CLK	ET1_TXC/ TX_CLK	Ethernet PHY_1 (IC23)	—	—
AD17	P7_1/ ET1_TX_CTL/ TX_EN/ SCI1_SCK/ RSPI2_MOSI/ CAN0_TX/ MTIOC0B/ SCIF2_RXD	ET1_TX_CTL/ TX_EN	ET1_TX_CTL/ TX_EN	ET1_TX_CTL/ TX_EN	Ethernet PHY_1 (IC23)	—	—
AD16	P7_2/ET1_TXD0/ SCI1_TXD/ RSPI2_MISO/ CAN0_RX/ MTIOC0C/ SCIF2_SCK	ET1_TXD0	ET1_TXD0	ET1_TXD0	Ethernet PHY_1 (IC23)	—	—
AE16	P7_3/ET1_TXD1/ SCI1_RXD/ RSPI2_SSL/ CAN0_TX_ DATARATE_EN/ MTIOC0D/ SCIF2_CTS#	ET1_TXD1	ET1_TXD1	ET1_TXD1	Ethernet PHY_1 (IC23)	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (13/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AD15	P7_4/ET1_TXD2/ SCI1_CTS#/ RTS#/IRQ2/ CAN0_RX_ DATARATE_EN/ SCIF2_RTS#	ET1_TXD2	ET1_TXD2	ET1_TXD2	Ethernet PHY_1 (IC23)	—	—
AE15	P8_0/ET1_TXD3/ SCIF0_SCK/ SCIF1_RXD/ SSI1_BCK/ SCI0_SCK/ MTIOC7A/IRQ1	ET1_TXD3	ET1_TXD3	ET1_TXD3	Ethernet PHY_1 (IC23)	—	—
AE17	P8_1/ ET1_TX_ERR/ SCIF0_RXD/ SCIF1_TXD/ SSI1_RCK/ SCI0_TXD/ MTIOC7B	ET1_TX_ERR	ET1_TX_ERR	ET1_TX_ERR	Unused	—	—
AC16	P8_2/ ET1_TX_COL/ SCIF0_TXD/ SCIF1_CTS#/ SSI1_TXD/ SCI0_RXD/ MTIOC7C	ET1_TX_COL	ET1_TX_COL	ET1_TX_COL	Unused	—	—
AC15	P8_3/ ET1_TX_CRS/ SCIF0_CTS#/ SCIF1_RTS#/ SSI1_RXD/ SCI0_CTS#/ RTS#/MTIOC7D	ET1_TX_CRS	ET1_TX_CRS	ET1_TX_CRS	Unused	—	—
AC17	P8_4/ET1_RXC/ RX_CLK/ SCIF0_RTS#	ET1_RXC/ RX_CLK	ET1_RXC/ RX_CLK	ET1_RXC/ RX_CLK	Ethernet PHY_1 (IC23)	—	—
AC18	P9_0/ ET1_RX_CTL/ RX_DV/ RSPI0_CK/ SSI2_BCK/ MTIOC4A/ SCIF4_SCK	ET1_RX_CTL_ RX_DV	ET1_RX_CTL_ RX_DV	ET1_RX_CTL_ RX_DV	Ethernet PHY_1 (IC23)	—	—
AE19	P9_1/ET1_RXD0/ RSPI0_MOSI/ SSI2_RCK/ MTIOC4B/ SCIF4_RXD	ET1_RXD0	ET1_RXD0	ET1_RXD0	Ethernet PHY_1 (IC23)	—	—
AD19	P9_2/ET1_RXD1/ RSPI0_MISO/ SSI2_DATA/ MTIOC4C/ SCIF4_TXD	ET1_RXD1	ET1_RXD1	ET1_RXD1	Ethernet PHY_1 (IC23)	—	—
AE20	P9_3/ET1_RXD2/ RSPI0_SSL/ IRQ3/MTIOC4D/ IRQ1	ET1_RXD2	ET1_RXD2	ET1_RXD2	Ethernet PHY_1 (IC23)	—	—
L3	PLL1_AVDD18	PLL1_AVDD18	PLL1_AVDD18	PLL1_AVDD18	1.8 V	—	—
U3	PLL23_AVDD18	PLL23_AVDD18	PLL23_AVDD18	PLL23_AVDD18	1.8 V	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (14/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
T6	PLL23_DVDD11	PLL23_DVDD11	PLL23_DVDD11	PLL23_DVDD11	1.1 V	—	—
N17	PLL4_AVDD18	PLL4_AVDD18	PLL4_AVDD18	PLL4_AVDD18	1.8 V	—	—
Y14	PLL5_AVDD18	PLL5_AVDD18	PLL5_AVDD18	PLL5_AVDD18	1.8 V	—	—
Y15	PLL5_DVDD11	PLL5_DVDD11	PLL5_DVDD11	NC	1.1 V *Note*: Unused on the board for the RZ/Five	—	—
F11	PLL6_AVDD18	PLL6_AVDD18	PLL6_AVDD18	PLL6_AVDD18	1.8 V	—	—
W2	PRST#	PRST#	PRST#	PRST#	Input system reset signal from DA9062	—	—
C19	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
F13	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
F19	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
F9	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
W6	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
Y10	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
Y18	PVDD	PVDD	PVDD	PVDD	3.3 V	—	—
A7	QSPI_RESET#	QSPI_RESET#	QSPI_RESET#	QSPI_RESET#	OctaFlash (IC2)	—	—
A6	QSPI_WP#	QSPI_WP#	QSPI_WP#	QSPI_WP#	Unused *Note*: On the board for the RZ/Five, this pin is used as WDTOVF_PERROUT#. A resistor (R79) is mounted for the WDTOVF option and a connection to a logic IC is made for using the NRESET function of the PMIC, but the WDT function is not currently available on the board.	—	—
C7	QSPI0_IO0	QSPI0_IO0	QSPI0_IO0	QSPI0_IO0	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
A5	QSPI0_IO1	QSPI0_IO1	QSPI0_IO1	QSPI0_IO1	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B7	QSPI0_IO2	QSPI0_IO2	QSPI0_IO2	QSPI0_IO2	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
C6	QSPI0_IO3	QSPI0_IO3	QSPI0_IO3	QSPI0_IO3	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B6	QSPI0_SPCLK	QSPI0_SPCLK	QSPI0_SPCLK	QSPI0_SPCLK	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B5	QSPI0_SSL	QSPI0_SSL	QSPI0_SSL	QSPI0_SSL	QSPI flash memory (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B19	RIIC0_SCL	RIIC0_SCL	RIIC0_SCL	RIIC0_SCL	24-pin FFC connector (CN1) on the RZ SMARC Carrier	S1	I2C_CAM_CK
B20	RIIC0_SDA	RIIC0_SDA	RIIC0_SDA	RIIC0_SDA	24-pin FFC connector (CN1) on the RZ SMARC Carrier	S2	I2C_CAM_DAT
A19	RIIC1_SCL	RIIC1_SCL	RIIC1_SCL	RIIC1_SCL	45-pin FFC/FPC connector, PMOD1 connector (J2), and audio codec (IC2) on the RZ SMARC Carrier	S48	I2C_GP_CK

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (15/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A20	RIIC1_SDA	RIIC1_SDA	RIIC1_SDA	RIIC1_SDA	45-pin FFC/FPC connector, PMOD1 connector (J2), and audio codec (IC2) on the RZ SMARC Carrier	S39	I2C_GP_DAT
G1	SD0_CLK	SD0_CLK	SD0_CLK	SD0_CLK	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
E2	SD0_CMD	SD0_CMD	SD0_CMD	SD0_CMD	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
F1	SD0_DATA0	SD0_DATA0	SD0_DATA0	SD0_DATA0	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
H3	SD0_DATA1	SD0_DATA1	SD0_DATA1	SD0_DATA1	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
F2	SD0_DATA2	SD0_DATA2	SD0_DATA2	SD0_DATA2	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
D2	SD0_DATA3	SD0_DATA3	SD0_DATA3	SD0_DATA3	eMMC memory (IC6) or microSD ch. 0 card slot (CN3)	—	—
E1	SD0_DATA4	SD0_DATA4	SD0_DATA4	SD0_DATA4	eMMC memory (IC6)	—	—
D1	SD0_DATA5	SD0_DATA5	SD0_DATA5	SD0_DATA5	eMMC memory (IC6)	—	—
E3	SD0_DATA6	SD0_DATA6	SD0_DATA6	SD0_DATA6	eMMC memory (IC6)	—	—
F3	SD0_DATA7	SD0_DATA7	SD0_DATA7	SD0_DATA7	eMMC memory (IC6)	—	—
G3	SD0_PVDD	SD0_PVDD	SD0_PVDD	SD0_PVDD	1.8/3.3 V	—	—
C1	SD0_RST#	SD0_RST#	SD0_RST#	SD0_RST#	eMMC memory (IC6)	—	—
G2	SD1_CLK	SD1_CLK	SD1_CLK	SD1_CLK	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P36	SD1_CLK
H6	SD1_CMD	SD1_CMD	SD1_CMD	SD1_CMD	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P34	SD1_CMD
H2	SD1_DATA0	SD1_DATA0	SD1_DATA0	SD1_DATA0	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P39	SDIO_D0
J3	SD1_DATA1	SD1_DATA1	SD1_DATA1	SD1_DATA1	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P40	SDIO_D1
J1	SD1_DATA2	SD1_DATA2	SD1_DATA2	SD1_DATA2	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P41	SDIO_D2
J2	SD1_DATA3	SD1_DATA3	SD1_DATA3	SD1_DATA3	microSD ch. 1 card slot (CN10) on the RZ SMARC Carrier	P42	SDIO_D3
K3	SD1_PVDD	SD1_PVDD	SD1_PVDD	SD1_PVDD	1.8/3.3 V	—	—
C8	SPI_PVDD	SPI_PVDD	SPI_PVDD	SPI_PVDD	1.8 V	—	—
U2	TCK/SWDCLK	TCK/SWDCLK	TCK/SWDCLK	TCK/SWDCLK	JTAG connector (CN2)	—	—
W1	TDI	TDI	TDI	TDI	JTAG connector (CN2)	—	—
V2	TDO	TDO	TDO	TDO	JTAG connector (CN2)	—	—
AD22	VSS	VSS	VSS	VSS	GND	—	—
U1	TMS/SWDIO	TMS/SWDIO	TMS/SWDIO	TMS/SWDIO	JTAG connector (CN2)	—	—
V1	TRST#	TRST#	TRST#	TRST#	JTAG connector (CN2)	—	—
AC9	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8 V	—	—
AC8	USB_RREF	USB_RREF	USB_RREF	USB_RREF	Connected to GND via the 1.8-kΩ resistor	—	—
AC4	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8 V	—	—
AC5	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8 V	—	—
Y7	USB_VDD33	USB_VDD33	USB_VDD33	USB_VDD33	3.3 V	—	—
Y8	USB_VDD33	USB_VDD33	USB_VDD33	USB_VDD33	3.3 V	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (16/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AC6	VSS	VSS	VSS	VSS	GND	—	—
AC7	VSS	VSS	VSS	VSS	GND	—	—
AD4	VSS	VSS	VSS	VSS	GND	—	—
AD7	VSS	VSS	VSS	VSS	GND	—	—
AE4	VSS	VSS	VSS	VSS	GND	—	—
AE7	VSS	VSS	VSS	VSS	GND	—	—
Y9	VSS	VSS	VSS	VSS	GND	—	—
AE6	USB0_DM	USB0_DM	USB0_DM	USB0_DM	USB2.0 OTG, USB Type-microAB (CN11) on the RZ SMARC Carrier	P61	USB0_DM
AD6	USB0_DP	USB0_DP	USB0_DP	USB0_DP	USB2.0 OTG, USB Type-microAB (CN11) on the RZ SMARC Carrier	P60	USB0_DP
AD8	USB0_VBUSIN	USB0_VBUSIN	USB0_VBUSIN	USB0_VBUSIN	USB2.0 OTG, USB Type-microAB (CN11) on the RZ SMARC Carrier	P63	USB0_VBUS_DET
AE5	USB1_DM	USB1_DM	USB1_DM	USB1_DM	USB2.0 Host, USB Type-A (CN12) on the RZ SMARC Carrier	P66	USB1_DM
AD5	USB1_DP	USB1_DP	USB1_DP	USB1_DP	USB2.0 Host, USB Type-A (CN12) on the RZ SMARC Carrier	P65	USB1_DP
K10	VDD	VDD	VDD	VDD	1.1 V	—	—
K12	VDD	VDD	VDD	VDD	1.1 V	—	—
K14	VDD	VDD	VDD	VDD	1.1 V	—	—
K16	VDD	VDD	VDD	VDD	1.1 V	—	—
L11	VDD	VDD	VDD	VDD	1.1 V	—	—
L13	VDD	VDD	VDD	VDD	1.1 V	—	—
L15	VDD	VDD	VDD	VDD	1.1 V	—	—
M10	VDD	VDD	VDD	VDD	1.1 V	—	—
M12	VDD	VDD	VDD	VDD	1.1 V	—	—
M14	VDD	VDD	VDD	VDD	1.1 V	—	—
M16	VDD	VDD	VDD	VDD	1.1 V	—	—
N11	VDD	VDD	VDD	VDD	1.1 V	—	—
N13	VDD	VDD	VDD	VDD	1.1 V	—	—
N15	VDD	VDD	VDD	VDD	1.1 V	—	—
P10	VDD	VDD	VDD	VDD	1.1 V	—	—
P12	VDD	VDD	VDD	VDD	1.1 V	—	—
P14	VDD	VDD	VDD	VDD	1.1 V	—	—
P16	VDD	VDD	VDD	VDD	1.1 V	—	—
R11	VDD	VDD	VDD	VDD	1.1 V	—	—
R13	VDD	VDD	VDD	VDD	1.1 V	—	—
R15	VDD	VDD	VDD	VDD	1.1 V	—	—
T10	VDD	VDD	VDD	VDD	1.1 V	—	—
T12	VDD	VDD	VDD	VDD	1.1 V	—	—
T14	VDD	VDD	VDD	VDD	1.1 V	—	—
T16	VDD	VDD	VDD	VDD	1.1 V	—	—
A1	VSS	VSS	VSS	VSS	GND	—	—
A25	VSS	VSS	VSS	VSS	GND	—	—
A8	VSS	VSS	VSS	VSS	GND	—	—
AA25	VSS	VSS	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (17/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AA3	VSS	VSS	VSS	VSS	GND	—	—
AB1	VSS	VSS	VSS	VSS	GND	—	—
AB23	VSS	VSS	VSS	VSS	GND	—	—
AC10	VSS	VSS	VSS	VSS	GND	—	—
AC11	VSS	VSS	VSS	VSS	GND	—	—
AC12	VSS	VSS	VSS	VSS	GND	—	—
AC13	VSS	VSS	VSS	VSS	GND	—	—
AC14	VSS	VSS	VSS	VSS	GND	—	—
AC21	VSS	VSS	VSS	VSS	GND	—	—
AC22	VSS	VSS	VSS	VSS	GND	—	—
AC23	VSS	VSS	VSS	VSS	GND	—	—
AC25	VSS	VSS	VSS	VSS	GND	—	—
AD14	VSS	VSS	VSS	VSS	GND	—	—
AE1	VSS	VSS	VSS	VSS	GND	—	—
AE14	VSS	VSS	VSS	VSS	GND	—	—
AE23	VSS	VSS	VSS	VSS	GND	—	—
AE25	VSS	VSS	VSS	VSS	GND	—	—
AE8	VSS	VSS	VSS	VSS	GND	—	—
C18	VSS	VSS	VSS	VSS	GND	—	—
C22	VSS	VSS	VSS	VSS	GND	—	—
C23	VSS	VSS	VSS	VSS	GND	—	—
D24	VSS	VSS	VSS	VSS	GND	—	—
E23	VSS	VSS	VSS	VSS	GND	—	—
F10	VSS	VSS	VSS	VSS	GND	—	—
F12	VSS	VSS	VSS	VSS	GND	—	—
F15	VSS	VSS	VSS	VSS	GND	—	—
F18	VSS	VSS	VSS	VSS	GND	—	—
F24	VSS	VSS	VSS	VSS	GND	—	—
F6	VSS	VSS	VSS	VSS	GND	—	—
F7	VSS	VSS	VSS	VSS	GND	—	—
F8	VSS	VSS	VSS	VSS	GND	—	—
G20	VSS	VSS	VSS	VSS	GND	—	—
G23	VSS	VSS	VSS	VSS	GND	—	—
G24	VSS	VSS	VSS	VSS	GND	—	—
H1	VSS	VSS	VSS	VSS	GND	—	—
J11	VSS	VSS	VSS	VSS	GND	—	—
J13	VSS	VSS	VSS	VSS	GND	—	—
J15	VSS	VSS	VSS	VSS	GND	—	—
J17	VSS	VSS	VSS	VSS	GND	—	—
J20	VSS	VSS	VSS	VSS	GND	—	—
J23	VSS	VSS	VSS	VSS	GND	—	—
J6	VSS	VSS	VSS	VSS	GND	—	—
J9	VSS	VSS	VSS	VSS	GND	—	—
K24	VSS	VSS	VSS	VSS	GND	—	—
L17	VSS	VSS	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function selections for Use with the Corresponding SMARC Module (18/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
L20	VSS	VSS	VSS	VSS	GND	—	—
L6	VSS	VSS	VSS	VSS	GND	—	—
L9	VSS	VSS	VSS	VSS	GND	—	—
M23	VSS	VSS	VSS	VSS	GND	—	—
N20	VSS	VSS	VSS	VSS	GND	—	—
N25	VSS	VSS	VSS	VSS	GND	—	—
N6	VSS	VSS	VSS	VSS	GND	—	—
N9	VSS	VSS	VSS	VSS	GND	—	—
P20	VSS	VSS	VSS	VSS	GND	—	—
R17	VSS	VSS	VSS	VSS	GND	—	—
R23	VSS	VSS	VSS	VSS	GND	—	—
R6	VSS	VSS	VSS	VSS	GND	—	—
R9	VSS	VSS	VSS	VSS	GND	—	—
T1	VSS	VSS	VSS	VSS	GND	—	—
T20	VSS	VSS	VSS	VSS	GND	—	—
U11	VSS	VSS	VSS	VSS	GND	—	—
U13	VSS	VSS	VSS	VSS	GND	—	—
U15	VSS	VSS	VSS	VSS	GND	—	—
U17	VSS	VSS	VSS	VSS	GND	—	—
U24	VSS	VSS	VSS	VSS	GND	—	—
U6	VSS	VSS	VSS	VSS	GND	—	—
U9	VSS	VSS	VSS	VSS	GND	—	—
V20	VSS	VSS	VSS	VSS	GND	—	—
V23	VSS	VSS	VSS	VSS	GND	—	—
V3	VSS	VSS	VSS	VSS	GND	—	—
V6	VSS	VSS	VSS	VSS	GND	—	—
W25	VSS	VSS	VSS	VSS	GND	—	—
W3	VSS	VSS	VSS	VSS	GND	—	—
Y1	VSS	VSS	VSS	VSS	GND	—	—
Y13	VSS	VSS	VSS	VSS	GND	—	—
Y16	VSS	VSS	VSS	VSS	GND	—	—
Y20	VSS	VSS	VSS	VSS	GND	—	—
Y23	VSS	VSS	VSS	VSS	GND	—	—
Y6	VSS	VSS	VSS	VSS	GND	—	—
B21	WDTOVF_ PERROUT#	WDTOVF_ PERROUT#	WDTOVF_ PERROUT#	NC	Connected to the SLG7RN45356 for using the NRESET function of DA9062 *Note*: Unused on the board for the RZ/Five	—	—
Y2	XIN	XIN	XIN	XIN	GND	—	—
AA1	XOUT	XOUT	XOUT	XOUT	OPEN	—	—

Note 1. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

4.2 Memory

QSPI flash memory and DDR4 SDRAM are mounted on the RZ/G2UL SMARC Module as external memory.

Please refer to the following for details.

4.2.1 QSPI Flash Memory

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board
QSPI Version

RZ/Five SMARC Module Board

Figure 4.1 shows a block diagram of the serial flash memory interface.

The QSPI flash memory is controlled by the SPI multi I/O bus controller (SPIBSC) of the RZ/G2UL. This flash memory defaults to standard SPI mode, and supports both single data rate (SDR) and double data rate (DDR) transfers at clock frequencies of 66 MHz and 50 MHz.

NOTE

For the pull-up resistor of the clock line “RZ_QSPI0_SPCLK”, place it wherever you want.

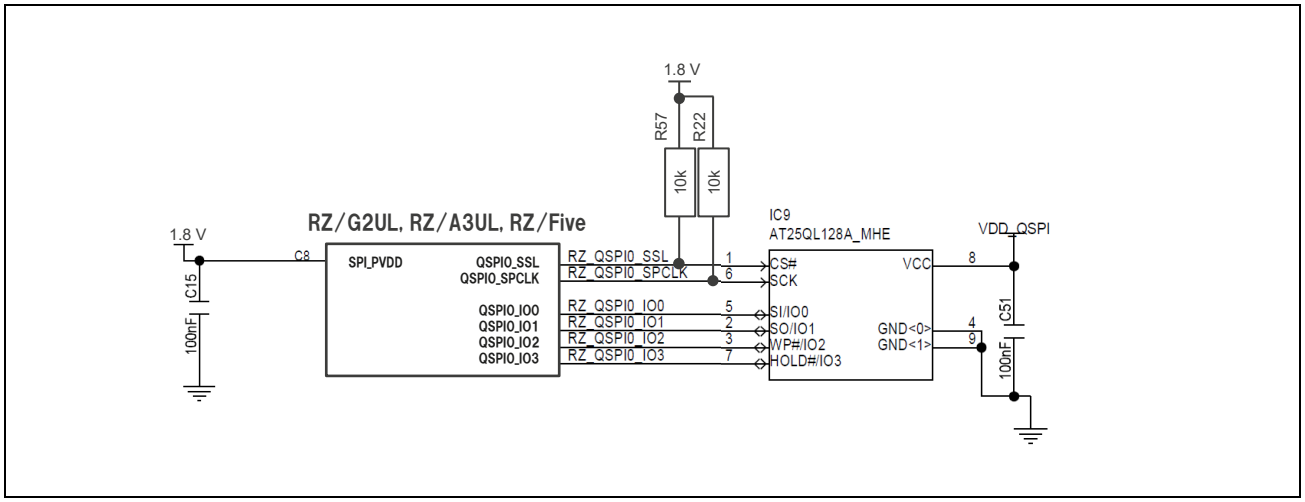


Figure 4.1 Block Diagram of Serial Flash Memory I/F

4.2.2 DDR4 SDRAM

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version

RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.2 shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the memory controller (MEMC) of the RZ/G2UL. It supports a data bus with of 16 bits, a data transfer rate of 1600 Mbps, and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

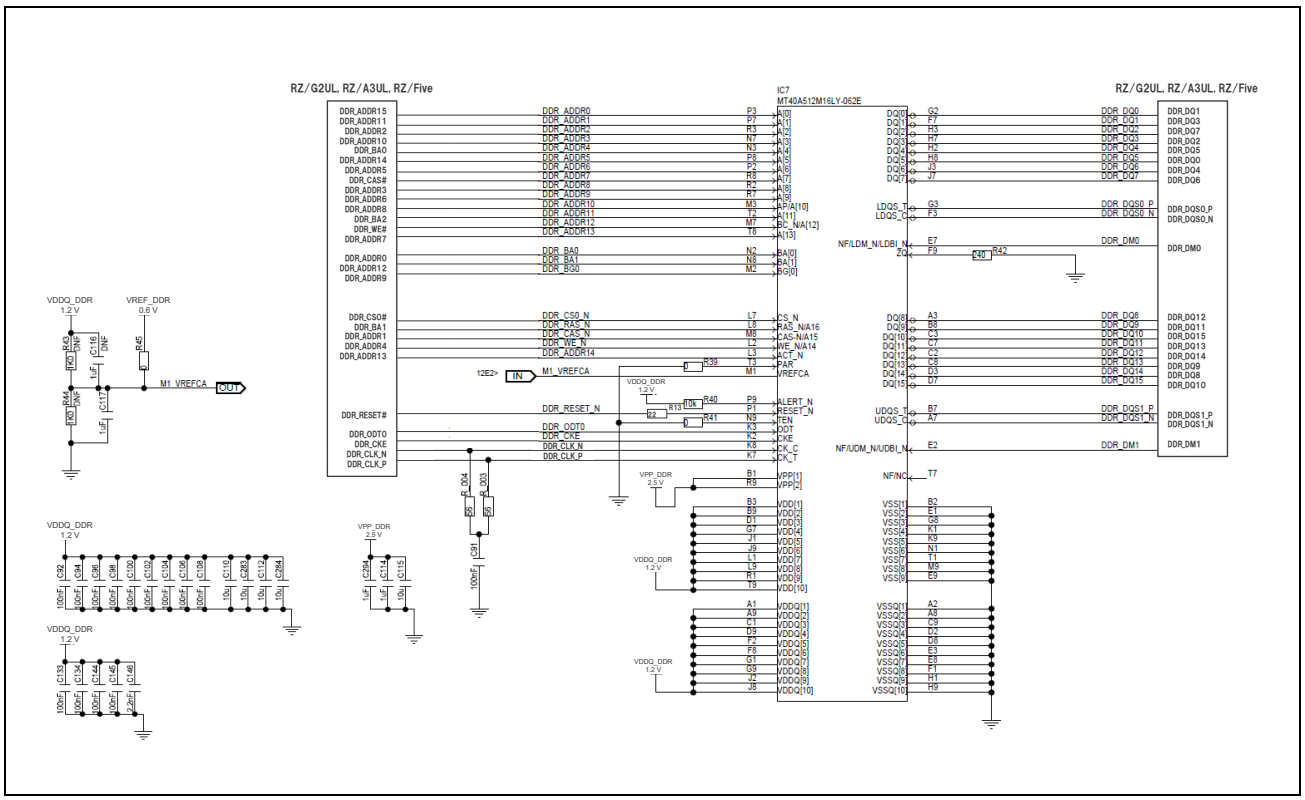


Figure 4.2 Block Diagram of DDR4 SDRAM I/F

4.2.3 Octa Peripheral Interface

RZ/A3UL SMARC Module Board
Octal-SPI Version

Figure 4.3 shows a block diagram of the Octa peripheral interface.

The OctaRAM and OctaFlash memories are controlled by the Octa memory controller of the RZ/A3UL. These memories support both single data rate (SOPI: Single Octa I/O) and double data rate (DOPI: Double Octa I/O) transfers at a clock frequency of 100 MHz.

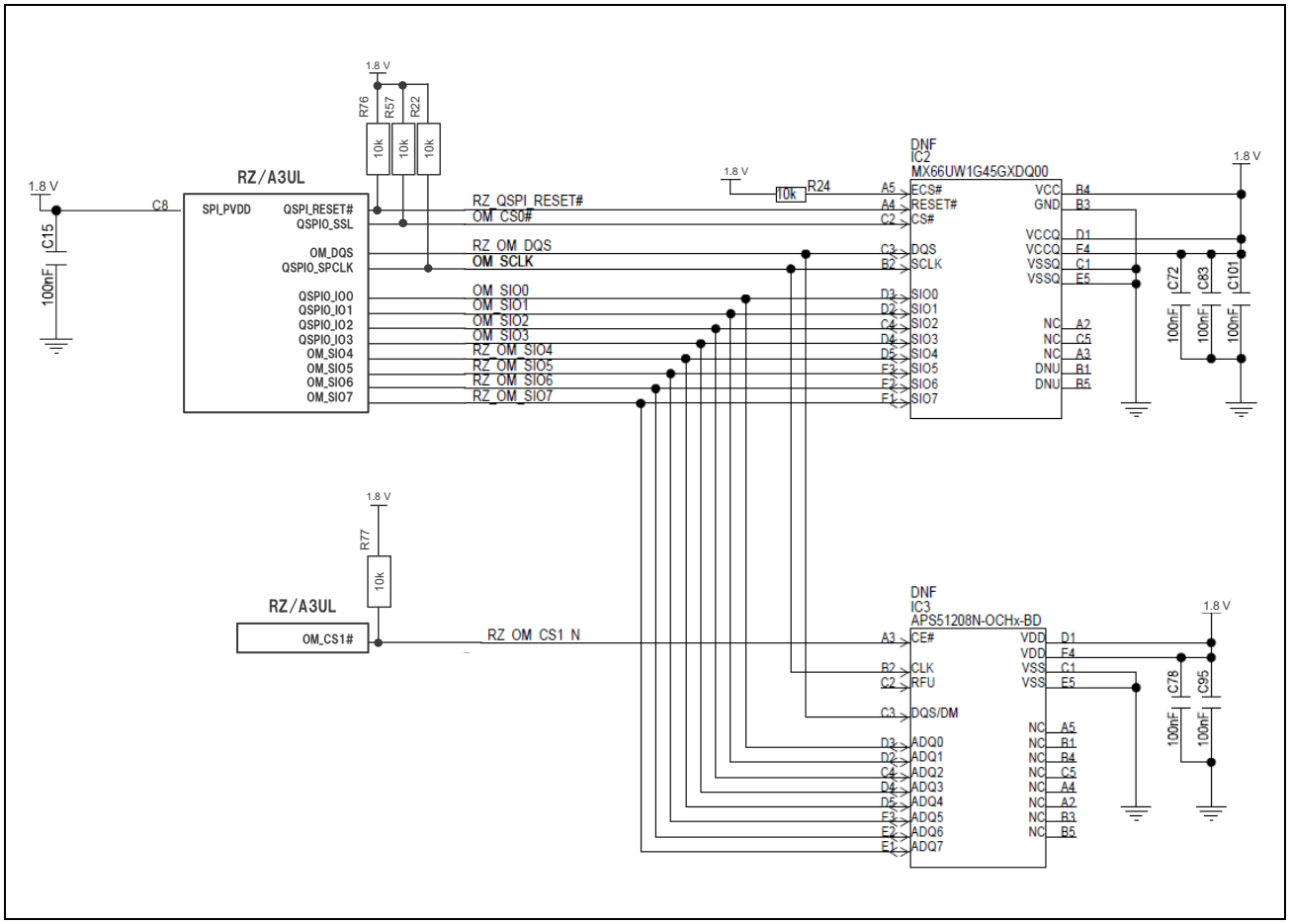


Figure 4.3 Block Diagram of Octa Peripheral I/F

4.3 Gigabit Ethernet Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version
RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.4 and **Figure 4.5** show block diagrams of the Gigabit Ethernet 0 and Ethernet 1 interfaces.

The Gigabit Ethernet interface is controlled by the Ethernet controller (E-MAC) of the RZ/G2UL. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

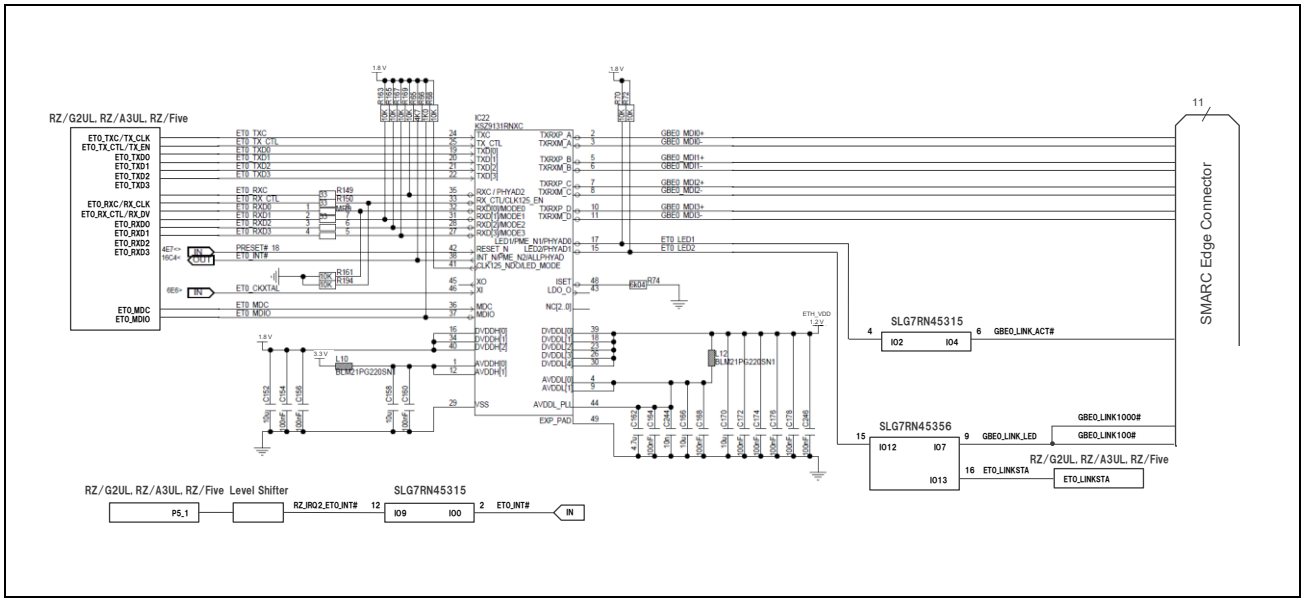


Figure 4.4 Block Diagram of Gigabit Ethernet 0 I/F

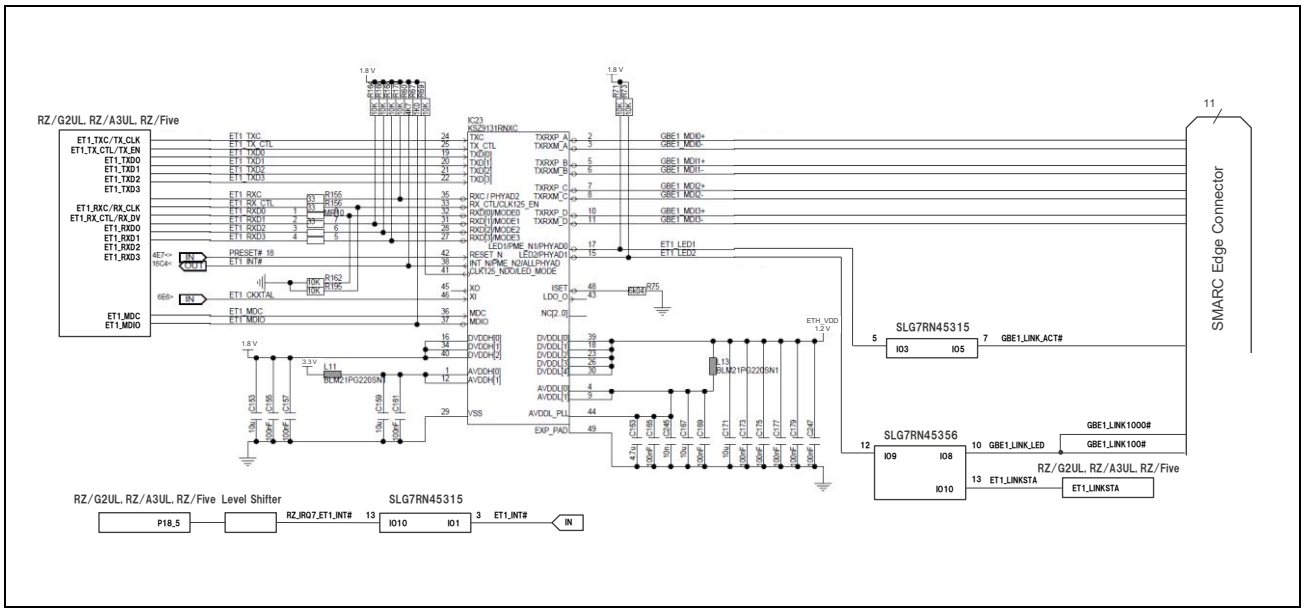


Figure 4.5 Block Diagram of Gigabit Ethernet 1 I/F

4.4 ADC Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version
RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.6 shows a block diagram of the ADC interface.

When the RZ/Five is used, the pin location is different from that of the RZ/G2UL, so option resistors are required.

The 6-pin connector is implemented on this board and the 2-channel input can be used as an analog signal.

NOTE

ADC_TRG is only available when SD0 is used for eMMC memory (not when microSD card is used).

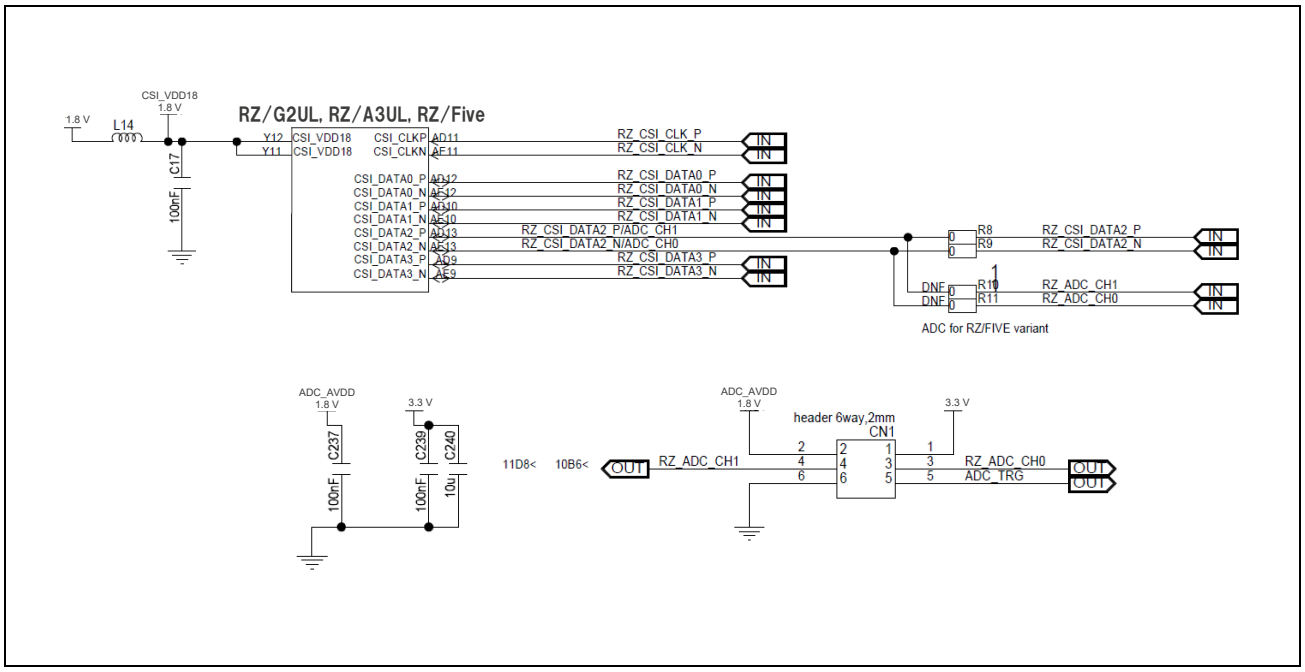


Figure 4.6 Block Diagram of ADC I/F

Table 4.2 Signal Connections of ADC Connector (CN1)

Pin	Signal Name	MPU
1	PVDD	—
2	ADC_AVDD18	—
3	RZ_ADC_CH0	ADC_CH0
4	RZ_ADC_CH1	ADC_CH1
5	RZ_SD0_PWR_SEL/ADC_TRG	P6_2
6	VSS	—

4.5 Clock Configuration

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.7 shows a block diagram of the clock configuration.

The clock generator (part number 5P35023B-629NLGI) provides the clock required for the RZ/G2UL and peripheral interfaces.

The 5P35023B is a Renesas VersaClock® 3S programmable clock generator that supports 6 unique frequency outputs.

The 5P35023B-629NLGI uses a 24-MHz crystal as the reference input and provides one 24-MHz reference clock output for the RZ/G2UL, two 11.2896-MHz LVCMOS clock outputs for the RZ/G2UL and Audio codec, two 25-MHz LVCMOS clock output for two Ethernet PHYs, and one 12.2880-MHz LVCMOS clock output for the RZ/G2UL.

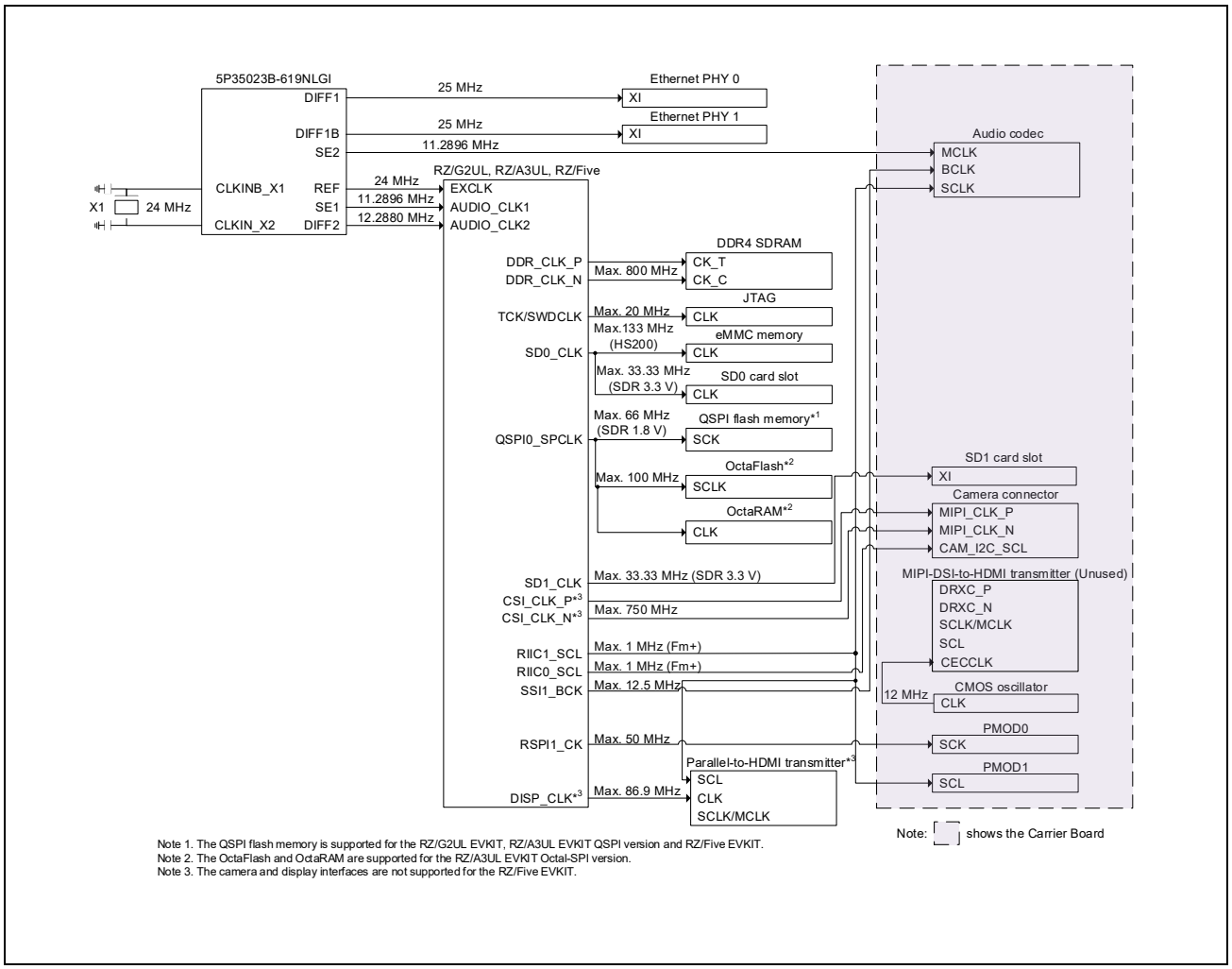


Figure 4.7 Block Diagram of Clock Configuration

4.6 Reset Control

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version
RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.8 shows a block diagram of reset control for the RZ/G2UL EVKIT.

Reset control for the RZ/G2UL and Ethernet PHYs is handled via the GreenPAK by reset signals generated by the PMIC.

The DDR4 SDRAM and eMMC memory are reset by the RZ/G2UL through software control.

The external emulator can reset the RZ/G2UL via the debug interface.

There are two types of system reset: a power-on reset and a reset by the button switch.

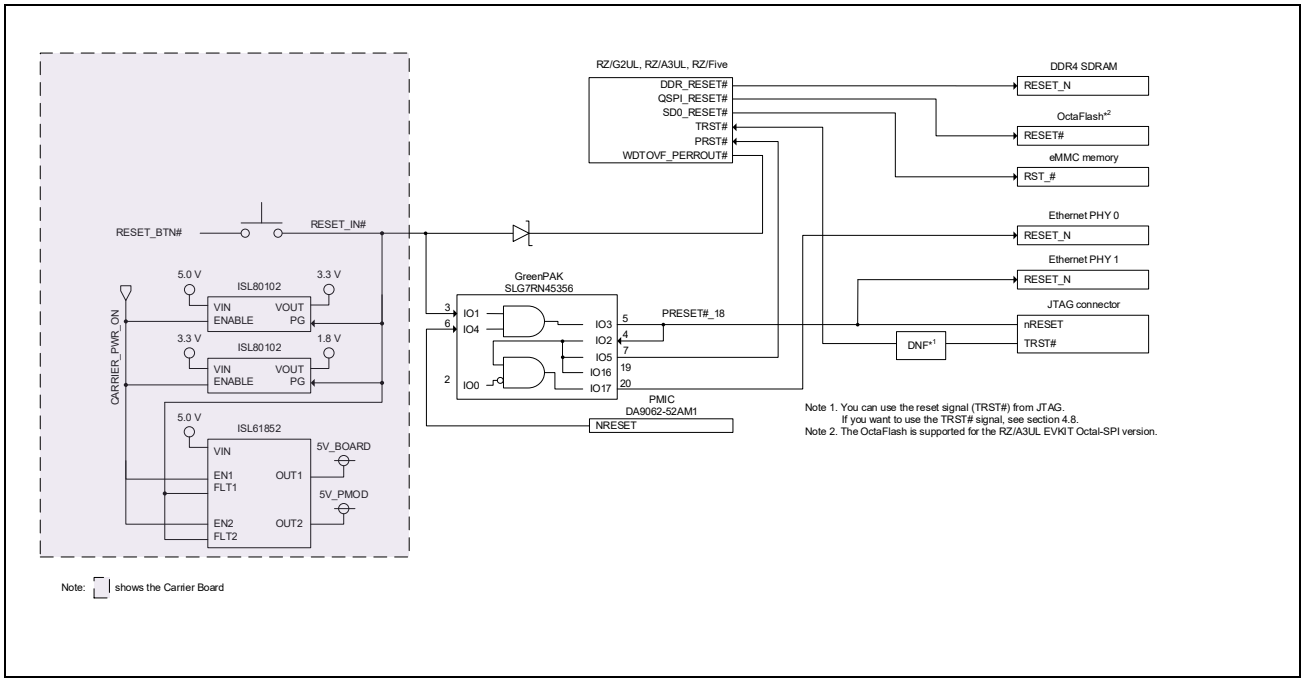


Figure 4.8 Block Diagram of Reset Control

4.7 Power Supply

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

4.7.1 Power Supply Configuration

Figure 4.9 shows a block diagram of the power configuration: **(a)** for RZ/G2UL and RZ/A3UL KITs, and **(b)** for RZ/Five EVKIT.

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5 V and 9 V.

The default setting for controlling the input voltage level is 5 V (max. 3 A input) when SW11-4 is switched on. When SW11-4 is switched off, the input voltage is set to 9 V (max. 3 A input). SW11-4 should be turned off only when the RZ/G2UL EVKIT is connected to external devices that require a lot of power and is expected to run out of power.

The 5-V power supply is supplied to the PMIC mounted on the RZ/G2UL SMARC Module, and the PMIC generates the power supply voltage for each interface.

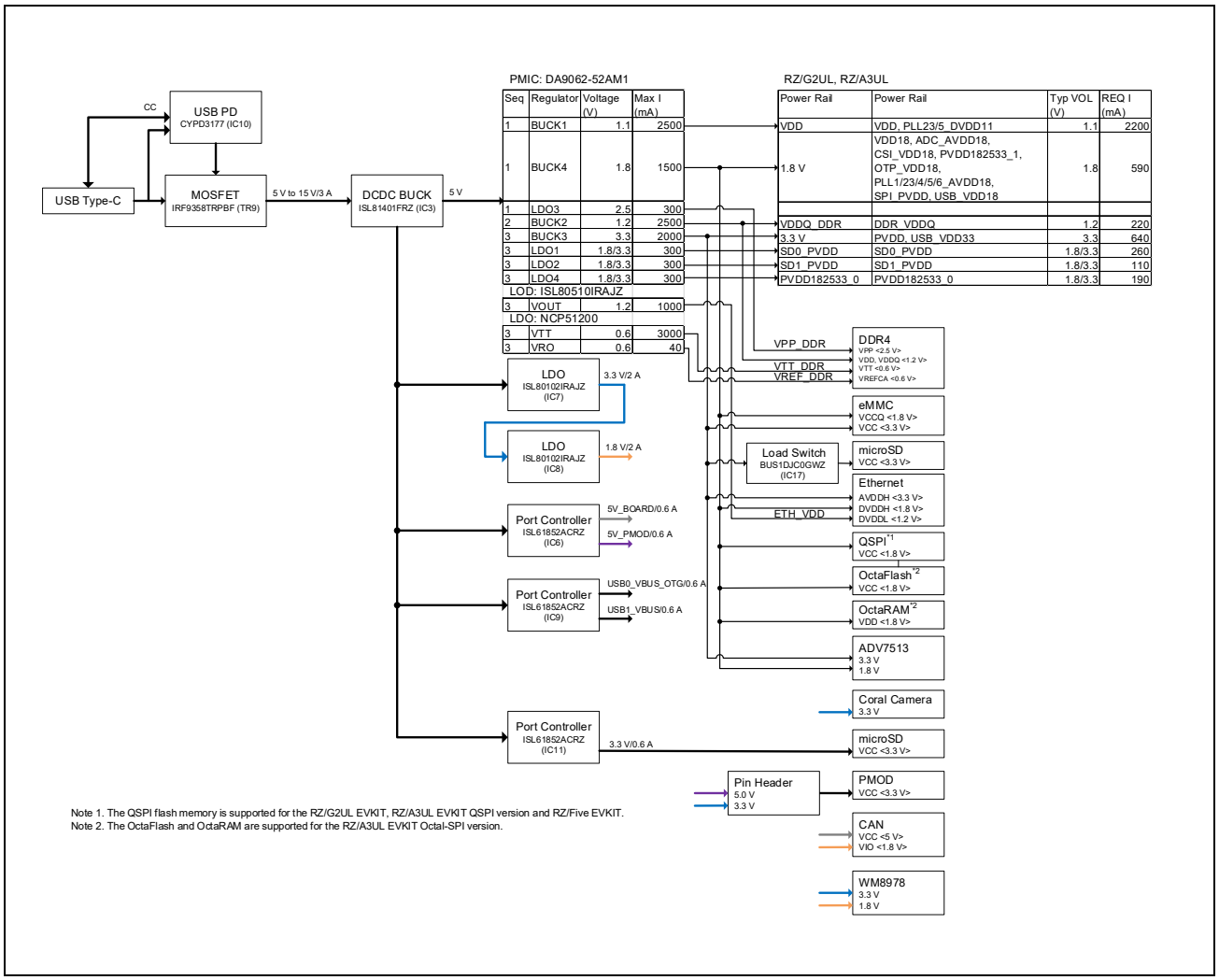


Figure 4.9 (a) Block Diagram of Power Configuration for RZ/G2UL and RZ/A3UL EVKIT

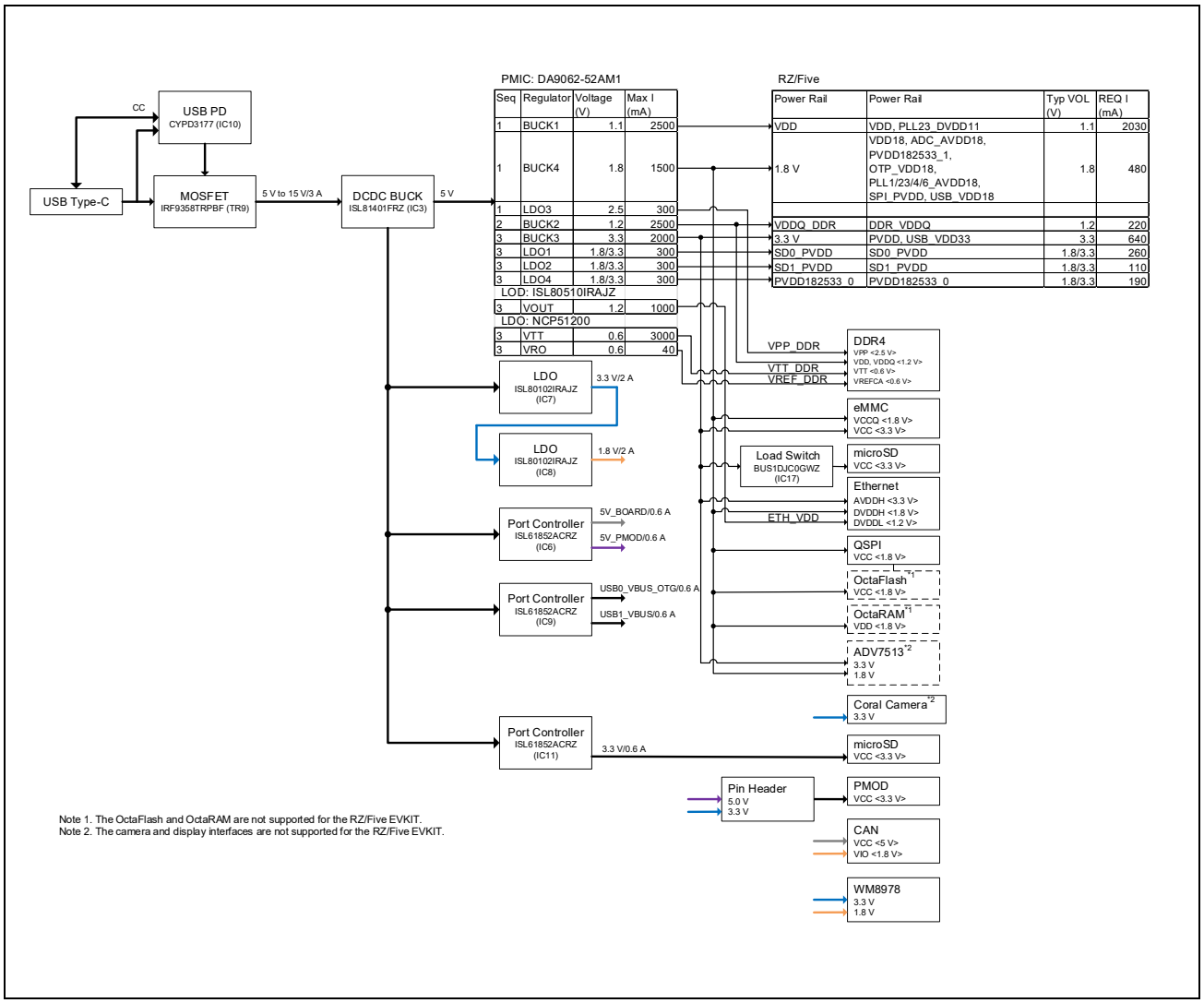


Figure 4.9 (b) Block Diagram of Power Configuration for RZ/Five EVKIT

4.7.2 PMIC

Figure 4.10 shows the RZ/G2UL pin assignment for the PMIC.

The DA9062-52AM1 is used as the PMIC on the RZ/G2UL EVKIT to supply and manage power for the RZ/G2UL.

It integrates 4 synchronous buck regulators and 4 LDO regulators to support power distribution and power sequencing control required by the RZ/G2UL.

The LDO2, LDO3, and LDO4 output voltage values for supply SD0_PVDD, SD1_PVDD, and PVDD182533_0 are fixed by P6_1, P6_2, and SW1-3.

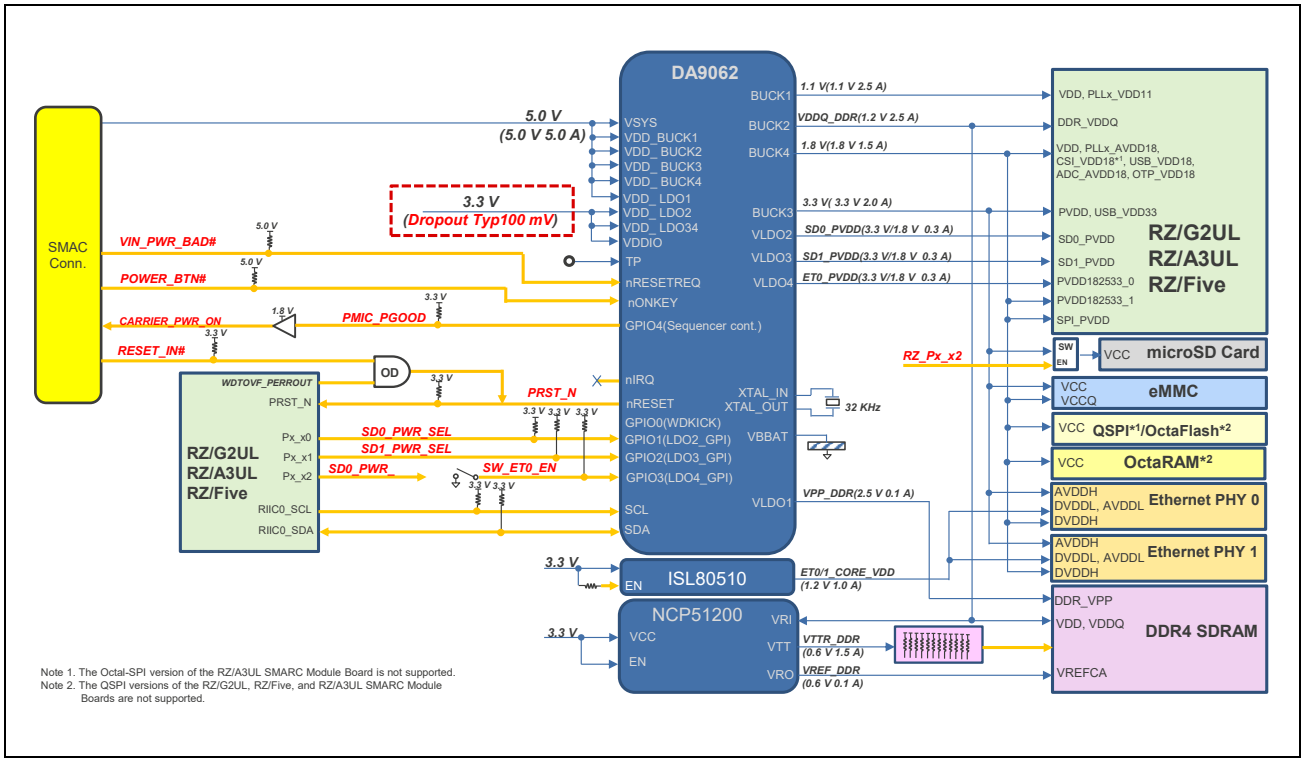


Figure 4.10 Block Diagram around PMIC

4.8 Debug Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version

RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.11 shows a block diagram of the debug interface.

This interface provides supports for debugging and development of the RZ/G2UL.

It allows an external debugger to be connected for debugging operations such as CPU core debugging and register access.

In default operation, pin 9 of the debug interface is used for ground detection. Although with resistor (R20) fitting options, it is possible to use the same pin to independently drive the JTAG_TRST# signal.

When debug mode is disabled (SW1-1: DEBUGEN is ON), JTAG_TRST# is permanently low.

On the other hand, when debug mode is enabled (SW1-1: DEBUGEN is OFF), JTAG_TRST# is initially low on powerup and then ramps up to 1.8 V.

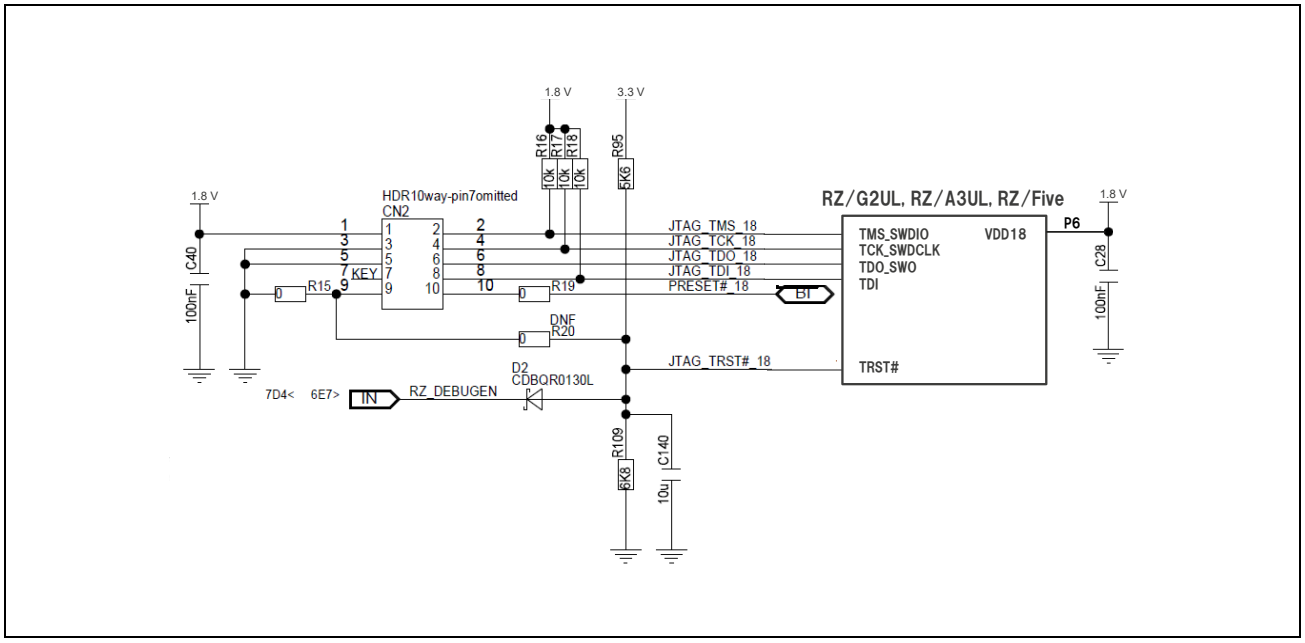


Figure 4.11 Block Diagram of Debug I/F

Table 4.3 Signal Connections of JTAG Connector (CN2)

Pin	Signal Name	MPU
1	1.8 V	—
2	JTAG_TMS_18	TMS/SWDIO
3	VSS	—
4	JTAG_TCK_18	TCK/SWDCLK
5	VSS	—
6	JTAG_TDO_18	TDO
7	—	—
8	JTAG_TDI_18	TDI
9	JTAG_TRST#_18	TRST#
10	PRESET#_18	PRST#

4.9 SD/MMC Host Interface

4.9.1 eMMC Memory

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version
RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.12 shows a block diagram of the MMC interface.

The eMMC memory is connected to channel 0 of the SD/MMC interface of the RZ/G2UL. This memory is used in conjunction with a microSD card.

The eMMC memory can be used when

- SW_SD0_DEV_SEL is enabled (SW1-2: Selection SD/MMC is OFF) *[1].

Note 1. The RZ/A3UL EVKIT does not support an eMMC boot.

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

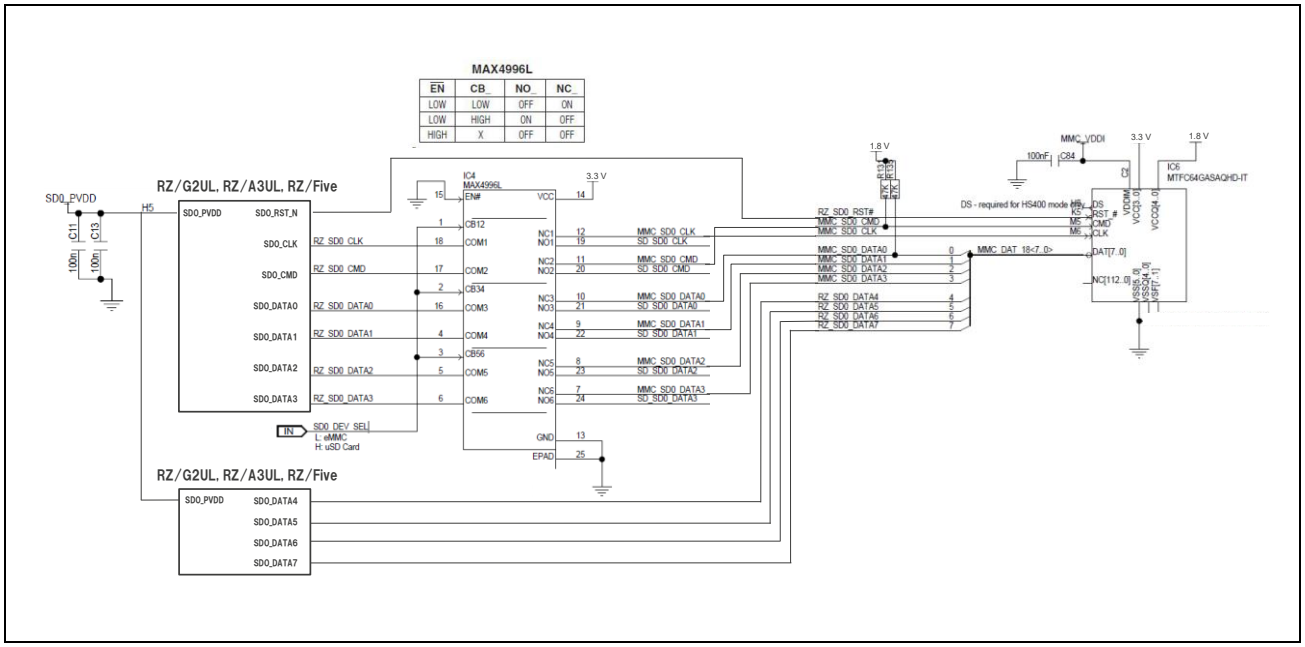


Figure 4.12 Block Diagram of eMMC I/F

4.9.2 microSD Card

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Version | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.13 shows a block diagram of the SDHI interface.

The microSD card is connected to channel 0 of the SD/MMC interface of the RZ/G2UL. This memory is used in conjunction with eMMC memory.

The microSD card can be used when

- microSD is the selected boot mode (SW11-1: ON, SW11-2: ON, SW11-3: OFF) *1, and
- SW_SD0_DEV_SEL is disabled (SW1-2: Selection SD/MMC is ON) and eMMC memory is not the selected boot mode (SW11-1: ON, SW11-2: OFF, SW11-3: OFF).

Note 1. The RZ/A3UL EVKIT does not support an eSD boot.

This interface complies with the memory card standard version 3.0 and supports UHS-I modes of 50MB/s (SDR50) and 104MB/s (SDR104).

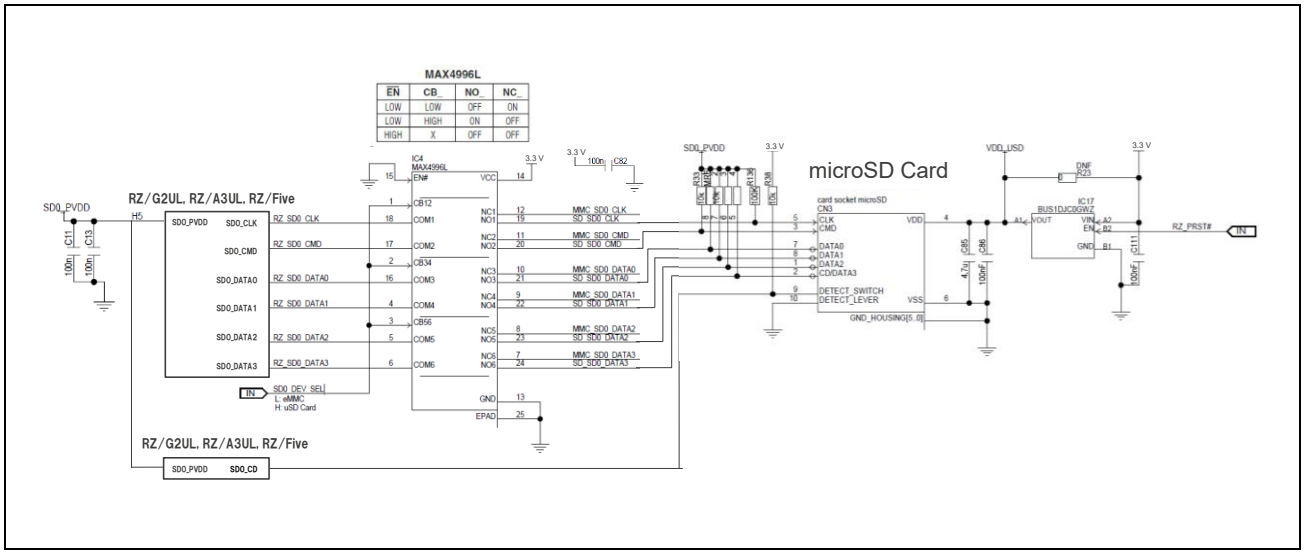


Figure 4.13 Block Diagram of SDHI I/F

Table 4.4 Signal Connections of microSD Card Slot (CN3)

Pin	Signal Name	MPU
1	SD_SD0_DATA2	SD0_DATA2
2	SD_SD0_DATA3	CD/SD0_DATA3
3	SD_SD0_CMD	SD0_CMD
4	3.3 V	PRST# (Power supply control*1)
5	SD_SD0_CLK	SD0_CLK
6	VSS	—
7	SD_SD0_DATA0	SD0_DATA0
8	SD_SD0_DATA1	SD0_DATA1
9	SD_SD0_CD	P0_0
10	—	—
—	SD0_PWR_SEL	P6_2 (IO voltage selection of SD0)

Note 1. Due to the circuit specifications, a software reset using GPIO is not supported. As a result, the power supply to the microSD ch.0 card cannot be controlled independently. In such cases, please use the power switch (SW9) to turn power to the board off and then back on again.

The following is an example of a circuit for executing a software reset.

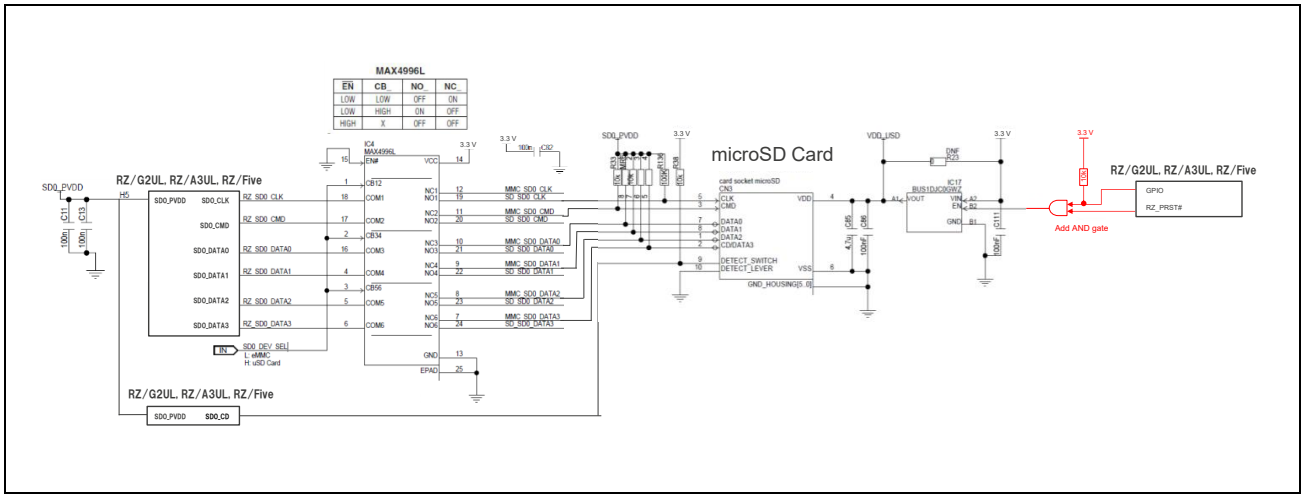


Figure 4.14 Proposed Block Diagram of SDHI I/F

4.10 GreenPAK

RZ/G2UL SMARC Module Board
RZ/A3UL SMARC Module Board QSPI Version
RZ/Five SMARC Module Board
RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.15 shows block diagrams of the GreenPAK ICs.

This board implements several types of GreenPAK with various integrated peripheral functions. **Table 4.5** lists the functions of each type of GreenPAK for use with this board.

GreenPAK is a programmable device.

The SLG7RN45314, SLG7RN45315, and SLG7RN45356 GreenPAK ICs are designed based on the SLG46538.

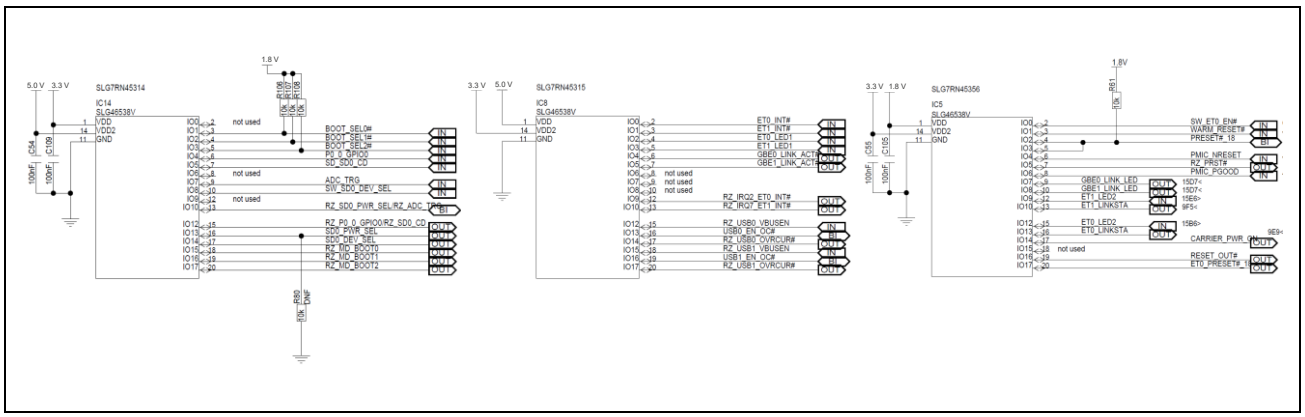


Figure 4.15 Block Diagrams of the GreenPAK ICs

Table 4.5 Features of the GreenPAK ICs

Part Number	Description
SLG7RN45314	SMARC boot mode SD0_CD / GPIO4 multiplexing SD0_PWR_SEL / ADC_TRG multiplexing SD0_DEV_SEL (microSD card or eMMC)
SLG7RN45315	USB0/1 Logic for EN_OC# Ethernet 0/1 Logic for interrupt level shifting LINK active LED driving
SLG7RN45356	Reset logic SMARC Carrier power on Ethernet 0/1 LINK LED driving LINK status inversion

The pin configuration and circuit diagram of each GreenPAK are shown below.

Table 4.6 Signal Connections of the SLG7RN45314 (IC14)

Pin	Pin Name	Signal Name	I/O	Buffer	Pin Function
1	VDD	3.3 V	Power	—	Connect to 3.3 V.
2	IO0	Not used	—	—	Open
3	IO1 (BOOT_SEL0#)	BOOT_SEL0#	I	LV	Connect to SW11-1 on the RZ SMARC Carrier. Select the boot mode.
4	IO2 (BOOT_SEL1#)	BOOT_SEL1#	I	LV	Connect to SW11-2 on the RZ SMARC Carrier. Select the boot mode.
5	IO3 (BOOT_SEL2#)	BOOT_SEL2#	I	LV	Connect to SW11-3 on the RZ SMARC Carrier. Select the boot mode.
6	IO4 (GPIO4)	P0_0_GPIO0	I	LV	Input for P0_0 of the RZ/G2UL
7	IO5 (SD0_CD)	SD_SD0_CD	I	LV	Input for card detection from a microSD card
8	IO6	Not used	—	—	Open
9	IO7 (ADC_TRG)	ADC_TRG	I	LV	Trigger input for starting A/D conversion
10	IO8 (SW_SD0_DEV_SEL)	SW_SD0_DEV_SEL	I	LV	Select the device connected to the SD0 I/F.
11	GND	—	GND	—	Connect to the ground.
12	IO9 (GPIO_SD_DEV_SEL)	Not used	—	—	Open
13	IO10 (GPIO_SD0_PWR_SEL/ ADC_TRG)	RZ_SD0_PWR_SEL/ RZ_ADC_TRG	I/O	Input: w/ Schmitt Output: PP	When the microSD card is connected, this pin selects input mode and can be used to select the IO voltage for the microSD card. When the eMMC memory is connected, this pin selects output mode and can be used as ADC_TRG.
14	VDD2	5.0 V	Power	—	Connect to 5.0 V.
15	IO12 (RZ_SD0_CD/GPIO4)	RZ_P0_0_GPIO0/ RZ_SD0_CD	O	PP	When the microSD card is selected by SW1-2, this pin can be used as SD0_CD. When the eMMC memory is selected by SW1-2, this pin can be used as GPIO0.
16	IO14 (SD0_PWR_SEL)	SD0_PWR_SEL	O	PP	Determine the IO voltage for the SD0 I/F. L: 1.8 V H: 3.3 V
17	IO15 (SD0_DEV_SEL)	SD0_DEV_SEL	O	PP	Determine the device connected to the SD0 I/F. L: eMMC H: microSD card
18	IO16 (RZ_BD_BOOT0)	RZ_BD_BOOT0	O	PP	Determine the boot mode.
19	IO17 (RZ_BD_BOOT1)	RZ_BD_BOOT1	O	PP	
20	IO18 (RZ_BD_BOOT2)	RZ_BD_BOOT2	O	PP	

MD_BOOT2	MD_BOOT1	MD_BOOT0	Connected Device
0	0	0	eSD (3.3 V at startup)
0	0	1	1.8-V eMMC
0	1	1	1.8-V QSPI flash memory
1	0	1	Downloading through SCIF

Remarks: LV: Low voltage digital input
PP: Push pull output
w/ Schmitt: Digital in with Schmitt trigger

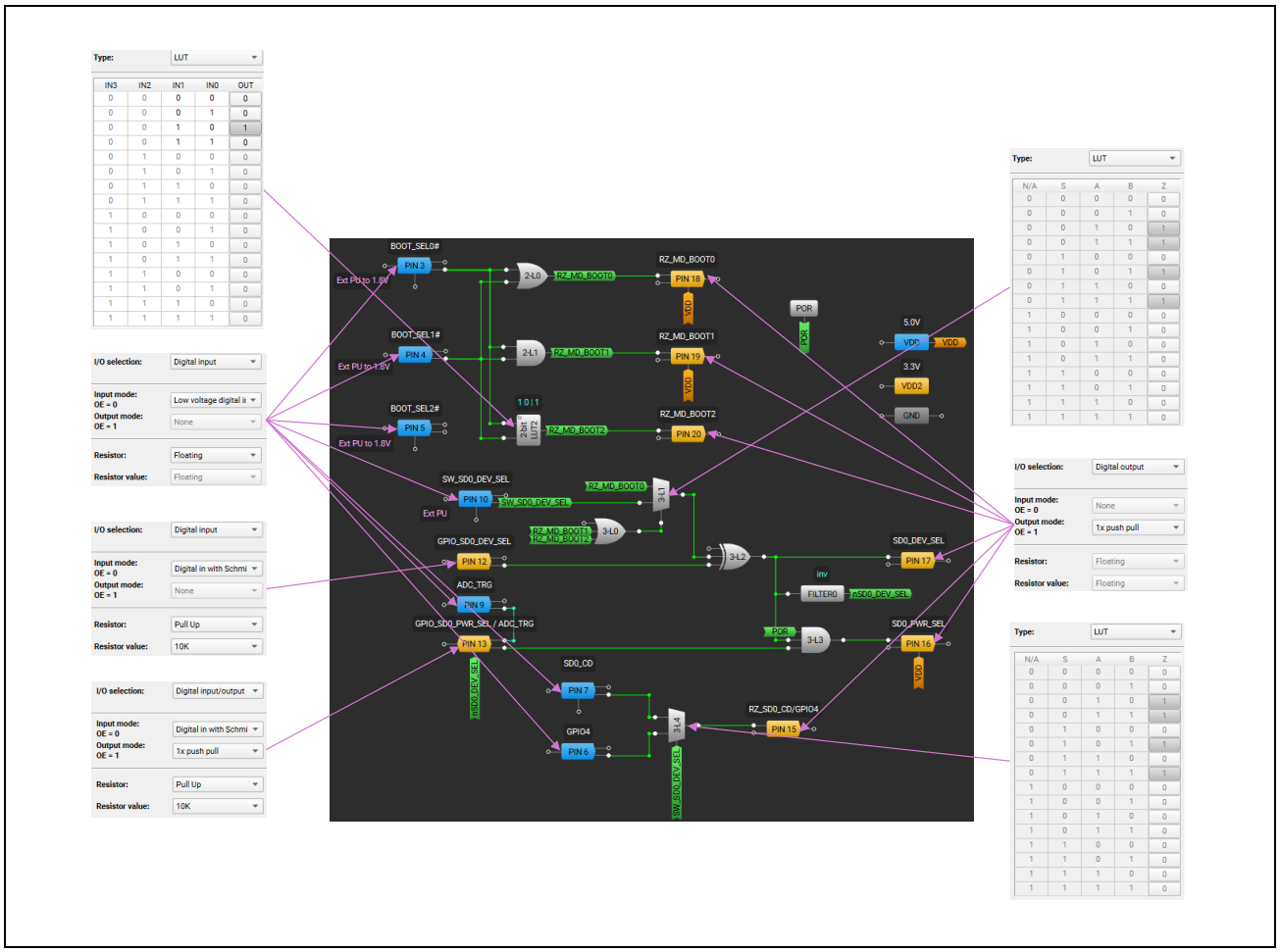


Figure 4.16 Circuit Diagram of the SLG7RN45314

Table 4.7 Signal Connections of the SLG7RN45315 (IC8)

Pin	Pin Name	Signal Name	I/O	Buffer	Pin Function
1	VDD	3.3 V	Power	—	Connect to 3.3 V.
2	IO0 (ET0_INT#)	ET0_INT#	I	LV	Interrupt input from Ethernet PHY 0
3	IO1 (ET1_INT#)	ET1_INT#	I	LV	Interrupt input from Ethernet PHY 1
4	IO2 (ET0_LED0#)	ET0_LED1	I	LV	Activity status indication of Ethernet PHY 0
5	IO3 (ET0_LED1#)	ET1_LED1	I	LV	Activity status indication of Ethernet PHY 1
6	IO4 (GBE0_LINK#)	GBE0_LINK_ACT#	O	OD	Link/Activity indication for Ethernet 0
7	IO5 (GBE1_LINK#)	GBE1_LINK_ACT#	O	OD	Link/Activity indication for Ethernet 1
8	IO6	Not used	—	—	Open
9	IO7	Not used	—	—	Open
10	IO8	Not used	—	—	Open
11	GND	—	GND	—	Connect to the ground.
12	IO9 (RZ_ET0_INT#)	RZ_IRQ2_ET0_INT#	O	PP	Interrupt output from Ethernet PHY 0 to the RZ/G2UL
13	IO10 (RZ_ET1_INT#)	RZ_IRQ7_ET1_INT#	O	PP	Interrupt output from Ethernet PHY 1 to the RZ/G2UL
14	VDD2	5.0 V	Power	—	Connect to 5.0 V.
15	IO12 (USB0_VBUSEN)	RZ_USB0_VBUSEN	I	w/ Schmit	VBUS input enable for channel 0 from the RZ/G2UL USB2.0
16	IO14 (USB0_EN_OC#)	USB0_EN_OC#	I/O	Input: w/ Schmitt Output: OD	Enable VBUS output of channel 0 of the USB port controller (IC9) on the RZ SMARC Carrier. Over-current input: This signal is driven low by channel 0 of the port controller.
17	IO15 (USB0_OVRCUR#)	RZ_USB0_OVRCUR#	O	PP	Output the over-current detection signal to channel 0 of the RZ/G2UL USB2.0.
18	IO16 (USB1_VBUSEN)	RZ_USB1_VBUSEN	I	Schmitt	VBUS input enable for channel 1 from the RZ/G2UL USB2.0
19	IO17 (USB1_EN_OC#)	USB1_EN_OC#	I/O	Input: w/ Schmitt Output: OD	Enable VBUS output of channel 0 of the USB port controller (IC9) on the RZ SMARC Carrier. Over-current input: This signal is driven low by channel 1 of the port controller.
20	IO18 (USB1_OVRCUR#)	RZ_USB1_OVRCUR#	O	PP	Output the over-current detection signal to channel 1 of the RZ/G2UL USB2.0.

Remarks: LV: Low voltage digital input
PP: Push pull output
w/ Schmitt: Digital in with Schmitt trigger
OD: Open drain output

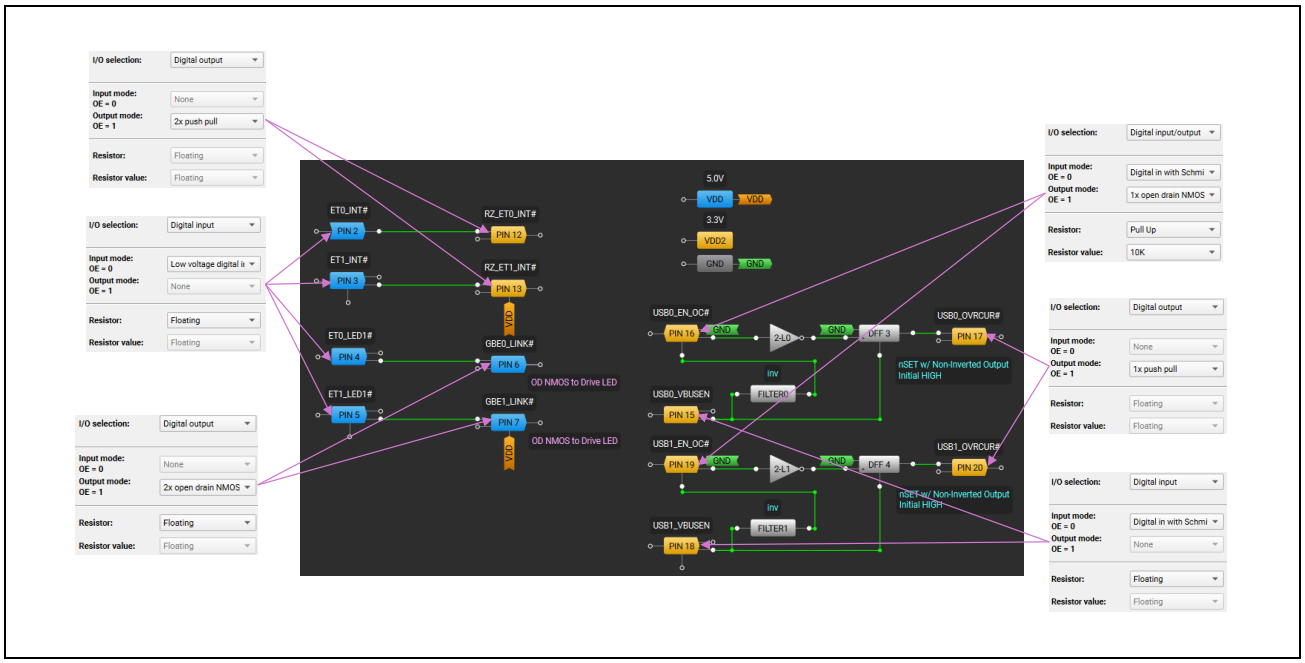


Figure 4.17 Circuit Diagram of the SLG7RN45315

Table 4.8 Signal Connections of the SLG7RN45356 (IC5)

Pin	Pin Name	Signal Name	I/O	Buffer	Pin Function
1	VDD	3.3 V	Power	—	Connect to 3.3 V.
2	IO0 (SW_ET0_EN#)	SW_ET0_EN#	I	w/ Schmitt	Connect to SW1-3. See **Table 4.12**.
3	IO1 (RESET_IN#)	WARM_RESET#	I	w/ Schmitt	Connect to RESET_BTN# and WDTOVF_PERROUT# from the RZ/G2UL.
4	IO2 (RESET_18#_IN)	PRESET#_18	I	w/o Schmitt	Reset input from an external debugger connected via the debug I/F (CN2)
5	IO3 (RESET_18#_OD)	PRESET#_18	O	OD	Reset output to Ethernet PHY 1
6	IO4 (PMIC_nRESET)	PMIC_NRESET	I	LV	Reset input generated form the PMIC
7	IO5 (RZ_PRST#)	RZ_PRST#	O	PP	Reset output to the RZ/G2UL
8	IO6 (PMIC_PGOOD)	PMIC_PGOOD	I	w/o Schmitt	PGOOD signal form the PMIC
9	IO7 (GBE0_LINK_1000#)	GBE0_LINK_LED	O	OD	Link speed indication of Ethernet PHY 0
10	IO8 (GBE1_LINK_100#)	GBE1_LINK_LED	O	OD	Link speed indication of Ethernet PHY 1
11	GND	—	GND	—	Connect to the ground.
12	IO9 (ET1_LED2)	ET1_LED2	I	LV	Link status indication of Ethernet PHY 1
13	IO10 (RZ_ET1_LINKSTA)	ET1_LNKSTA	O	PP	PHY Link status signal for channel 1 of the RZ/G2UL
14	VDD2	5.0 V	Power	—	Connect to 5.0 V.
15	IO12 (ET0_LED2)	ET0_LED2	I	LV	Link status indication of Ethernet PHY 0
16	IO14 (RZ_ET0_LINKSTA)	ET0_LNKSTA	O	PP	PHY Link status signal for channel 0 of the RZ/G2UL
17	IO15 (CARRIER_PWR_ON)	CARRIER_PWR_ON	O	PP	Enable regulators on the RZ SMARC Carrier. This signal is generated by the PMIC.
18	IO16	Not used	—	—	Open
19	IO17 (RESET_OUT#)	RESET_OUT#	O	PP	General purpose reset output to the RZ SMARC Carrier
20	IO18 (ET0_RESET#)	ET0_PRESET#_18	O	PP	Reset output to Ethernet PHY 0 when Ethernet PHY 0 is selected

Remarks: LV: Low voltage digital input
PP: Push pull output
w/ Schmitt: Digital in with Schmitt trigger
w/o Schmitt: Digital in without Schmitt trigger
OD: Open drain output

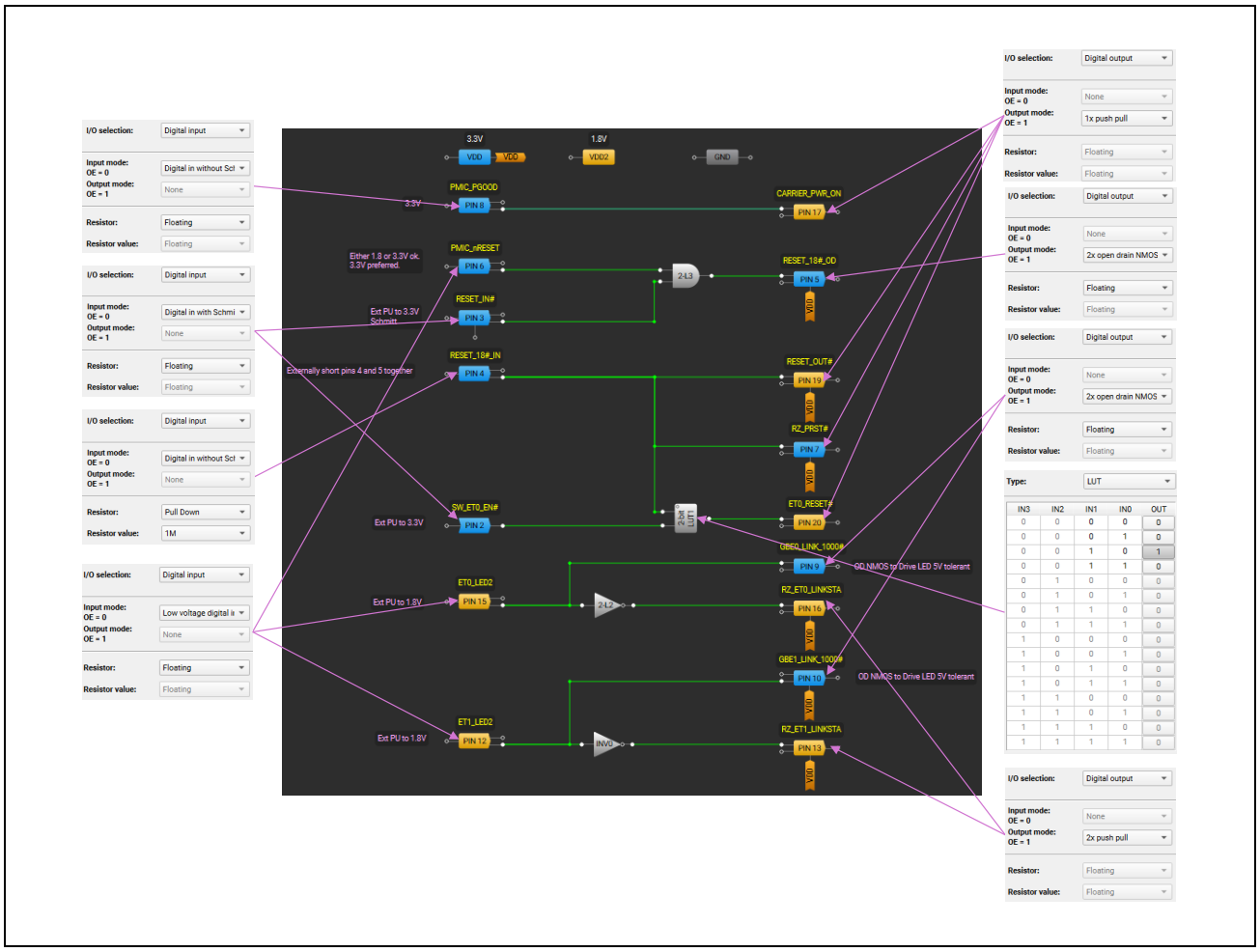


Figure 4.18 Circuit Diagram of the SLG7RN45356

Please refer to the following data sheet and configuration files included with the design data in detail (RZ/G2UL SMARC Module Board Design Data). If you want to see the configuration files, please download Go Configure Software Hub | Renesas.

- SLG7RN45314_DS_r014_12152021.pdf
- SLG7RN45314_GP_r003U_12132021.gp5
- SLG7RN45315_DS_r011_10292021.pdf
- SLG7RN45315_GP_r002U_10292021.gp5
- SLG7RN45356_DS_r010_11012021.pdf
- SLG7RN45356_GP_r001U_11012021.gp5

4.11 Parallel Output Interface

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board QSPI Version

RZ/A3UL SMARC Module Board Octal-SPI Version

Figure 4.19 shows a block diagram of the parallel output interface.

This interface is controlled by the LCD controller (LCDC) of the RZ/G2UL. It supports up to RGB888 as input format.

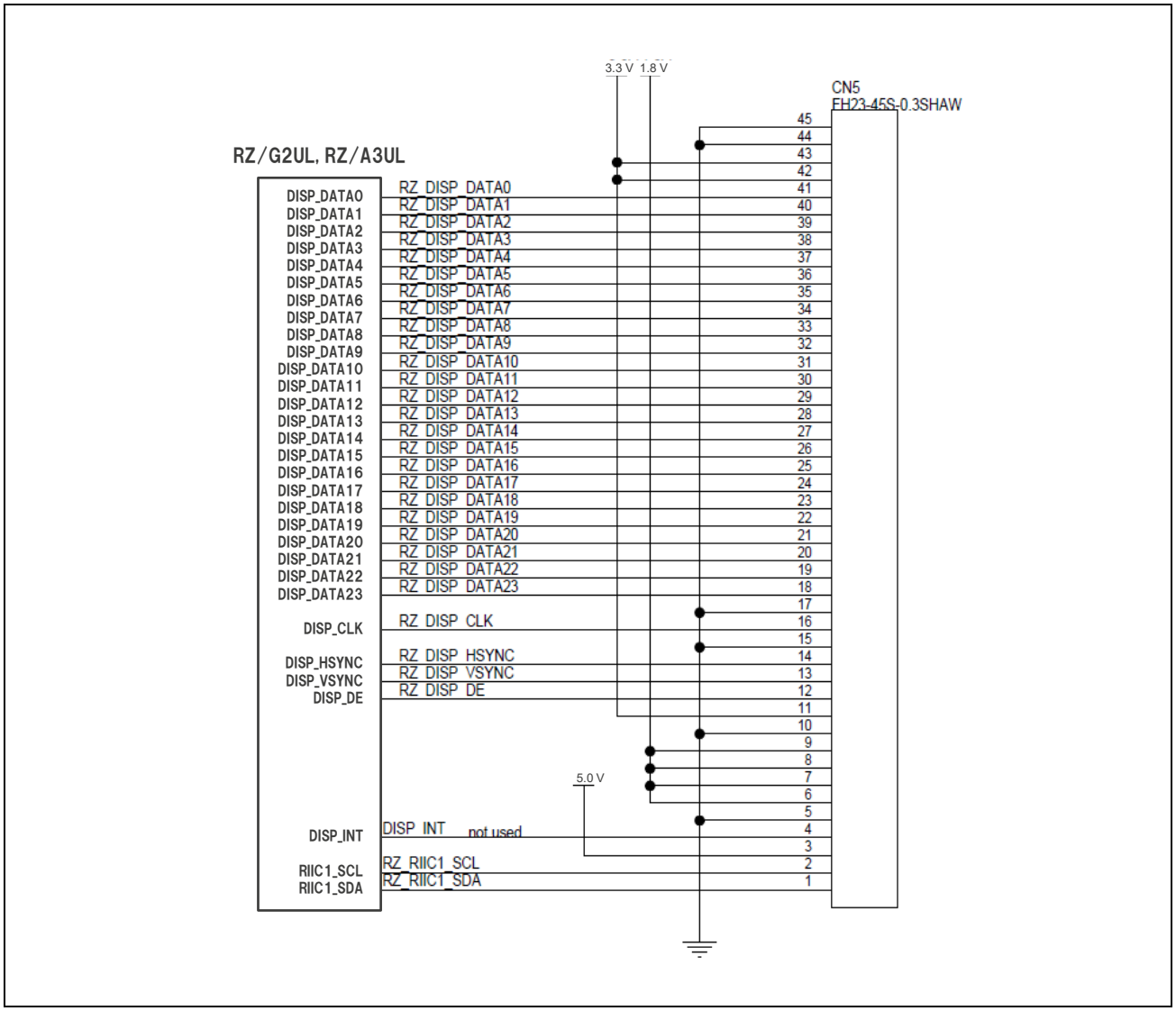


Figure 4.19 Block Diagram of Parallel Output I/F

Table 4.9 Signal Connections of FFC/FPC Connector (CN5)

Pin	Signal Name	MPU	Pin	Signal Name	MPU
1	RZ_RIIC1_SDA	RIIC1_SDA	24	DISP_DATA17	P17_0
2	RZ_RIIC1_SCL	RIIC1_SCL	25	DISP_DATA16	P15_2
3	5.0 V	—	26	DISP_DATA15	P18_0
4	DISP_INT	—	27	DISP_DATA14	P15_3
5	VSS	—	28	DISP_DATA13	P15_1
6	1.8 V	—	29	DISP_DATA12	P16_1
7	1.8 V	—	30	DISP_DATA11	P15_0
8	1.8 V	—	31	DISP_DATA10	P16_0
9	1.8 V	—	32	DISP_DATA9	P14_1
10	VSS	—	33	DISP_DATA8	P14_2
11	3.3 V	—	34	DISP_DATA7	P14_0
12	DISP_DE	P11_1	35	DISP_DATA6	P13_2
13	RZ_DISP_VSYNC	P12_0	36	DISP_DATA5	P12_1
14	RZ_DISP_HSYNC	P11_0	37	DISP_DATA4	P13_3
15	VSS	—	38	DISP_DATA3	P13_4
16	RZ_DISP_CLK	P11_3	39	DISP_DATA2	P13_0
17	VSS	—	40	DISP_DATA1	P13_1
18	DISP_DATA23	P18_3	41	DISP_DATA0	P11_2
19	DISP_DATA22	P17_3	42	3.3 V	—
20	DISP_DATA21	P18_2	43	3.3 V	—
21	DISP_DATA20	P18_1	44	VSS	—
22	DISP_DATA19	P17_1	45	VSS	—
23	DISP_DATA18	P17_2			

4.12 SMARC Edge Finger

Figure 4.20 illustrates the layout of the edge finger for mating with the SMARC edge connector on the RZ SMARC Carrier.

The SMARC edge connector is a 314-pin, 0.5 mm-pitch, right angle part designed for use with 1.2-mm thick mating PCBs with the edge finger pattern. The SMARC edge connector has a Primary side (Pxx) and a Secondary side (Sxx). The SMARC signal names and edge connector pin numbers are listed in **section 4.1.4, List of Pin Functions** along with the RZ/G2UL port pins (if applicable) and signal names.

For the pin assignment of the SMARC edge connector, please refer to “4 MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification”.

Figure 4.20 Layout of Carrier Board Connecting Pins

4.13 Operation Components

4.13.1 Configuration at Shipment

Figure 4.21 illustrates the switch settings at the time of shipment.

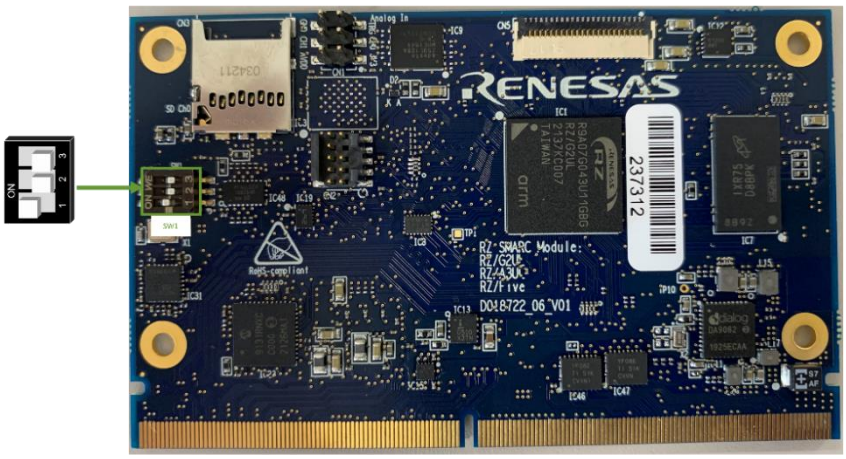


Figure 4.21 Switch Settings at Shipment

4.13.2 Configuration by Switches and Mode Terminals

This board is equipped with DIP switches SW1 for selecting the functions. The functions set by the switches are explained below.

Figure 4.22 shows a block diagram of the system setting interface.

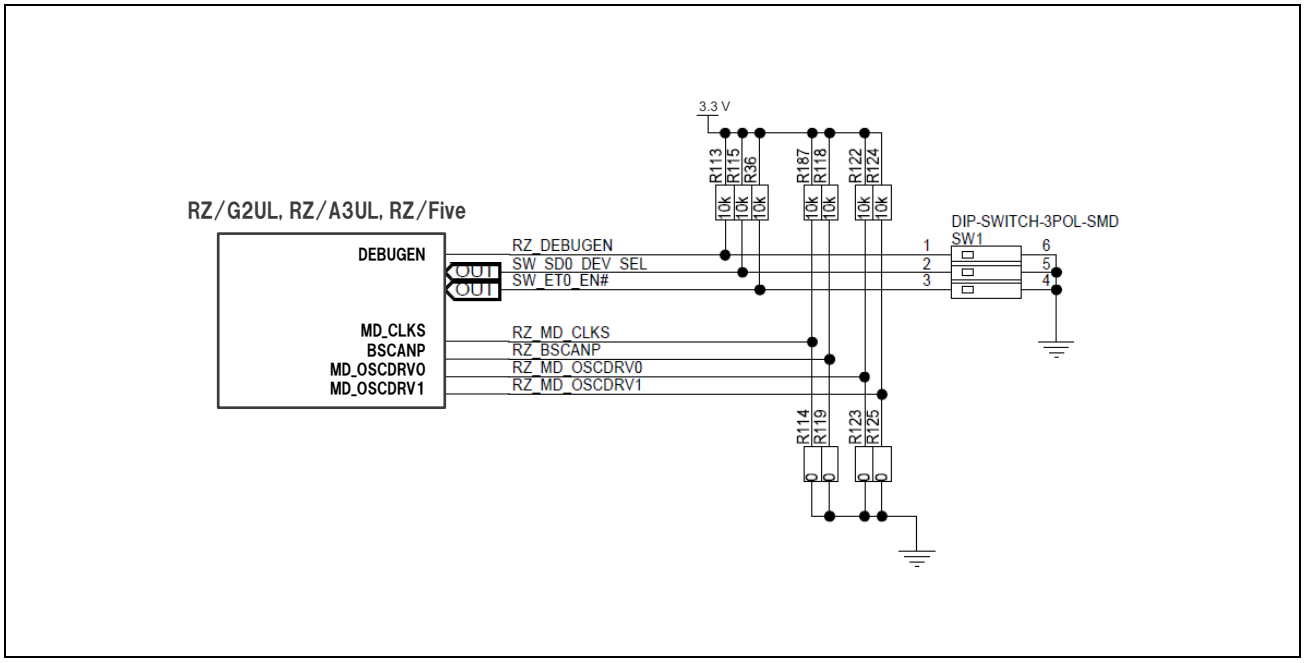


Figure 4.22 Block Diagram of System Setting I/F

Table 4.10 and **Table 4.11** list the functions of SW1 and the mode terminals, respectively. The default settings are highlighted.

Table 4.10 Functions of System Setting Switches (SW1)

No.	Setting		Function
SW1-1 DEBUGEN	OFF	DEBUGEN = “H”	Debugging with ARM debuggers
	ON	DEBUGEN = “L”	Normal operation
SW1-2 Selection of SD or MMC	OFF	Selection = “H”	Select eMMC memory
	ON	Selection = “L”	Select microSD card
SW1-3 Selection Ethernet0/Peripherals	OFF	Selection = “H”	Select CAN0*1, CAN1*1, RSPI1, and SSI1 signals
	ON	Selection = “L”	Select Ethernet 0 signals

Note 1. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

Table 4.11 Functions of System Settings (Mode Terminals)

No.	Setting		Function
MD_CLKS	1	MD_CLKS = “H”	SSCG ON
	0	MD_CLKS = “L”	SSCG OFF
BSCANP	1	BSCANP = “H”	Connection test between the LSIs on the customer’s board
	0	BSCANP = “L”	Normal operation
MD_OSCDRV0	1	MD_OSCDRV0 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)
	0	MD_OSCDRV0 = “L”	Adjust the drive capacity of the OSC buffer
MD_OSCDRV1	1	MD_OSCDRV1 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)
	0	MD_OSCDRV1 = “L”	Adjust the drive capacity of the OSC buffer

By setting SW1-3 to the following settings, the RZ/G2UL SMARC Module can be used with various interfaces. **Table 4.12** lists the functions set by SW1-3.

Table 4.12 GPIO Signals Set by SW1-3

		Setting	
		SW1-3 = “L”	SW1-3 = “H”
Signal Name	P1_2	ET0_TXD0	CAN0_RX*1
	P1_3	ET0_TXD1	GPIO6
	P1_4	ET0_TXD2	GPIO7
	P2_0	ET0_TXD3	CAN1_TX*1
	P3_2	ET0_RXD0	SSI1_TXD
	P3_3	ET0_RXD1	SSI1_RXD
	P4_0	ET0_RXD2	RSPI1_CK
	P4_1	ET0_RXD3	RSPI1_MOSI
	P1_0	ET0_TXC	GPIO5
	P1_1	ET0_TX_CTL	CAN0_TX*1
	P3_0	ET0_RXC	SSI1_BCK
	P3_1	ET0_RX_CTL	SSI1_RCK
	P4_3	ET0_MDC	RSPI1_SSL
	P4_4	ET0_MDIO	GPIO1
	P4_5	ET0_LINKSTA	GPIO11
	P5_1	ET0_INT#	GPIO10
Application		Ethernet 0	CAN0/1*1 Audio PMOD0 (Type-2A) PMOD1 (Type-6)

Note 1. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

5. Parallel to HDMI Conversion Board

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board QSPI Version

RZ/A3UL SMARC Module Board Octal-SPI Version

5.1 Configuration

The parallel to HDMI conversion board is connected to the FFC/FPC connector (CN5) described in **section 5.2** to realize parallel output via the 50-mm FPC cable.

Figure 5.1 shows an example of system configuration using the parallel to HDMI conversion board.

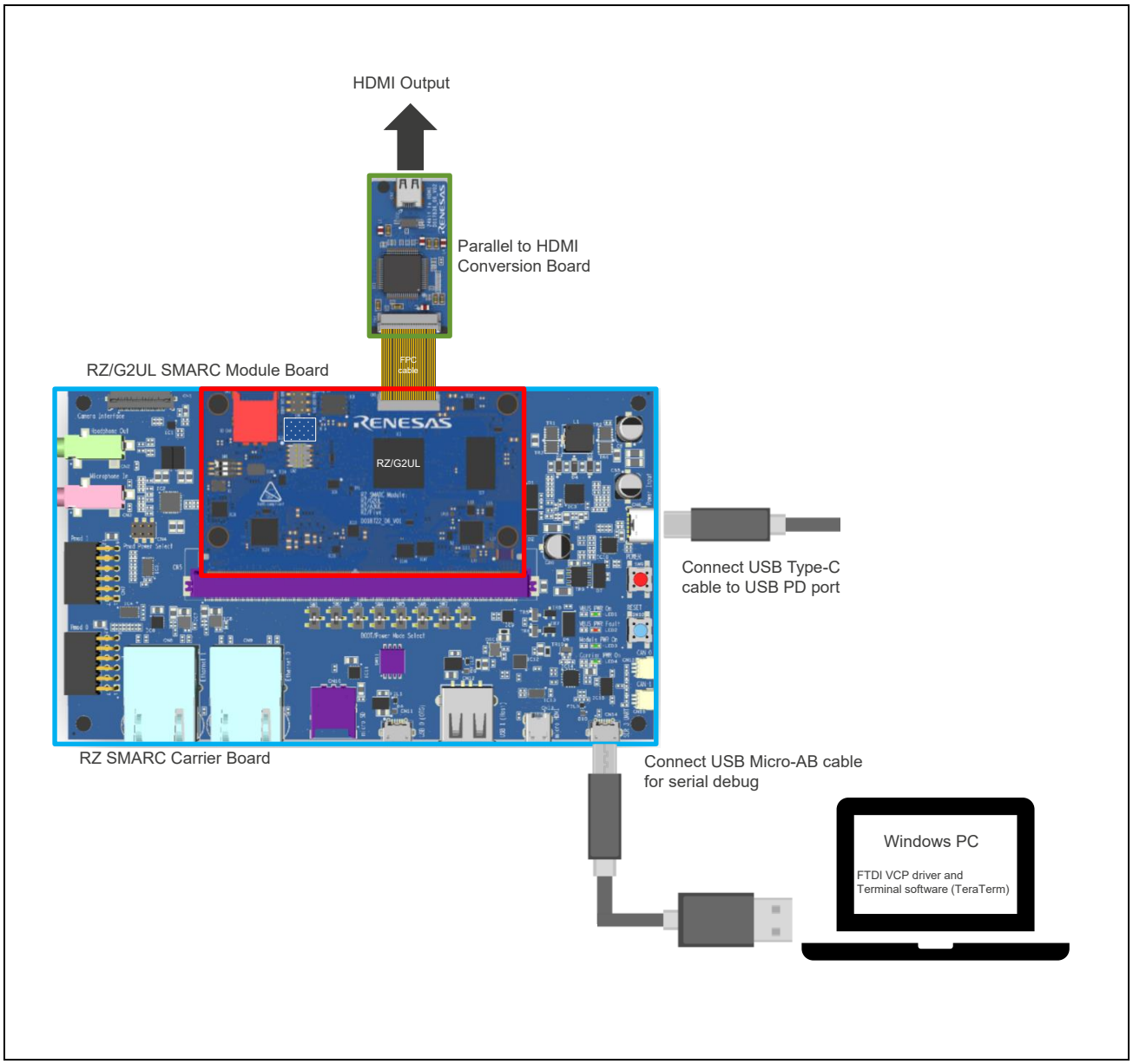
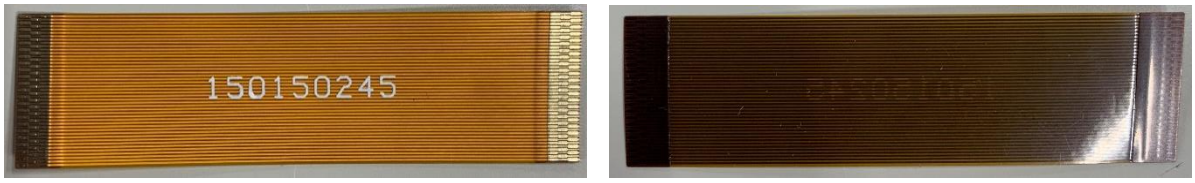


Figure 5.1 Example of System Configuration Using the Parallel to HDMI Conversion Board

The connection procedure of the 50-mm FPC cable is follows.

The top and bottom surfaces of the FPC cable are shown below.



Top surface Bottom surface

Figure 5.2 Top and Bottom Views of the 50-mm FPC Cable

1. Lift up the actuator. Use thumb or index finger.

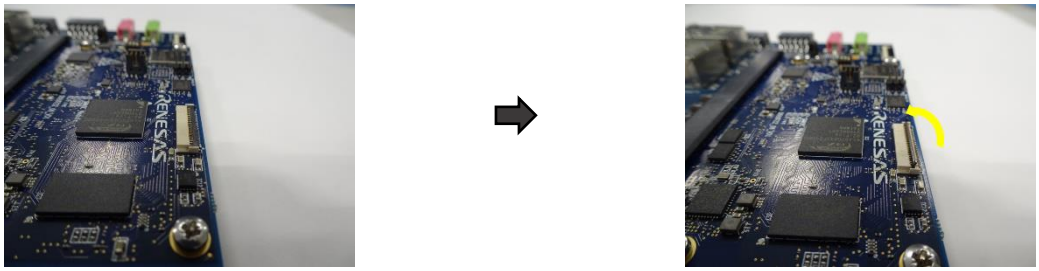


Figure 5.3 How to Install the 50-mm FPC Cable (1)

2. Fully insert the FPC cable in the connector parallel to the mounting surface, with the exposed conductive traces facing down.

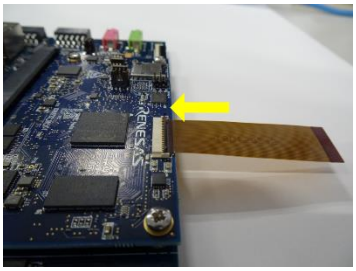


Figure 5.4 How to Install the 50-mm FPC Cable (2)

3. Rotate down the actuator until firmly closed.

NOTE

The FPC cable must be fully inserted in the connector. If not fully inserted, the actuator will not close properly.

If this is the case, lift up the actuator and repeat the process (starting with step 1 above)

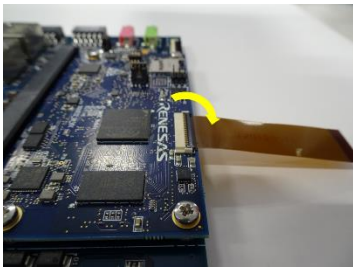


Figure 5.5 How to Install the 50-mm FPC Cable (3)

4. FPC Cable Removal
   1) Lift up the actuator.
   2) Carefully remove the FPC cable.

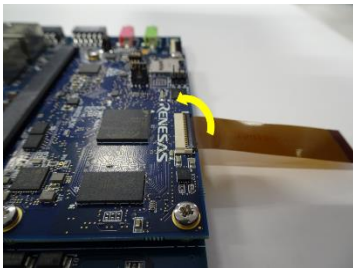


Figure 5.6 How to Remove the 50-mm FPC Cable

5.2 Features

Table 5.1 shows the features of the parallel to HDMI conversion board.

Table 5.1 Features of the Parallel to HDMI Conversion Board

Item	Details
Video IC	Parallel to HDMI transmitter: ADV7513BSWZ
Connector	45-pin FFC/FPC connector Micro HDMI connector
Circuit board specifications	Dimensions: 40 mm (W) × 20 mm (L) × 1.6 mm (H) Mount: Single-sided mounting (6 layers)

5.3 Component Layout

Figure 5.7 shows the component layouts on the top and bottom sides of the parallel to HDMI conversion board.

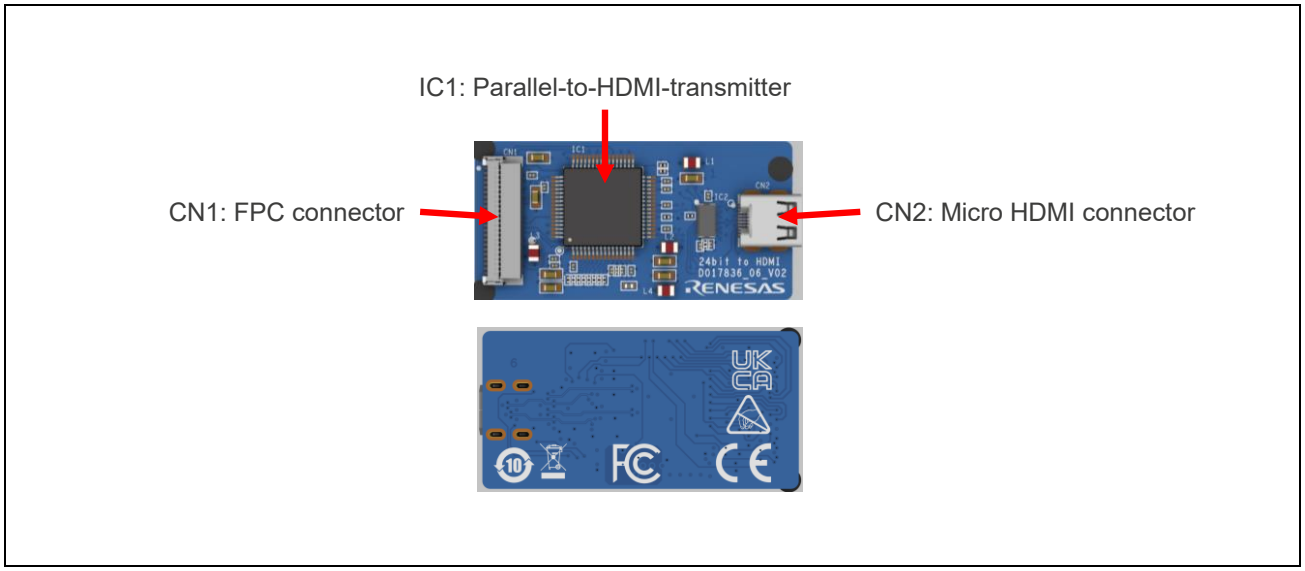


Figure 5.7 Component Layouts of the Parallel to HDMI Conversion Board (Top and Bottom Views)

6. Appendix

6.1 Part Number and Features of Each Board

This section describes the part number and features of each board.

Figure 6.1 shows a picture of the SMARC Module Board.

Figure 6.1 Top View of the SMARC Module Board

The SMARC Module Boards with RZ/G2UL, RZ/A3UL, and RZ/Five use a common PCB and are designed to be pin-compatible.

Please refer to **section 1.3, Features** onwards for the actual functions of the board.

Board Name	Part Number	MPU	Security	Memory Configuration	Parallel to HDMI Conversion Board	On-chip Debugging Emulator
RZ/G2UL SMARC Module Board	RTK9743U11C01000BE	R9A07G043U11GBG	No	QSPI flash memory DDR4 SDRAM	Included	Not Included
	RTK9743U15C01000BE	R9A07G043U15GBG	Yes			
RZ/Five SMARC Module Board	RTK9743F01C01000BE	R9A07G043F01GBG	No	QSPI flash memory DDR4 SDRAM	Not Included	Not Included
	RTK9743F05C01000BE	R9A07G043F05GBG	Yes			
RZ/A3UL SMARC Module Board QSPI Version	RTK9763U02C01002BE	R9A07G063U02GBG	No	QSPI flash memory DDR4 SDRAM	Included	Included
RZ/A3UL SMARC Module Board Octal-SPI Version	RTK9763U02C01003BE	R9A07G063U02GBG	No	OctaRAM OctaFlash DDR4 SDRAM	Included	Included

Figure 6.2 shows a picture of the RZ SMARC Series Carrier Board.

Figure 6.2 Top View of the RZ SMARC Series Carrier Board

Board Name	Part Number
RZ SMARC Series Carrier Board	RTK97X4XXXB00000BE

Figure 6.3 shows the EVKIT. This board consists of the SMARC Module Board and the RZ SMARC Series Carrier Board via a 314-pin, 0.5-mm pitch connector. This picture is of the RZ/G2UL EVKIT.

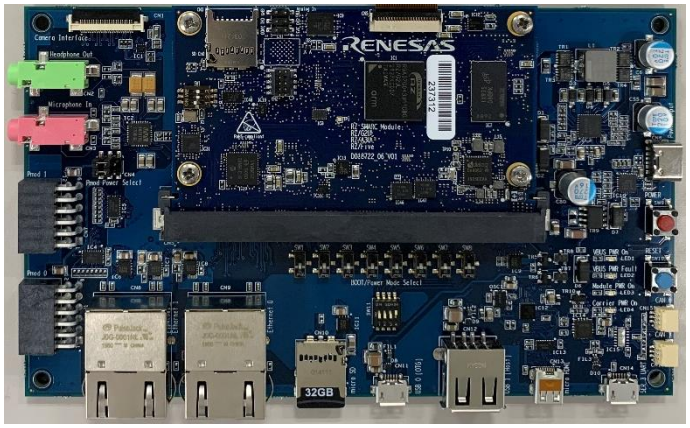


Figure 6.3 Top View of the EVKIT

6.2 How to Identify Each SMARC Module Board

Table 6.1, **Table 6.2**, and **Table 6.3** list the differences among the SMARC Module Boards. **Figure 6.4** shows pictures of the RZ/G2UL SMARC Module.

Table 6.1 Comparison of the RZ/G2UL and RZ/Five SMARC Module Boards

Type Name	RZ/G2UL SMARC Module Board	RZ/Five SMARC Module Board
IC1	RZ/G2UL (R9A07G043U11GBG or R9A07G043U15GBG)	RZ/Five (R9A07G043F01GBG or R9A07G043F05GBG)

Table 6.2 Comparison of the RZ/G2UL and RZ/A3UL SMARC Module Boards

Type Name	RZ/G2UL SMARC Module Board	RZ/A3UL SMARC Module Board
IC1	RZ/G2UL (R9A07G043U11GBG or R9A07G043U15GBG)	RZ/A3UL (R9A07G063U02GBG)

Table 6.3 Comparison of the QSPI and Octal-SPI Versions of the RZ/A3UL SMARC Module Board

Type Name	QSPI Version	Octal-SPI Version
IC2	Not mounted	OctaFlash
IC3	Not mounted	OctaRAM
IC9	QSPI flash memory	Not mounted

Figure 6.4 Top and Bottom Views of the SMARC Module Board

6.3 How to Replace the SMARC Module Board

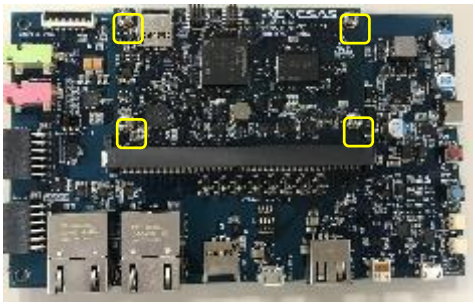
Take care with the following when replacing the board.

1. Remove the four screws.

NOTE

The screw head has a special shape, so be careful not to crush the screw head.

We recommend preparing a torx screwdriver with “T6” head size.



Specially shaped screw head

Figure 6.5 How to Remove the Screws

2. After removing the screws, the SMARC Module Board will stand up at an angle. Slide it out.

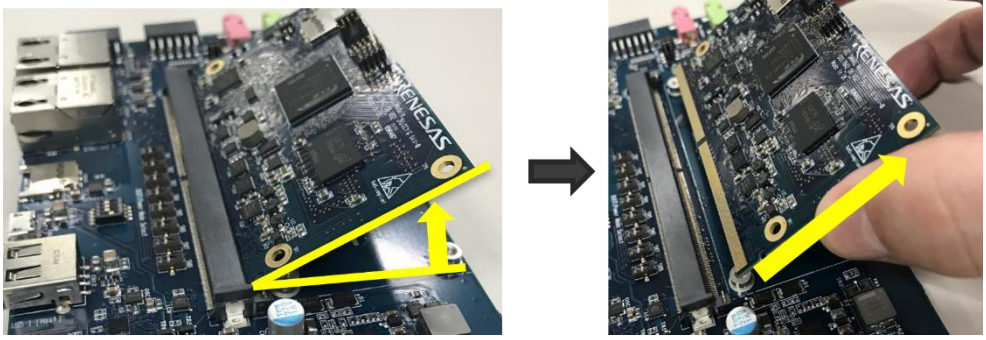


Figure 6.6 How to Remove the SMARC Module Board

3. Insert the replacement SMARC Module Board diagonally, then roll the board until it is parallel to the RZ SMARC Carrier and fix it in place with screws.

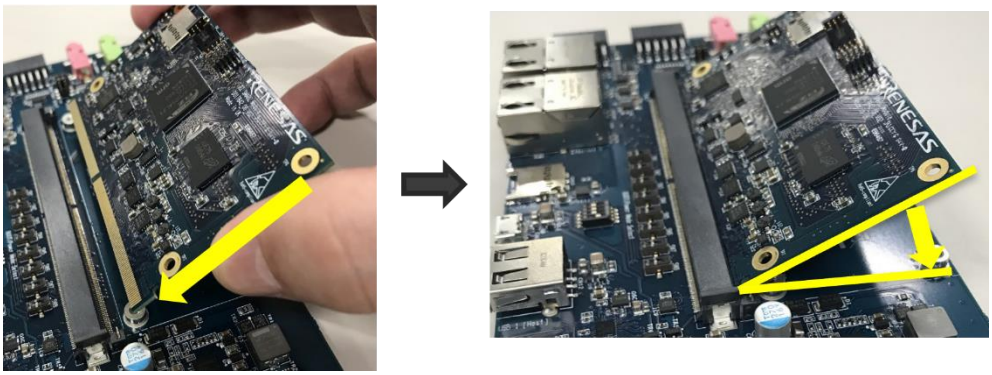


Figure 6.7 How to Install the SMARC Module Board

7. Certifications

The RZ/G2UL, RZ/A3UL, and RZ/Five SMARC Module Boards comprising the RZ/G2UL, RZ/A3UL, and RZ/Five EVKITs meet the following certification/standards. For important disclaimers and safety precautions, please refer to the page following the cover page of this user's manual.

7.1 EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  [NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
  CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)

  This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

7.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013

For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at:
https://www.renesas.com/en/support/regional-customer-support/weee

7.3 Safety Standards

- UL 94V-0

REVISION HISTORY	RZ/G2UL, RZ/A3UL, RZ/Five SMARC Module Board User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	June 27, 2022	—	First edition issued
1.01	July 28, 2022	9, 15	The section title is changed from "RT9743U11C01000BE" to "RTK9743U11C01000BE"
		10, 16	The section title is changed from "RT9763U02C01000BE" to "RTK9763U02C01000BE"
		11, 17	The section title is changed from "RT9763U02C01001BE" to "RTK9763U02C01001BE"
		12, 18	The section title is changed from "RT9743F01C01000BE" to "RTK9743F01C01000BE"
1.10	Dec. 13, 2022	34, 35, 42, 68, 69	Restrictions on use are added. When used in combination with the RZ SMARC Series Carrier Board (P/N: RTR97X4XXXB00000BE), CAN0 and CAN1 interface cannot be used because a CAN transceiver is not fitted on the RTK97X4XXXB00000BE.
		57, 58	For section "GreenPAK", the link of GreenPAK is added.
1.20	Nov. 28, 2025	82, 83	Section 6 Certifications, added
1.30	Jan. 28, 2026	1	For section 1.1 "Overview", the description was updated.
		9 to 12	For section 1.3 "Features", the tables for the respective boards were updated.
		24	For section 2.2 "MPU", the descriptions of the respective products were updated. Added a note for the specific RZ/A3UL EVKIT where TSU correction code is 0.
2.00	May 28, 2026	All	Restructured the sections of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.
		9 to 11	For section 1.3 "Features", added supported boot modes to the tables for the respective boards.
		17, 18	Section 2 "Box Contents", added
		19	Section 3 "Ordering Information", added
		20	For section 4.1.2 "RZ/A3UL", added the restriction and countermeasure on TSU correction code for some boards.
		53	For section 4.9.2 "microSD Card", added the specification restriction and countermeasure for software reset.
		54 to 60	For section "4.10 GreenPAK", added the pin configurations and circuit diagrams.
		66	For section 4.13.2 "Configuration by Switches and Mode Terminals", modified the table for system settings (mode terminals).

RZ/G2UL, RZ/A3UL, RZ/Five SMARC Module Board
User's Manual: Hardware

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