User's Manual

RZ/G3E SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

Renesas Electronics
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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Introduction

The RZ/G3E SMARC Module board (hereinafter referred to as "G3E SMARC Module") is a platform designed according to the SMARC 2.1.1 Specification providing evaluation of the Renesas RZ/G3E microcontroller R9A09G047E57GBG.

Basically, the G3E SMARC Module is connected to the Renesas RZ SMARC Series Carrier Board II (hereinafter referred to as "RZ SMARC Carrier II") and used as the RZ/G3E SMARC Evaluation Board (hereinafter referred to as "G3E SMARC EVK").

This guide includes system setup and configuration. This guide also provides detailed information on the overall design and use of the G3E SMARC Module from a hardware system perspective.

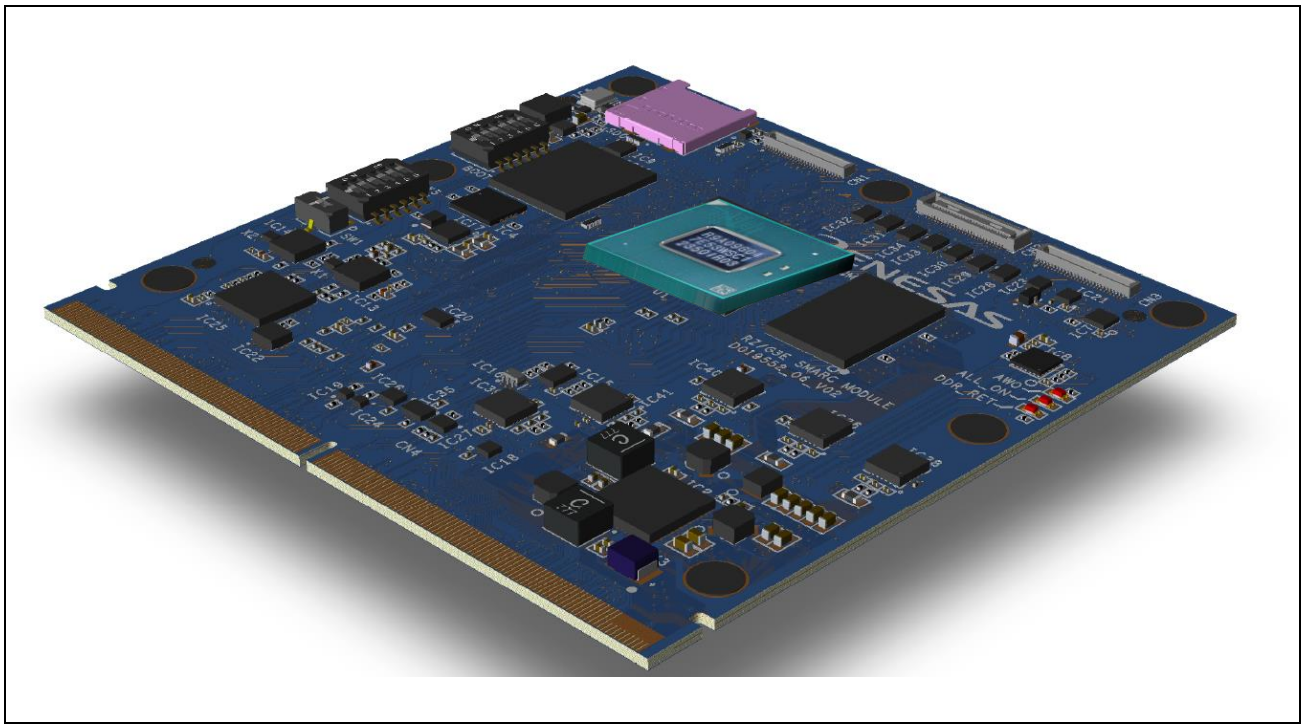


Figure 1.1 RZ/G3E SMARC Module Board

The key features of the G3E SMARC Module are as follows.

Board Features	Details
Processor	RZ/G3E (P/N: R9A09G047E57GBG), 15 mm × 15 mm, 0.5-mm pitch, 529-pin FCBGA
Memory	4 GB of 1Gx16 LPDDR4X SDRAM supporting data rate up to 3200 MT/s
	Micro SD card slot with default, high-speed, UHS-I/SDRR50, SDR104 transfer modes support x2
	64-GB eMMC flash with HS200 transfer mode support
	128-Mbit Quad SPI flash memory
Supported interface and peripherals	Supports JTAG connection from a debugger
	Supports ADC connection for 8 channels
	I3C interface
	5x ISL28025FRZ for current monitoring
	2x Gigabit Ethernet Transceiver
	Parallel Output interface
	MIPI DSI interface
	MEMS microphone for PDM interface
	9-channel PMIC (P/N: RAA215300A2GNP#HA8)
	6-channel clock generator (P/N: 5L35023B-617NLGI) 6-channel clock generator (P/N: 5P35023B-789NLGI)
Board dimensions	82 mm (W) * 80 mm (L), 10-layer

The G3E SMARC Module may be used in any carrier board which follows the SMARC 2.1.1 Specification; however, Renesas recommends using the Renesas RZ SMARC Carrier II board.

The details of the RZ SMARC Carrier II board are to be found in the ***RZ SMARC Carrier II User Manual***.

1.1 Kit Contents

The following components are included in the RZ/G3E SMARC Module Board Kit.

- RZ/G3E SMARC Module Board
- RZ SMARC Series Breakout Adaptor Board
  (hereinafter referred to as “SMARC Breakout Adaptor”)
- RZ SMARC Series Parallel to HDMI Conversion Adaptor Board
  (hereinafter referred to as “SMARC RGB-HDMI Adaptor”)
- Heat spreader*[1]

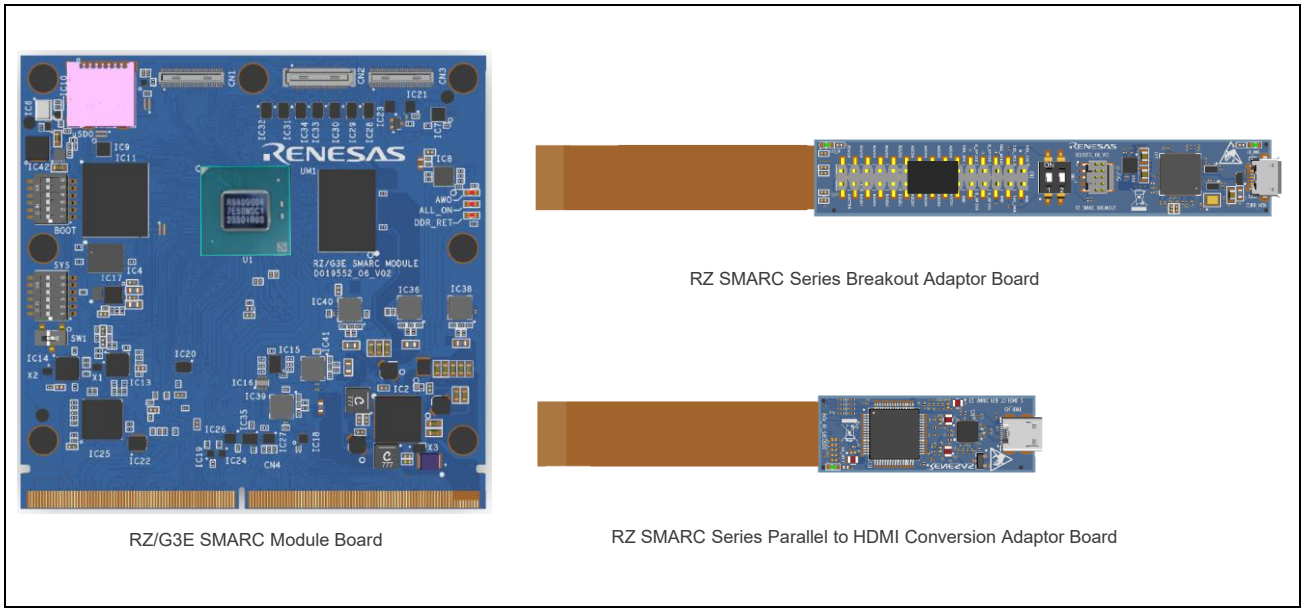


Figure 1.2 RZ/G3E SMARC Module Board Kit Contents

If you have purchased the RZ/G3E SMARC Evaluation Board Kit (P/N: RTK9947E57S01000BE), your contents will include:

- RZ/G3E SMARC Module Board Kit
  - RZ/G3E SMARC Module Board
  - RZ SMARC Series Breakout Adaptor Board
  - RZ SMARC Series Parallel to HDMI Adaptor Board
  - Heat spreader*[1]
- RZ/G3E SMARC Carrier Board II Kit
  - RZ SMARC Series Carrier Board II
  - Fitted with the RZ SMARC Series Dual LVDS to HDMI Adaptor Board to DISP0 and DISP1 (hereinafter referred to as “SMARC Dual LVDS-HDMI Adaptor”)
  - RZ SMARC Series Pi Camera Adaptor Board (hereinafter referred to as “SMARC Pi Camera Adaptor”)
  - USB Type-A to USB Micro B cable for serial debug
  - Accessories bag:
    - 2off M2.5 × 6 mm pan-head machine screws (for securing M.2 cards)

- 1off 2.5 mm spacer (for securing M.2 key B cards)

NOTE

The Module will have been fitted to the Carrier using 7off M2.5 × 4 mm pan-head machine screws.
The heat spreader will have been fitted to the Module and Carrier Board using 6off pozi countersunk head machine screws.

*1. For installation of the heat spreader, refer to the material included with this board.

1.2 Module Assembly

The G3E SMARC Module can only be used when fitted to a SMARC compliant Carrier board.

Secure the Module using 7off M2.5 × 4 mm pan-head machine screws (these are provided with the RZ SMARC Carrier II). If you want to use the heat spreader, use 6off pozi countersunk head machine screws bundled in the box.

If connections to the JTAG, ADC and I3C interfaces and current monitor functionality are required, it may be necessary to connect the SMARC Breakout Adaptor. Refer to **sections 3.12, ADC**, **3.13, I3C**, **3.14, JTAG**, and **3.15, Current Monitor**.

If connection to the Parallel Output interface is required, it may be necessary to connect the SMARC RGB-HDMI Adaptor. Refer to **section 3.16, Parallel Output**.

2. System Description

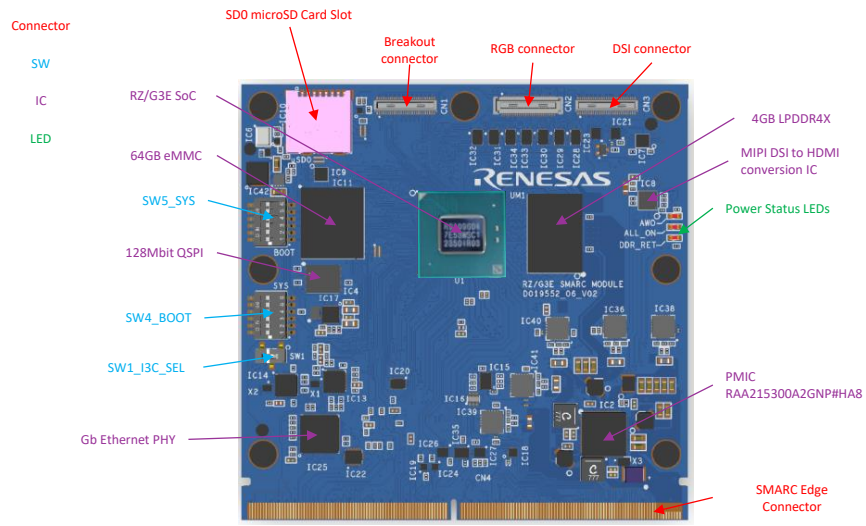


Figure 2.1 RZ/G3E SMARC Module Board Top View

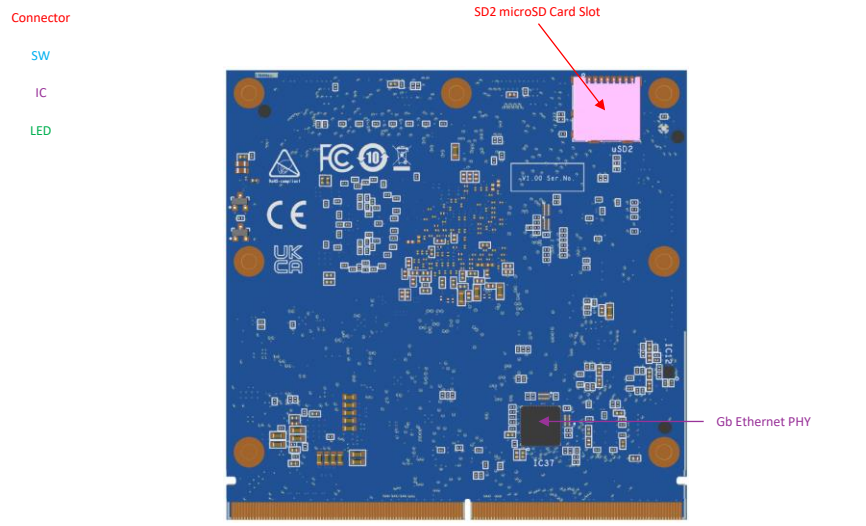


Figure 2.2 RZ/G3E SMARC Module Board Bottom View

The G3E SMARC Module has several switched configuration options and on-board interfaces. These are detailed in the following sections.

The default settings are highlighted.

2.1 G3E SMARC EVK Functional Block

Figure 2.3 shows the functional block diagram of the G3E SMARC EVK. ICs, connectors and switches surrounded by red frame indicate functions used on the G3E SMARC Module.

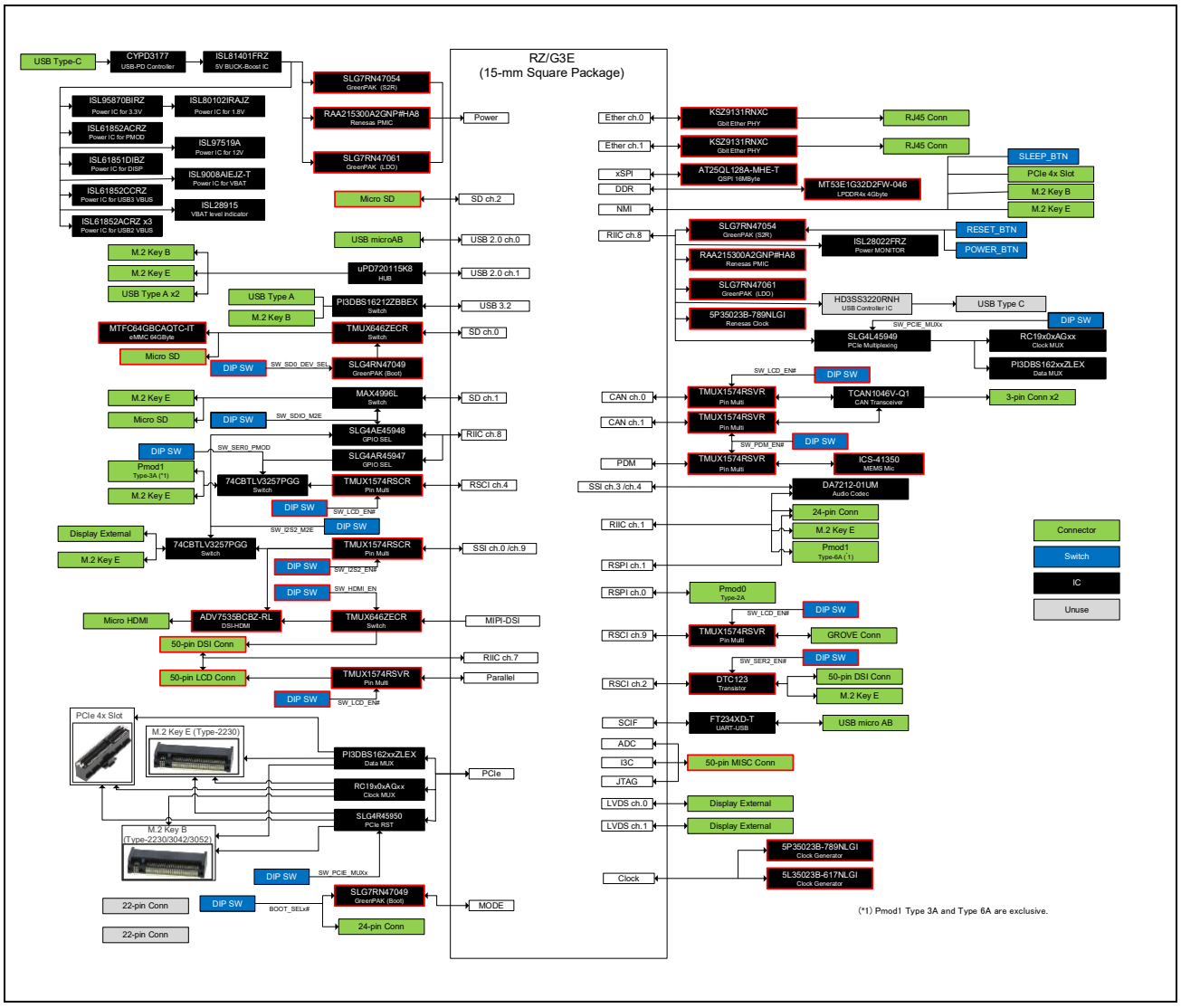


Figure 2.3 G3E SMARC EVK Block Diagram

2.2 G3E SMARC EVK Interface Mapping

Renesas parts are highlighted.

Table 2.1 Interface Mapping (1/2)

SMARC Interface Name	RZ/G3E I/F	Device Part Number	Description
USB0	USB2.0 ch0	629105150921	USB2.0 Type-microAB receptacle
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB2.0 Hub IC
		72309-8014BLF	USB2.0 Type-A receptacle
USB2	USB3.2 Gen2	692122030100	USB3.0 Type-A receptacle
USB3	—	1054500101	USB Type-C receptacle
USB4	—	72309-8014BLF	USB2.0 Type-A receptacle
USB5	—	72309-8014BLF	USB2.0 Type-A receptacle
CAN0	CAN ch0	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
CAN1	CAN ch1	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
I2S0	SSI ch3	DA7212-01UM	Audio Codec
		STX-4335-5BGP-S1	Stereo Headphone, Stereo Mic, Aux for connector
		M20-9990246	Pin header for speaker
I2S2	SSI ch0	MDT420B01001	M.2 Key E for I2S interface
SPI0	—	GRPB122VWQS-RC	24-pin header
SPI1	RSPI ch0	SSW-106-02-T-D-RA	PMOD Type-2A connector
SER0	SCIF ch4	SSW-106-02-T-D-RA	PMOD Type-3A connector
SER1	SCIF ch9	110990037	Grove connector
SER2	SCIF ch2	MDT420E01001	M.2 Key E
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC
		629105150921	UART Debug for USB Type-microB receptacle
PCIE_A	PCIe Gen3	10061913-111PLF	PCIe 4x Slot
PCIE_B		MDT420B01001	M.2 Key B
		MDT420E01001	M.2 Key E
		78646-3001	SIM card for M.2 Key B
—	Parallel	DF40C-50DS-0.4V	LCD connector
		ADV7513BSWZ	Parallel to HDMI conversion IC(*1)
		46765-1301	Micro HDMI connector(*1)
HDMI	MIPI DSI	ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC
		46765-1301	Micro HDMI connector
—	MIPI-DSI	DF40C-50DP-0.4V	DSI connector
LVDS0	LVDS ch0	2041262-1	Mini PCI Express & mSATA connector
		IT2623	Dual LVDS to HDMI conversion IC(*2)
		46765-1301	Micro HDMI connector(*2)
LVDS1	LVDS ch1	2041262-1	Mini PCI Express & mSATA connector
CSI0	—	2-1734592-2	22-pin FPC connector
CSI1	MIPI CSI-2	2-1734592-2	22-pin FPC connector
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector

Table 2.1 Interface Mapping (2/2)

SMARC Interface Name	RZ/G3E I/F	Device Part Number	Description
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector
I2C_GP	RIIC ch1	GRPB122VWQS-RC	GPIO pin header
		MDT420E01001	M.2 Key E for I2C interface
		DA7212-01UM	Audio Codec for I2C interface
		SSW-106-02-T-D-RA	PMOD Type-6A connector
I2C_PM	RIIC ch8	ISL28022FRZ	Current monitor for measuring SMARC module
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)
		SLG4R45950	GreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)
		SLG4AE45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)
		RAA215300A2GNP#HA8	PMIC
		SLG7RN47061	GreenPAK (Power Regulator)
		SLG7RN47054	GreenPAK (Power/Reset control)
		5P35023B-789NLGI	Clock generator
I2C_LCD	RIIC ch7	2041262-1	Mini PCI Express & mSATA connector
		ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC
		DF40C-50DP-0.4V	DSI connector
		DF40C-50DS-0.4V	LCD connector
I2C_CAM0	—	2-1734592-2	22-pin FPC connector
I2C_CAM1	RIIC ch0	2-1734592-2	22-pin FPC connector
—	SD/MMC ch0	1040310811	USB Type-microB receptacle
		MTFC64GBCAQTC-IT	64-GB eMMC memory
SDIO	SD/MMC ch1	1040310811	microSD card connector
—	SD/MMC ch2	1040310811	microSD card connector
—	DDR	MT53E1G32D2FW-046 WT:C	4-GB LPDDR4X SDRAM
—	xSPI	AT25QL128A-MHE	128-Mbit Quad SPI Flash memory
—	ADC	DF40C-50DP-0.4V	MISC connector
		TSM-115-01-L-DV-P-TR	30-pin connector(*3)
—	I3C	DF40C-50DP-0.4V	MISC connector
		TSM-115-01-L-DV-P-TR	30-pin connector(*3)
—	JTAG	DF40C-50DP-0.4V	MISC connector
		10051922-1010EHLF	10-pin connector(*3)
—	CPG	5L35023B-617NLGI	Clock generator
		5P35023B-789NLGI	Clock generator
—	Power	ISL28025FRZ	Current monitor for measuring five power rails on SMARC module
		DF40C-50DP-0.4V	MISC connector
		FT232HQ-REEL	USB to I2C conversion IC(*3)
		629105150921	USB2.0 Type-microAB receptacle(*3)

Note 1. The SMARC RGB to HDMI Adaptor is required. It is bundled with the G3E SMARC EVK.

Note 2. The SMARC Dual LVDS to HDMI Adaptor is required. However, it is not bundled with the G3E SMARC EVK for mass production.

Note 3. The SMARC Breakout Adaptor is required. It is bundled with the G3E SMARC EVK.

2.3 Board Configuration and Status

This section provides details of the G3E SMARC Module switch settings.

2.3.1 BOOT

A bank of 6-switches is used to configure operating modes of the Module. The default settings are highlighted.

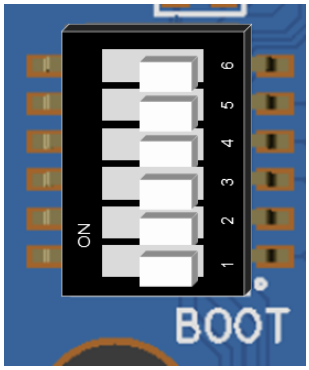


Figure 2.4 The Location and the Default Setting of BOOT

Table 2.2 DIP Switch “BOOT” Settings

BOOT[x]	Signal	ON	OFF
6	SW_PDM_EN#	Module MEMS microphone (PDM0)	Carrier CAN1 (CAN1)
5	RZ_MD_CLKS	SSCG is disabled	SSCG is enabled
4	RZ_BOOTPLLCA_1	2’00: 1.1 GHz (BOOT[3] = ON, BOOT[4] = ON) 2’01: 1.5 GHz (BOOT[3] = OFF, BOOT[4] = ON) 2’10: 1.6 GHz (BOOT[3] = ON, BOOT[4] = OFF) 2’11: 1.7 GHz (BOOT[3] = OFF, BOOT[4] = OFF)	
3	RZ_BOOTPLLCA_0		
2	RZ_BOOTSELCPU	Cold boot from Cortex-M33	Cold boot from Cortex-A55
1	RZ_DEBUGEN	JTAG Debug is disabled	JTAG Debug is enabled

2.3.2 SYS

A bank of 6-switches is used to configure operating modes of the Module. The default settings are highlighted.

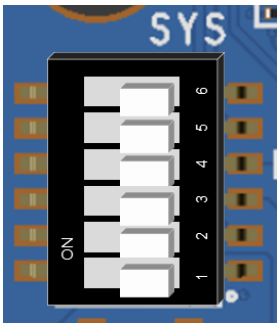


Figure 2.5 The Location and the Default Setting of SYS

Table 2.3 DIP Switch “SYS” Settings

SYS[x]	Signal	ON	OFF
6	SW_OTEHRS_IOVS	3.3 V (VDD_OTHERS)	1.8 V (VDD_OTHERS)
5	SW_LCD_EN#	Module LCD connector	Carrier CAN0, I2S2, SER0, SER1, SPI0
4	SW_SER2_EN#	Module DSI connector (GPIO)	Carrier SER2 (SCI2)
3	SW_I2S2_EN#	Carrier I2S2 (SSI0/9)	Carrier HDMI (SSI0)
2	SW_HDMI_EN	Module DSI connector (DSI)	Carrier HDMI (Converted DSI)
1	SW_SD0_DEV_SEL	SD0 connected to microSD0 card	SD0 connected to eMMC

2.3.3 SW1

A bank of 1-switch is used to select the VDD_I3C voltage of the Module. The default setting is highlighted.

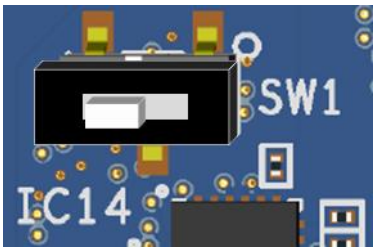


Figure 2.6 The Location and the Default Setting of SW1

Table 2.4 DIP Switch “SW1” Settings

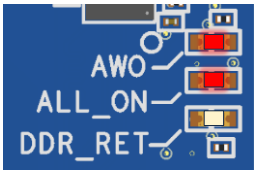
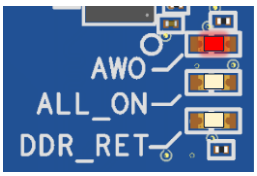
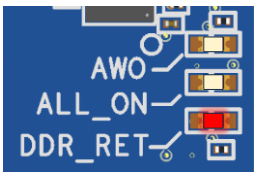
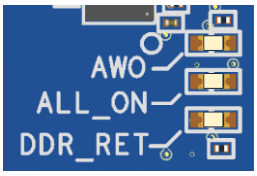
SW1	Function
1 – 2	1.2 V (VDD_I3C)
2 – 3	1.8 V (VDD_I3C)

2.4 List of Pin Functions

2.4.1 LED Indicators

The RZ/G3E has the following four power modes depending on the power on/off combination of the power domain. There are three Red LEDs on the G3E SMARC Module to provide indication of the RZ/G3E power modes.

Table 2.5 Indicator LEDs – Power Status

LED Status	Power Mode
	ALL_ON All CPUs and peripheral modules are active
	AWO Cortex-M33 and peripheral modules in the AWO domain are active
	AWO + DDR_Retention Cortex-M33 and peripheral modules in the AWO domain + DDR domain are active
	DDR_Retention Only the DDR domain is active
	ALL_OFF All CPUs and peripheral modules are disabled

2.5 Recommended Operating Condition

Table 2.6 lists operating conditions of the G3E SMARC Module.

Table 2.6 Operating Conditions of G3E SMARC Module

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage*1	3.0 V to 5.25 V	Reference: SMARC 2.1.1 Specification
—	Maximum power consumption	5 A	Reference: SMARC 2.1.1 Specification
Topr	Operating ambient temperature*2	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Supplied from the connected RZ SMARC Carrier II.

Note 2. The ambient temperature is the air temperature at a point as close to the board as possible.

3. Functional Specifications

3.1 Processor

The RZ/G3E (P/N: R9A09G047E57GBG, 15 mm × 15 mm, 0.5-mm pitch, 529-pin) includes a quad ARM Cortex-A55 core with speeds up to 1.8 GHz, an Arm Ethos-U55 as NPU with speeds up to 1.0 GHz, and a single Arm Cortex-M33 core with speeds up to 200 MHz.

The Arm Mali-G52 as 3D graphics, selectable 2 channel display interface, and H.264/H.265 as video codec are supported for HMI application. Also, low power stand-by/quick wake-up, and low power processing are realized by the Cortex-M33 and RTOS stand alone with Linux. In addition, dual 1-Gbit/s Ethernet controllers, USB3.2 Gen2, and PCI Express Gen3 drive 5G and high speed wireless/wired communications.

The RZ/G3E is useful for application such as:

- Mid-class HMI including edge computing such as industrial HMI, video conference, solar panel system, and plain paper copier (PPC)

For details on the processor, see the ***RZ SMARC Series Carrier Board II User's Manual: Hardware***.

3.2 Power Supply

Figure 3.1 shows a block diagram of power system of the G3E SMARC EVK.

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected among 5 V, 9 V, 15 V, and 20 V.

The 5 V power supply is supplied to the PMIC (RAA215300A2GNP#HA8) installed in the G3E SMARC Module, and the PMIC generates the power supply voltage for each interface.

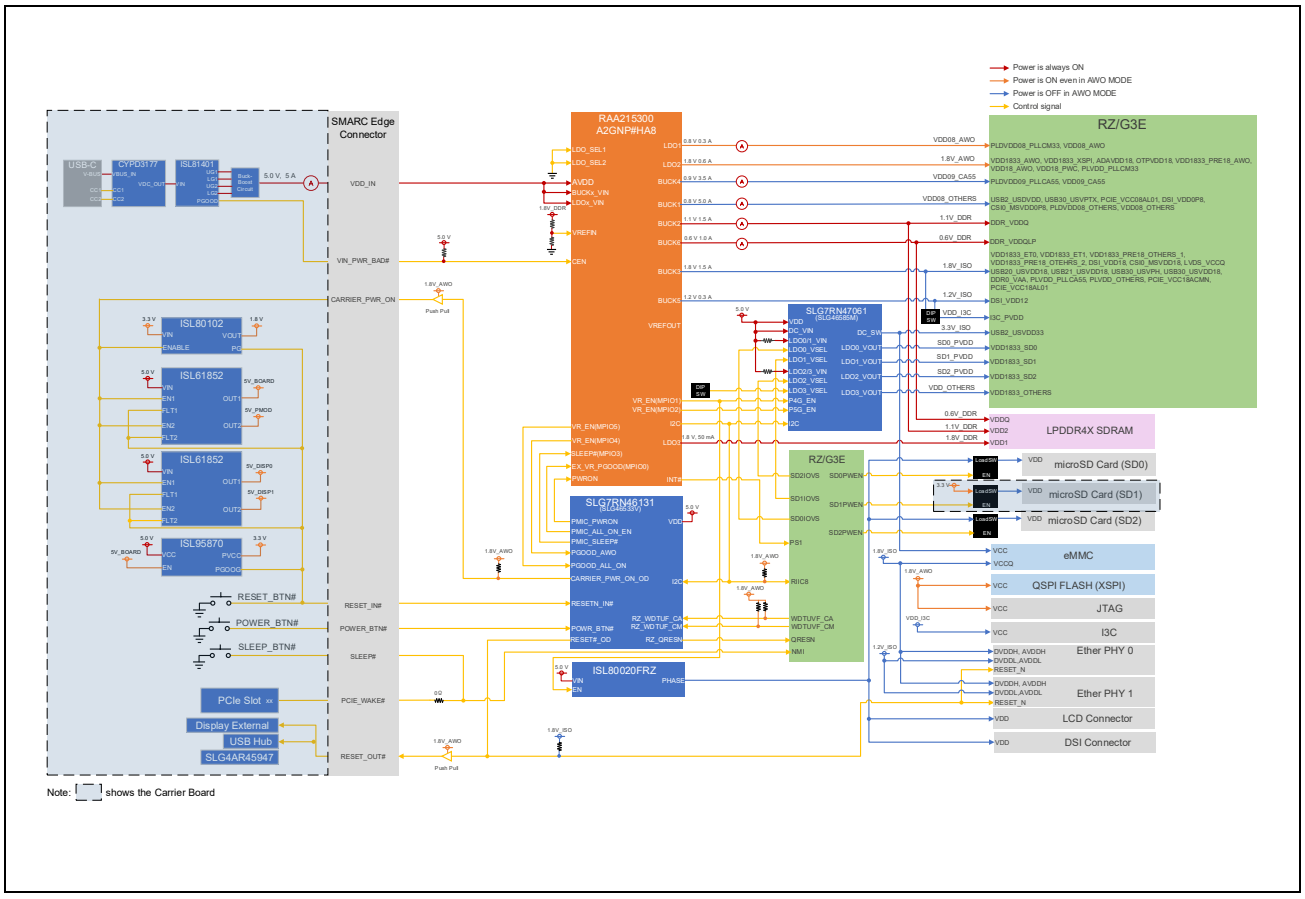


Figure 3.1 Power System Circuitry of G3E SMARC EVK

Figure 3.2 and **Figure 3.3** show the power sequence of all the G3E SMARC EVK power supplies during CA55 and CM33 cold boot.

The G3E SoC power rails are shown in red text. The control signals for PMIC or GreenPAKs are shown in purple. The control signals for the G3E SoC are shown in light green.

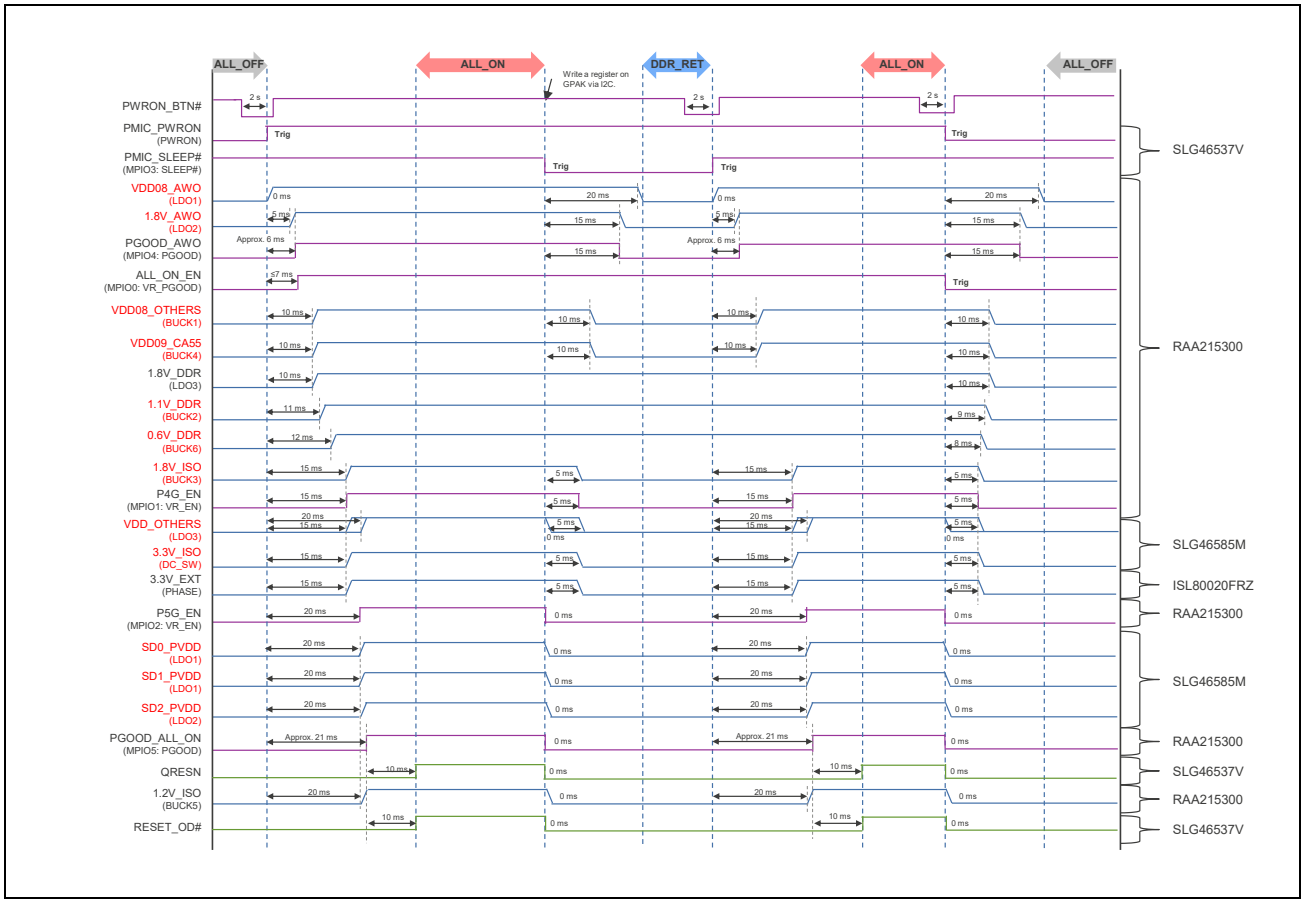


Figure 3.2 Power Sequence of G3E SMARC EVK during CA55 Cold Boot

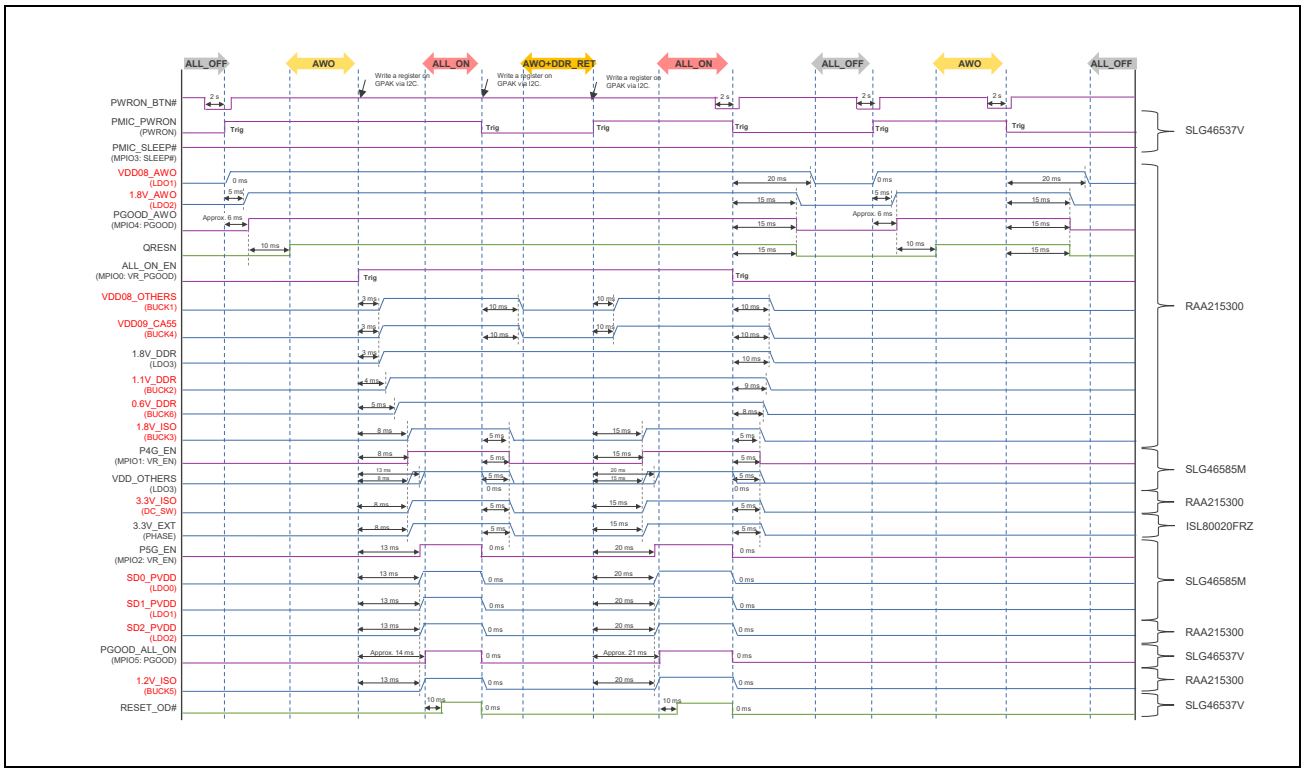


Figure 3.3 Power Sequence of G3E SMARC EVK during CM33 Cold Boot

3.3 Clock

The clock generators (part numbers 5L35023B-617NLGI and 5P35023B-789NLGI) provide the clock required for the G3E SoC and peripheral interfaces.

The 5L35023B and 5P35023B are Renesas VersaClock 3S programmable clock generators and support 6 unique frequency outputs.

The 5L35023B-617NLGI takes the 24 MHz crystal (part number ECS-240-10-47-CKM) as a reference input and provides one 24 MHz reference clock output for the G3E SoC, one 48 MHz LVCMOS clock output for the G3E SoC, one 12 MHz clock output for the MIPI DSI to HDMI conversion IC, one 32.768 kHz clock output for the RTC domain of the G3E SoC, and two 100 MHz LPHSCL clock outputs for the G3E SoC and a PCI Express Card Module.

The 5P35023B-789NLGI takes the 24 MHz crystal (part number ECS-240-10-47-CKM) as a reference input and provides two 11.2896 MHz LVCMOS clock outputs for the G3E SoC and Audio Codec, one 12.2880 MHz clock output for the G3E SoC, and two 25 MHz LVCMOS clock outputs for two Ethernet PHYs.

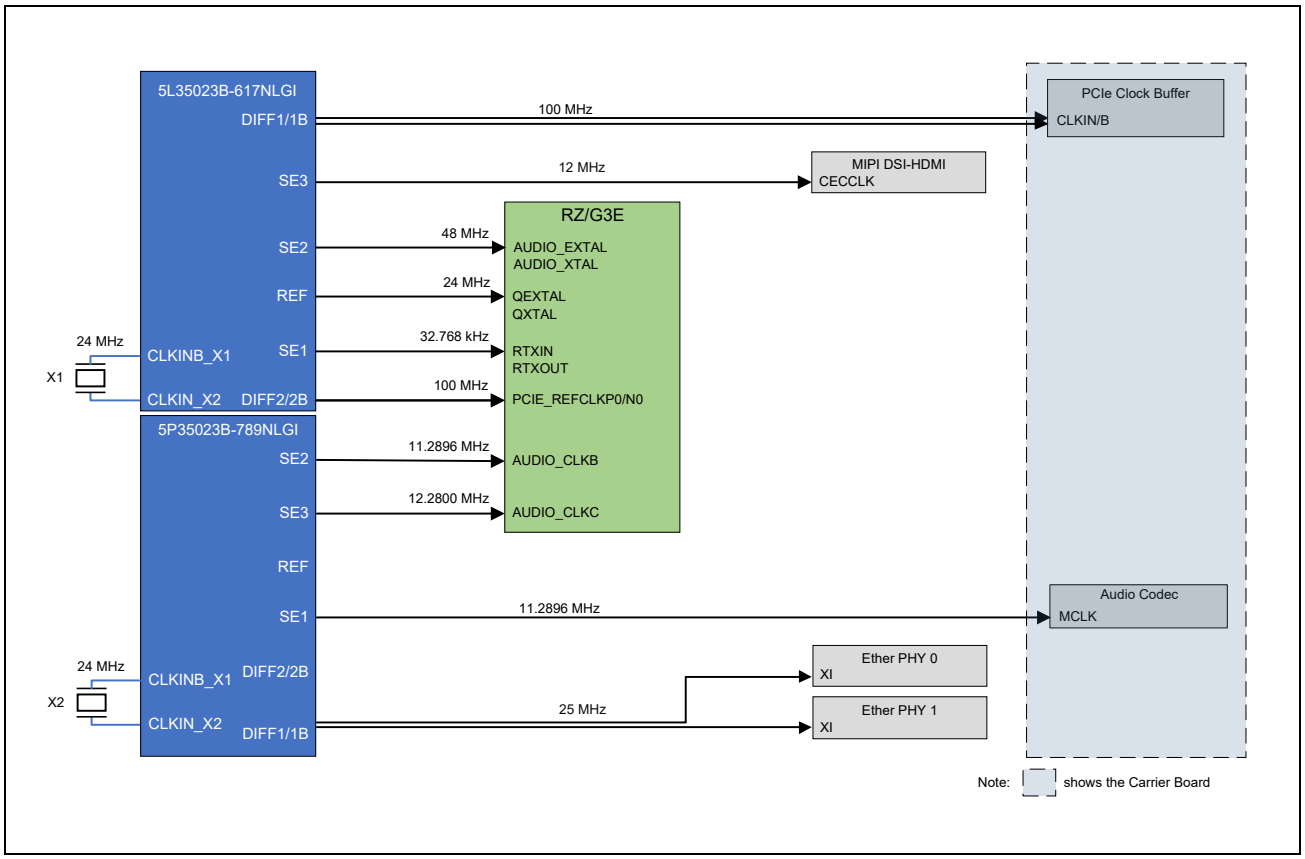


Figure 3.4 Clock Architecture of G3E SMARC EVK

Clock inputs required for peripherals such as FT232HQ, USB Hub, M.2 Key E Card Module, and HDMI Transmitter are generated locally using separate crystals or oscillators. The crystals or oscillators used to provide the reference clocks for the G3E SMARC EVK peripherals are shown in the table below.

Table 3.1 Clock Table

Peripheral	Device Part Number	Frequency
PMIC	ABS06-32.768KHZ-1-T	32.768 kHz
USB Hub*1	FL2400022	24.000 MHz
M.2 Key E*1	7XZ-32.768KBE	32.768 kHz
FT232HQ Bridge*2	ECS-120-10-36B-CWY-TR	12.000 MHz
HDMI Transmitter*3	ABM11-27.000MHZ-D2X	27.000 MHz

Note 1. RZ SMARC Carrier II

Note 2. SMARC Breakout Adaptor

Note 3. SMARC Dual LVDS to HDMI Adaptor

3.4 Reset

Figure 3.5 shows a block diagram of reset control for the G3E SMARC EVK.

For the G3E SMARC EVK, the G3E SoC, Ethernet PHY, etc. on the G3E SMARC Module and some modules on the RZ SMARC Carrier II are controlled by the reset signal from the SLG7RN47054 which is programmed as SLG46537V.

There are two types of system resets.

- Cold reset by power-on reset
- Warm reset by the reset button switch

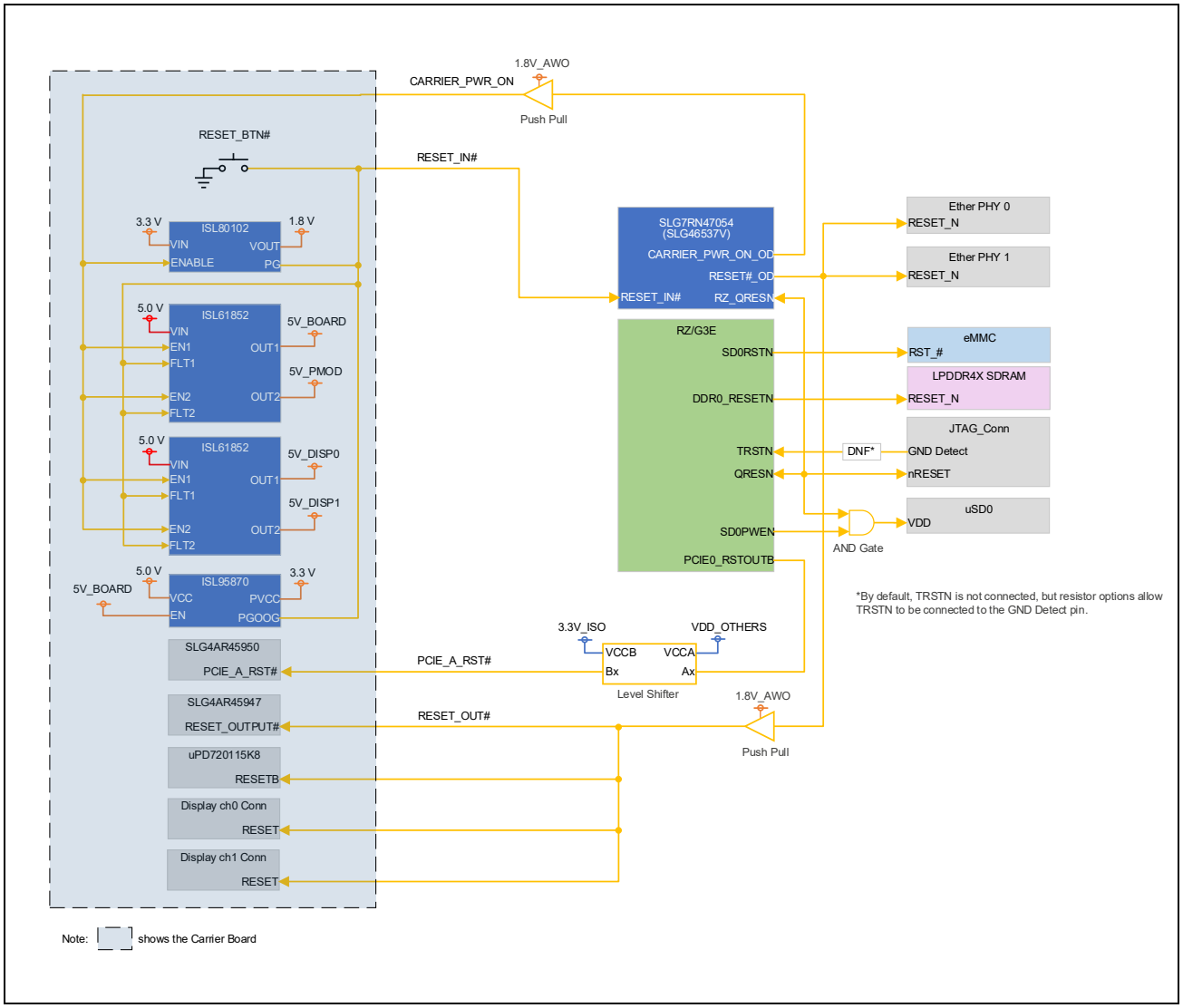


Figure 3.5 Reset Architecture of G3E SMARC EVK

3.5 LPDDR4X SDRAM

The G3E SMARC Module supports LPDDR4X SDRAM. A LPDDR4X SDRAM from Micron Technology (part number MT53E1G32D2FW-046 WT:C) is provided for connection to the RZ/G3E DDR IO.

3.6 xSPI Interface

The G3E SMARC Module supports QSPI flash memory for xSPI interfaces. A QSPI flash memory from Renesas (part number AT25QL128A-MHE) is provided for connection to the RZ/G3E xSPI IO.

3.7 eMMC Memory

This eMMC is on the top side of the G3E SMARC Module. An eMMC from Micron Technology (part number MTFC64GBCAQTC-IT) is provided for connection to the RZ/G3E MMC IO. The default settings are highlighted.

The RZ/G3E MMC IO may be used either for eMMC (SYS[1] = OFF) or for the microSD0 Card interface (SYS[1] = ON).

3.8 microSD0 Card Interface

This microSD card interface is on the top side of the G3E SMARC Module. Cards must be inserted with the contacts facing down.

The connector is a push-pull type. The default settings are highlighted.

The RZ/G3E SD0 IO may be used either for eMMC (SYS[1] = OFF) or for the microSD0 Card interface (SYS[1] = ON).

Additional control of the microSD0 card using the RZG3E port pins is shown below.

Table 3.2 microSD0 Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD0 Card Detect	P50/SD0CD	Input	0: Card present 1: No card present
microSD0 Card Power Enable	SD0PWEN	Output	0: Power disabled 1: Power enabled
microSD0 Card IO Power Select	SD0IOVS	Output	0: 3.3 V 1: 1.8 V

3.9 microSD2 Card Interface

This microSD card interface is on the bottom side of the G3E SMARC Module. Cards must be inserted with the contacts facing up.

The connector is a push-pull type.

The microSD2 card signals, using the RZG3E port pins, are shown below.

Table 3.3 microSD2 card Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD2 Data0	PH2/SD2DAT0	In/Out	microSD2 data
microSD2 Data1	PH3/SD2DAT1	In/Out	microSD2 data
microSD2 Data2	PH4/SD2DAT2	In/Out	microSD2 data
microSD2 Data3	PH5/SD2DAT3	In/Out	microSD2 data
microSD2 Command	PH1/SD2CMD	In/Out	microSD2 CMD
microSD2 Clock	PH0/SD2CLK	Output	microSD2 clock
microSD2 Card Detect	PK0/SD0CD	Input	0: Card present 1: No card present
microSD2 Card Power Enable	PK2/SD2PWEN	Output	0: Power disabled 1: Power enabled
microSD2 Card IO Power Select	PK1/SD2IOVS	Output	0: 3.3 V 1: 1.8 V

3.10 Gigabit Ethernet Interface

Two gigabit Ethernet transceivers with RGMII support are mounted on the G3E SMARC Module.

There are RJ45 connectors on the RZ SMARC Carrier II through the SMARC Edge connector. Refer to **section 3.19.12, Ethernet** for pin assignment.

3.11 I2C

There are four I2C interfaces connected to the SMARC Edge connector.

RIIC ch0 is connected to the MIPI CSI serial camera “I2C_CAM” interface. RIIC ch1 is connected to the general purpose “I2C_GP” interface. RIIC ch7 is connected to the LCD display “I2C_LCD” interface. RIIC ch8 is connected to the power management “I2C_PM” interface.

RIIC0 and RIIC1 are not connected to any devices on the G3E SMARC Module.

Table 3.4 Address Mapping for RIIC7

RIIC7 Device	7-bit Address
ADV7535BCBZ-RL (MIPI DSI to HDMI conversion)	0x72

Table 3.5 Address Mapping for RIIC8

RIIC8 Device	7-bit Address
Renesas RAA215300A2GNP#HA8 (PMIC)	0x12
Renesas GreenPAK SLG7RN47061 (Power Regulator)	0x28
Renesas GreenPAK SLG7RN47054 (Power/Reset control)	0x38
Renesas 5P35023B-789NLGI (clock generator)	0x68

3.12 ADC

This ADC interface is the FPC-to-Board (CN1) on the top side of the G3E SMARC Module. A 30-pin, 2.54-mm pitch FPC connector from Samtec (part number TSM-115-01-L-DV-P-TR) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3E ADC IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3E SMARC Module as shown in **Figure 3.6**.

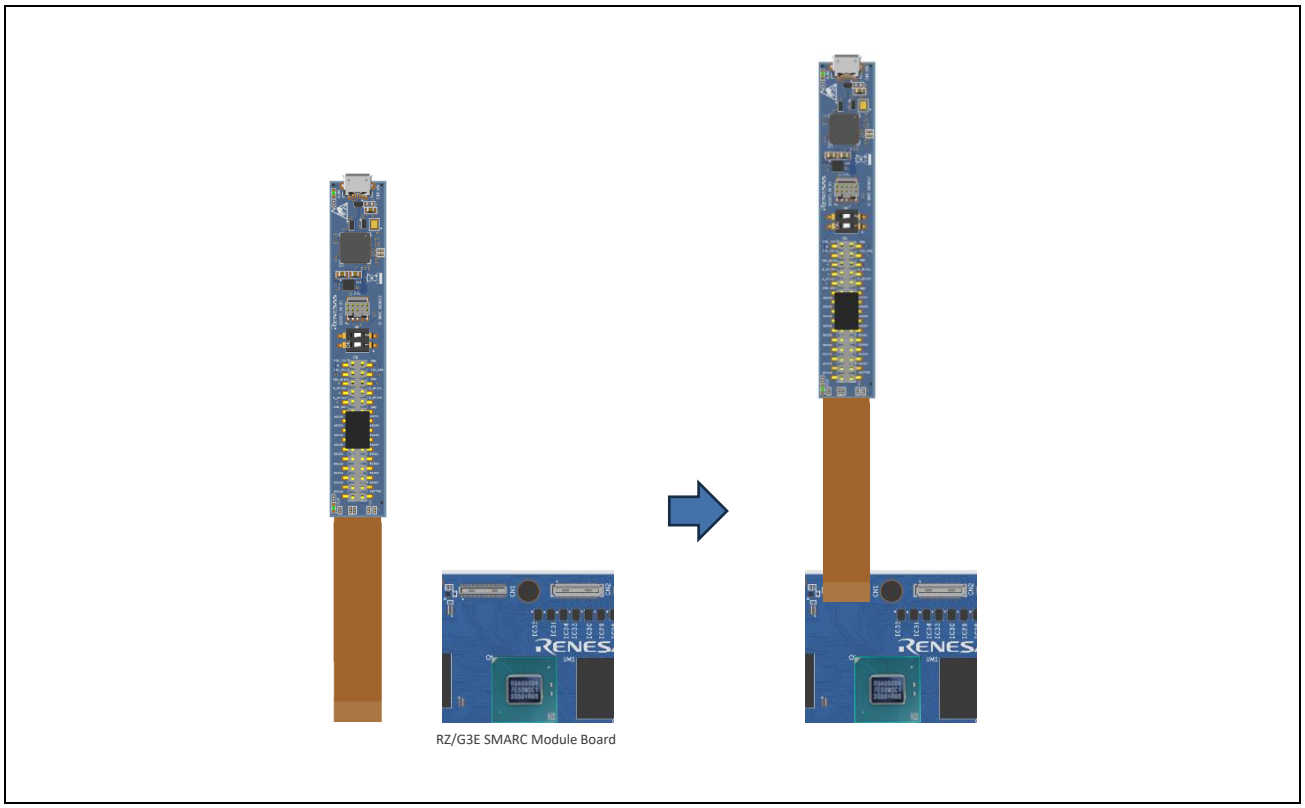


Figure 3.6 SMARC Breakout Adaptor Connection

The ADC interface voltage is 1.8 V. It has a common ground with a digital ground in terms of noise reduction.

Table 3.6 ADC Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	B_GPIO0	B_GPIO1	4
5	B_GPIO2	B_GPIO3 (Not connected)	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	RZ_SCL30	RZ_SDA30	18
19	ADC_AVDD (1.8 V)	Ground	20
21	RZ_ANI000	RSVD0 (Ground)	22
23	RZ_ANI001	RSVD1 (Ground)	24
25	RZ_ANI002	RSVD2 (Ground)	26
27	RZ_ANI003	RSVD3 (Ground)	28
29	RZ_ANI004	RSVD4 (Ground)	30
31	RZ_ANI005	RSVD5 (Ground)	32
33	RZ_ANI006	RSVD6 (Ground)	34
35	RZ_ANI007	RSVD7 (Ground)	36
37	RZ_P30/ADTRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	JTAG_TRST#	JTAG_TMS	42
43	JTAG_TDO	JTAG_TDI	44
45	JTAG_TCK	JTAG_RESET#	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

The ADC interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.13 I3C

This I3C interface is the FPC-to-Board (CN1) on the top side of the G3E SMARC Module. A 30-pin, 2.54-mm pitch FPC connector from Samtec (part number TSM-115-01-L-DV-P-TR) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3E I3C IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3E SMARC Module as shown in **Figure 3.6**.

Table 3.7 I3C Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	B_GPIO0	B_GPIO1	4
5	B_GPIO2	B_GPIO3 (Not connected)	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)*1	Ground	16
17	RZ_SCL30	RZ_SDA30	18
19	ADC_AVDD (1.8 V)	Ground	20
21	RZ_ANI000	RSVD0 (Ground)	22
23	RZ_ANI001	RSVD1 (Ground)	24
25	RZ_ANI002	RSVD2 (Ground)	26
27	RZ_ANI003	RSVD3 (Ground)	28
29	RZ_ANI004	RSVD4 (Ground)	30
31	RZ_ANI005	RSVD5 (Ground)	32
33	RZ_ANI006	RSVD6 (Ground)	34
35	RZ_ANI007	RSVD7 (Ground)	36
37	RZ_P30/ADTRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	JTAG_TRST#	JTAG_TMS	42
43	JTAG_TDO	JTAG_TDI	44
45	JTAG_TCK	JTAG_RESET#	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

Note 1. The I3C interface voltage is either 1.8 V (when SW1 = 2-3 short) or 1.2 V (when SW1 = 1-2 short).

The I3C interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.14 JTAG

This JTAG interface is the FPC-to-Board (CN1) on the top side of the G3E SMARC Module. A 10-pin, 1.27-mm pitch Cortex debug connector from Samtec (part number FTSH-105-01-L-DV-007-K) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3E JTAG IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3E SMARC Module as shown in **Figure 3.6**.

The JTAG interface voltage is 1.8 V.

Table 3.8 JTAG Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	B_GPIO0	B_GPIO1	4
5	B_GPIO2	B_GPIO3 (Not connected)	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	RZ_SCL30	RZ_SDA30	18
19	ADC_AVDD (1.8 V)	Ground	20
21	RZ_ANI000	RSVD0 (Ground)	22
23	RZ_ANI001	RSVD1 (Ground)	24
25	RZ_ANI002	RSVD2 (Ground)	26
27	RZ_ANI003	RSVD3 (Ground)	28
29	RZ_ANI004	RSVD4 (Ground)	30
31	RZ_ANI005	RSVD5 (Ground)	32
33	RZ_ANI006	RSVD6 (Ground)	34
35	RZ_ANI007	RSVD7 (Ground)	36
37	RZ_P30/ADTRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	JTAG_TRST#*1	JTAG_TMS	42
43	JTAG_TDO	JTAG_TDI	44
45	JTAG_TCK	JTAG_RESET#	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

Note 1. To use the JTAG interface, RZ_DEBUGEN must be high (BOOT[1] = OFF). If RZ_DEBUGEN is low (BOOT[1] = ON), the TRST# pin is held low and the JTAG interface will not function.

The JTAG interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.15 Current Monitor

A current monitoring circuitry that is accessed through the micro-USB connector on the Renesas SMARC Breakout Adaptor is provided via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3E SMARC Module as shown in **Figure 3.6**.

The current monitoring circuitry is powered from the USB and is completely independent of all other module and RZ/G3E functions.

A software application is required to execute on a host PC and provides current measurements for

- VDD08_AWO
- VDD08_OTHERS
- VDD09_CA55
- 1.1V_DDR
- 0.6V_DDR

Table 3.9 I2C Address Mapping for Current Monitoring

Device	7-bit Address
Renesas ISL28025FR12Z (VDD8_AWO)	0xa0
Renesas ISL28025FR12Z (VDD08_OTHERS)	0x9c
Renesas ISL28025FR12Z (VDD9_CA55)	0x84
Renesas ISL28025FR12Z (1.1V_DDR)	0x86
Renesas ISL28025FR12Z (0.6_DDR)	0x9e

Table 3.10 Current Monitor Pin Assignment on the FPC-to Board Connector (1/2)

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	B_GPIO0	B_GPIO1	4
5	B_GPIO2	B_GPIO3 (Not connected)	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	RZ_SCL30	RZ_SDA30	18
19	ADC_AVDD (1.8 V)	Ground	20
21	RZ_ANI000	RSVD0 (Ground)	22
23	RZ_ANI001	RSVD1 (Ground)	24
25	RZ_ANI002	RSVD2 (Ground)	26
27	RZ_ANI003	RSVD3 (Ground)	28
29	RZ_ANI004	RSVD4 (Ground)	30
31	RZ_ANI005	RSVD5 (Ground)	32
33	RZ_ANI006	RSVD6 (Ground)	34
35	RZ_ANI007	RSVD7 (Ground)	36
37	RZ_P30/ADTRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40

Table 3.10 Current Monitor Pin Assignment on the FPC-to Board Connector (2/2)

Pin Number	Module Connection	Module Connection	Pin Number
41	JTAG_TRST#	JTAG_TMS	42
43	JTAG_TDO	JTAG_TDI	44
45	JTAG_TCK	JTAG_RESET#	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

The current monitor function is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.15.1 Breakout Adaptor

The SMARC Breakout Adaptor is required to convert the MISC IO on the G3E SMARC Module to a 30-pin header for the ADC, I3C, and GPIO interfaces, a Cortex debug connector for the JTAG interface, and the current monitoring circuitry.

The current monitoring function can be realized by connecting to the console/terminal via micro-USB with the I2C to USB conversion IC from FTDI (part number FT232HQ).

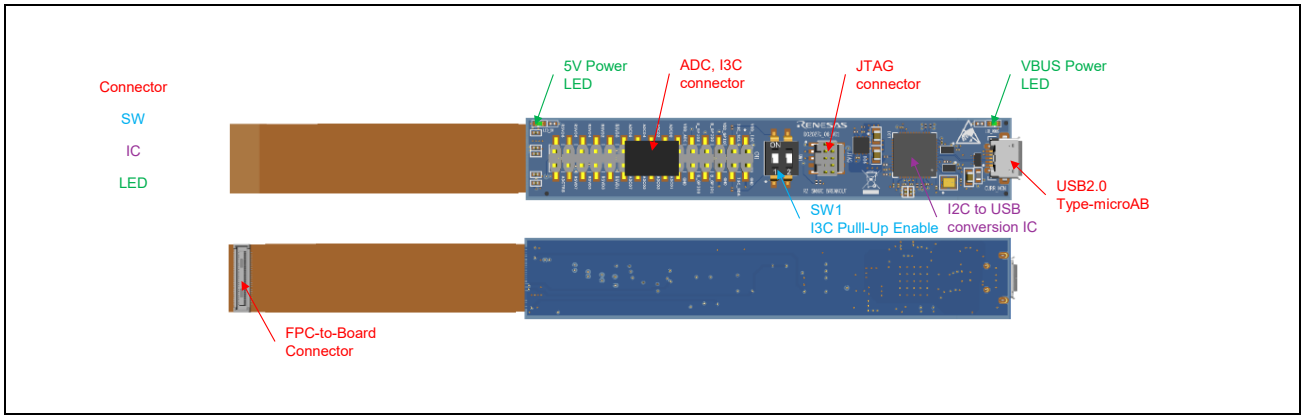


Figure 3.7 SMARC Breakout Adaptor Top and Bottom View

A bank of two switches is used to configure the pull-up functionality of the I3C interface. The default settings are highlighted.

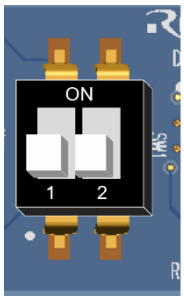


Figure 3.8 The Location and the Default Setting of SW1

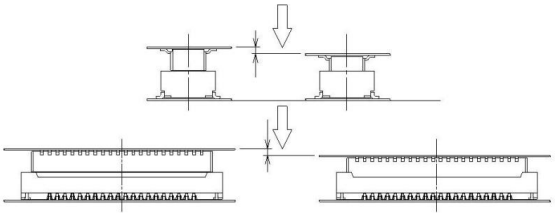
Table 3.11 DIP Switch “SW1” Settings

SW1	Signal	ON	OFF
2	I3C_SDA	Pull-up is enabled	Pull-up is disabled
1	I3C_SCL	Pull-up is enabled	Pull-up is disabled

Regarding the connector mating operation of the SMARC Breakout Adaptor, insert the adaptor to the connector in vertical direction. Regarding the connector unmating operation, remove the adaptor from the connector in vertical direction. If vertical removal is difficult, lift up either side in longitudinal, contact pitch direction. Do not unmate the connector in lateral direction; otherwise, the contacts could receive great stress.

Refer to DF40C-50DP-0.4V(51) for details.

When mating the adaptor to the connector on the G3E SMARC Module:



When unmating the adaptor from the connector on the G3E SMARC Module:

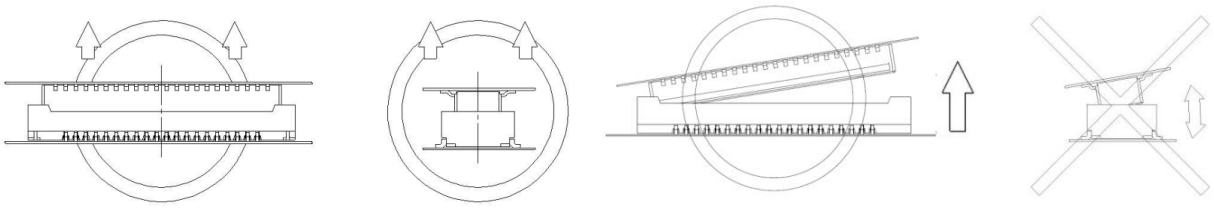


Figure 3.9 Caution when Mating/Unmating SMARC Breakout Adaptor to/from Connector

Table 3.12 ADC, I3C, and GPIO Interface Pin Assignment on the 30-pin Header

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_I3C (1.8 V or 1.2 V)	Ground	2
3	I3C_SCL	I3C_SDA	4
5	VDD_GPIO (3.3 V or 1.8 V)	Ground	6
7	B_GPIO0	B_GPIO1	8
9*1	B_GPIO2	B_GPIO3	10
11	VDD_ADC (1.8 V)	Ground	12
13	ADC00	ADC01	14
15	ADC02	ADC03	16
17	ADC04	ADC05	18
19	ADC06	ADC07	20
21	RSVD0	RSVD1	22
23	RSVD2	RSVD3	24
25	RSVD4	RSVD5	26
27	RSVD6	RSVD7	28
29	RSVD8	ADCTRG	30

Table 3.13 JTAG Pin Assignment on the Cortex Debug Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_JTAG (1.8 V)	JTAG_TMS	2
3	Ground	JTAG_TCK	4
5	Ground	JTAG_TDO	6
7	No pin (key)	JTAG_TDI	8
9*1	Ground	JTAG_RESET#	10

Note 1. By default, TRSTN is not connected and pin 9 is ground. However, resistor options allow TRSTN to be connected to pin 9.

3.16 Parallel Output

This Parallel Output interface is CN2 on the top side of the G3E SMARC Module. A 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DS-0.4V(51)) is provided for connection to the RZ/G3E Parallel Output IO.

The RZ/G3E Parallel Output IO belongs to dual purpose terminals, and may be used either for each connector as the CAN0, GPIO, I2S2, SER1, or SPI0 interface on the RZ SMARC Carrier II (SYS[1] = OFF) or for the LCD connector on the G3E SMARC Module (SYS[1] = ON).

The Parallel Output interface is realized by using the Renesas SMARC RGB-HDMI Adaptor which is included in the kit, then connecting to the FPC-to-Board on the G3E SMARC Module as shown in **Figure 3.8**.

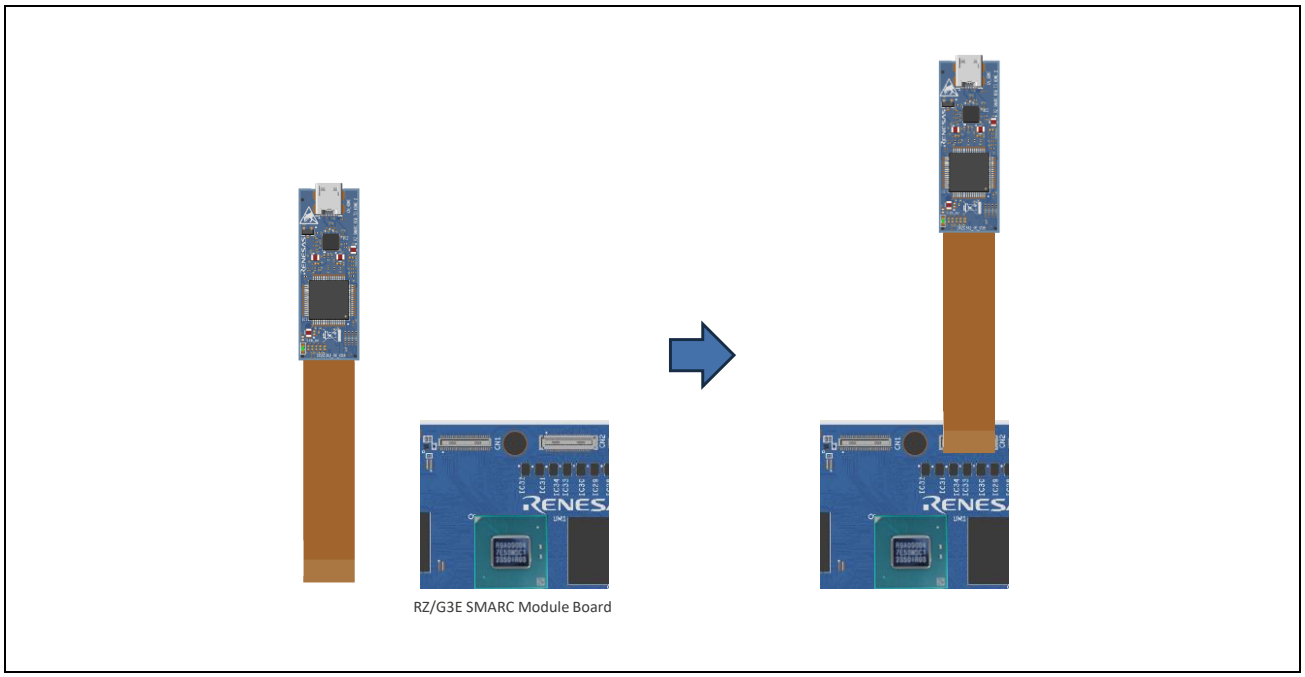


Figure 3.10 SMARC RGB-HDMI Adaptor Connection

The output form of this interface supports HDMI output as default. If you want to output parallel output signals directly to the display panel, this can be realized by developing the custom adaptor board by yourself, then connecting to the FPC-to-Board on the G3E SMARC Module.

Table 3.14 LCD Pin Assignment on the FPC-to Board Connector (1/2)

Pin Number	Module Connection	Module Connection	Pin Number
1	1.8V_ISO (1.8 V)	Ground	2
3	I2C_LCD_CK	I2C_LCD_DAT	4
5	RZ_P44/IRQ9_LCD_INT#	RZ_P17_LCD_RESET#	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	3.3V_EXT (3.3 V)	Ground	16
17	RZ_P07_LCD_BKLT_PWM	RZ_P06_LCD_VDD_EN	18
19	3.3V_EXT (3.3 V)	Ground	20
21	LCD1_R0	LCD1_R1	22

Table 3.14 LCD Pin Assignment on the FPC-to Board Connector (2/2)

Pin Number	Module Connection	Module Connection	Pin Number
23	LCD1_R2	LCD1_R3	24
25	LCD1_R4	LCD1_R5	26
27	LCD1_R6	LCD1_R7	28
29	LCD1_G0	LCD1_G1	30
31	LCD1_G2	LCD1_G3	32
33	LCD1_G4	LCD1_G5	34
35	LCD1_G6	LCD1_G7	36
37	LCD1_B0	LCD1_B1	38
39	LCD1_B2	LCD1_B3	40
41	LCD1_B4	LCD1_B5	42
43	LCD1_B6	LCD1_B7	44
45	Ground	LCD1_CLK	46
47	LCD1_HSYNC	LCD1_VSYNC	48
49	LCD1_DE	Ground	50

The Parallel Output interface is realized by using the Renesas SMARC RGB-HDMI Adaptor which is included in the kit.

3.16.1 RGB-HDMI Adaptor

The SMARC RGB-HDMI Adaptor is required to convert the RZG3E Parallel Output IO to HDMI output via the RGB to HDMI conversion IC (part number ADV7513BSWZ).

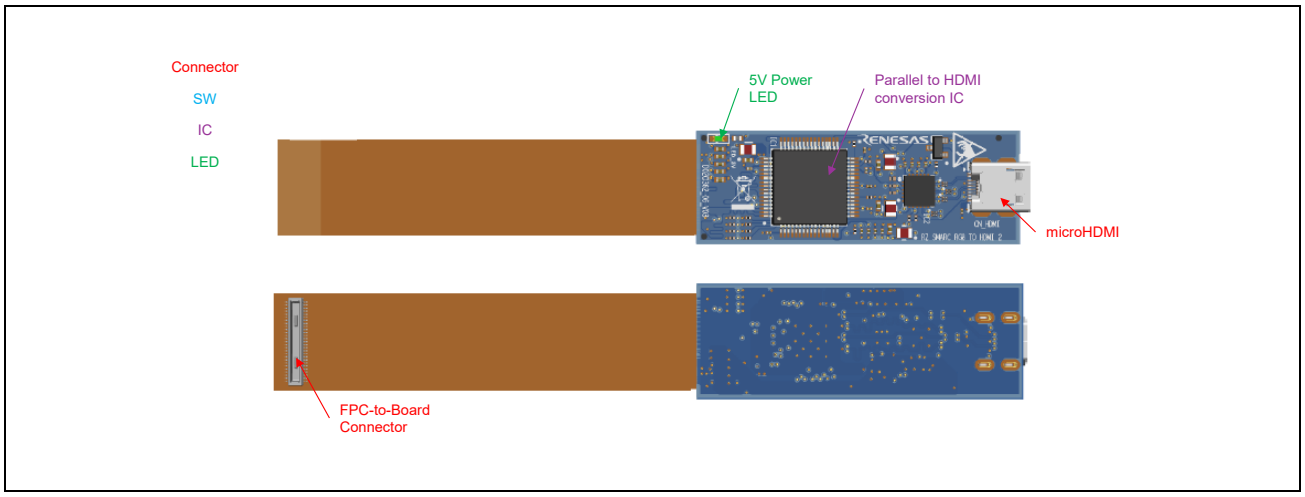
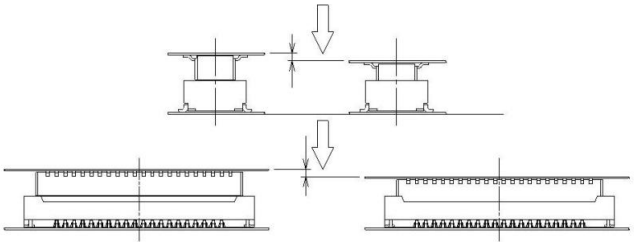


Figure 3.11 SMARC RGB-HDMI Adaptor Top and Bottom View

Regarding the connector mating operation of the SMARC RGB-HDMI Adaptor, insert the adaptor to the connector in vertical direction. Regarding the connector unmating operation, remove the adaptor from the connector in vertical direction. If vertical removal is difficult, lift up either side in longitudinal, contact pitch direction. Do not unmate the connector in lateral direction; otherwise, the contacts could receive great stress.

Refer to DF40C-50DS-0.4V(51) for details.

When mating the adaptor to the connector on the G3E SMARC Module:



When unmating the adaptor from the connector on the G3E SMARC Module:

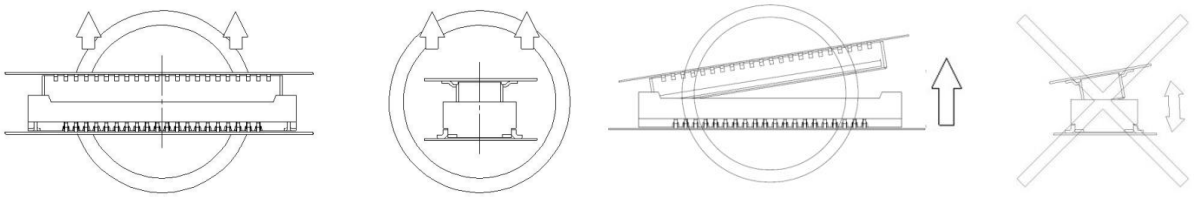


Figure 3.12 Caution when Mating/Unmating SMARC RGB-HDMI Adaptor to/from Connector

3.17 MIPI DSI

This MIPI DSI interface is supported for:

(1) the DSI connector (CN3) on the top side of the SMARC Module.

(2) the microHDMI connector on the RZ SMARC Carrier II through the SMARC Edge connector. Refer to **section 3.19.1, Display Interfaces** for pin assignment. (This is a default setting.)

Regarding (1), a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) is provided for connection to the RZ/G3E MIPI DSI IO. Regarding (2), the microHDMI connector via the MIPI DSI to HDMI conversion IC from Analog Devices (part number ADV7535BCBZ-RL) on the G3E SMARC Module is provided for connection to the RZ/G3E MIPI DSI IO as shown in **Figure 3.10**.

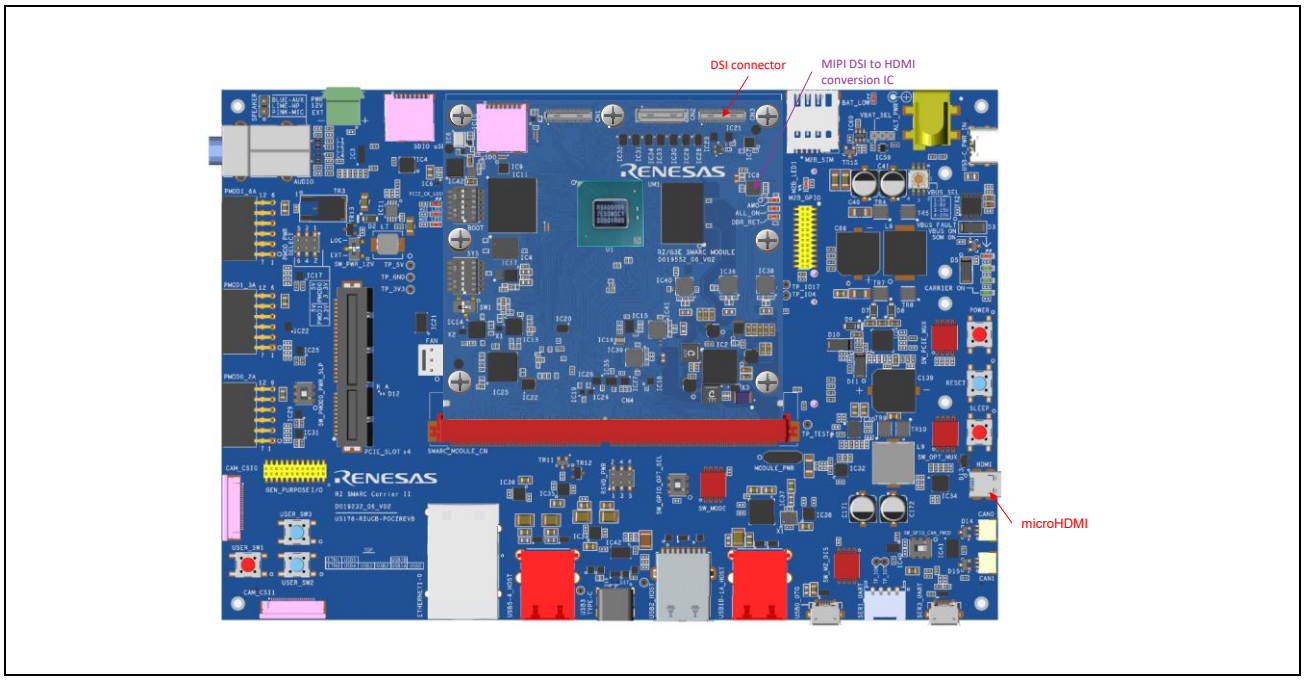


Figure 3.13 MIPI DSI to HDMI Conversion

The output form of this interface supports HDMI output as default. If you want to output MIPI DSI signals directly to the display panel, this can be realized developing the custom adaptor board by yourself, then connecting to the FPC-to-Board on the G3E SMARC Module.

The RZ/G3E MIPI DSI IO is used either for the HDMI output on the RZ SMARC Carrier II (SYS[2] = OFF) or for the DSI connector on the G3E SMARC Module (SYS[2] = ON). The default settings are highlighted.

Table 3.15 MIPI DSI Signals (1/2)

RZ Port Pin	Signal	Signal Passing through a Multiplexer
DSI_DPDATA0	RZ_DSI_DPDATA0	CN_DSI_D0+*1
		H_DSI_D0+*1
DSI_DNDATA0	RZ_DSI_DNDATA0	CN_DSI_D0-*1
		H_DSI_D0-*1
DSI_DPDATA1	RZ_DSI_DPDATA1	CN_DSI_D1+*1
		H_DSI_D1+*1
DSI_DNDATA1	RZ_DSI_DNDATA1	CN_DSI_D1-*1
		H_DSI_D1-*1

Table 3.15 MIPI DSI Signals (2/2)

RZ Port Pin	Signal	Signal Passing through a Multiplexer
DSI_DPDATA2	RZ_DSI_DPDATA2	CN_DSI_D2+*1
		H_DSI_D2+*1
DSI_DNDATA2	RZ_DSI_DNDATA2	CN_DSI_D2-*1
		H_DSI_D2-*1
DSI_DPDATA3	RZ_DSI_DPDATA2	CN_DSI_D3+*1
		H_DSI_D3+*1
DSI_DNDATA3	RZ_DSI_DNDATA2	CN_DSI_D3-*1
		H_DSI_D3-*1
DSI_DPCLK	RZ_DSI_DPCLK	CN_DSI_CLK+*1
		H_DSI_CLK+*1
DSI_DNCLK	RZ_DSI_DNCLK	CN_DSI_CLK-*1
		H_DSI_CLK-*1

Note 1. SYS[2] switch option on the G3E SMARC Module

3.18 PDM

This MEMS microphone is on the top side of the G3E SMARC Module. A MEMS microphone from TDK InvenSense (part number ICS-41350) is provided for connection to the RZ/G3E PDM IO.

The RZ/G3E PDM IO may be used either for the CAN transceiver as the CAN1 interface on the RZ SMARC Carrier II (BOOT[6] = OFF) or for the MEMS microphone on the G3E SMARC Module (BOOT[6] = ON).

3.19 SMARC Edge Connector

The SMARC edge connector has a Primary side (Pxx) and Secondary side (Sxx). The SMARC signal names and edge connector pin numbers are listed in the tables below along with the G3E port pin (if applicable) and signal name. The default settings are highlighted.

3.19.1 Display Interfaces

The HDMI signals converted from MIPI DSI and LVDS signals are routed to the SMARC Edge Connector.

The RZ/G3E MIPI DSI IO is used either for the uHDMI connector on the RZ SMARC Carrier II (SYS[2] = OFF) or for the MIPI DSI connector on the G3E SMARC Module (SYS[2] = ON).

Table 3.16 HDMI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
HDMI_D0+	P98	DSI_DPDATA0	RZ_DSI_DPDATA0/H_DSI_D0+
HDMI_D0-	P99	DSI_DNDATA0	RZ_DSI_DNDATA0/H_DSI_D0-
HDMI_D1+	P95	DSI_DPDATA1	RZ_DSI_DPDATA1/H_DSI_D1+
HDMI_D1-	P96	DSI_DNDATA1	RZ_DSI_DNDATA1/H_DSI_D1-
HDMI_D2+	P92	DSI_DPDATA2	RZ_DSI_DPDATA2/H_DSI_D2+
HDMI_D2-	P93	DSI_DNDATA2	RZ_DSI_DNDATA2/H_DSI_D2-
HDMI_CK+	P101	DSI_DPCLK	RZ_DSI_DPCLK/H_DSI_CLK+
HDMI_CK-	P102	DSI_DNCLK	RZ_DSI_DNCLK/H_DSI_CLK-
HDMI_CTRL_CK	P105	PA5/SDA7	I2C_LCD_DAT
HDMI_CTRL_DAT	P106	PA4/SCL7	I2C_LCD_CK
HDMI_HPD	P104	—	HDMI_HPD

NOTE

Do not connect the SMARC Dual LVDS to two mini-PCIe connectors on the RZ SMARC Carrier II during AWO or AWO + DDR_Retention mode.

The details of camera interface of the RZ SMARC Carrier II board are to be found in the **RZ SMARC Carrier II User Manual**.

Table 3.17 LVDS Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
LVDS0_0+	S125	LVDS0_DATA0P	LVDS0_0+
LVDS0_0-	S126	LVDS0_DATA0N	LVDS0_0-
LVDS0_1+	S128	LVDS0_DATA1P	LVDS0_1+
LVDS0_1-	S129	LVDS0_DATA1N	LVDS0_1-
LVDS0_2+	S131	LVDS0_DATA2P	LVDS0_2+
LVDS0_2-	S132	LVDS0_DATA2N	LVDS0_2-
LVDS0_3+	S137	LVDS0_DATA3P	LVDS0_3+
LVDS0_3-	S138	LVDS0_DATA3N	LVDS0_3-
LVDS0_CK+	S134	LVDS0_CLKP	LVDS0_CK+
LVDS0_CK-	S135	LVDS0_CLKN	LVDS0_CK-
LCD0_VDD_EN	S133	PL5/GPIO	LCD0_VDD_EN
LCD0_BKLT_EN	S107	PL7/GPIO	LCD0_BKLT_EN
LCD0_BKLT_PWM	S141	PL7/GPIO	LCD0_BKLT_PWM
LVDS1_0+	S111	LVDS1_DATA0P	LVDS1_0+
LVDS1_0-	S112	LVDS1_DATA0N	LVDS1_0-
LVDS1_1+	S114	LVDS1_DATA1P	LVDS1_1+
LVDS1_1-	S115	LVDS1_DATA1N	LVDS1_1-
LVDS1_2+	S117	LVDS1_DATA2P	LVDS1_2+
LVDS1_2-	S118	LVDS1_DATA2N	LVDS1_2-
LVDS1_3+	S120	LVDS1_DATA3P	LVDS1_3+
LVDS1_3-	S121	LVDS1_DATA3N	LVDS1_3-
LVDS1_CK+	S108	LVDS1_CLKP	LVDS1_CK+
LVDS1_CK-	S109	LVDS1_CLKN	LVDS1_CK-
LCD1_VDD_EN	S116	PA6/GPIO	LCD1_VDD_EN
LCD1_BKLT_EN	S107	P37/GPIO	LCD1_BKLT_EN
LCD1_BKLT_PWM	S122	PA7/GPIO	LCD1_BKLT_PWM
I2C_LCD_DAT	S140	PA5/SDA7	I2C_LCD_DAT
I2C_LCD_CK	S139	PA4/SCL7	I2C_LCD_CK

3.19.2 Camera Interfaces

The CSI1 signals are routed to the SMARC Edge Connector.

NOTE

Do not connect the SMARC Coral Camera Adaptor to a 22-pin FPC connector on the RZ SMARC Carrier II during AWO or AWO + DDR_Retention mode.

The details of camera interface of the RZ SMARC Carrier II board are to be found in the **RZ SMARC Carrier II User Manual**.

Table 3.18 MIPI CSI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CSI1_RX0+	P7	CSI0_DATA0P	CSI1_RX0+
CSI1_RX0-	P8	CSI0_DATA0N	CSI1_RX0-
CSI1_RX1+	P10	CSI0_DATA1P	CSI1_RX1+
CSI1_RX1-	P11	CSI0_DATA1N	CSI1_RX1-
CSI1_RX2+	P13	CSI0_DATA2P	CSI1_RX2+
CSI1_RX2-	P14	CSI0_DATA2N	CSI1_RX2-
CSI1_RX3+	P16	CSI0_DATA3P	CSI1_RX3+
CSI1_RX3-	P17	CSI0_DATA3N	CSI1_RX3-
CSI1_CK+	P3	CSI0_CLKP	CSI1_CK+
CSI1_CK-	P4	CSI0_CLKN	CSI1_CK-
I2C_CAM1_DAT	S2	PD5/SDA0	I2C_CAM1_DAT
I2C_CAM1_CK	S1	PD4/SCL0	I2C_CAM1_CK
CAM1_PWR#	P109	PD6/GPIO	GPIO1/CAM1_PWR#
CAM1_RST#	P111	PD7/GPIO	GPIO3/CAM1_RST#
CAM_MCK	S6	—	Not connected

3.19.3 SDIO Card (4-bit) Interface

The SDIO signal is routed to the SMARC Edge Connector.

Table 3.19 SDIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SDIO_D0	P39	PG2/SD1DAT0	SDIO_D0
SDIO_D1	P40	PG3/SD1DAT1	SDIO_D1
SDIO_D2	P41	PG4/SD1DAT2	SDIO_D2
SDIO_D3	P42	PG5/SD1DAT3	SDIO_D3
SDIO_WP	P33	—	Not connected
SDIO_CMD	P34	PG1/SD1CMD	SDIO_CMD
SDIO_CD#	P35	P14/SD1CD	SDIO_CD#
SDIO_CK	P36	PG0/SD1CLK	SDIO_CK
SDIO_PWR_EN	P37	P16/SD1PWEN	RZ_SD1PWEN

3.19.4 SPI Interfaces

The SPI0 and SPI1 signals are routed to the SMARC Edge Connector.

The RZ/G3E RSPI ch1 IO belongs to dual purpose terminals, and is used either for the PMOD0 connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3E SMARC Module (SYS[5] = ON).

Table 3.20 SPI0 and SPI1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal Passing through a Multiplexer
SPI0_CS0#	P43	P63/LCD_G5/SSLB0	LCD1_G5*1
			SPI0_CS0#*1
SPI0_CS1#	P31	—	Not connected
SPI0_CK*1	P44	P62/LCD_R6/RSPCKB	LCD1_R6*1
			SPI0_CK*1
SPI0_DIN*1	P45	P60/LCD_G6/MISOB	LCD1_G6*1
			SPI0_DIN*1
SPI0_DO*1	P46	P61/LCD_B6/MOSIB	LCD1_B6*1
			SPI0_DO*1
SPI1_CS0#	P54	PM7/SSLA0	SPI1_CS0#
SPI1_CS1#	P55	—	Not connected
SPI1_CK	P56	PM6/RSPCKA	SPI1_CK
SPI1_DIN	P57	PM4/MISOA	SPI1_DIN
SPI1_DO	P58	PM5/MOSIA	SPI1_DO

Note 1. SYS[5] switch option on the G3E SMARC Module

3.19.5 Audio

The I2S0 and I2S2 signals are routed to the SMARC Edge Connector.

The RZ/G3E SSI ch0 IO belongs to dual purpose terminals, and is used either for each connector as SSI interface (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3E SMARC Module (SYS[5] = ON).

In addition, if the SSI interface is selected, the RZ/G3E SSI ch0 IO is used either for the MIPI DSI to HDMI conversion IC on the G3E SMARC Module (SYS[3] = OFF) or for the M.2 Key E or the DISP0 connector on the RZ SMARC Carrier II (SYS[3] = ON).

Table 3.21 I2S0 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S0_LRCK	S39	P04/SSI3_WS	RZ_SSI3_WS
I2S0_SDOUT	S40	P02/SSI3_SDATA	RZ_SSI3_SDATA
I2S0_SDIN	S41	P05/SSI4_SDATA	RZ_SSI4_SDATA
I2S0_CK	S42	P03/SSI3_SCK	RZ_SSI3_SCK
AUDIO_MCK	S38	N/A	AUDIO_MCK (clock generator)

Table 3.22 I2S2 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal Passing through a Multiplexer	
I2S2_LRCK	S50	P72/LCD0_G3/SSI0_WS	LCD1_G3*1	—
			SSI0_WS*1	I2S2_LRCK*2
				H_SSI0_WS*2
I2S2_SDOUT	S51	P70/LCD0_B4/SSI0_SDATA	LCD1_B4*1	—
			SSI0_SDATA*1	I2S2_SDOUT*2
				H_SSI0_SDATA*2
I2S2_SDIN	S52	P73/LCD0_B3/SSI9_SDATA	LCD1_B3*1	—
			SSI9_SDATA*1	I2S2_SDIN*2
				Not connected*2
I2S2_CK	S53	P71/LCD0_R4/SSI0_SCK	LCD1_R4*1	—
			SSI0_SCK*1	I2S2_CK*2
				H_SSI0_SCK*2

Note 1. SYS[5] switch option on the G3E SMARC Module

Note 2. SYS[3] switch option on the G3E SMARC Module

3.19.6 I2C Interfaces

The I2C_GP, I2C PM, I2C_CAM1, and I2C_LCD signals are routed to the SMARC Edge Connector.

The I2C_CAM0 is not connected to the SMARC Edge Connector.

Table 3.23 I2C_GP, I2C_PM, I2C_CAM1, and I2C_LCD Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2C_CAM1_CK	S1	PD4/SCL0	I2C_CAM1_CK
I2C_CAM1_DAT	S2	PD5/SDA0	I2C_CAM1_DAT
I2C_GP_CK	S48	P32/SCL1	I2C_GP_CK
I2C_GP_DAT	S49	P33/SDA1	I2C_GP_DAT
I2C_PM_CK	P121	P34/SCL8	I2C_PM_CK
I2C_PM_DAT	P122	P35/SDA8	I2C_PM_DAT
I2C_LCD_CK	S139	PA4/SCL7	I2C_LCD_CK
I2C_LCD_DAT	S140	PA4/SDA7	I2C_LCD_DAT

NOTE

RIIC8 bus is also used on the G3E SMARC Module itself for:

- Power/Reset Control: SLG7RN47054
- PMIC: RAA215300A2GNP#HA8
- Power Regulator: SLG7RN47061
- Clock Generator: 5P35023B-789NLGI

3.19.7 Asynchronous Serial Ports

The SER0, SER1, SER2, and SER3 signals are routed to the SMARC Edge Connector.

The RZ/G3E RSCI ch3 and ch4 IO belong to dual purpose terminals, and are used either for the PMOD1 connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3E SMARC Module (SYS[5] = ON).

The RZ/G3E RSCI ch2 IO belongs to dual purpose terminals, and is used either for the M.2 Key E on the RZ SMARC Carrier II (SYS[4] = OFF) or for the DSI connector as the MIPI DSI interface on the G3E SMARC Module (SYS[4] = ON).

Table 3.24 SER0, SER1, SER2, and SER3 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SER0_TX	P129	P77/LCD_R2/TXD4_MOSI4_SDA4	LCD1_R2*1
			SER0_TX*1
SER0_RX*1	P130	P76/LCD_B2/RXD4_MISO4_SCL4	LCD1_B2*1
		—	SCR0_RX*1
SER0_RTS#	P131	P81/LCD_B1/SS4_CTS4N_RTS4N	LCD1_B1*1
			SER0_RTS#*1
SER0_CTS#	P132	P80/LCD_G1/CTS4N	LCD1_G1*1
			SER0_CTS0#*1
SER1_TX	P134	P83/LCD_G0/TXD9_MOSI9_SDA9	LCD1_G0*1
			SER1_TX*1
SER1_RX	P135	P82/LCD_R1/TXD9_MISO9_SDA9	LCD1_R1*1
			SER1_RX*1
SER2_TX	P136	P11/TXD2_MOSI2_SDA2	DSI_TE*2
			SER2_TX*2
SER2_RX	P137	P10/RXD2_MISO2_SCL2	DSI_BKLT_PWM*2
			SER2_RX*2
SER2_RTS#	P138	P13/SS2_SS_CTS2N_RTS2N	DSI_BKLT_EN*2
			SER2_RTS#*2
SER2_CTS#	P139	P12/CTS2N	DSI_VDD_EN*2
			SER2_CTS#*2
SER3_TX	P140	SCIF0_TXD	SER3_TX
SER3_RX	P141	SCIF0_RXD	SER3_RX

Note 1. SYS[5] switch option on the G3E SMARC Module

Note 2. SYS[4] switch option on the G3E SMARC Module

3.19.8 CAN Bus

These signals are routed to the SMARC Edge Connector.

The RZ/G3E CAN ch0 IO belongs to dual purpose terminals, and is used either for the CAN transceiver on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the RZ SMARC Carrier II (SYS[5] = ON).

The RZ/G3E CAN ch1 IO belongs to dual purpose terminals, and is used either for the MEMS microphone on the G3E SMARC Module (BOOT[6] = OFF) or for the CAN transceiver on the RZ SMARC Carrier II (BOOT[6] = ON).

Table 3.25 CAN0 and CAN1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CAN0_TX	P143	P52/LCD_CLK/CRX4	LCD1_VSYNC*1
			CAN0_TX*1
CAN0_RX	P144	P53/LCD_DE/CTX4	LCD1_DE*1
			CAN0_RX*1
CAN1_TX	P145	PL2/CRX1¥PDMCLK01	PDM0_CLK1*2
			CAN1_TX*2
CAN1_RX	P146	PL3/CTX1¥PDMDAT01	PDM0_DAT1*2
			CAN1_RX*2

Note 1. SYS[5] switch option on the G3E SMARC Module

Note 2. BOOT[6] switch option on the G3E SMARC Module

3.19.9 USB Interfaces

The USB ch0, ch1, and ch2 signals are routed to the SMARC Edge Connector.

The USB ch3, ch4, and ch5 signals are not connected to the SMARC Edge connector.

Table 3.26 USB0 and USB1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
USB0+	P60	USB20_DP	USB0+
USB0-	P61	USB20_DM	USB0-
USB0_EN_OC#	P62	P01/USB20_VBUSEN	RZ_P01/USB20_VBUSEN*1
		P00/USB20_OVRCURN	RZ_P00/USB20_OVRCURN*1
USB0_VBUS_DET	P63	USB20_VBUSIN	USB0_VBUS_DET
USB0_OTG_ID	P64	USB20_OTGID	USB0_OTG_ID
USB1+	P65	USB21_DP	USB1+
USB1-	P66	USB21_DP	USB1-
USB1_EN_OC#	P67	PK3/USB21_VBUSEN	RZ_PK3/USB21_VBUSEN*1
		PG6/USB21_OVRCURN	RZ_PG6/USB21_OVRCURN*1
USB2+	P69	USB30_DP	USB2+
USB2-	P70	USB30_DM	USB2-
USB2_SSRX+	S74	USB30_TX0M	USB2_SSRX+
USB2_SSRX-	S75	USB30_TX0P	USB2_SSRX-
USB2_SSTX+	S71	USB30_RX0M	USB2_SSTX+
USB2_SSTX-	S72	USB30_RXDP	USB2_SSTX-
USB2_EN_OC#	P71	P41/USB30_VBUSEN	RZ_P41/USB30_VBUSEN*1
		P40/USB30_OVRCURN	RZ_P40/USB30_OVRCURN*1

Note 1. Logic circuitry is used to provide independent enable and overcurrent IO.

3.19.10 PCI Express

The PCIE_A and PCIE_B signals are routed to the SMARC Edge Connector.

The PCIE_C and PCIE_D signals are not connected to the SMARC Edge Connector.

Table 3.27 PCIE_A Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
PCIE_A_TX+	P89	PCIE_TXDPL0	PCIE_A_TX+
PCIE_A_TX-	P90	PCIE_TXDNL0	PCIE_A_TX-
PCIE_A_RX+	P86	PCIE_RXDPL0	PCIE_A_RX+
PCIE_A_RX-	P87	PCIE_RXDNL0	PCIE_A_RX-
PCIE_A_REFCK+	P83	N/A	PCIE_A_REFCK+ (clock generator)
PCIE_A_REFCK-	P84	N/A	PCIE_A_REFCK- (clock generator)
PCIE_A_RST#	P75	PG7/PCIE0_RSTOUTB	RZ_PCIE0_RSTOUTB
PCIE_A_CKREQ#	P78	P45	RZ_P45_PCIE_CKREQ#
PCIE_B_TX+	S90	PCIE_TXDPL1	PCIE_B_TX+
PCIE_B_TX-	S91	PCIE_TXDNL1	PCIE_B_TX-
PCIE_B_RX+	S87	PCIE_RXDPL1	PCIE_B_RX+
PCIE_B_RX-	S88	PCIE_RXDNL1	PCIE_B_RX-

3.19.11 SATA

The RZG3E does not support SATA interfaces. None of the SATA signals are connected.

3.19.12 Ethernet

These signals are routed to the SMARC Edge Connector.

Table 3.28 GBE0 and GBE1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET0_xxx
GBE0_LINK100#	P21	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK1000#	P22	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK_ACT#	P25	N/A	ET0_LED1 (ET0 PHY)
GBE0_CTREF	P28	—	Not connected
GBE0_SDP	P6	—	Not connected
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET1_xxx
GBE1_LINK100#	S19	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK1000#	S22	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK_ACT#	S31	N/A	ET1_LED1 (ET1 PHY)
GBE1_CTREF	S28	—	Not connected
GBE1_SDP	P5	—	Not connected

3.19.13 GPIO

These signals are routed to the SMARC Edge Connector.

Table 3.29 GPIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GPIO0	P108	—	Not connected
GPIO1	P109	PD6	GPIO1/CAM1_PWR#
GPIO2	P110	—	Not connected
GPIO3	P111	PD7	GPIO3/CAM1_RST#
GPIO4	P112	P31	GPIO4
GPIO5	P113	P36	GPIO5
GPIO6	P114	P84/LCD0_B0	LCD1_B0*1
			GPIO6*1
GPIO7	P115	P85/LCD_R0	LCD1_R0*1
			GPIO7*1
GPIO8	P116	P54/LCD_G7	LCD1_G7*1
			GPIO8*1
GPIO9	P117	P55/LCD_B7	LCD1_B7*1
			GPIO9*1
GPIO10	P118	P65/LCD_R5	LCD1_R5*1
			GPIO10*1
GPIO11	P119	P56/LCD_R7	LCD1_R7*1
			GPIO11*1
GPIO12	S142	P66/LCD_G4	LCD1_G4*1
			GPIO12*1
GPIO13	S123	P64/LCD_B5	LCD1_B5*1
			GPIO13*1

Note 1. SYS[5] switch option on the G3E SMARC Module

Appendix A Heatspreader Assembly

Figure A.1 to **Figure A.4** show how to install a heatspreader to the G3E SMARC Module.

Step 1:

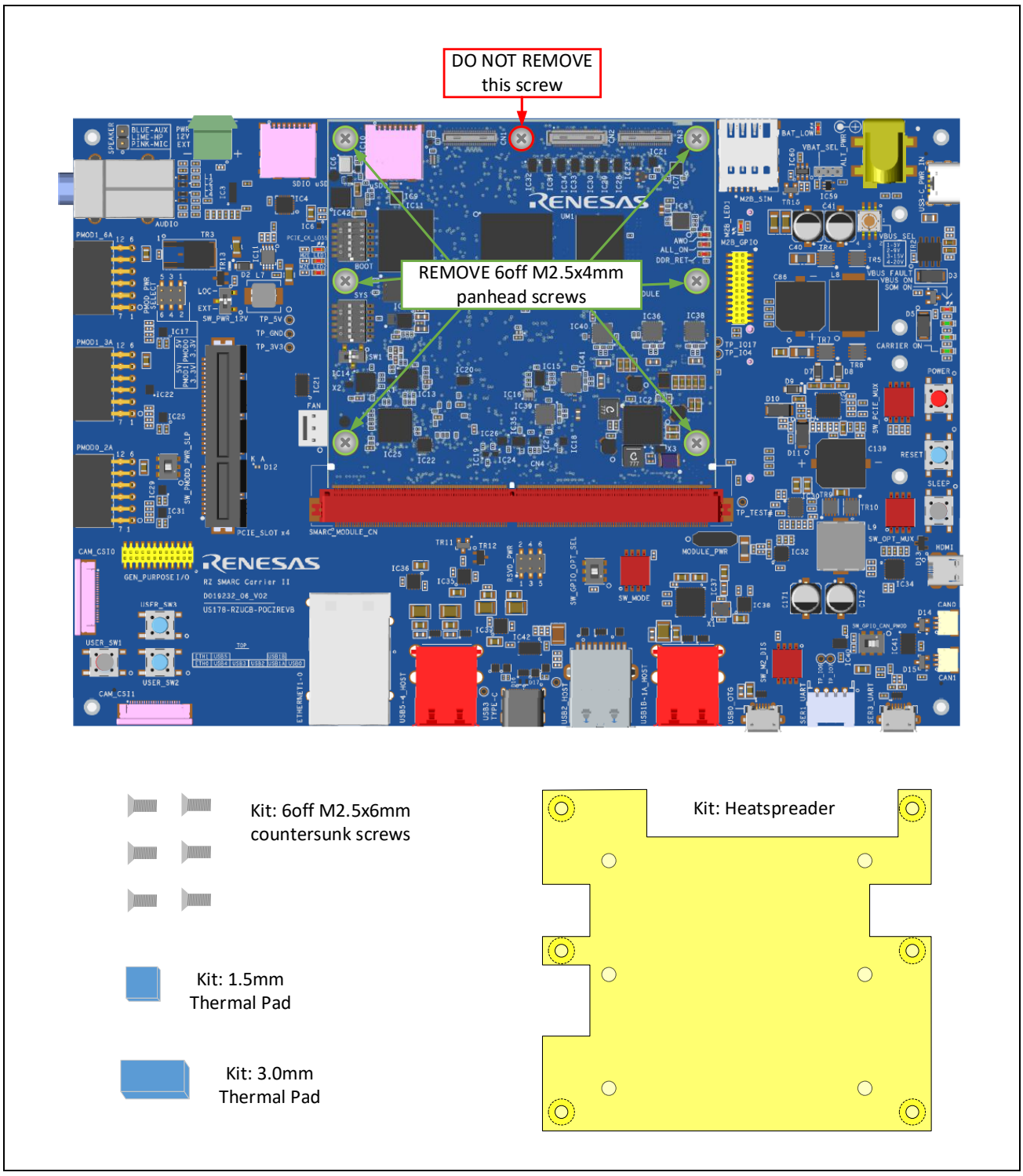


Figure A.1 How to Remove the Screws

Step 2:

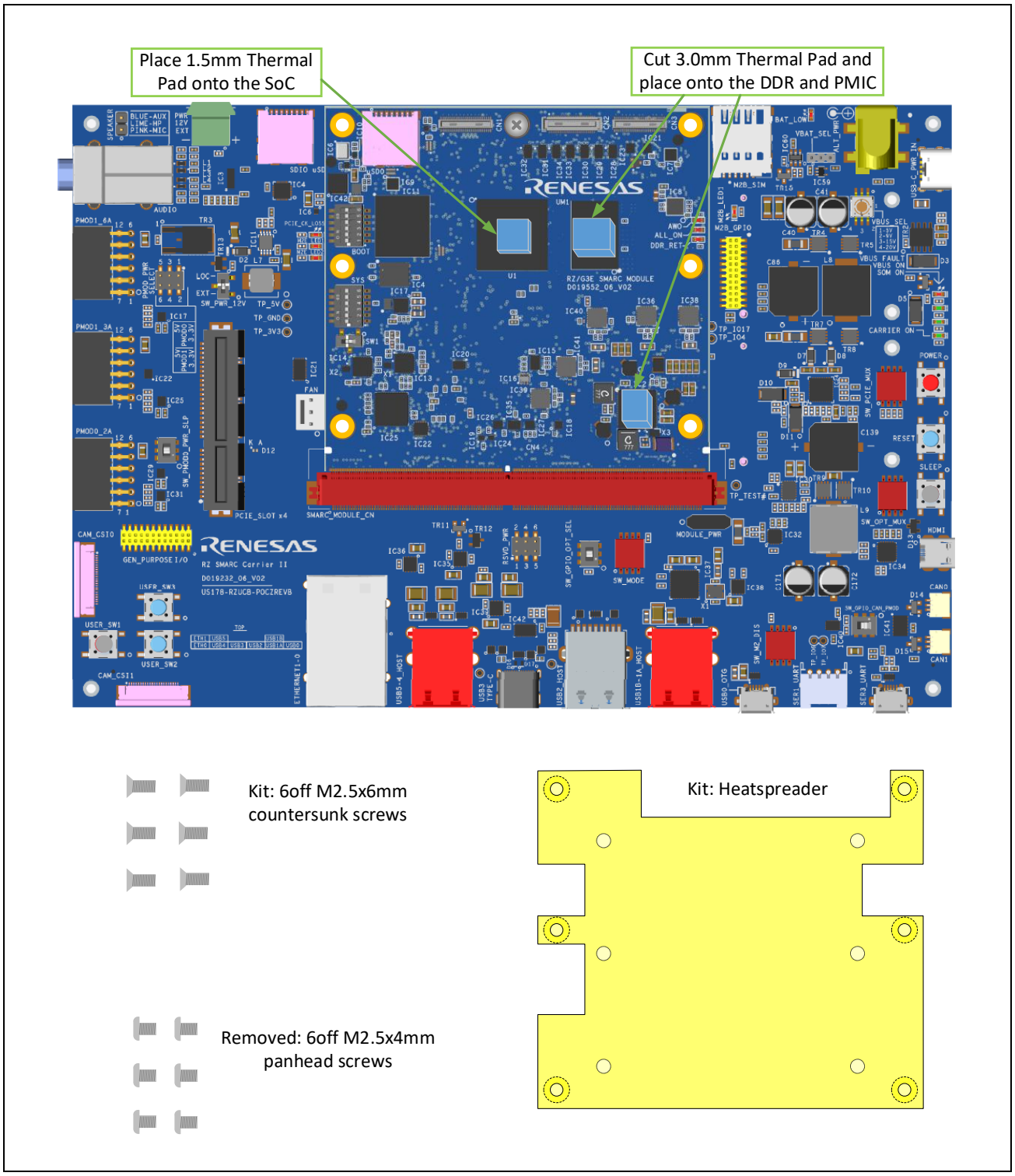


Figure A.2 How to Cut and Where to Place the Thermal Pad

Step 3:

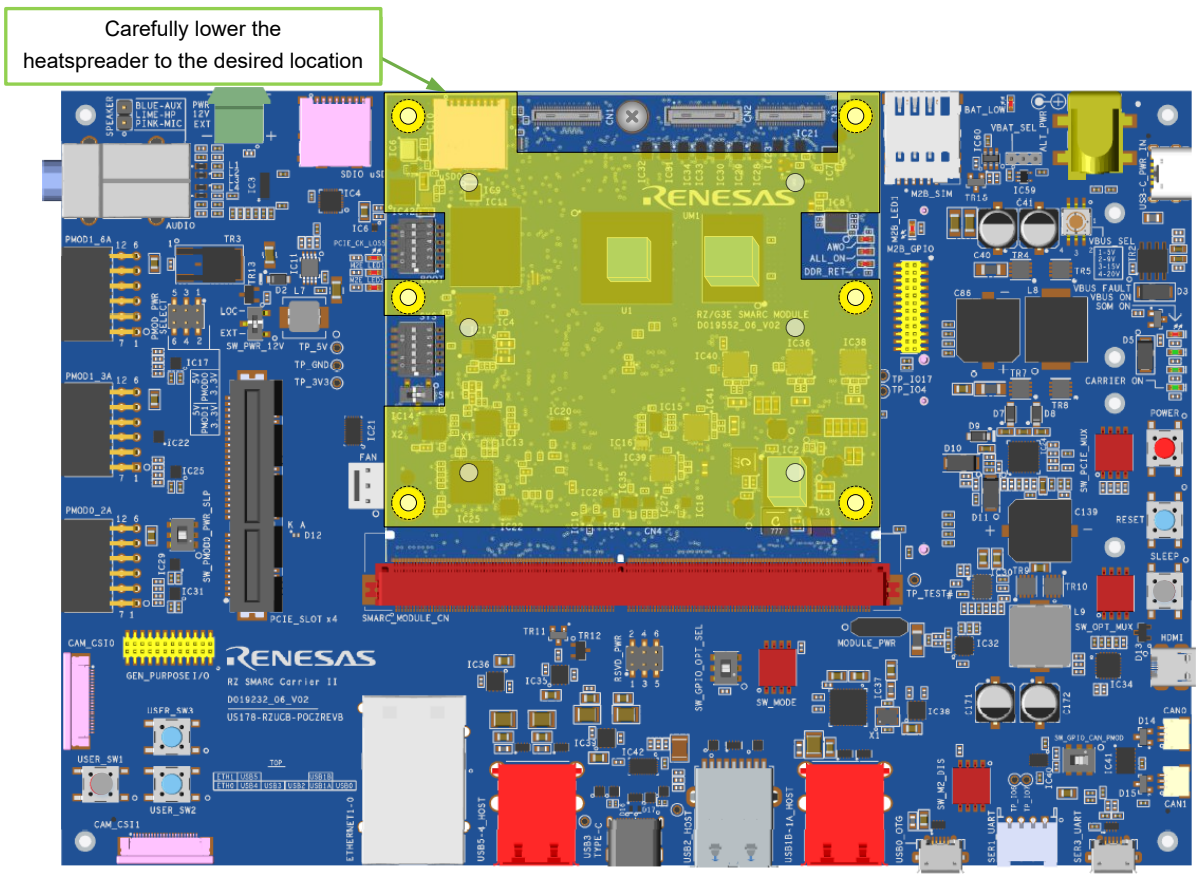
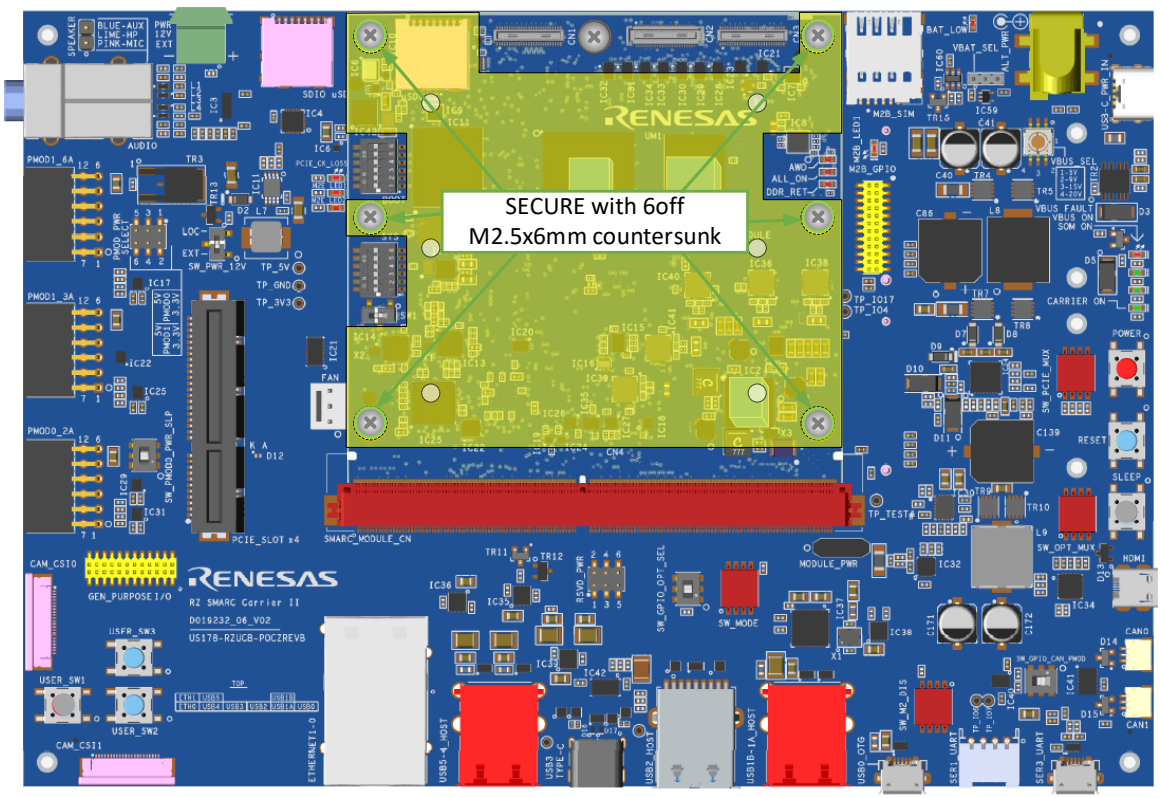


Figure A.3 How to Install a Heatspreader on the G3E SMARC Module

Step 4:



Removed: 6off M2.5x4mm
panhead screws

Figure A.4 How to Secure the Heatspreader

The heatspreader assembly is now complete.

REVISION HISTORY	RZ Family / RZ/G Series RZ/G3E SMARC Module Board

Rev.	Date	Description	
		Page	Summary
1.00	July 10, 2025	—	First edition issued

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